# Si515

# VOLTAGE-CONTROLLED CRYSTAL OSCILLATOR (VCXO)
# 100 kHz TO 250 MHz

## Features

- Supports any frequency from 100 kHz to 250 MHz
- Low-jitter operation
- Short lead times: <2 weeks
- AT-cut fundamental mode crystal ensures high reliability/low aging
- High power supply noise rejection
- 1% control voltage linearity
- Available CMOS, LVPECL, LVDS, and HCSL outputs
- Optional integrated 1:2 CMOS fanout buffer
- 3.3 and 2.5 V supply options
- Industry-standard 5x7, 3.2x5, and 2.5x3.2 mm packages
- Pb-free/RoHS-compliant
- Selectable Kv (60, 90, 120, 150 ppm/V)

5x7MM, 3.2x5MM 2.5x3.2MM

**Ordering Information:**

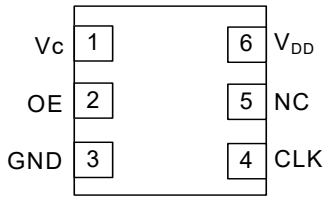
See page 14.

## Applications

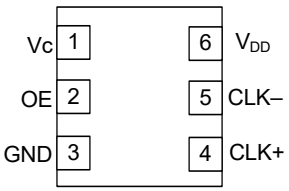
- SONET/SDH/OTN
- PON
- Low Jitter PLLs
- xDSL
- Broadcast video
- Telecom
- Switches/routers
- FPGA/ASIC clock generation

**Pin Assignments:**

See page 12.




**CMOS VCXO**

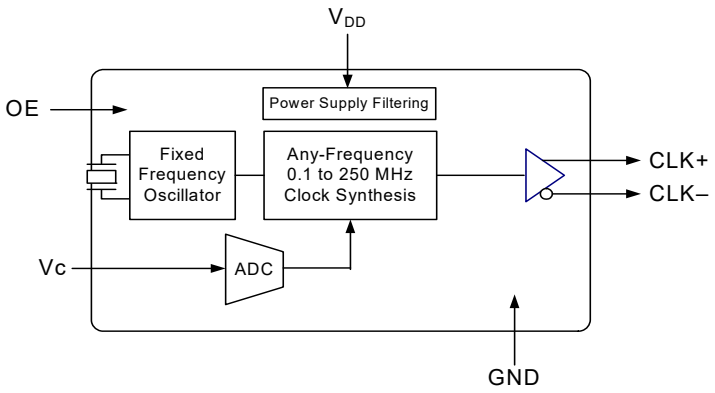



**LVPECL/LVDS/HCSL/ Dual CMOS VCXO**

## Description

The Si515 VCXO utilizes Silicon Laboratories' advanced PLL technology to provide any frequency from 100 kHz to 250 MHz. Unlike a traditional VCXO where a different crystal is required for each output frequency, the Si515 uses one fixed crystal and Silicon Labs' proprietary synthesizer to generate any frequency across this range. This IC-based approach allows the crystal resonator to provide enhanced reliability, improved mechanical robustness, and excellent stability. In addition, this solution provides superior control voltage linearity and supply noise rejection, improving PLL stability and simplifying low jitter PLL design in noisy environments. The Si515 is factory-configurable for a wide variety of user specifications, including frequency, supply voltage, output format, tuning slope and stability. Specific configurations are factory-programmed at time of shipment, eliminating long lead times and non-recurring engineering charges associated with custom frequency oscillators.

## Functional Block Diagram





Copyright © 2018 by Silicon Laboratories

# TABLE OF CONTENTS

**Section** **Page**

**1. Electrical Specifications . . . . . 3**
**2. Solder Reflow and Rework Requirements for 2.5x3.2 mm Packages . . . . . 11**
**3. Pin Descriptions . . . . . 12**
3.1. Dual CMOS Buffer . . . . . 13
**4. Ordering Information . . . . . 14**
**5. Package Outline Diagram: 5 x 7 mm, 6-pin . . . . . 15**
**6. PCB Land Pattern: 5 x 7 mm, 6-pin . . . . . 16**
**7. Package Outline Diagram: 3.2 x 5.0 mm, 6-pin . . . . . 17**
**8. PCB Land Pattern: 3.2 x 5.0 mm, 6-pin . . . . . 18**
**9. Package Outline Diagram: 2.5 x 3.2 mm, 6-pin . . . . . 19**
**10. PCB Land Pattern: 2.5 x 3.2 mm, 6-pin . . . . . 21**
**11. Top Marking . . . . . 22**
11.1. Si515 Top Marking . . . . . 22
11.2. Top Marking Explanation . . . . . 22
**Document Change List . . . . . 23**

# 1. Electrical Specifications

### Table 1. Recommended Operating Conditions

$V_{DD}$ = 2.5 or 3.3 V ±10%, $T_A$ = –40 to +85 °C

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 3.3 V option | 2.97 | 3.3 | 3.63 | V |
| | | 2.5 V option | 2.25 | 2.5 | 2.75 | V |
| Supply Current | $I_{DD}$ | CMOS, 100 MHz, single-ended | — | 24 | 29 | mA |
| | | LVDS (output enabled) | — | 22 | 26 | mA |
| | | LVPECL (output enabled) | — | 42 | 46 | mA |
| | | HCSL (output enabled) | — | 44 | 47 | mA |
| | | Tristate (output disabled) | — | — | 22 | mA |
| OE “1” Setting | $V_{IH}$ | See Note | 0.80 x $V_{DD}$ | — | — | V |
| OE “0” Setting | $V_{IL}$ | See Note | — | — | 0.20 x $V_{DD}$ | V |
| OE Internal Pull-Up/ Pull-Down Resistor* | $R_I$ | | — | 45 | — | kΩ |
| Operating Temperature | $T_A$ | | –40 | — | 85 | °C |

***Note:** Active high and active low polarity OE options available. Active high uses internal pull-up. Active low uses internal pull-down. See ordering information on page 13.

### Table 2. Vc Control Voltage Input

$V_{DD}$ = 2.5 or 3.3 V ±10%, $T_A$ = –40 to +85 °C

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Control Voltage Range | $V_C$ | | 0.1 x $V_{DD}$ | $V_{DD}$/2 | 0.9 x $V_{DD}$ | V |
| Control Voltage Tuning Slope (10 to 90% $V_{DD}$) | Kv | Positive slope, ordering option | 60, 90, 120, 150 | | | ppm/V |
| Kv Variation | Kv_var | | — | — | ±10 | % |
| Control Voltage Linearity | $L_{VC}$ | BSL | –5 | ±1 | +5 | % |
| Modulation Bandwidth | BW | | — | 10 | — | kHz |
| Vc Input Impedance | $Z_{VC}$ | | — | 100 | — | kΩ |

### Table 3. Output Clock Frequency Characteristics

$V_{DD}$ = 2.5 or 3.3 V ±10%, $T_A$ = –40 to +85 °C

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Nominal Frequency | $F_O$ | CMOS, Dual CMOS | 0.1 | — | 212.5 | MHz |
| | $F_O$ | LVDS/LVPECL/HCSL | 0.1 | — | 250 | MHz |
| Temperature Stability | $S_T$ | $T_A$ = –40 to +85 °C | –20 | — | +20 | ppm |
| Aging | A | Frequency drift over 10 year life | — | — | ±8.5 | ppm |
| Minimum Absolute Pull Range | APR | Ordering option | ±30, ±50,±80, ±100 | | | ppm |
| Startup Time | $T_{SU}$ | Minimum $V_{DD}$ to output frequency ($F_O$) within specification | — | — | 10 | ms |
| Disable Time | $T_D$ | $F_O \geq$ 10 MHz | — | — | 5 | µs |
| | | $F_O$ < 10 MHz | | | 40 | µs |
| Enable Time | $T_E$ | $F_O \geq$ 10 MHz | — | — | 20 | µs |
| | | $F_O$ < 10 MHz | | | 60 | µs |

### Table 4. Output Clock Levels and Symmetry

$V_{DD}$ = 2.5 or 3.3 V ±10%, $T_A$ = –40 to +85 °C

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| CMOS Output Logic High | $V_{OH}$ | | 0.85 x $V_{DD}$ | — | — | V |
| CMOS Output Logic Low | $V_{OL}$ | | — | — | 0.15 x $V_{DD}$ | V |
| CMOS Output Logic High Drive | $I_{OH}$ | 3.3 V | –8 | — | — | mA |
| | | 2.5 V | –6 | — | — | mA |
| CMOS Output Logic Low Drive | $I_{OL}$ | 3.3 V | 8 | — | — | mA |
| | | 2.5 V | 6 | — | — | mA |
| CMOS Output Rise/Fall Time (20 to 80% $V_{DD}$) | $T_R/T_F$ | 0.1 to 125 MHz, $C_L$ = 15 pF | — | 0.8 | 1.2 | ns |
| | | 0.1 to 212.5 MHz, $C_L$ = no load | — | 0.6 | 0.9 | ns |
| LVPECL/HCSL Output Rise/Fall Time (20 to 80% $V_{DD}$) | $T_R/T_F$ | | — | — | 565 | ps |
| LVDS Output Rise/Fall Time (20 to 80% $V_{DD}$) | $T_R/T_F$ | | — | — | 800 | ps |
| LVPECL Output Common Mode | $V_{OC}$ | 50 Ω to $V_{DD}$ – 2 V, single-ended | — | $V_{DD}$ – 1.4 V | — | V |
| LVPECL Output Swing | $V_O$ | 50 Ω to $V_{DD}$ – 2 V, single-ended | 0.55 | 0.8 | 0.90 | $V_{PPSE}$ |
| LVDS Output Common Mode | $V_{OC}$ | 100 Ω line-line, $V_{DD}$ = 3.3/2.5 V | 1.13 | 1.23 | 1.33 | V |
| LVDS Output Swing | $V_O$ | Single-ended 100 Ω differential termination | 0.25 | 0.38 | 0.42 | $V_{PPSE}$ |
| HCSL Output Common Mode | $V_{OC}$ | 50 Ω to ground | 0.35 | 0.38 | 0.42 | V |
| HCSL Output Swing | $V_O$ | Single-ended | 0.58 | 0.73 | 0.85 | $V_{PPSE}$ |
| Duty Cycle | DC | | 48 | 50 | 52 | % |

### Table 5. Output Clock Jitter and Phase Noise (LVPECL)

$V_{DD}$ = 2.5 or 3.3 V ±10%, $T_A$ = –40 to +85 °C; Output Format = LVPECL

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Period Jitter (RMS) | $J_{PRMS}$ | 10 k samples[1] | — | — | 1.3 | ps |
| Period Jitter (PK-PK) | $J_{PPKPK}$ | 10 k samples[1] | — | — | 11 | ps |
| Phase Jitter (RMS) | φJ | 12 kHz to 20 MHz[2] (brickwall) | — | 0.9 | 1.3 | ps |
| | | 1.875 MHz to 20 MHz[2] (brickwall) | — | 0.25 | 0.5 | ps |
| Phase Noise, 155.52 MHz | φN | 100 Hz offset | — | –71 | — | dBc/Hz |
| | | 1 kHz offset | — | –93 | — | dBc/Hz |
| | | 10 kHz offset | — | –113 | — | dBc/Hz |
| | | 100 kHz offset | — | –124 | — | dBc/Hz |
| | | 1 MHz offset | — | –136 | — | dBc/Hz |
| Additive RMS Jitter Due to External Power Supply Noise[3] | $J_{PSRR}$ | 100 kHz sinusoidal noise | — | 4.0 | — | ps |
| | | 200 kHz sinusoidal noise | — | 3.5 | — | ps |
| | | 500 kHz sinusoidal noise | — | 3.5 | — | ps |
| | | 1 MHz sinusoidal noise | — | 3.5 | — | ps |
| Spurious Performance | SPR | $F_O$ = 156.25 MHz, Offset > 10 kHz | — | –75 | — | dBc |

**Notes:**
1. Applies to output frequencies: 74.17582, 74.25, 75, 77.76, 100, 106.25, 125, 148.35165, 148.5, 150, 155.52, 156.25, 212.5, 250 MHz.
2. Applies to output frequencies: 100, 106.25, 125, 148.35165, 148.5, 150, 155.52, 156.25, 212.5, 250 MHz.
3. 156.25 MHz. Increase in jitter on output clock due to spurs introduced by sinewave noise added to VDD (100 $mV_{PP}$).

### Table 6. Output Clock Jitter and Phase Noise (LVDS)

$V_{DD}$ = 1.8 V ±5%, 2.5 or 3.3 V ±10%, $T_A$ = –40 to +85 °C; Output Format = LVDS

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Period Jitter (RMS) | JPRMS | 10k samples[1] | — | — | 2.1 | ps |
| Period Jitter (Pk-Pk) | JPPKPK | 10k samples[1] | — | — | 18 | ps |
| Phase Jitter (RMS) | φJ | 1.875 MHz to 20 MHz integration bandwidth[2] (brickwall) | — | 0.25 | 0.55 | ps |
| | | 12 kHz to 20 MHz integration bandwidth[2] (brickwall) | — | 0.8 | 1.1 | ps |
| Phase Noise, 156.25 MHz | φN | 100 Hz | — | –72 | — | dBc/Hz |
| | | 1 kHz | — | –93 | — | dBc/Hz |
| | | 10 kHz | — | –114 | — | dBc/Hz |
| | | 100 kHz | — | –123 | — | dBc/Hz |
| | | 1 MHz | — | –136 | — | dBc/Hz |
| Spurious | SPR | LVPECL output, 156.25 MHz, offset>10 kHz | — | –75 | — | dBc |

**Notes:**
1. Applies to output frequencies: 74.17582, 74.25, 75, 77.76, 100, 106.25, 125, 148.35165, 148.5, 150, 155.52, 156.25, 212.5, 250 MHz.
2. Applies to output frequencies: 100, 106.25, 125, 148.35165, 148.5, 150, 155.52, 156.25, 212.5 and 250 MHz.

### Table 7. Output Clock Jitter and Phase Noise (HCSL)

$V_{DD}$ = 1.8 V ±5%, 2.5 or 3.3 V ±10%, $T_A$ = –40 to +85 °C; Output Format = HCSL

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Period Jitter (RMS) | JPRMS | 10k samples* | — | — | 1.2 | ps |
| Period Jitter (Pk-Pk) | JPPKPK | 10k samples* | — | — | 11 | ps |
| Phase Jitter (RMS) | φJ | 1.875 MHz to 20 MHz integration bandwidth* (brickwall) | — | 0.25 | 0.30 | ps |
| | | 12 kHz to 20 MHz integration bandwidth* (brickwall) | — | 0.8 | 1.0 | ps |
| Phase Noise, 156.25 MHz | φN | 100 Hz | — | –75 | — | dBc/Hz |
| | | 1 kHz | — | –98 | — | dBc/Hz |
| | | 10 kHz | — | –117 | — | dBc/Hz |
| | | 100 kHz | — | –127 | — | dBc/Hz |
| | | 1 MHz | — | –136 | — | dBc/Hz |
| Spurious | SPR | LVPECL output, 156.25 MHz, offset>10 kHz | — | –75 | — | dBc |

***Note:** Applies to an output frequency of 100 MHz.

### Table 8. Output Clock Jitter and Phase Noise (CMOS, Dual CMOS)

$V_{DD}$ = 1.8 V ±5%, 2.5 or 3.3 V ±10%, $T_A$ = –40 to +85 °C; Output Format = CMOS, Dual CMOS

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Phase Jitter (RMS) | φJ | 1.875 MHz to 20 MHz integration bandwidth[2] (brickwall) | — | 0.25 | 0.35 | ps |
| | | 12 kHz to 20 MHz integration bandwidth[2] (brickwall) | — | 0.8 | 1.1 | ps |
| Phase Noise, 156.25 MHz | φN | 100 Hz | — | –71 | — | dBc/Hz |
| | | 1 kHz | — | –93 | — | dBc/Hz |
| | | 10 kHz | — | –113 | — | dBc/Hz |
| | | 100 kHz | — | –123 | — | dBc/Hz |
| | | 1 MHz | — | –136 | — | dBc/Hz |
| Spurious | SPR | LVPECL output, 156.25 MHz, offset>10 kHz | — | –75 | — | dBc |

**Notes:**
1. Applies to output frequencies: 74.17582, 74.25, 75, 77.76, 100, 106.25, 125, 148.35165, 148.5, 150, 155.52, 156.25, 212.5 MHz.
2. Applies to output frequencies: 100, 106.25, 125, 148.35165, 148.5, 150, 155.52, 156.25, 212.5 MHz.

### Table 9. Environmental Compliance and Package Information

| Parameter | Conditions/Test Method |
|---|---|
| Mechanical Shock | MIL-STD-883, Method 2002 |
| Mechanical Vibration | MIL-STD-883, Method 2007 |
| Solderability | MIL-STD-883, Method 2003 |
| Gross and Fine Leak | MIL-STD-883, Method 1014 |
| Resistance to Solder Heat | MIL-STD-883, Method 2036 |
| Contact Pads | Gold over Nickel |

### Table 10. Thermal Characteristics

| Parameter | Symbol | Test Condition | Value | Unit |
|---|---|---|---|---|
| CLCC, Thermal Resistance Junction to Ambient | $\theta_{JA}$ | Still air | 110 | °C/W |
| 2.5x3.2mm, Thermal Resistance Junction to Ambient | $\theta_{JA}$ | Still air | 164 | °C/W |

### Table 11. Absolute Maximum Ratings[1]

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Maximum Operating Temperature | $T_{AMAX}$ | 85 | °C |
| Storage Temperature | $T_S$ | –55 to +125 | °C |
| Supply Voltage | $V_{DD}$ | –0.5 to +3.8 | V |
| Input Voltage (any input pin) | $V_I$ | –0.5 to $V_{DD}$ + 0.3 | V |
| ESD Sensitivity (HBM, per JESD22-A114) | HBM | 2 | kV |
| Soldering Temperature (Pb-free profile)[2] | $T_{PEAK}$ | 260 | °C |
| Soldering Temperature Time at $T_{PEAK}$ (Pb-free profile)[2] | $T_P$ | 20–40 | sec |

**Notes:**
1. Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation or specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. The device is compliant with JEDEC J-STD-020E.

## 2. Solder Reflow and Rework Requirements for 2.5x3.2 mm Packages

Reflow of Silicon Labs' components should be done in a manner consistent with the IPC/JEDEC J-STD-20E standard. The temperature of the package is not to exceed the classification Temperature provided in the standard. The part should not be within -5°C of the classification or peak reflow temperature ($T_{PEAK}$) for longer than 30 seconds. Key to maintaining the integrity of the component is providing uniform heating and cooling of the part during reflow and rework. Uniform heating is achieved through having a preheat soak and controlling the temperature ramps in the process. J-STD-20E provides minimum and maximum temperatures and times for the preheat/Soak step that need to be followed, even for rework. The entire assembly area should be heated during rework. Hot air should be flowed from both the bottom of the board and the top of the component. Heating from the top only will cause un-even heating of component and can lead to part integrity issues. Temperature Ramp-up rate are not to exceed 3°C/second. Temperature ramp-down rates from peak to final temperature are not to exceed 6°C/second. Time from 25°C to peak temperature is not to exceed 8 min for Pb-free solders.

## 3. Pin Descriptions

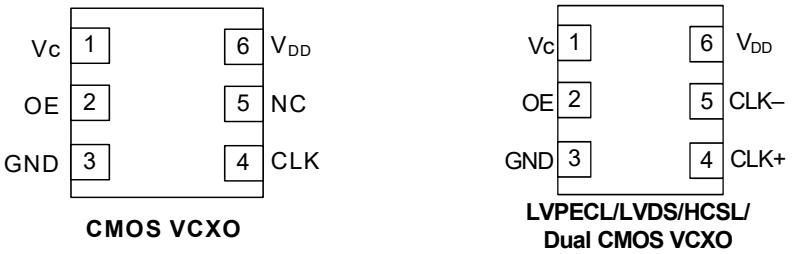



**Table 12. Si515 Pin Descriptions (CMOS)**

| Pin | Name | CMOS Function |
|---|---|---|
| 1 | $V_C$ | Control Voltage Input. |
| 2 | OE | Output Enable. Internal pull-up for OE active high. Pull-down for OE active low. See ordering information. |
| 3 | GND | Electrical and Case Ground. |
| 4 | CLK | Clock Output. |
| 5 | NC | No connect. Make no external connection to this pin. |
| 6 | $V_{DD}$ | Power Supply Voltage. |

**Table 13. Si515 Pin Descriptions (LVPECL/LVDS/HCSL/Dual CMOS)**

| Pin | Name | LVPECL/LVDS/HCSL/Dual CMOS Function |
|---|---|---|
| 1 | $V_C$ | Control Voltage Input. |
| 2 | OE | Output Enable. Internal pull-up for OE active high. Pull-down for OE active low. See ordering information. |
| 3 | GND | Electrical and Case Ground. |
| 4 | CLK+ | Clock Output. |
| 5 | CLK– | Complementary Clock Output. |
| 6 | $V_{DD}$ | Power Supply Voltage. |

## 3.1. Dual CMOS Buffer

Dual CMOS output format ordering options support either complementary or in-phase output signals. This feature enables replacement of multiple VCXOs with a single Si515 device.

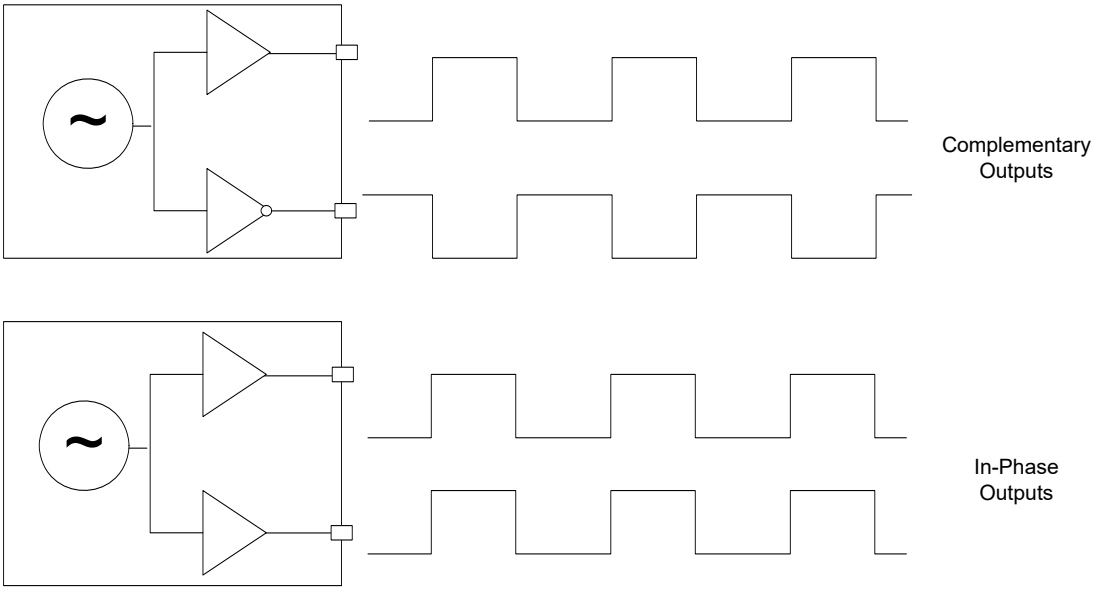



**Figure 1. Integrated 1:2 CMOS Buffer Supports Complementary or In-Phase Outputs**

## 4. Ordering Information

The Si515 supports a variety of options including frequency, stability, tuning slope, output format, and $V_{DD}$. Specific device configurations are programmed into the Si515 at time of shipment. Configurations are specified using the Part Number Configuration chart shown below. Silicon Labs provides a web browser-based part number configuration utility to simplify this process. To access this tool refer to www.silabs.com/oscillators and click "Customize" in the product table. The Si515 VCXO series is supplied in industry-standard, RoHS compliant, lead-free, 2.5 x 3.2 mm, 3.2 x 5.0 mm, and 5 x 7 mm packages. Tape and reel packaging is an ordering option.

| Series | Output Format | Package |
|---|---|---|
| 515<br>Single Frequency VCXO | LVPECL, LVDS, HCSL,<br>CMOS, Dual CMOS | 6-pin |

A = Revision: A
G = Temp Range: -40°C to 85°C
R = Tape & Reel; Blank = Coil Tape

1st Option Code:
Output Format

| | VDD | Output Format |
|---|---|---|
| A | 3.3V | LVPECL |
| B | 3.3V | LVDS |
| C | 3.3V | CMOS |
| D | 3.3V | HCSL |
| E | 2.5V | LVPECL |
| F | 2.5V | LVDS |
| G | 2.5V | CMOS |
| H | 2.5V | HCSL |
| M | 3.3V | Dual CMOS (In-phase) |
| N | 3.3V | Dual CMOS (Complementary) |
| P | 2.5V | Dual CMOS (In-phase) |
| Q | 2.5V | Dual CMOS (Complementary) |

3rd Option Code:
Output Enable

| | OE Polarity |
|---|---|
| A | OE Active High |
| B | OE Active Low |

Package Option

| | Dimensions |
|---|---|
| A | 5 x 7 mm |
| B | 3.2 x 5 mm |
| C | 2.5 x 3.2 mm |

2nd Option Code: Stability & APR

| | Temp Stability | Kv | Minimum APR | |
|---|---|---|---|---|
| | | | 3.3 V | 2.5 V |
| A | ±20ppm | ±150ppm/V | ±100ppm | ±80ppm |
| B | ±20ppm | ±120ppm/V | ±80ppm | ±50ppm |
| C | ±20ppm | ±90ppm/V | ±50ppm | ±30ppm |
| D | ±20ppm | ±60ppm/V | ±30ppm | Not Supported |

Frequency Code

| Frequency | Description |
|---|---|
| Mxxxxxx | $f_{OUT}$ < 1 MHz |
| xMxxxxx | 1 MHz ≤ $f_{OUT}$ < 10 MHz |
| xxMxxxx | 10 MHz ≤ $f_{OUT}$ < 100 MHz |
| xxxMxxx | 100 MHz ≤ $f_{OUT}$ < 250 MHz |
| xxxxxx | Code if frequency requires >6 digit resolution |

**Figure 2. Part Number Convention**

Example ordering part number: 515BBB212M500BAGR.

The series prefix, 515, indicates the device is a single frequency VCXO.

The 1st option code B specifies the output format is LVDS and powered from a 3.3 V supply. The stability and APR code B indicates a temperature stability of ±20 ppm with a tuning slope of ±120 ppm/V. The 3rd option code B specifies the OE pin is active low.

The frequency code is 212M500. Per this convention, and as indicated by the part number lookup utility at www.silabs.com/VCXOpartnumber, the output frequency is 212.5 MHz. The package code B refers to the 3.2 x 5 mm footprint with six pins. The last A refers to the product revision, G indicates the temperature range (–40 to +85 °C), and R specifies the device ships in tape and reel format.

**Note:** CMOS and Dual CMOS maximum frequency is 212.5 MHz.

## 5. Package Outline Diagram: 5 x 7 mm, 6-pin

Figure 3 illustrates the package details for the Si515. Table 14 lists the values for the dimensions shown in the illustration.

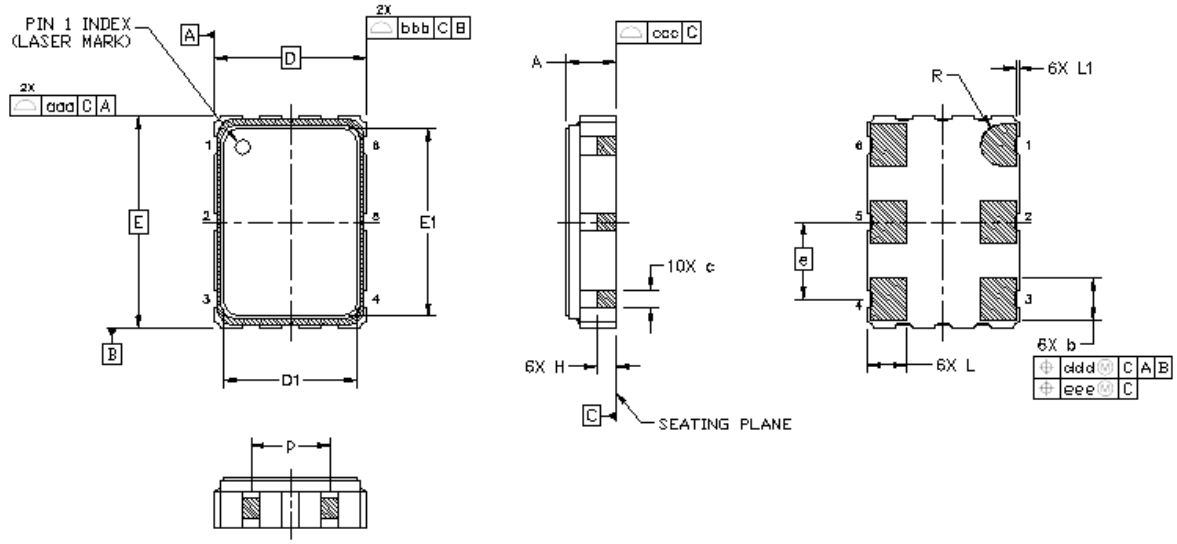



**Figure 3. Si515 Outline Diagram**

**Table 14. Package Diagram Dimensions (mm)**

| Dimension | Min | Nom | Max |
|---|---|---|---|
| A | 1.50 | 1.65 | 1.80 |
| b | 1.30 | 1.40 | 1.50 |
| c | 0.50 | 0.60 | 0.70 |
| D | | 5.00 BSC. | |
| D1 | 4.30 | 4.40 | 4.50 |
| e | | 2.54 BSC. | |
| E | | 7.00 BSC. | |
| E1 | 6.10 | 6.20 | 6.30 |
| H | 0.55 | 0.65 | 0.75 |
| L | 1.17 | 1.27 | 1.37 |
| L1 | 0.05 | 0.10 | 0.15 |
| p | 1.80 | — | 2.60 |
| R | | 0.7 REF. | |
| aaa | | 0.15 | |
| bbb | | 0.15 | |
| ccc | | 0.10 | |
| ddd | | 0.10 | |
| eee | | 0.05 | |

**Notes:**
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

## 6. PCB Land Pattern: 5 x 7 mm, 6-pin

Figure 4 illustrates the 5 x 7 mm PCB land pattern for the Si515. Table 15 lists the values for the dimensions shown in the illustration.

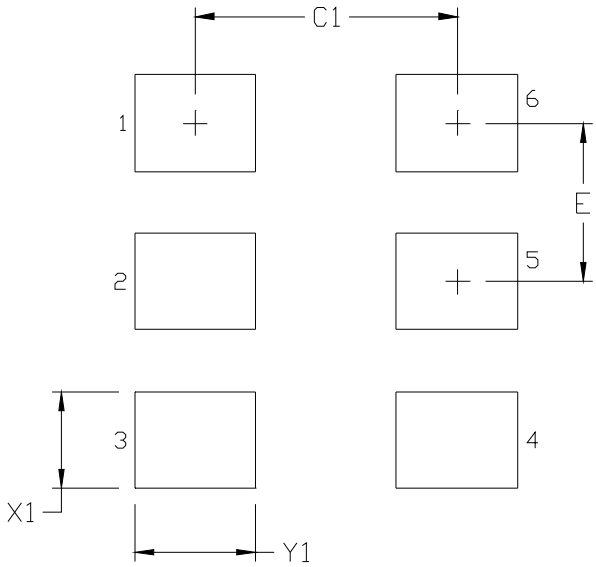



**Figure 4. Si515 PCB Land Pattern**

**Table 15. PCB Land Pattern Dimensions (mm)**

| Dimension | (mm) |
|---|---|
| C1 | 4.20 |
| E | 5.08 |
| X1 | 1.55 |
| Y1 | 1.95 |

**Notes:**

**General**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

**Solder Mask Design**

5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

**Stencil Design**

6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1.

**Card Assembly**

9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

## 7. Package Outline Diagram: 3.2 x 5.0 mm, 6-pin

Figure 5 illustrates the package details for the 3.2 x 5 mm Si515. Table 16 lists the values for the dimensions shown in the illustration.

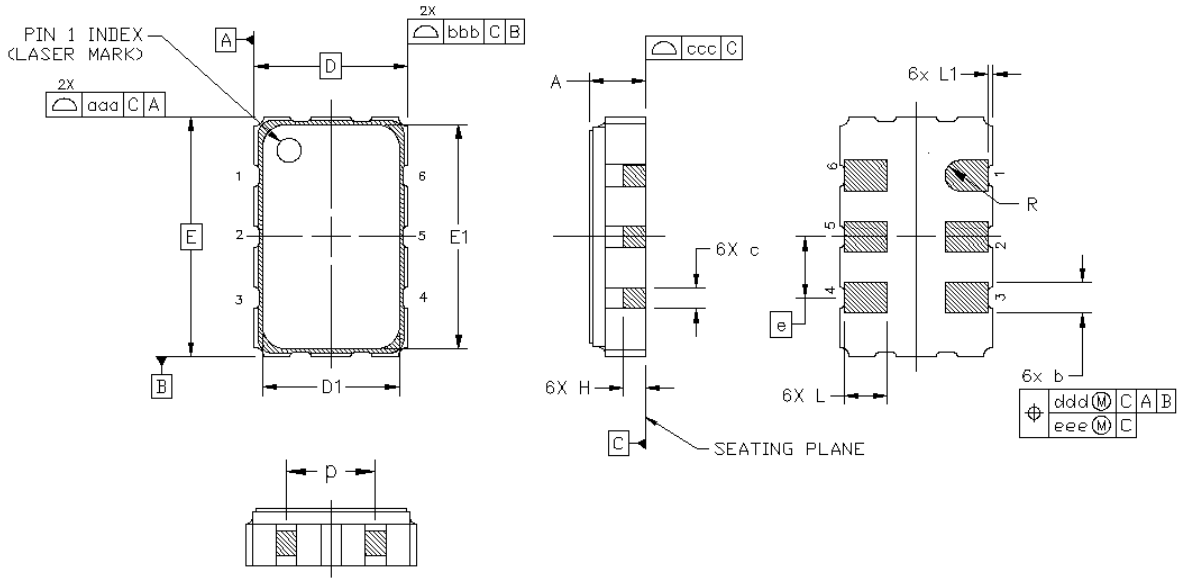



**Figure 5. Si515 Outline Diagram**

**Table 16. Package Diagram Dimensions (mm)**

| Dimension | Min | Nom | Max |
|---|---|---|---|
| A | 1.06 | 1.17 | 1.33 |
| b | 0.54 | 0.64 | 0.74 |
| c | 0.35 | 0.45 | 0.55 |
| D | | 3.20 BSC | |
| D1 | 2.55 | 2.60 | 2.65 |
| e | | 1.27 BSC | |
| E | | 5.00 BSC | |
| E1 | 4.35 | 4.40 | 4.45 |
| H | 0.45 | 0.55 | 0.65 |
| L | 0.80 | 0.90 | 1.00 |
| L1 | 0.05 | 0.10 | 0.15 |
| p | 1.17 | 1.27 | 1.37 |
| R | | 0.32 REF | |
| aaa | | 0.15 | |
| bbb | | 0.15 | |
| ccc | | 0.10 | |
| ddd | | 0.10 | |
| eee | | 0.05 | |

**Notes:**
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

## 8. PCB Land Pattern: 3.2 x 5.0 mm, 6-pin

Figure 6 illustrates the recommended 3.2 x 5 mm PCB land pattern for the Si515. Table 17 lists the values for the dimensions shown in the illustration.

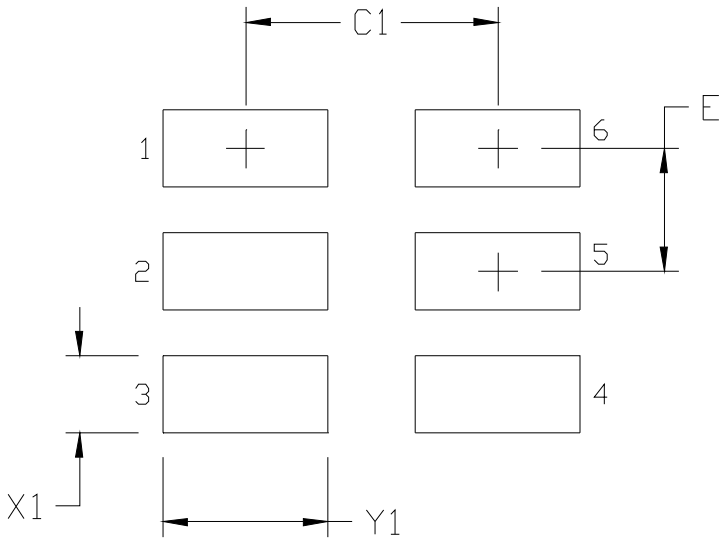



**Figure 6. Si515 PCB Land Pattern**

**Table 17. PCB Land Pattern Dimensions (mm)**

| Dimension | (mm) |
|---|---|
| C1 | 2.60 |
| E | 1.27 |
| X1 | 0.80 |
| Y1 | 1.70 |

**Notes:**

**General**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

**Solder Mask Design**

5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

**Stencil Design**

6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1.

**Card Assembly**

9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

## 9. Package Outline Diagram: 2.5 x 3.2 mm, 6-pin

Figure 7 illustrates the package details for the 2.5 x 3.2 mm Si515. Table 18 lists the values for the dimensions shown in the illustration.

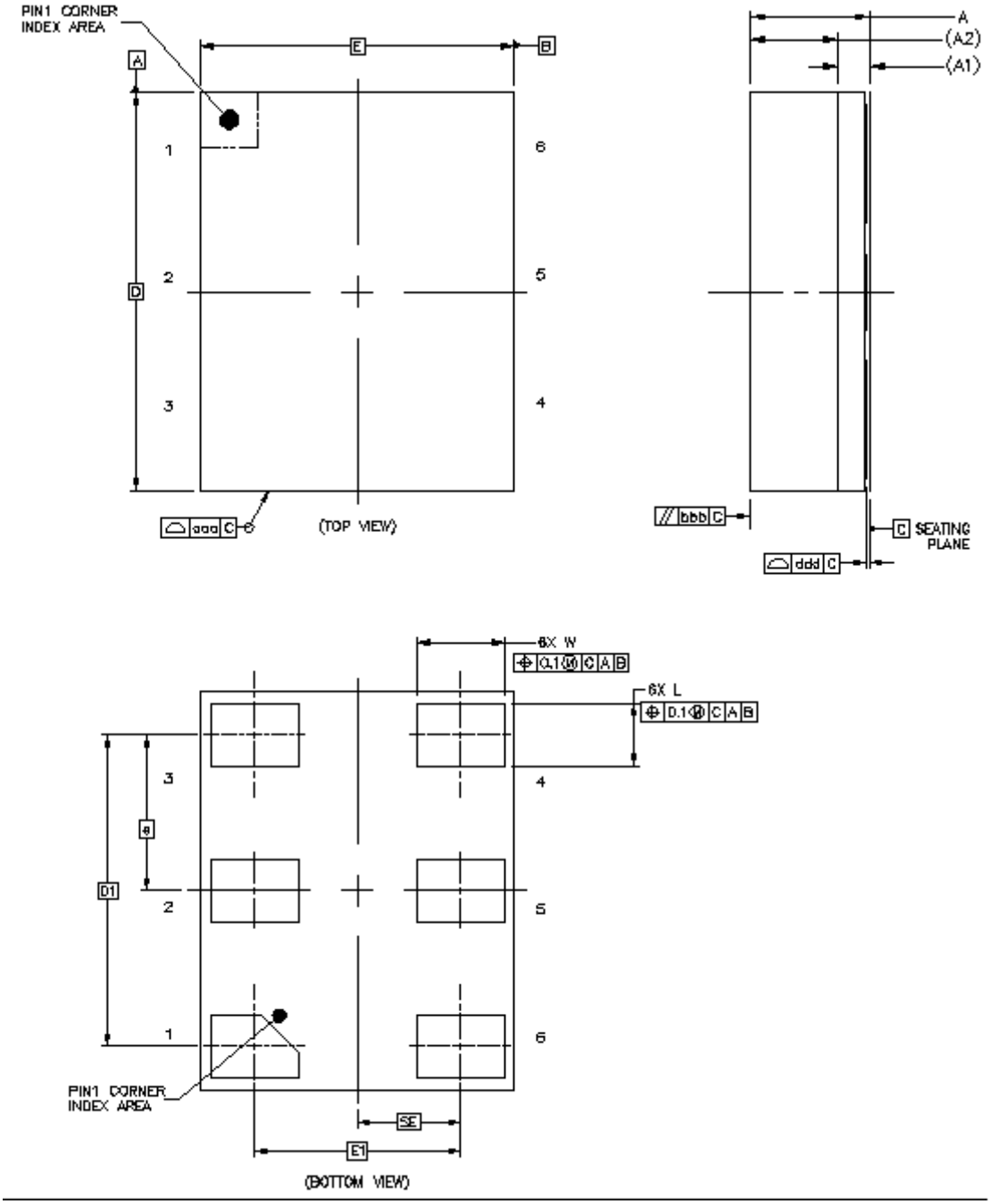



**Figure 7. Si515 Outline Diagram**

**Table 18. Package Diagram Dimensions (mm)**

| Dimension | Min | Nom | Max |
|---|---|---|---|
| A | — | — | 1.1 |
| A1 | | 0.26 REF | |
| A2 | | 0.7 REF | |
| W | 0.65 | 0.7 | 0.75 |
| D | | 3.20 BSC | |
| e | | 1.25 BSC | |
| E | | 2.50 BSC | |
| M | | 0.30 BSC | |
| L | 0.45 | 0.5 | 0.55 |
| D1 | | 2.5 BSC | |
| E1 | | 1.65 BSC | |
| SE | | 0.825 BSC | |
| aaa | | 0.1 | |
| bbb | | 0.2 | |
| ddd | | 0.08 | |

**Notes:**
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

## 10. PCB Land Pattern: 2.5 x 3.2 mm, 6-pin

Figure 8 illustrates the 2.5 x 3.2 mm PCB land pattern for the Si515. Table 19 lists the values for the dimensions shown in the illustration.

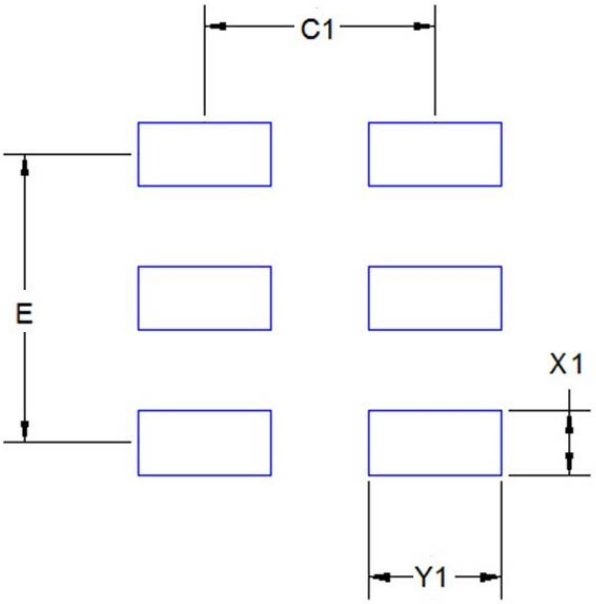



**Figure 8. Si515 Recommended PCB Land Pattern**

**Table 19. PCB Land Pattern Dimensions (mm)**

| Dimension | (mm) |
|---|---|
| C1 | 1.9 |
| E | 2.50 |
| X1 | 0.70 |
| Y1 | 1.05 |

**Notes:**

**General**

3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.
4. This Land Pattern Design is based on the IPC-7351 guidelines.

**Solder Mask Design**

5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

**Stencil Design**

6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.

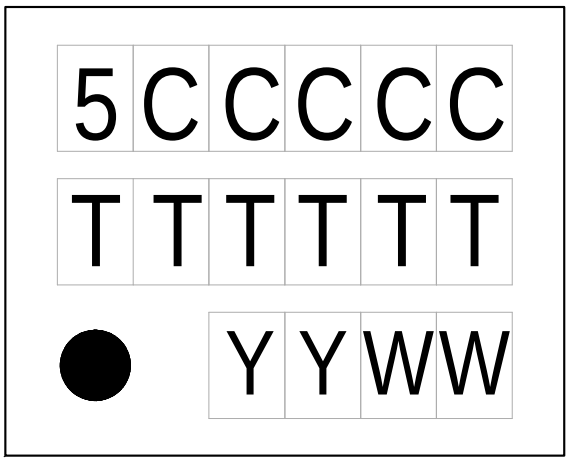
**Card Assembly**

9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

# 11. Top Marking

Use the part number configuration utility located at: www.silabs.com/VCXOPartNumber to cross-reference the mark code to a specific device configuration.

## 11.1. Si515 Top Marking




## 11.2. Top Marking Explanation

| | | |
|---|---|---|
| **Mark Method:** | Laser | |
| **Line 1 Marking:** | 5 = Si515<br>CCCCC = Mark Code | 5CCCCC |
| **Line 2 Marking:** | TTTTTT = Assembly Manufacturing Code | TTTTTT |
| **Line 3 Marking:** | Pin 1 indicator. | Circle with 0.5 mm diameter; left-justified |
| | YY = Year.<br>WW = Work week.<br>Characters correspond to the year and work week of package assembly. | YYWW |

# Revision History

## Revision 1.2

June, 2018

- Changed “Trays” to “Coil Tape” in Ordering Guide.

## Revision 1.1

December, 2017

- Added 2.5 x 3.2 mm package.

## Revision 1.0

- Updated Table 1 on page 3.
  - Updates to supply current typical and maximum values for CMOS, LVDS, LVPECL and HCSL.
  - CMOS frequency test condition corrected to 100 MHz.
  - Updates to OE VIH minimum and VIL maximum values.
- Updated Table 3 on page 4.
  - Dual CMOS nominal frequency maximum added.
  - Disable time maximum values updated.
  - Enable time parameter added.
- Updated Table 4 on page 5.
  - CMOS output rise / fall time typical and maximum values updated.
  - LVPECL/HCSL output rise / fall time maximum value updated.
  - LVPECL output swing maximum value updated.
  - LVDS output common mode typical and maximum values updated.
  - HCSL output swing maximum value updated.
  - Duty cycle minimum and maximum values tightened to 48/52%.
- Updated Table 5 on page 6.
  - Phase jitter test condition, typical and maximum value updated.
  - Phase noise typical values updated.
  - Additive RMS jitter due to external power supply noise typical values updated.
- Added Tables 6, 7, 8 for LVDS, HCSL, CMOS and Dual CMOS operations.
- Added note to Figure 2 clarifying CMOS and Dual CMOS maximum frequency.
- Updated Figure 5 outline diagram to correct pinout.
- Updated “11. Top Marking” section and moved to page 22.

## ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows and iOS (CBGo only).

*www.silabs.com/CBPro*

**Timing Portfolio**
*www.silabs.com/timing*

**SW/HW**
*www.silabs.com/CBPro*

**Quality**
*www.silabs.com/quality*

**Support and Community**
*community.silabs.com*

**Disclaimer**
Silicon Labs intends to provide customers with the latest, accurate, and in-depth documentation of all peripherals and modules available for system and software implementers using or intending to use the Silicon Labs products. Characterization data, available modules and peripherals, memory sizes and memory addresses refer to each specific device, and "Typical" parameters provided can and do vary in different applications. Application examples described herein are for illustrative purposes only. Silicon Labs reserves the right to make changes without further notice to the product information, specifications, and descriptions herein, and does not give warranties as to the accuracy or completeness of the included information. Without prior notification, Silicon Labs may update product firmware during the manufacturing process for security or reliability reasons. Such changes will not alter the specifications or the performance of the product. Silicon Labs shall have no liability for the consequences of use of the information supplied in this document. This document does not imply or expressly grant any license to design or fabricate any integrated circuits. The products are not designed or authorized to be used within any FDA Class III devices, applications for which FDA premarket approval is required or Life Support Systems without the specific written consent of Silicon Labs. A "Life Support System" is any product or system intended to support or sustain life and/or health, which, if it fails, can be reasonably expected to result in significant personal injury or death. Silicon Labs products are not designed or authorized for military applications. Silicon Labs products shall under no circumstances be used in weapons of mass destruction including (but not limited to) nuclear, biological or chemical weapons, or missiles capable of delivering such weapons. Silicon Labs disclaims all express and implied warranties and shall not be responsible or liable for any injuries or damages related to use of a Silicon Labs product in such unauthorized applications.

**Trademark Information**
Silicon Laboratories Inc.® , Silicon Laboratories®, Silicon Labs®, SiLabs® and the Silicon Labs logo®, Bluegiga®, Bluegiga Logo®, ClockBuilder®, CMEMS®, DSPLL®, EFM®, EFM32®, EFR, Ember®, Energy Micro, Energy Micro logo and combinations thereof, "the world's most energy friendly microcontrollers", Ember®, EZLink®, EZRadio®, EZRadioPRO®, Gecko®, Gecko OS, Gecko OS Studio, ISOmodem®, Precision32®, ProSLIC®, Simplicity Studio®, SiPHY®, Telegesis, the Telegesis Logo®, USBXpress® , Zentri, the Zentri logo and Zentri DMS, Z-Wave®, and others are trademarks or registered trademarks of Silicon Labs. ARM, CORTEX, Cortex-M3 and THUMB are trademarks or registered trademarks of ARM Holdings. Keil is a registered trademark of ARM Limited. Wi-Fi is a registered trademark of the Wi-Fi Alliance. All other products or brand names mentioned herein are trademarks of their respective holders.

**Silicon Laboratories Inc.**
**400 West Cesar Chavez**
**Austin, TX 78701**
**USA**

**http://www.silabs.com**