Easy to Use, Low Power, Sub GHz, ISM/SRD, FSK/GFSK, Transceiver IC

Data Sheet **ADF7024**

FEATURES

- Radio frequency (RF) bands: 431 MHz to 435 MHz and 862 MHz to 928 MHz
- Data rates supported: 9.6 kbps, 38.4 kbps, 50 kbps, 100 kbps, 200 kbps, and 300 kbps
- Modulation: two-level frequency (FSK) and Gaussian frequency (GFSK) shift keying
- 2.2 V to 3.6 V power supply
- Ultralow power sleep modes for long battery life
- Simple serial port interface (SPI) control interface
- Fast radio state transitions
- Automatic frequency control (AFC) and automatic gain control (AGC)
- Digital received signal strength indication (RSSI)
- Fully integrated low noise RF synthesizer and transmit (Tx)/receive (Rx) switch
- Image rejection calibration (U.S. Patent 8,238,865 and U.S. Patent 8,358,993)
- Integrated packet management support
  - Insertion/detection of preamble/sync word/cyclic redundancy check (CRC)
  - Manchester and 8-bit/10-bit data encoding and decoding
  - Data whitening
- 240-byte packet buffer for Tx/Rx data
- Smart wake mode (SWM)
  - Autonomous carrier sense, packet sniffing, and reception
- Integrated battery alarm and temperature sensor
- Integrated RC oscillator
- On-chip, 8-bit analog-to-digital converter (ADC)
- 5 mm × 5 mm, 32-lead LFCSP
- Receiver performance
  - Highly linear: −11.5 dBm input IP3
  - Blocking: 76 dB at 10 MHz offset
  - Receiver sensitivity, bit error rate (BER)
    - −111 dBm at 9.6 kbps
    - −105 dBm at 100 kbps
  - Low power: 12.8 mA in Rx
- Transmitter performance
  - High efficiency power amplifier (PA): 23.3 mA in Tx at 10 dBm
  - Output power range: −20 dBm to +13.5 dBm
  - Output power resolution: 0.5 dB
- Low power mode performance
  - 0.33 µA in PHY_SLEEP mode (Deep Sleep Mode 1)
  - 0.75 µA in PHY_SLEEP mode (32 kHz RC oscillator active)
  - 11.75 µA autonomous Rx sniff using SWM, 300 kbps
- Supported regulations
  - ETSI EN 300 220
  - FCC Part 15.231, Part 15.247, Part 15.249

APPLICATIONS

- Wireless sensor networks (WSNs)
- Home and building automation
- sset tracking
- Process and building control
- Industrial control
- Internet of Things (IoT)

FUNCTIONAL BLOCK DIAGRAM

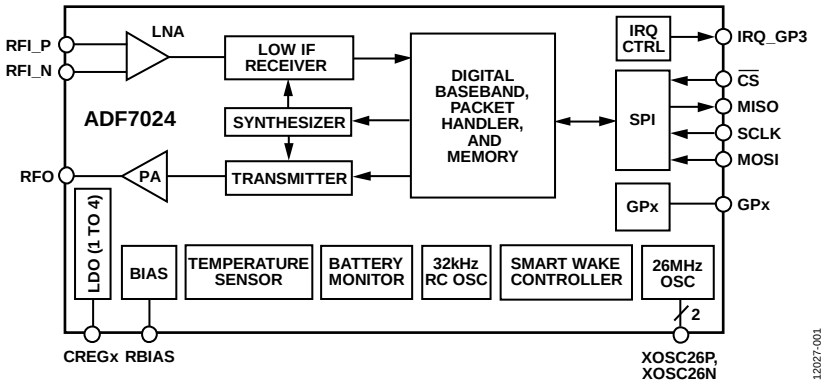

Figure 1.

Document Feedback

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6/14—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADF7024 is an ultralow power, integrated transceiver for use in the license-free ISM bands at 433 MHz, 868 MHz, and 915 MHz. Its ease of use and high performance make it suitable for a wide variety of wireless applications. The ADF7024 is suitable for operation under the European ETSI EN 300-220 regulation, the North American FCC Part 15 regulation, and other similar regulatory standards.

The ADF7024 can operate under a number of predefined radio profiles. For each radio profile, optimized register settings are provided for the ADF7024 radio. This ensures that the RF communication layer works seamlessly, allowing the user to concentrate on the protocol and system level design and prototyping. The radio profiles cover common data rate and modulation options. There are six radio profiles in total, as shown in Table 1.

The ADF7024 operates with a power supply range of 2.2 V to 3.6 V and has very low power consumption in both Tx and Rx modes, enabling long lifetimes in battery-operated systems while maintaining excellent RF performance.

The low IF receiver minimizes power consumption and provides excellent sensitivity. The receiver is exceptionally linear and, therefore, is very resilient to the presence of interferers in spectrally noisy environments. The highly efficient transmitter has programmable output power up to 13.5 dBm and automatic power amplifier (PA) ramping to meet transient spurious specifications. The RF synthesizer comprises a voltage controlled oscillator (VCO), a low noise fractional-N phase-locked loop (PLL) and a loop filter, all of which are fully integrated and automatically calibrated. This agile frequency synthesizer facilitates the implementation of frequency-hopping spread spectrum (FHSS) systems.

The smart wake mode (SWM) allows the ADF7024 to wake up autonomously from sleep using the internal wake-up timer without intervention from the host processor. This functionality allows carrier sense, packet sniffing, and packet reception while the host processor is in sleep, thereby reducing overall system current consumption.

The ADF7024 eases the processing burden of the host processor by integrating the lower layers of a typical communication protocol stack. The host processor can configure the ADF7024 using a simple command-based protocol over a standard 4-wire SPI interface. A single-byte command transitions the radio between states or performs a radio function.

A complete wireless solution can be built using a small number of external discrete components and a host processor (typically a microcontroller).

For more information, see the ADF7024 Hardware Reference Manual, UG-698, which is only available as part of the ADF7024 design resource package.

Table 1. Radio Profiles

Radio Profile	Data Rate (kbps)	Modulation	Frequency Deviation (kHz)	IF Bandwidth (kHz)	Typical Channel Spacing (kHz)	RF Range (MHz)
A	9.6	FSK/GFSK	9.6	100	200	862 to 928
B	38.4	FSK/GFSK	20	100	200	431 to 435, 862 to 928
C	50	FSK/GFSK	25	100	200	862 to 928
D	100	FSK/GFSK	25	100	200	862 to 928
E	200	FSK/GFSK	50	200	400	862 to 928
F	300	FSK/GFSK	75	300	600	862 to 928

SPECIFICATIONS

V_{DD} = VDDBAT1 = VDDBAT2 = 2.2 V to 3.6 V, GND = 0 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical specifications are at V_{DD} = 3 V, T_A = 25°C.

RF AND SYNTHESIZER SPECIFICATIONS

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
RF CHARACTERISTICS					
Frequency Ranges	862		928	MHz	All radio profiles
	431		435	MHz	Radio Profile B only
PHASE-LOCKED LOOP (PLL)					
Channel Frequency Resolution		396.7		Hz	
Phase Noise (In-Band)		−88		dBc/Hz	10 kHz offset, PA output power = 10 dBm, RF = 868 MHz
Phase Noise at Offset					
1 MHz		−126		dBc/Hz	PA output power = 10 dBm, RF = 868 MHz
2 MHz		−131		dBc/Hz	PA output power = 10 dBm, RF = 868 MHz
10 MHz		−142		dBc/Hz	PA output power = 10 dBm, RF = 868 MHz
VCO Calibration Time		142		µs	
Synthesizer Settling Time		56		µs	Frequency synthesizer settles to within ±5 ppm of the target frequency within this time following the VCO calibration in transmit and receive
CRYSTAL OSCILLATOR					
Crystal Frequency		26		MHz	Parallel load resonant crystal
Recommended Load Capacitance	7		18	pF	
Maximum Crystal ESR		1800		Ω	26 MHz crystal with 18 pF load capacitance
Pin Capacitance		2.1		pF	Capacitance for XOSC26P and XOSC26N
Start-Up Time		310		µs	26 MHz crystal with 7 pF load capacitance
		388		µs	26 MHz crystal with 18 pF load capacitance
SPURIOUS EMISSIONS					
Integer Boundary Spurious					
910.1 MHz		−39		dBc	Radio Profile A, integer boundary spur at 910 MHz (26 MHz × 35), inside synthesizer loop bandwidth
911.0 MHz		−79		dBc	Radio Profile A, integer boundary spur at 910 MHz (26 MHz × 35), outside synthesizer loop bandwidth
Reference Spurious					
868 MHz/915 MHz		−80		dBc	Radio Profile A
Clock Related Spur Level		−60		dBc	Measured in a span of ±350 MHz, RF = 868.95 MHz, PA output power = 10 dBm, V_{DD} = 3.6 V

TRANSMITTER SPECIFICATIONS

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DATA RATE					
Radio Profile A		9.6		kbps	
Radio Profile B		38.4		kbps	
Radio Profile C		50		kbps	
Radio Profile D		100		kbps	
Radio Profile E		200		kbps	
Radio Profile F		300		kbps	
FSK/GFSK FREQUENCY DEVIATION					
Radio Profile A		9.6		kHz	
Radio Profile B		20		kHz	
Radio Profile C		25		kHz	
Radio Profile D		25		kHz	
Radio Profile E		50		kHz	
Radio Profile F		75		kHz	
GAUSSIAN FILTER BANDWITH TIME (BT)		0.5			Not programmable
POWER AMPLIFIER					
Maximum Power[1]		13.5		dBm	Programmable, separate PA and LNA match[2]
Minimum Power		−20		dBm	
Transmit Power					
Variation vs. Temperature		±0.5		dB	−40°C to +85°C, RF = 868 MHz
Variation vs. V_{DD}		±1		dB	2.2 V to 3.6 V, RF = 868 MHz
Flatness		±1		dB	902 MHz to 928 MHz and 863 MHz to 870 MHz
Programmable Step Size		0.5		dB	−20 dBm to +13.5 dBm, programmable in 60 steps
HARMONICS					868 MHz, unfiltered conductive, PA output power = 10 dBm
Second Harmonic		−15.1		dBc	
Third Harmonic		−29.3		dBc	
All Other Harmonics		−47.6		dBc	
OPTIMUM PA LOAD IMPEDANCE					
PA Output in Transmit Mode					
f_{RF} = 915 MHz		50.8 + j10.2		Ω	
f_{RF} = 868 MHz		45.5 + j12.1		Ω	
f_{RF} = 433 MHz		46.8 + j19.9		Ω	
PA Output in Receive Mode					
f_{RF} = 915 MHz		9.4 − j124		Ω	
f_{RF} = 868 MHz		9.5 − j130.6		Ω	
f_{RF} = 433 MHz		11.9 − j260.1		Ω	

[1] Measured as the maximum unmodulated power.
[2] A combined single-ended PA and LNA match can reduce the maximum achievable output power by as much as 1 dB.

RECEIVER SPECIFICATIONS

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT SENSITIVITY, BIT ERROR RATE (BER)[1]					BER = 10^{-3}, LNA and PA matched separately[2]
Radio Profile A		−111		dBm	9.6 kbps
Radio Profile B		−107.5		dBm	38.4 kbps
Radio Profile C		−107.4		dBm	50 kbps
Radio Profile D		−105		dBm	100 kbps
Radio Profile E		−103		dBm	200 kbps
Radio Profile F		−100.5		dBm	300 kbps
INPUT SENSITIVITY, PACKET ERROR RATE (PER)[3]					At PER = 1%, LNA and PA matched separately,[2] packet length = 128 bits
Radio Profile A		−110.6		dBm	9.6 kbps
Radio Profile B		−106		dBm	38.4 kbps
Radio Profile C		−104.1		dBm	50 kbps
Radio Profile D		−102.6		dBm	100 kbps
Radio Profile E		−99.1		dBm	200 kbps
Radio Profile F		−97.9		dBm	300 kbps
LNA AND MIXER, INPUT IP3					Receiver local oscillator (LO) frequency (f_{LO}) = 914.8 MHz, $f_{SOURCE1} = f_{LO} + 0.4$ MHz, $f_{SOURCE2} = f_{LO} + 0.7$ MHz
LNA Gain					
Minimum		−11.5		dBm	
Maximum		−12.2		dBm	
LNA AND MIXER, INPUT IP2					f_{LO} = 920.8 MHz, $f_{SOURCE1} = f_{LO} + 1.1$ MHz, $f_{SOURCE2} = f_{LO} + 1.3$ MHz
Gain					
Maximum LNA, Maximum Mixer		18.5		dBm	
Minimum LNA, Minimum Mixer		27		dBm	
LNA AND MIXER, 1 dB COMPRESSION POINT					RF = 915 MHz
Gain					
Maximum LNA, Maximum Mixer		−21.9		dBm	
Minimum LNA, Minimum Mixer		−21		dBm	
ADJACENT CHANNEL REJECTION					
CW Interferer					Wanted signal 3 dB above the input sensitivity level (BER = 10^{-3}), CW interferer power level increased until BER = 10^{-3}, image calibrated
200 kHz Channel Spacing		41		dB	Radio Profile B, RF = 433 MHz
400 kHz Channel Spacing		40		dB	Radio Profile E
600 kHz Channel Spacing		41		dB	Radio Profile F
Modulated Interferer					Wanted signal 3 dB above the input sensitivity level (BER = 10^{-3}), modulated interferer with the same modulation as the wanted signal; interferer power level increased until BER = 10^{-3}, image calibrated
200 kHz Channel Spacing		37		dB	Radio Profile B, RF = 433 MHz
400 kHz Channel Spacing		34		dB	Radio Profile E
600 kHz Channel Spacing		35		dB	Radio Profile F
CO-CHANNEL REJECTION		−4		dB	Desired signal 10 dB above the input sensitivity level (BER = 10^{-3}), Radio Profile B, RF = 868 MHz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
BLOCKING					Desired signal 3 dB above the input sensitivity level (BER = 10^{-3}), carrier wave interferer, power level increased until BER = 10^{-3}, Radio Profile B
RF = 433 MHz					
±2 MHz		68		dB	
±10 MHz		76		dB	
RF = 868 MHz					
±2 MHz		66		dB	
±10 MHz		74		dB	
RF = 915 MHz					
±2 MHz		66		dB	
±10 MHz		74		dB	
BLOCKING, ETSI EN 300 220					Measurement procedure as per ETSI EN 300-220-1 V2.3.1; desired signal 3 dB above the ETSI EN 300-220 reference sensitivity level of −99 dBm, Radio Profile B, unmodulated interferer
±2 MHz		−28		dBm	
±10 MHz		−20.5		dBm	
WIDEBAND INTERFERENCE REJECTION		75		dB	RF = 868 MHz, swept from 10 MHz to 100 MHz either side of the RF
IMAGE CHANNEL ATTENUATION					Measured as image attenuation at the IF filter output, carrier wave interferer at 400 kHz below the channel frequency, 100 kHz IF filter bandwidth
868 MHz, 915 MHz		36/45		dB	Uncalibrated/calibrated
433 MHz		40/54		dB	Uncalibrated/calibrated
AFC					
Accuracy		1		kHz	
RSSI					
Range at Input		−97 to −26		dBm	
Linearity		±2		dB	
Absolute Accuracy		±3		dB	
MAXIMUM RF INPUT LEVEL		12		dBm	
LNA INPUT IMPEDANCE, DIFFERENTIAL					
Receive Mode					
f_{RF} = 915 MHz		75.9 – j32.3		Ω	
f_{RF} = 868 MHz		78.0 – j32.4		Ω	
f_{RF} = 433 MHz		95.5 – j23.9		Ω	
Transmit Mode					
f_{RF} = 915 MHz		7.6 + j9.2		Ω	
f_{RF} = 868 MHz		7.7 + j8.6		Ω	
f_{RF} = 433 MHz		7.9 + j4.6		Ω	
RX SPURIOUS EMISSIONS[4]					
Maximum < 1 GHz		−66		dBm	At antenna input, unfiltered conductive
Maximum > 1 GHz		−62		dBm	At antenna input, unfiltered conductive

[1] Sensitivity measured with FSK modulation.
[2] Sensitivity for combined Tx/Rx matching network case is typically 1 dB less than separate Tx/Rx matching networks.
[3] Sensitivity measured with FSK modulation and AFC disabled.
[4] Follow the matching and layout guidelines to achieve the relevant FCC/ETSI specifications.

TIMING AND DIGITAL SPECIFICATIONS

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Rx AND Tx TIMING PARAMETERS						
PHY_ON to PHY_RX (on CMD_PHY_RX)			300		µs	Includes VCO calibration and synthesizer settling
PHY_ON to PHY_TX (on CMD_PHY_TX)			296		µs	Includes VCO calibration and synthesizer settling, does not include PA ramp-up
LOGIC INPUTS						
Input Voltage						
High	V_{INH}	$0.7 \times V_{DD}$			V	
Low	V_{INL}			$0.2 \times V_{DD}$	V	
Input Current	I_{INH}/I_{INL}			±1	µA	
Input Capacitance	C_{IN}			10	pF	
LOGIC OUTPUTS						
Output Voltage						
High	V_{OH}	$V_{DD} - 0.4$			V	I_{OH} = 500 µA
Low	V_{OL}			0.4	V	I_{OL} = 500 µA
GPx Rise/Fall				5	ns	
GPx Load				10	pF	
Maximum Output Current			5		mA	
ATB OUTPUTS						Used for external PA and LNA control
ADCIN_ATB3 and ATB4						
Output High Voltage, V_{OH}			1.8		V	
Output Low Voltage, V_{OL}			0.1		V	
Maximum Output Current			0.5		mA	
GP5_ATB1 and ATB2						
Output High Voltage, V_{OH}			V_{DD}		V	
Output Low Voltage, V_{OL}			0.1		V	
Maximum Output Current			5		mA	

AUXILARY BLOCK SPECIFICATIONS

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
32 kHz RC OSCILLATOR					
Frequency		32.768		kHz	After calibration
Frequency Accuracy		1.5		%	After calibration at 25°C
Frequency Drift					
Temperature Coefficient		0.14		%/°C	
Voltage Coefficient		4		%/V	
Calibration Time		1.25		ms	
WAKE-UP CONTROLLER (WUC)					
Hardware Timer					
Wake-Up Period	61×10^{-6}		1.31×10^{5}	sec	
Firmware Timer					
Wake-Up Period	1		2^{16}	Hardware periods	Firmware counter counts of the number of hardware wake-up cycles, resolution of 16 bits
ADC					
Resolution		8		Bits	
DNL		±1		LSB	V_{DD} from 2.2 V to 3.6 V, T_A = 25°C
INL		±1		LSB	V_{DD} from 2.2 V to 3.6 V, T_A = 25°C
Conversion Time		1		µs	
Input Capacitance		12.4		pF	
BATTERY MONITOR					
Absolute Accuracy		±45		mV	
Alarm Voltage Set Point	1.7		2.7	V	
Alarm Voltage Step Size		62		mV	5-bit resolution
Start-Up Time			100	µs	
Current Consumption		30		µA	When enabled
TEMPERATURE SENSOR					
Range	−40		+85	°C	
Resolution		0.3		°C	With averaging
Accuracy of Temperature Readback		−4 to +7		°C	Temperature range = −40°C to +85°C (calibrated at 25°C)
		±4		°C	Temperature range = −36°C to +84°C (calibrated at 25°C)
		±3		°C	Temperature range = −12°C to +79°C (calibrated at 25°C)

GENERAL SPECIFICATIONS

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TEMPERATURE RANGE, T_A	−40		+85	°C	
VOLTAGE SUPPLY					
V_{DD}	2.2		3.6	V	Applied to VDDBAT1 and VDDBAT2
TRANSMIT CURRENT CONSUMPTION					In the PHY_TX state, PA matched to 50 Ω, separate PA and LNA match
433 MHz					
−10 dBm		8.7		mA	
0 dBm		12.2		mA	
10 dBm		23.3		mA	
13.5 dBm		32.1		mA	
868 MHz/915 MHz					
−10 dBm		10.3		mA	
0 dBm		13.3		mA	
10 dBm		24.1		mA	
13.5 dBm		32.1		mA	
POWER MODES					
PHY_SLEEP (Deep Sleep Mode 2)		0.18		µA	Sleep mode, memory not retained
PHY_SLEEP (Deep Sleep Mode 1)		0.33		µA	Sleep mode, memory retained
PHY_SLEEP (RC Oscillator Active)		0.75		µA	WUC active, RC oscillator running, memory retained
PHY_OFF		1		mA	Device in PHY_OFF state, 26 MHz oscillator running, digital and synthesizer regulators active, all register values retained
PHY_ON		1		mA	Device in PHY_ON state, 26 MHz oscillator running, digital, synthesizer, VCO, and RF regulators active, baseband filter calibration performed, all register values retained
PHY_RX		12.8		mA	Device in PHY_RX state
SMART WAKE MODE					Average current consumption
		21.78		µA	Autonomous reception every 1 sec, with receive dwell time of 1.25 ms, using RC oscillator, Radio Profile B
		11.75		µA	Autonomous reception every 1 sec, with receive dwell time of 0.5 ms, using RC oscillator, Radio Profile F

TIMING SPECIFICATIONS

V_{DD} = VDDBAT1 = VDDBAT2 = 2.2 V to 3.6 V, V_{GND} = GND = 0 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 8. SPI Interface Timing

Parameter	Limit	Unit	Test Conditions/Comments
t_2	85	ns min	$\overline{CS}$ low to SCLK setup time
t_3	85	ns min	SCLK high time
t_4	85	ns min	SCLK low time
t_5	170	ns min	SCLK period
t_6	10	ns max	SCLK falling edge to MISO delay
t_7	5	ns min	MOSI to SCLK rising edge setup time
t_8	5	ns min	MOSI to SCLK rising edge hold time
t_9	85	ns min	SCLK falling edge to $\overline{CS}$ hold time
t_{11}	270	ns min	$\overline{CS}$ high time
t_{12}	310	µs typ	$\overline{CS}$ low to MISO high wake-up time, 26 MHz crystal with 7 pF load capacitance, T_A = 25°C
t_{13}	20	ns max	SCLK rise time
t_{14}	20	ns max	SCLK fall time
t_{15}	25	µs max	Initialization time; do not issue a command during this time; alternatively, poll the status word and wait for the CMD_READY bit to go high

Timing Diagrams

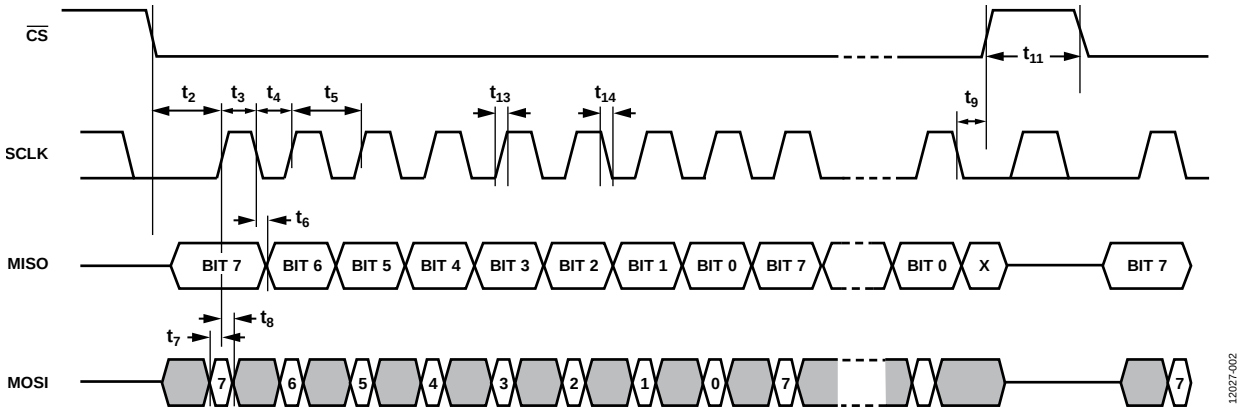

Figure 2. SPI Interface Timing

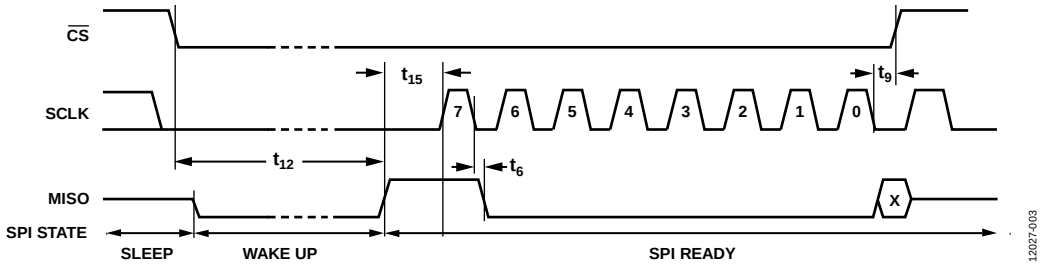

Figure 3. PHY_SLEEP to SPI Ready State Timing (SPI Ready t_{12} After the Falling Edge of $\overline{CS}$)

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 9.

Parameter	Rating
VDDBAT1, VDDBAT2 to GND	−0.3 V to +3.96 V
Operating Temperature Range	
Industrial	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	150°C
LFCSP θ_{JA} Thermal Impedance	26°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Connect the exposed pad of the LFCSP to ground.

This device is a high performance, RF integrated circuit with an ESD rating of <2 kV; it is ESD sensitive. Take proper precautions for handling and assembly.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

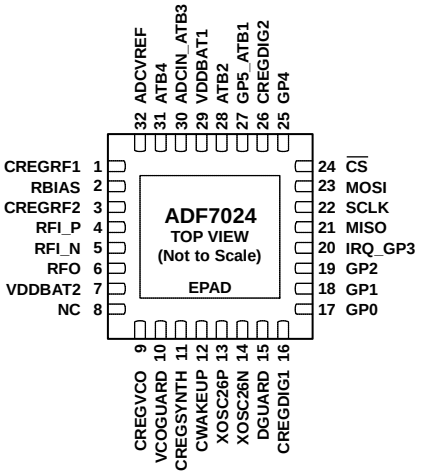

Figure 4. Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CREGRF1	Regulator Voltage for RF. For regulator stability and noise rejection, place a 220 nF capacitor between this pin and ground.
2	RBIAS	External Bias Resistor. Place a 36 kΩ resistor with 2% tolerance between this pin and ground.
3	CREGRF2	Regulator Voltage for RF. For regulator stability and noise rejection, place a 220 nF capacitor between this pin and ground.
4	RFI_P	LNA Positive Input in Receive Mode.
5	RFI_N	LNA Negative Input in Receive Mode.
6	RFO	PA Output.
7	VDDBAT2	Power Supply Pin 2. Place decoupling capacitors to the ground plane as close as possible to this pin.
8	NC	No Connect. Do not connect to this pin.
9	CREGVCO	Regulator Voltage for the VCO. For regulator stability and noise rejection, place a 220 nF capacitor between this pin and ground.
10	VCOGUARD	Guard/Screen for VCO. Connect this pin to Pin 9.
11	CREGSYNTH	Regulator Voltage for the Synthesizer. For regulator stability and noise rejection, place a 220 nF capacitor between this pin and ground.
12	CWAKEUP	External Capacitor for Wake-Up Control. Place a 150 nF capacitor between this pin and ground.
13	XOSC26P	Crystal Oscillator, Positive. Connect the 26 MHz reference crystal between this pin and XOSC26N. If an external reference is connected to XOSC26N, leave this pin open circuited.
14	XOSC26N	Crystal Oscillator, Negative. Connect the 26 MHz reference crystal between this pin and XOSC26P. Alternatively, an external 26 MHz reference signal can be ac-coupled to this pin.
15	DGUARD	Internal Guard/Screen for the Digital Circuitry. Connect this pin to Pin 16, CREGDIG1.
16	CREGDIG1	Regulator Voltage for Digital Section of the Chip. For regulator stability and noise rejection, place a 220 nF capacitor between this pin and ground.
17	GP0	Digital GPIO Pin 0.
18	GP1	Digital GPIO Pin 1.
19	GP2	Digital GPIO Pin 2.
20	IRQ_GP3	Interrupt Request/Digital GPIO Test Pin 3.
21	MISO	Serial Port Master Input/Slave Output.
22	SCLK	Serial Port Clock.
23	MOSI	Serial Port Master Output/Slave Input.
24	$\overline{CS}$	Chip Select (Active Low). A pull-up resistor of 100 kΩ to V_{DD} is recommended to prevent the host processor from inadvertently waking the ADF7024 from sleep.
25	GP4	Digital GPIO Test Pin 4.

Pin No.	Mnemonic	Description
26	CREGDIG2	Regulator Voltage for Digital Section of the Chip. For regulator stability and noise rejection, place a 220 nF capacitor between this pin and ground.
27	GP5_ATB1	Digital GPIO Test Pin 5/Analog Test Pin 1.
28	ATB2	Analog Test Pin 2.
29	VDDBAT1	Digital Power Supply Pin One. Place decoupling capacitors to the ground plane as close as possible to this pin.
30	ADCIN_ATB3	Analog-to-Digital Converter Input/Analog Test Pin 3.
31	ATB4	Analog Test Pin 4.
32	ADCVREF	ADC Reference Output. Place a 220 nF capacitor between this pin and ground for adequate noise rejection.
	EPAD	Exposed Package Pad. Connect the exposed pad to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

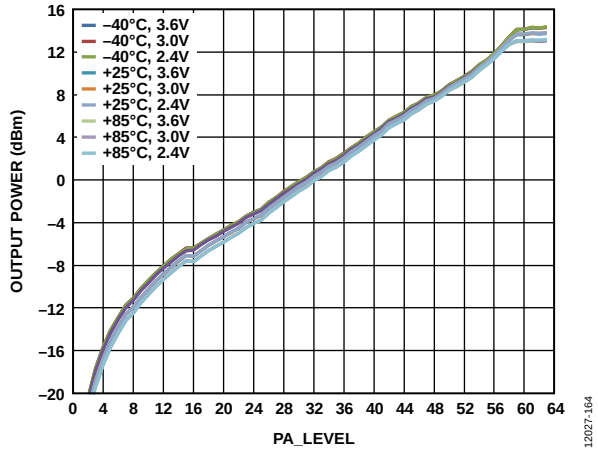

Figure 5. Output Power vs. PA_LEVEL Setting, Temperature, and V_{DD} at 433 MHz

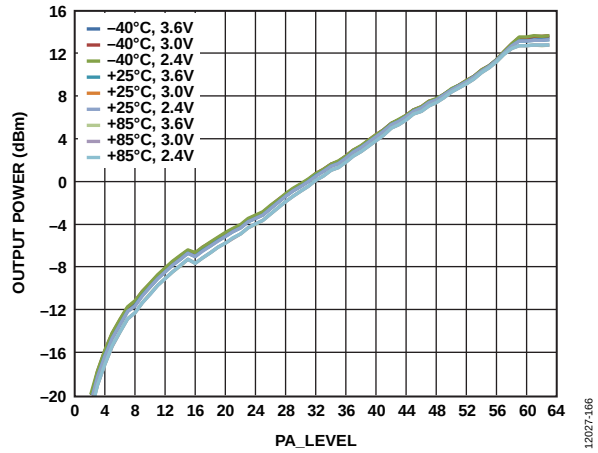

Figure 6. Output Power vs. PA_LEVEL Setting, Temperature, and V_{DD} at 868 MHz

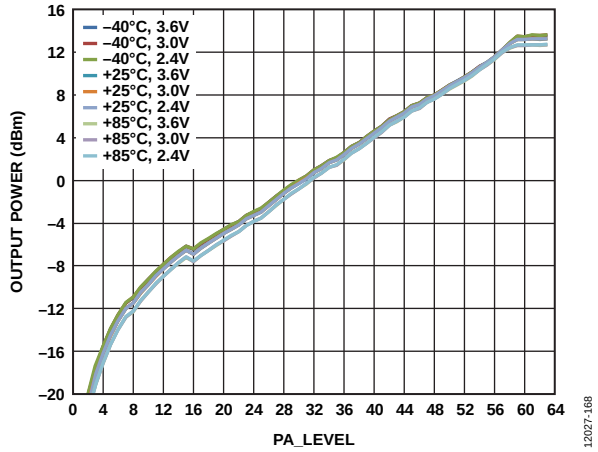

Figure 7. Output Power vs. PA_LEVEL Setting, Temperature, and V_{DD} at 915 MHz

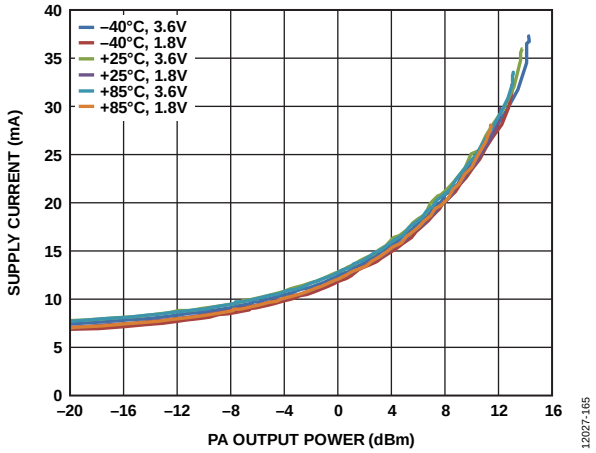

Figure 8. Supply Current vs. PA Output Power, Temperature, and V_{DD} at 433 MHz (Minimum Recommended V_{DD} = 2.2 V, 1.8 V Operation Shown for Robustness)

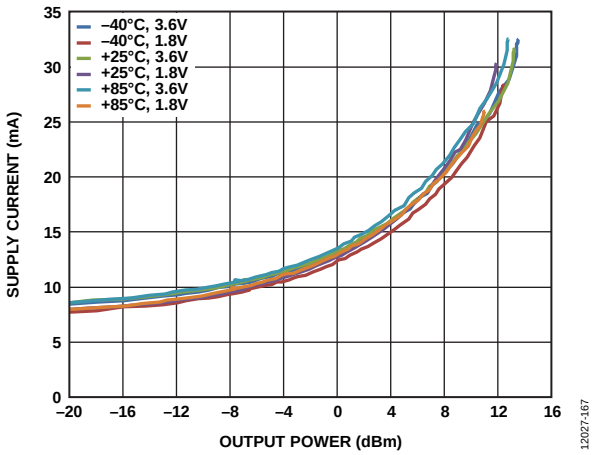

Figure 9. Supply Current vs. Output Power, Temperature, and V_{DD} at 868 MHz (Minimum Recommended V_{DD} = 2.2 V, 1.8 V Operation Shown for Robustness)

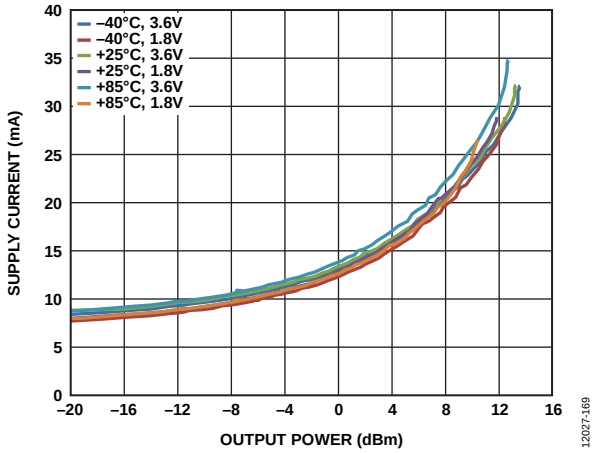

Figure 10. Supply Current vs. Output Power, Temperature, and V_{DD} at 915 MHz (Minimum Recommended V_{DD} = 2.2 V, 1.8 V Operation Shown for Robustness)

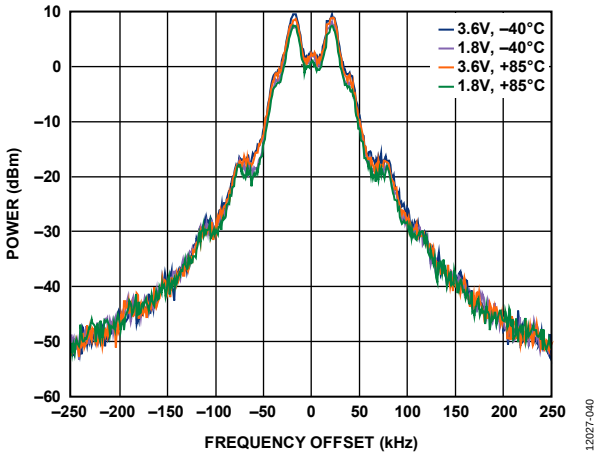

Figure 11. Transmit Spectrum at 868 MHz, FSK, Radio Profile B, (Minimum Recommended V_{DD} = 2.2 V, 1.8 V Operation Shown for Robustness)

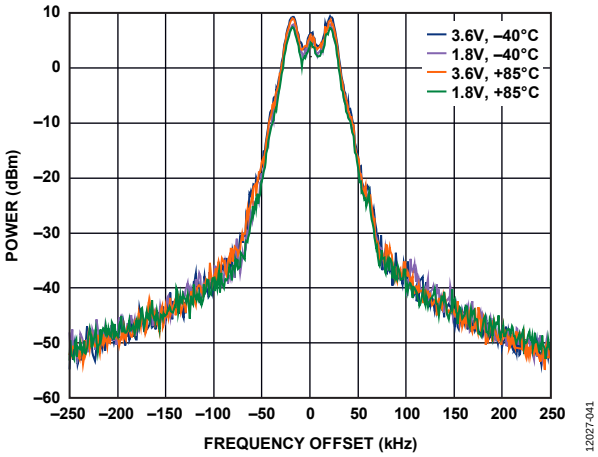

Figure 12. Transmit Spectrum at 868 MHz, GFSK, Radio Profile B, (Minimum Recommended V_{DD} = 2.2 V, 1.8 V Operation Shown for Robustness)

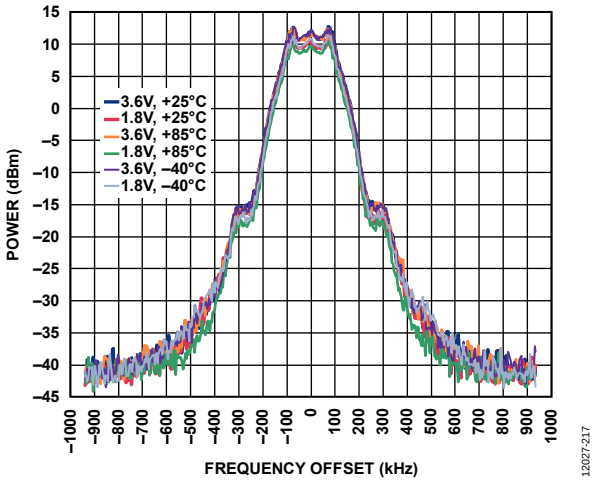

Figure 13. Transmit Spectrum at 928 MHz, GFSK, Radio Profile F, (Minimum Recommended V_{DD} = 2.2 V, 1.8 V Operation Shown for Robustness)

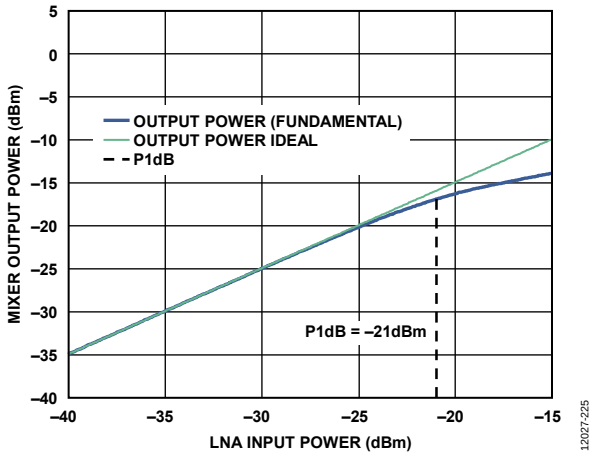

Figure 14. LNA/Mixer 1 dB Compression Point, V_{DD} = 3.0 V, Temperature = 25°C, RF = 915 MHz, LNA Gain = Low, Mixer Gain = Low

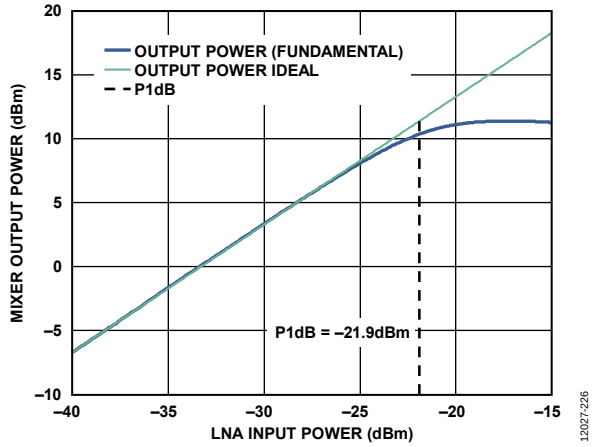

Figure 15. LNA/Mixer 1 dB Compression Point, V_{DD} = 3.0 V, Temperature = 25°C, RF = 915 MHz, LNA Gain = High, Mixer Gain = High

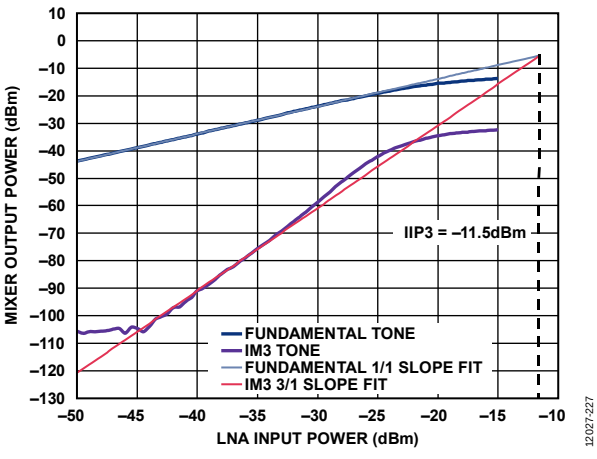

Figure 16. LNA/Mixer IIP3, V_{DD} = 3.0 V, Temperature = 25°C, RF = 915 MHz, LNA Gain = Low, Mixer Gain = Low, Source 1 Frequency = 915 MHz + 0.4 MHz, Source 2 Frequency = 915 MHz + 0.7 MHz

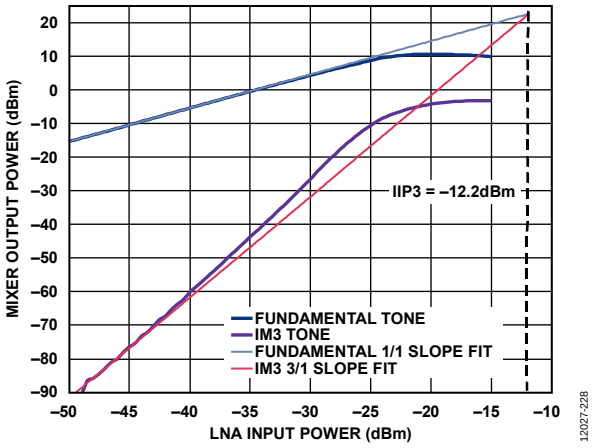

Figure 17. LNA/Mixer IIP3, V_{DD} = 3.0 V, Temperature = 25°C, RF = 915 MHz, LNA Gain = High, Mixer Gain = High, Source 1 Frequency = 915 MHz + 0.4 MHz, Source 2 Frequency = 915 MHz + 0.7 MHz

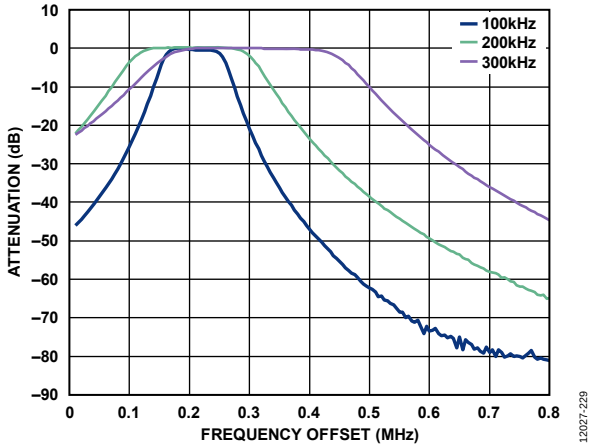

Figure 18. IF Filter Profile vs. IF Bandwidth, V_{DD} = 3.0 V, Temperature = 25°C

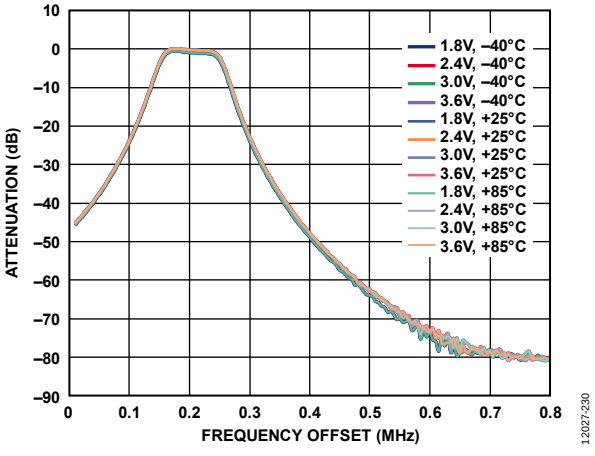

Figure 19. IF Filter Profile vs. V_{DD} and Temperature, 100 kHz IF Filter Bandwidth (Minimum Recommended V_{DD} = 2.2 V, 1.8 V Operation Shown for Robustness)

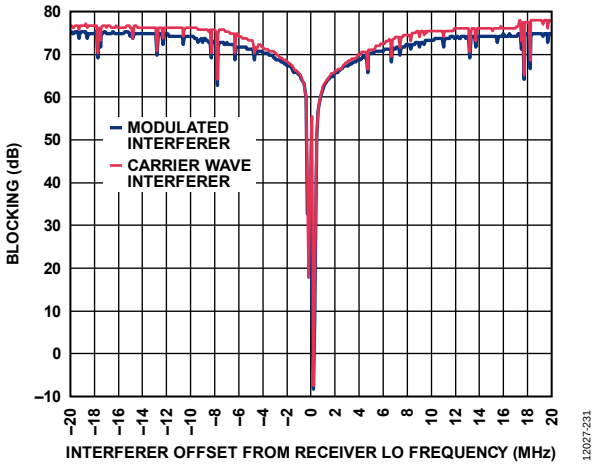

Figure 20. Receiver Wideband Blocking at 433 MHz, Radio Profile B

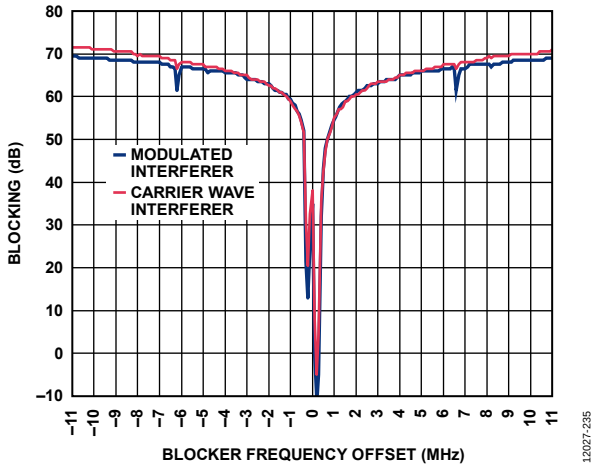

Figure 21. Receiver Wideband Blocking at 868 MHz, Radio Profile D

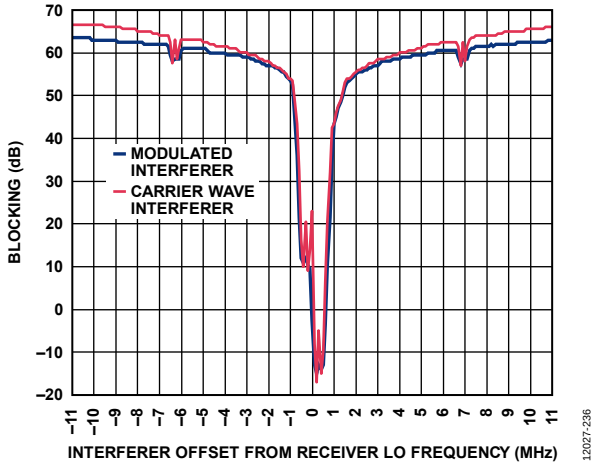

Figure 22. Receiver Wideband Blocking at 868 MHz, Radio Profile F

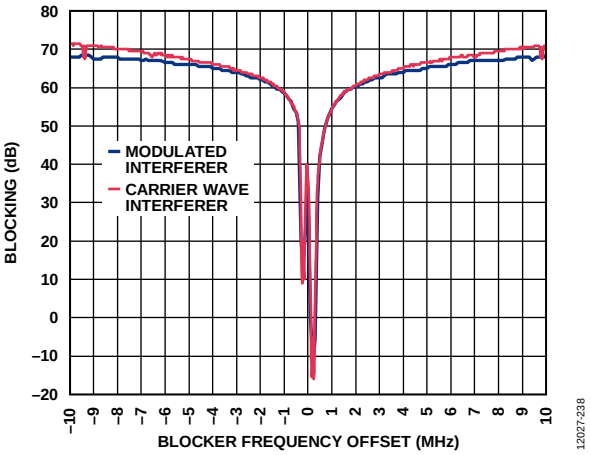

Figure 23. Receiver Wideband Blocking at 915 MHz, Radio Profile D

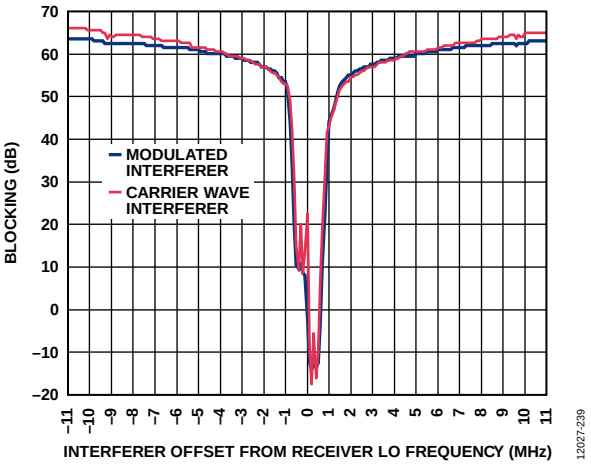

Figure 24. Receiver Wideband Blocking at 915 MHz, Radio Profile F

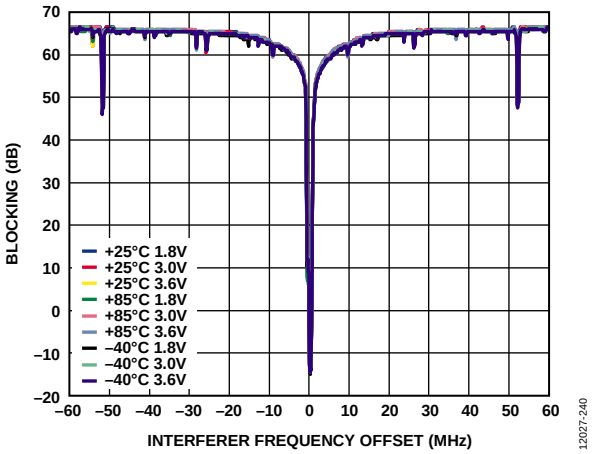

Figure 25. Receiver Wideband Blocking vs. V_{DD} and Temperature, 915 MHz, Radio Profile F

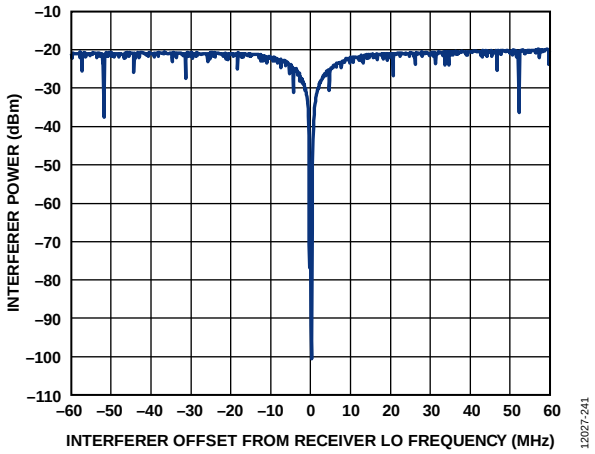

Figure 26. Receiver Wideband Blocking at 868 MHz, Radio Profile B, Measured as per ETSI EN 300 220

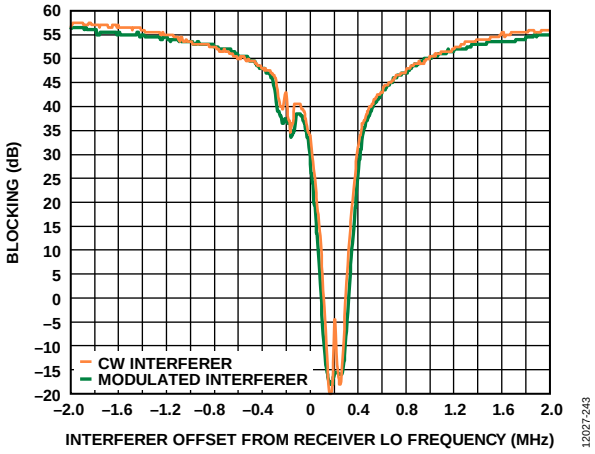

Figure 27. Receiver Close-In Blocking at 915 MHz, Radio Profile D, Image Calibrated

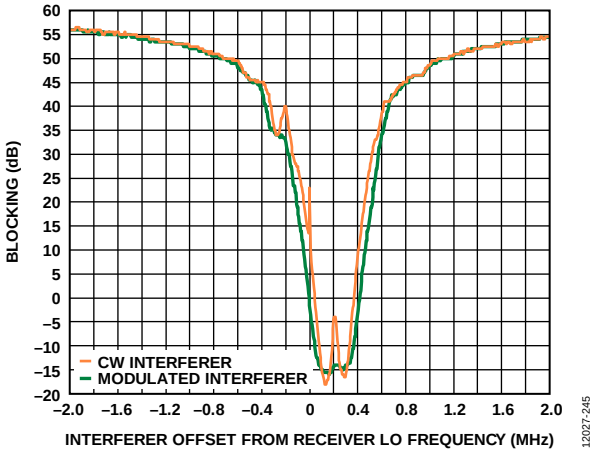

Figure 28. Receiver Close-In Blocking at 915 MHz, Radio Profile E, Image Calibrated

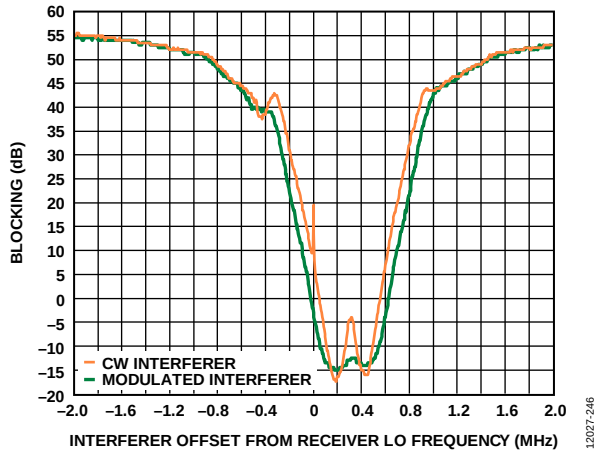

Figure 29. Receiver Close-In Blocking at 915 MHz, Radio Profile F, Image Calibrated

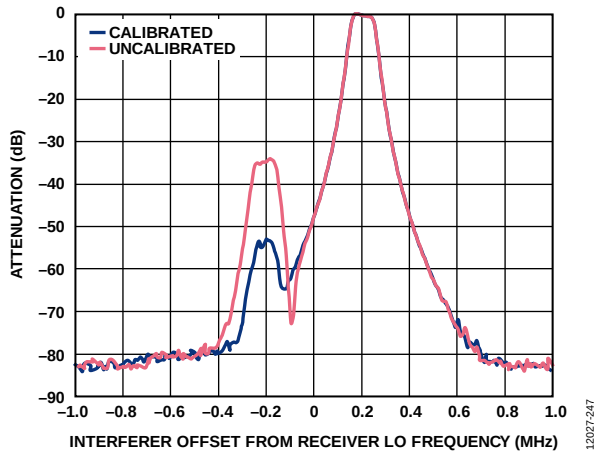

Figure 30. Image Attenuation with Calibrated and Uncalibrated Images, 915 MHz, IF Filter Bandwidth = 100 kHz, V_{DD} = 3.0 V, Temperature = 25°C

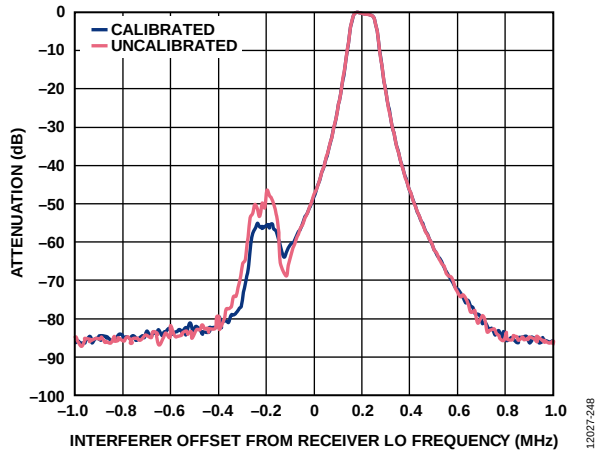

Figure 31. Image Attenuation with Calibrated and Uncalibrated Images, 433 MHz, IF Filter Bandwidth = 100 kHz, V_{DD} = 3.0 V, Temperature = 25°C

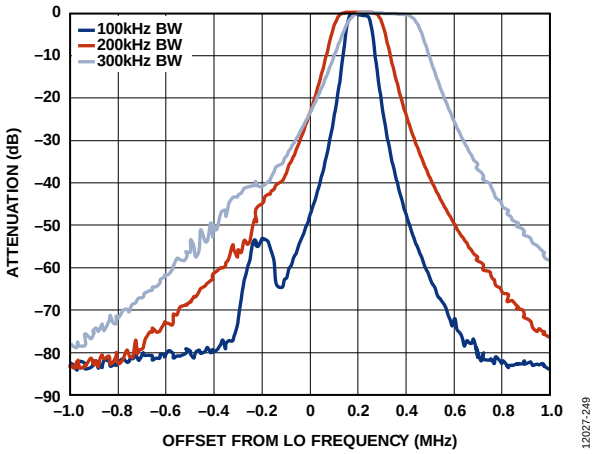

Figure 32. IF Filter Profile with Calibrated Image vs. IF Filter Bandwidth, 921 MHz, V_{DD} = 3.0 V, Temperature = 25°C

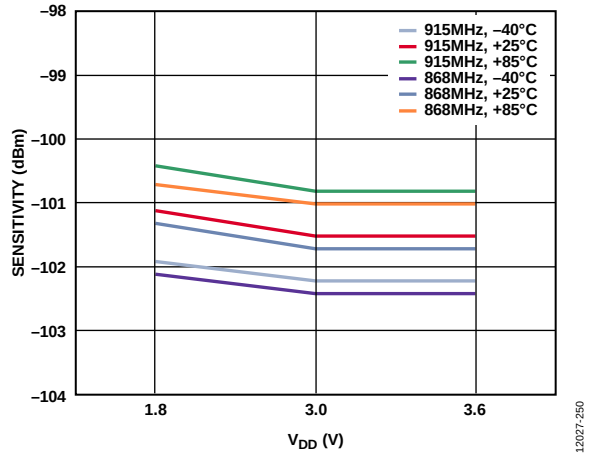

Figure 33. Receiver Sensitivity (Bit Error Rate at 10^{-3}) vs. V_{DD}, Temperature, and RF Frequency, Radio Profile F, FSK, (Minimum Recommended V_{DD} = 2.2 V, 1.8 V Operation Shown for Robustness)

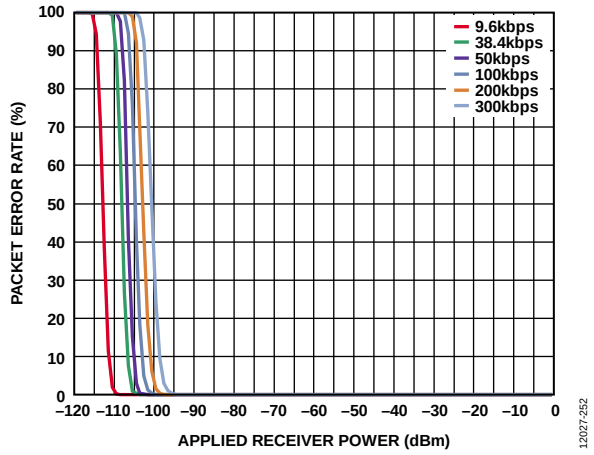

Figure 34. Packet Error Rate vs. RF Input Power and Radio Profile (Data Rate), FSK, 928 MHz, Preamble Length = 64 Bits, V_{DD} = 3.0 V, Temperature = 25°C

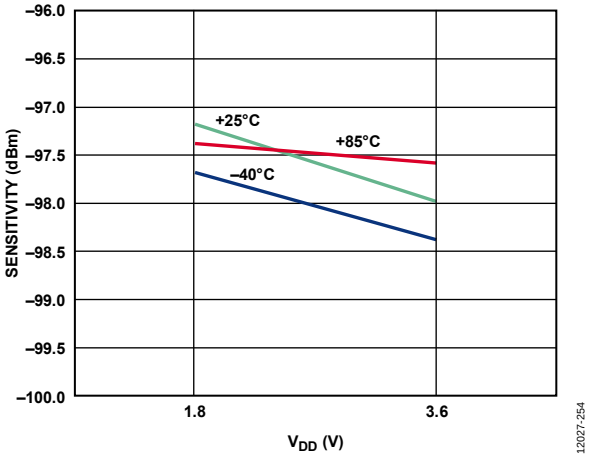

Figure 35. Receiver Sensitivity (Packet Error Rate at 1%) vs. V_{DD}, Temperature, and RF, Radio Profile F, FSK, (Minimum Recommended V_{DD} = 2.2 V, 1.8 V Operation Shown for Robustness)

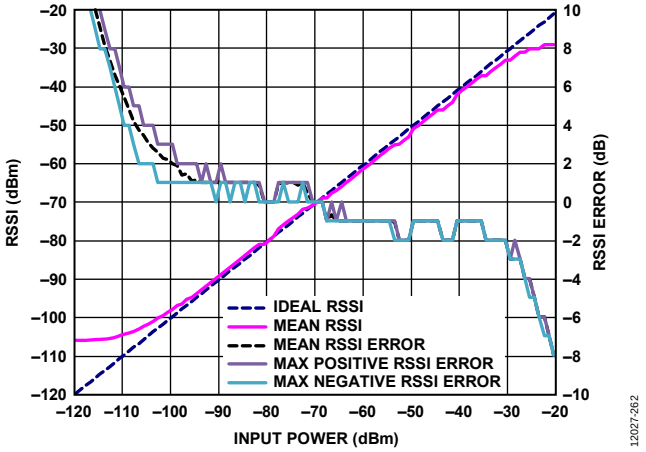

Figure 36. RSSI (via CMD_GET_RSSI) vs. RF Input Power, 868 MHz, GFSK, Radio Profile B, IF Bandwidth = 100 kHz, 100 RSSI Measurements at Each Power Level

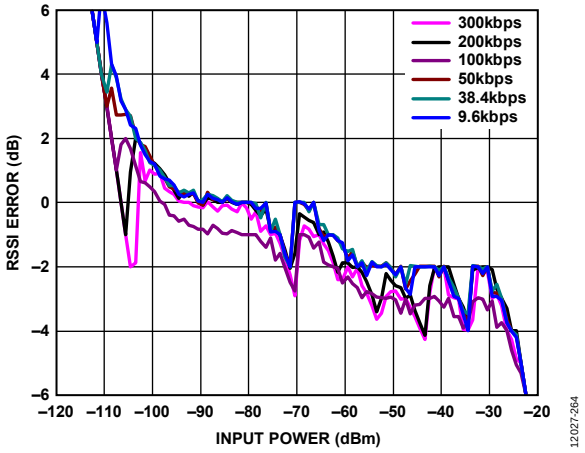

Figure 37. Mean RSSI Error (via Automatic End of Packet RSSI Measurement) vs. RF Input Power and Data Rate, RF = 868 MHz, GFSK, 100 RSSI Measurements at Each Input Power Level

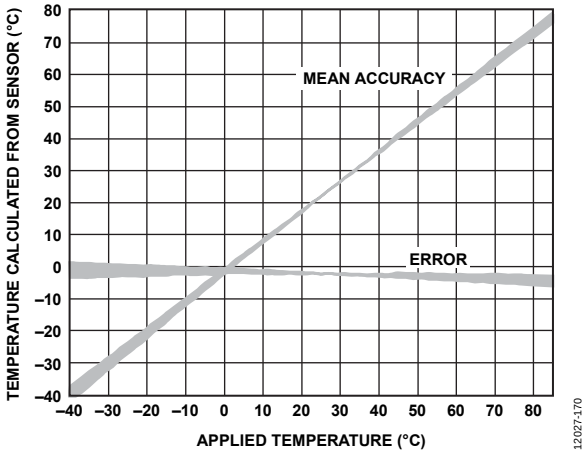

Figure 38. Typical Accuracy Range of Temperature Sensor vs. Applied Temperature, Calibration Performed at 25°C

THEORY OF OPERATION

For detailed information on the operation of the ADF7024, see the ADF7024 Hardware Reference Manual, UG-698, which is only available as part of the ADF7024 design resource package.

SPI INTERFACE

The ADF7024 is equipped with a 4-wire SPI interface, using the SCLK, MISO, MOSI, and $\overline{CS}$ pins. The ADF7024 always acts as a slave to the host processor. The SPI interface allows the host processor to perform the following operations on the ADF7024:

- Read and write to the ADF7024 memory spaces.
- Issue commands to the ADF7024.
- Read back the status of the ADF7024.
- Wake the ADF7024 from the PHY_SLEEP state.

Figure 39 shows a typical connection diagram between the processor and the ADF7024. The diagram also shows the direction of the signal flow for each pin.

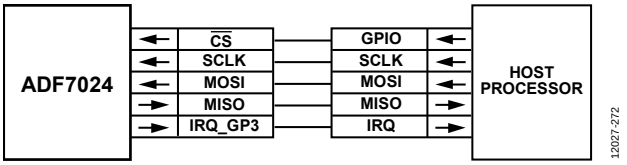

Figure 39. Host Processor Interface

The status word of the ADF7024 is returned over the MISO automatically each time a byte is transferred over the MOSI. The status word contains the current ADF7024 state, the interrupt status and flags to indicate that the ADF7024 is ready to accept a new SPI memory access command or a radio control command.

RADIO CONTROL

The ADF7024 has five radio states designated as PHY_SLEEP, PHY_OFF, PHY_ON, PHY_RX, and PHY_TX, as described in Table 11. The host processor can transition the ADF7024 between states by issuing single-byte, radio control commands over the SPI interface.

Table 11. Radio States

State	Current (Typical)	Conditions
PHY_SLEEP (Deep Sleep Mode 2)	0.18 µA	Wake-up timer off, configuration registers not retained, entered by issuing CMD_HW_RESET
PHY_SLEEP (Deep Sleep Mode 1)	0.33 µA	Wake-up timer off, configuration registers retained
PHY_SLEEP (WUC enabled)	0.75 µA	Wake-up timer on using the 32 kHz RC oscillator, configuration registers retained
PHY_OFF	1.0 mA	
PHY_ON	1.0 mA	
PHY_TX	24.1 mA	10 dBm, 868 MHz
PHY_RX	12.8 mA	

MEMORY MAP

The ADF7024 memory map is shown in Figure 40. Each memory space consists of 8-bit registers with an address length of 11 bits.

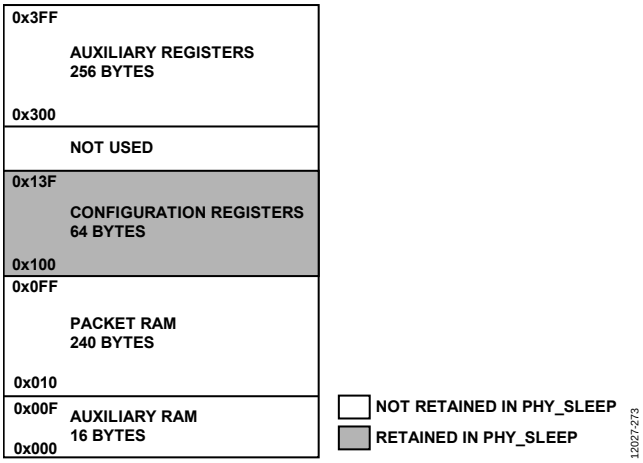

Figure 40. Memory Map

Configuration Registers

The configuration registers consist of 64 bytes of memory space used to configure the operation of the ADF7024. The radio profile registers form part of this memory space. The configuration registers are retained in the PHY_SLEEP radio state.

Auxiliary Registers

The auxiliary registers consist of 256 bytes of memory space used for auxiliary radio functions or observation of the radio blocks of the ADF7024.

Packet RAM

The packet RAM memory consists of 240 bytes of memory for storage of data from valid received packets and packet data to be transmitted.

Auxiliary RAM

The auxiliary RAM memory is reserved for use by the ADF7024.

RADIO BLOCKS

Frequency Synthesizer

A fully integrated RF synthesizer is used to generate both the transmit signal and the local oscillator (LO) signal of the receiver. A high speed, fully automatic calibration scheme ensures that the frequency and amplitude characteristics of the VCO are maintained over temperature, supply voltage, and process variations. The receive and transmit synthesizer bandwidths are automatically and independently configured to achieve optimum phase noise and settling time.

Crystal Oscillator

A 26 MHz crystal oscillator operating in parallel mode must be connected between the XOSC26P and XOSC26N pins to provide a reference for the ADF7024. Two parallel loading capacitors are required for oscillation at the correct frequency. Their values are dependent upon the crystal specification.

Transmitter

The ADF7024 supports binary frequency shift keying (FSK) and binary level Gaussian filtered FSK (GFSK) modulation. For GFSK modulation, the Gaussian filter uses a fixed BT of 0.5.

The ADF7024 PA has a single-ended output that can deliver up to 13.5 dBm of output power. The output power can be set with a typical resolution of 0.5 dB. The PA has built-in up and down ramping, which reduces spectral splatter.

Receiver

The ADF7024 is based on a fully integrated, low IF receiver architecture. The differential LNA is followed by a quadrature downconversion mixer that converts the RF signal to the IF frequency of 200 kHz (for IF filter bandwidths of 100 kHz and 200 kHz) or 300 kHz (for IF filter bandwidths of 300 kHz). The IF filter bandwidth is configured to 100 kHz, 200 kHz, or 300 kHz, depending on the radio profile selected. The bandwidth and center frequency of the IF filter are calibrated automatically.

The IF filter gives excellent interference suppression of adjacent and neighboring channels while also suppressing the image channel. The ADF7024 is capable of providing improved receiver image rejection performance by the use of a fully integrated image rejection calibration system.

A correlator demodulator is used for demodulation. An oversampled digital clock and data recovery (CDR) PLL is used to resynchronize the received bit stream to a local clock.

RADIO PROFILES

The ADF7024 radio profiles provide a set of optimized register settings for the ADF7024 radio. There are six radio profiles in total, as shown in Table 1. The profiles cover common data rates and modulation options. For further information on the ADF7024 radio profiles, see the ADF7024 Hardware Reference Manual, UG-698, which is only available as part of the ADF7024 design resource package.

PACKET MANAGEMENT

The ADF7024 includes comprehensive transmit and receive packet management capabilities and can be configured for use with a wide variety of packet-based radio protocols. There are 240 bytes of dedicated packet RAM available to store, transmit, and receive packets. In transmit mode, a preamble, sync word, and CRC can be added by the ADF7024 to the payload data stored in the packet RAM. In addition, all packet data after the sync word can be optionally whitened, Manchester encoded, or 8-bit/10-bit encoded on transmission and decoded on reception.

In receive mode, the ADF7024 can qualify received packets based on preamble detection, sync word detection, or CRC validation and generate an interrupt on the IRQ_GP3 pin. On reception of a valid packet, the received payload data is loaded to packet RAM memory.

SMART WAKE MODES

The ADF7024 can be configured to operate in a broad range of energy sensitive applications where battery lifetime is critical. This includes support for applications where the ADF7024 is required to operate in a fully autonomous mode or applications where the host processor controls the transceiver during low power mode operation. These low power modes are implemented using a hardware WUC, a firmware timer, and the SWM functionality.

The combination of the low power WUC, the firmware timer, and the SWM allows the ADF7024 to wake up autonomously from sleep without intervention from the host processor. This functionality allows carrier sense, packet sniffing, and packet reception while the host processor is in sleep, thereby dramatically reducing overall system current consumption. The SWM can then wake the host processor on an interrupt condition.

TYPICAL APPLICATION CIRCUIT

Figure 41 shows a typical application circuit for the ADF7024. All external components required for operation of the device, excluding supply decoupling capacitors, are shown. This example circuit uses a combined transmit and receive match. The bottom of the LFCSP has an exposed pad that must be soldered to ground on the PCB. The component values for the matching and harmonic filtering are dependent on the RF band and the matching topology. For more information, see the ADF7024 Hardware Reference Manual, UG-698, which is only available as part of the ADF7024 design resource package.

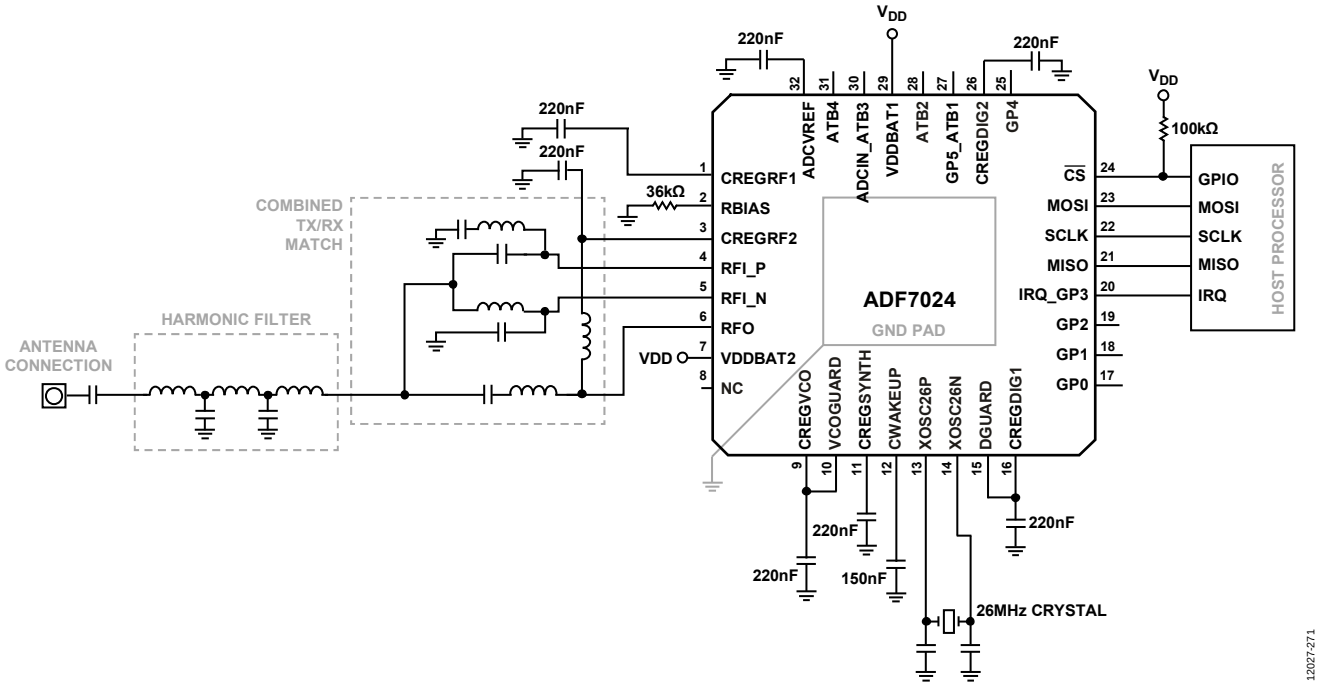

Figure 41. Typical ADF7024 Application Circuit Diagram

OUTLINE DIMENSIONS

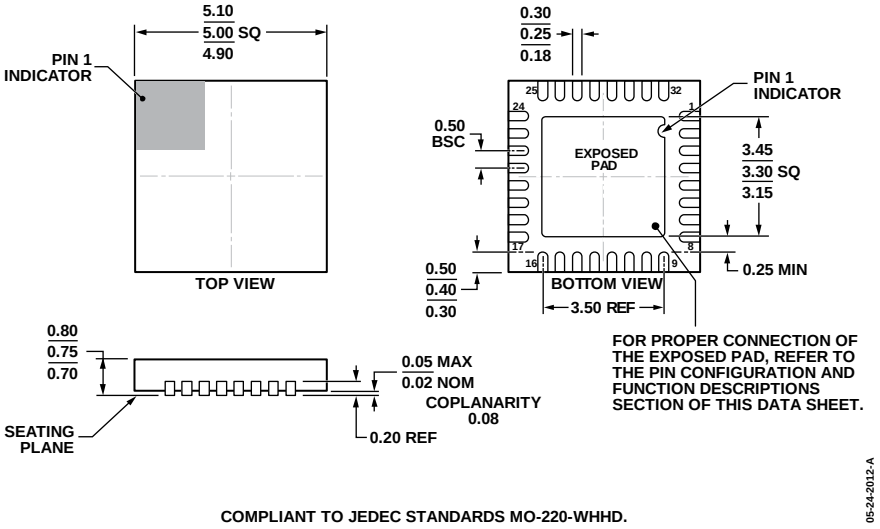

Figure 42. 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5 mm × 5 mm Body, Very Very Thin Quad
(CP-32-13)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADF7024BCPZ	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-13
ADF7024BCPZ-RL	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-13
EVAL-ADF7XXXMB4Z		Evaluation Board (Motherboard)	
EVAL-ADF7024DB1Z		Evaluation Board (RF Daughter Board, 862 MHz to 928 MHz, Separate Match)	
EVAL-ADF7024DB2Z		Evaluation Board (RF Daughter Board, 862 MHz to 928 MHz, Combined Match)	
EVAL-ADF7024DB3Z		Evaluation Board (RF Daughter Board, 431 MHz to 435 MHz, Separate Match)	
EVAL-ADF7024DB4Z		Evaluation Board (RF Daughter Board, 431 MHz to 435 MHz, Combined Match)	

[1] Z =RoHS Compliant Part.