Freescale Semiconductor
Technical Data

Document Number: MMRF1310H
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RoHS

RF Power LDMOS Transistors

N–Channel Enhancement–Mode Lateral MOSFETs

MMRF1310HR5
MMRF1310HSR5

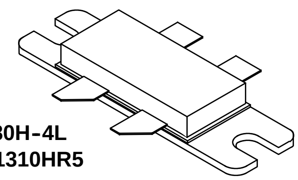
These high ruggedness devices are designed for use in high VSWR military, industrial (including laser and plasma exciters), broadcast (analog and digital), and radio/land mobile applications. They are unmatched input and output designs allowing wide frequency range utilization between 1.8 and 600 MHz.

- Typical Performance: V_{DD} = 50 Vdc, I_{DQ} = 100 mA

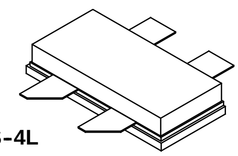
Signal Type	P_{out} (W)	f (MHz)	G_{ps} (dB)	η_D (%)	IRL (dB)
Pulse (100 μsec, 20% Duty Cycle)	300 Peak	230	26.5	74.0	–16
CW	300 Avg.	130	25.0	80.0	–15

- Capable of Handling a Load Mismatch of 65:1 VSWR @ 50 Vdc, 230 MHz, at all Phase Angles
  - 300 W CW Output Power
  - 300 W Pulse Peak Power, 20% Duty Cycle, 100 μsec
- Capable of 300 W CW Operation

1.8–600 MHz, 300 W CW, 50 V BROADBAND RF POWER MOSFETs



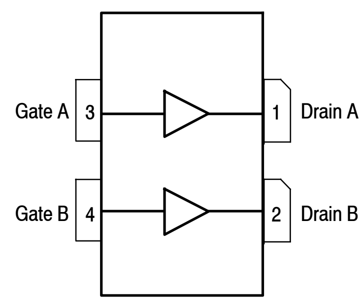
NI–780H–4L
MMRF1310HR5



NI–780S–4L
MMRF1310HSR5

Features

- Unmatched Input and Output Allowing Wide Frequency Range Utilization
- Device can be used Single–Ended or in a Push–Pull Configuration
- Qualified Up to a Maximum of 50 V_{DD} Operation
- Characterized from 30 V to 50 V for Extended Power Range
- Suitable for Linear Application with Appropriate Biasing
- Integrated ESD Protection
- Greater Negative Gate–Source Voltage Range for Improved Class C Operation
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- NI–780H–4L in Tape and Reel. R5 Suffix = 50 Units, 56 mm Tape Width, 13–inch Reel.
- NI–780S–4L in Tape and Reel. R5 Suffix = 50 Units, 32 mm Tape Width, 13–inch Reel.



(Top View)

Note: The backside of the package is the source terminal for the transistors.

Figure 1. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	–0.5, +133	Vdc
Gate–Source Voltage	V_{GS}	–6.0, +10	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature	T_C	150	°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1050 5.26	W W/°C
Operating Junction Temperature (1,2)	T_J	225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case (4) Pulse: Case Temperature 75°C, 300 W Peak, 100 μsec Pulse Width, 20% Duty Cycle, 50 Vdc, I_{DQ} = 100 mA, 230 MHz CW: Case Temperature 87°C, 300 W CW, 50 Vdc, I_{DQ} = 1100 mA, 230 MHz	 $Z_{\theta JC}$ $R_{\theta JC}$	 0.05 0.19	°C/W

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes – AN1955.
4. Same test circuit is used for both pulsed and CW.

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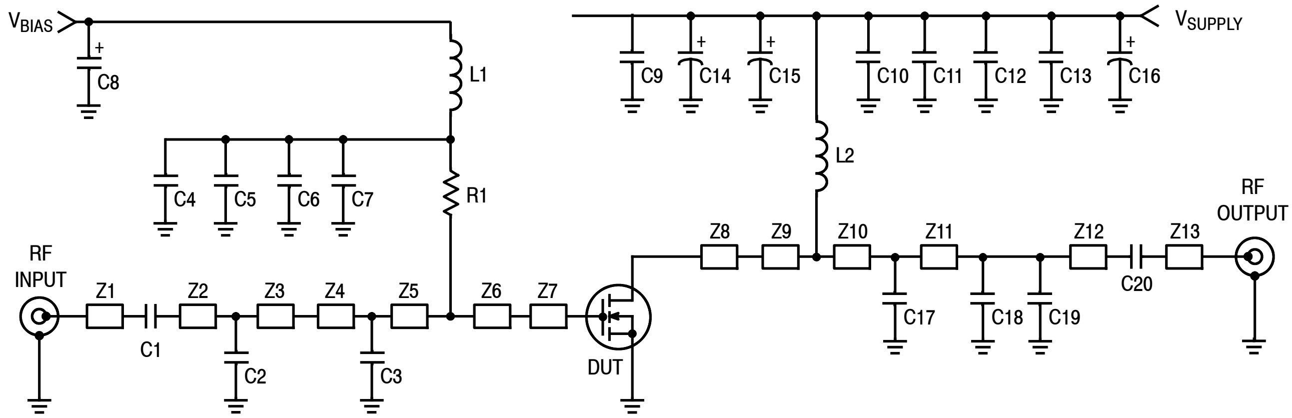
Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Machine Model (per EIA/JESD22-A115)	B
Charge Device Model (per JESD22-C101)	IV

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics (1)					
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Drain-Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 50 mA)	$V_{(BR)DSS}$	133	—	—	Vdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	5	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 100 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
On Characteristics					
Gate Threshold Voltage (1) (V_{DS} = 10 Vdc, I_D = 480 μAdc)	$V_{GS(th)}$	1.7	2.2	2.7	Vdc
Gate Quiescent Voltage (V_{DD} = 50 Vdc, I_D = 100 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	2.0	2.5	3.0	Vdc
Drain-Source On-Voltage (1) (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	—	0.25	—	Vdc
Dynamic Characteristics (1)					
Reverse Transfer Capacitance (V_{DS} = 50 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	0.8	—	pF
Output Capacitance (V_{DS} = 50 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	76	—	pF
Input Capacitance (V_{DS} = 50 Vdc, V_{GS} = 0 Vdc ± 30 mV(rms)ac @ 1 MHz)	C_{iss}	—	188	—	pF
Functional Tests (In Freescale Test Fixture, 50 ohm system) V_{DD} = 50 Vdc, I_{DQ} = 100 mA, P_{out} = 300 W Peak (60 W Avg.), f = 230 MHz, 100 μsec Pulse Width, 20% Duty Cycle					
Power Gain	G_{ps}	25.0	26.5	28.0	dB
Drain Efficiency	η_D	72.0	74.0	—	%
Input Return Loss	IRL	—	-16	-9	dB
Load Mismatch (In Freescale Application Test Fixture, 50 ohm system) V_{DD} = 50 Vdc, I_{DQ} = 100 mA					
VSWR 65:1 at all Phase Angles Pulse: P_{out} = 300 W Peak (60 W Avg.), f = 230 MHz, 100 μsec Pulse Width, 20% Duty Cycle CW: P_{out} = 300 W Avg., f = 130 MHz	Ψ	No Degradation in Output Power			

1. Each side of device measured separately.



Z1	0.352″ x 0.080″ Microstrip	Z9	0.192″ x 0.170″ Microstrip
Z2*	1.780″ x 0.080″ Microstrip	Z10*	0.366″ x 0.170″ Microstrip
Z3*	0.576″ x 0.080″ Microstrip	Z11*	2.195″ x 0.170″ Microstrip
Z4	0.220″ x 0.220″ Microstrip	Z12*	0.614″ x 0.170″ Microstrip
Z5	0.322″ x 0.220″ Microstrip	Z13	0.243″ x 0.080″ Microstrip
Z6	0.168″ x 0.220″ Microstrip		
Z7, Z8	0.282″ x 0.630″ Microstrip		

* Line length includes microstrip bends

Note: Same test circuit is used for both pulsed and CW.

Figure 2. MMRF1310HR5(HSR5) Test Circuit Schematic

Table 5. MMRF1310HR5(HSR5) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C20	15 pF Chip Capacitors	ATC100B150JT500XT	ATC
C2	82 pF Chip Capacitor	ATC100B820JT500XT	ATC
C3, C17	91 pF Chip Capacitors	ATC100B910JT500XT	ATC
C4, C10	1000 pF Chip Capacitors	ATC100B102JT50XT	ATC
C5, C11	10K pF Chip Capacitors	ATC200B103KT50XT	ATC
C6	0.1 μF, 50 V Chip Capacitor	CDR33BX104AKWS	AVX
C7	2.2 μF, 100 V Chip Capacitor	HMK432B7225KM-T	Taiyo Yuden
C8	10 μF, 35 V Tantalum Capacitor	T491D106K035AT	Kemet
C9	2.2 μF, 100 V Chip Capacitor	G2225X7R225KT3AB	ATC
C12	0.1 μF, 100 V Chip Capacitor	C1812F104K1RAC	Kemet
C13	0.01 μF, 100 V Chip Capacitor	C1825C103K1GAC	Kemet
C14, C15, C16	220 μF, 100 V Electolytic Capacitors	MCGPR100V227M16X26-RH	Multicomp
C18, C19	18 pF Chip Capacitors	ATC100B180JT500XT	ATC
L1	120 nH Inductor	1812SMS-R12JLC	Coilcraft
L2	17.5 nH Inductor	GA3095-ALC	Coilcraft
R1	1000 Ω, 1/2 W Chip Resistor	CRCW20101K00FKEF	Vishay
PCB	0.030″, ε_r = 2.55	AD255A	Arlon

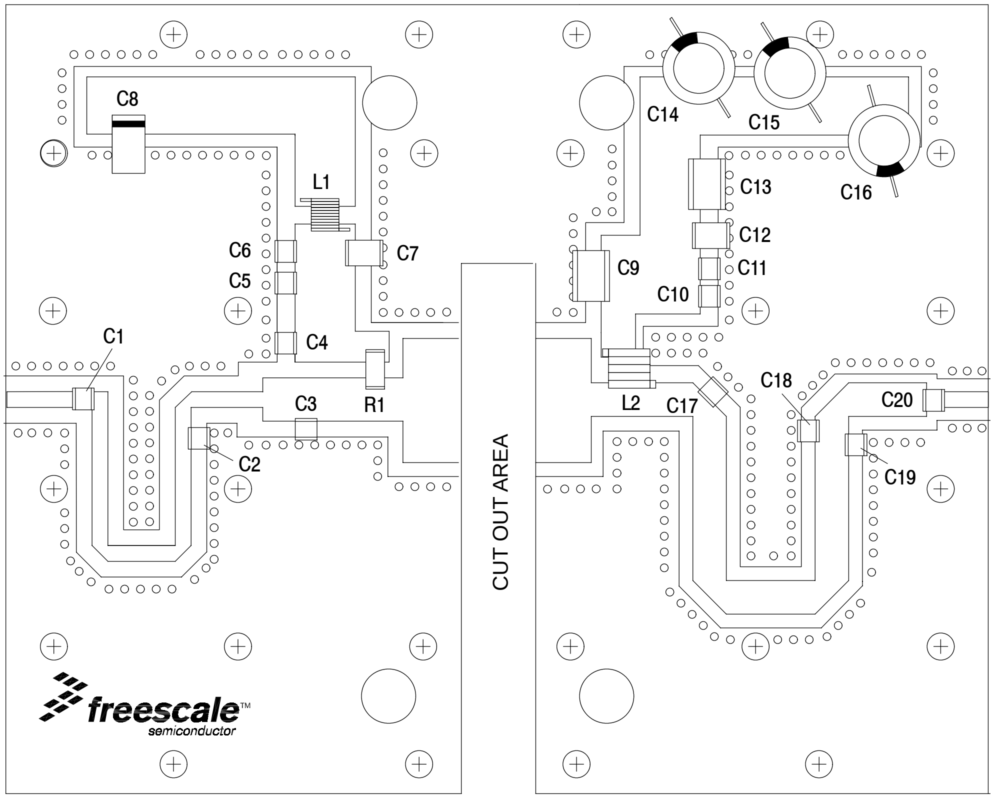
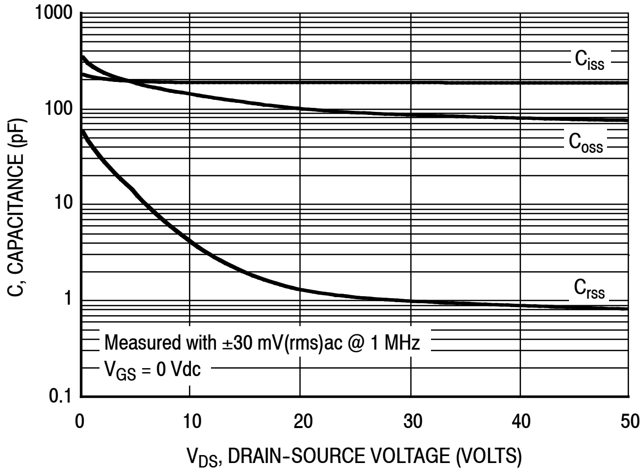


Figure 3. MMRF1310HR5(HSR5) Test Circuit Component Layout

TYPICAL CHARACTERISTICS — PULSED



Note: Each side of device measured separately.

Figure 4. Capacitance versus Drain-Source Voltage

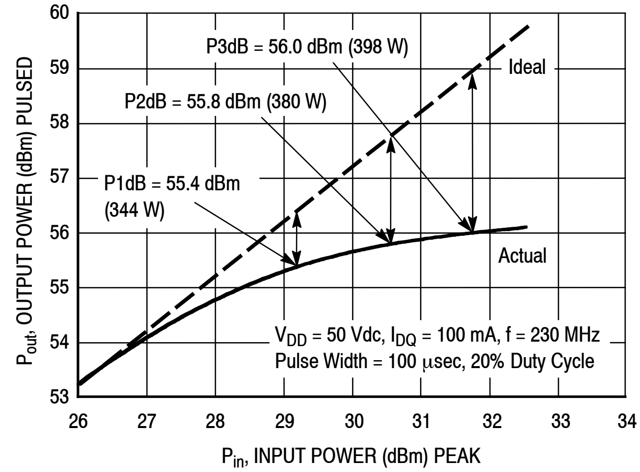


Figure 5. Output Power versus Input Power

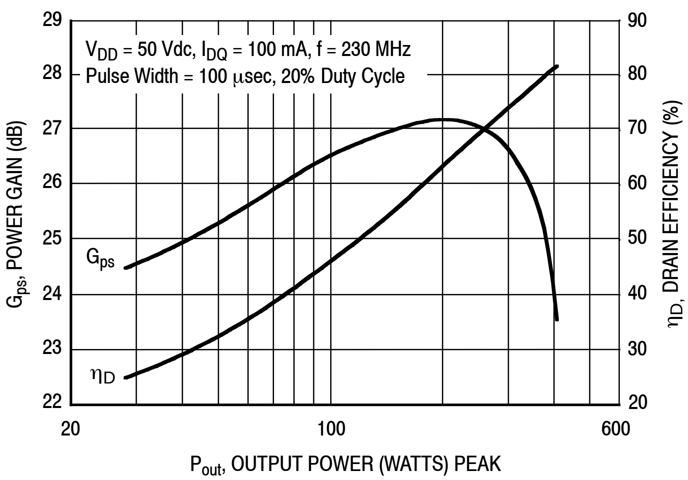


Figure 6. Power Gain and Drain Efficiency versus Output Power

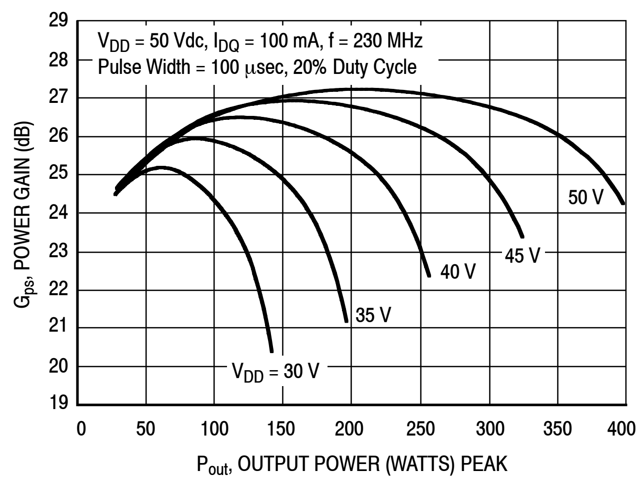


Figure 7. Power Gain versus Output Power

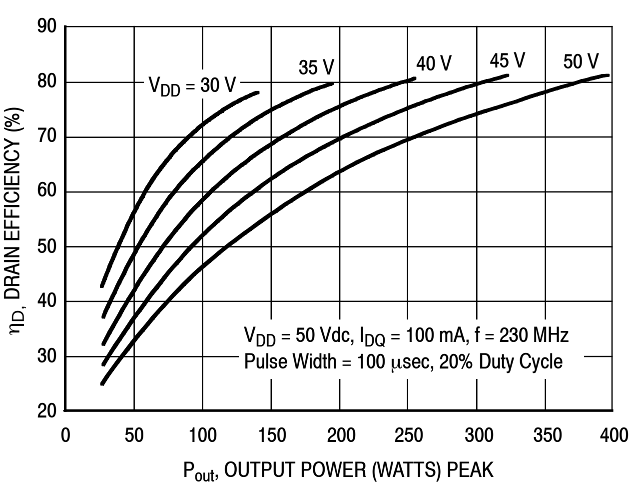


Figure 8. Drain Efficiency versus Output Power

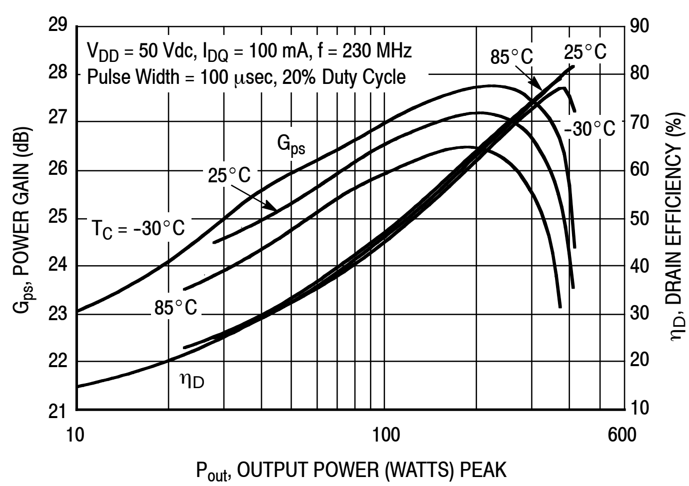


Figure 9. Power Gain and Drain Efficiency versus Output Power

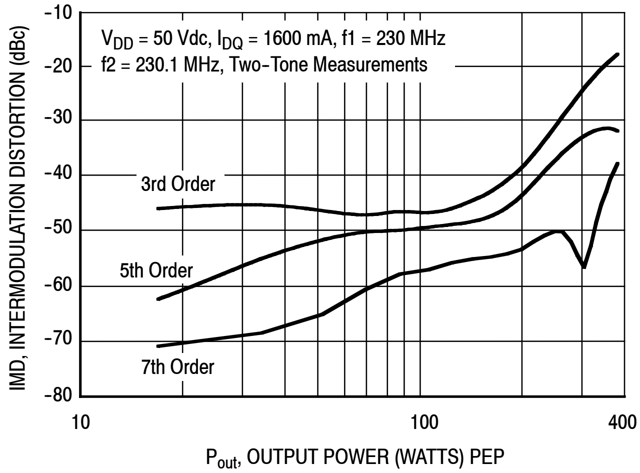


Figure 10. Intermodulation Distortion Products versus Output Power

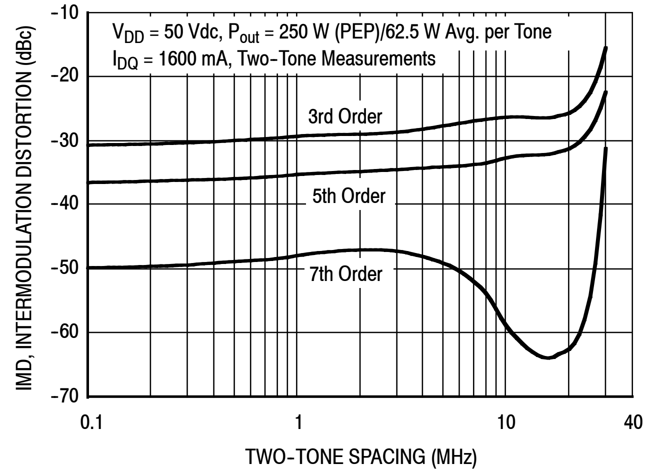


Figure 11. Intermodulation Distortion Products versus Two-Tone Spacing

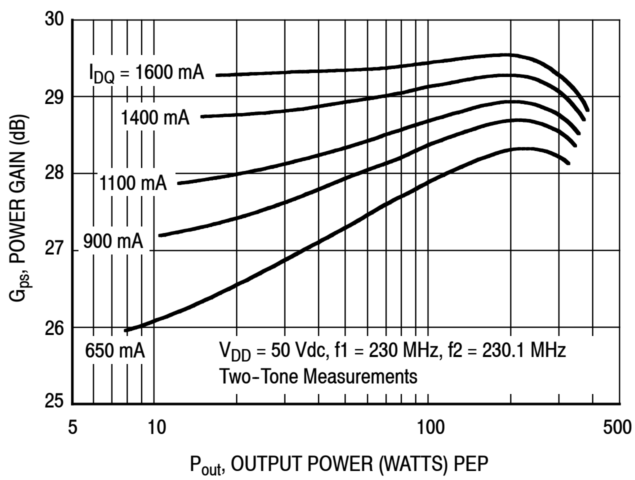


Figure 12. Two-Tone Power Gain versus Output Power

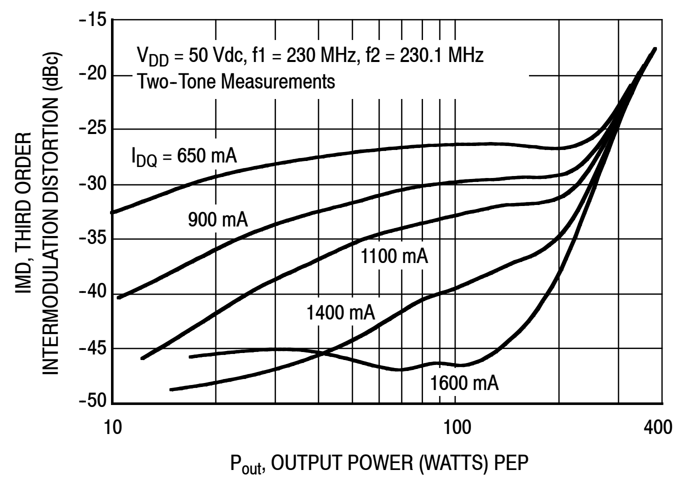
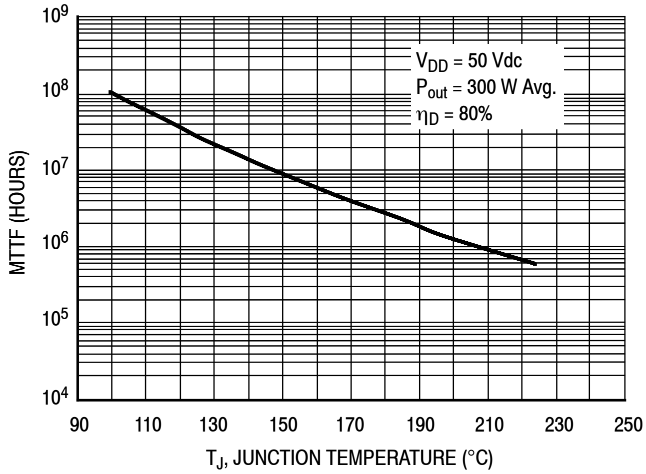


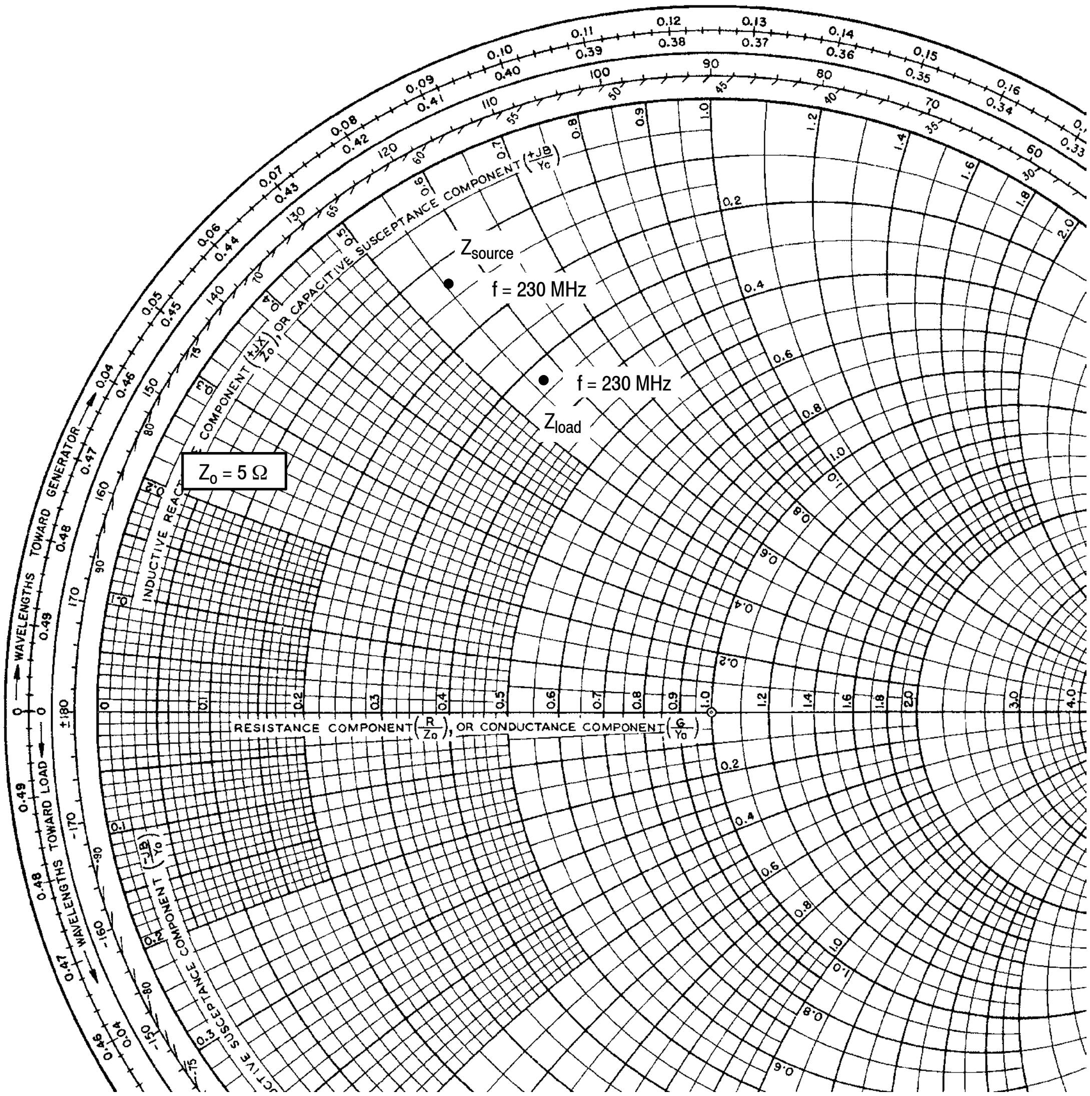
Figure 13. Third Order Intermodulation Distortion versus Output Power

1. The distortion products are referenced to one of the two tones and the peak envelope power (PEP) is 6 dB above the power in a single tone.



MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

Figure 14. MTTF versus Junction Temperature — CW



V_{DD} = 50 Vdc, I_{DQ} = 100 mA, P_{out} = 300 W Peak

f MHz	Z_{source} Ω	Z_{load} Ω
230	0.65 + j2.79	1.64 + j2.85

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

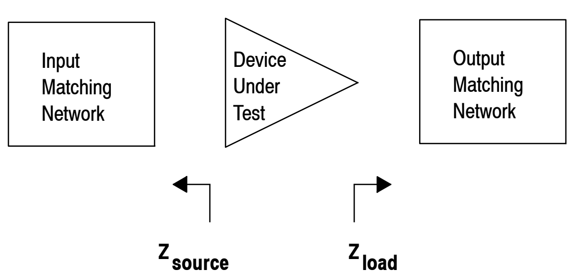


Figure 15. Series Equivalent Source and Load Impedance

V_{DD} = 50 Vdc, I_{DQ} = 100 mA

f MHz	Z_{source} Ω	Z_{load} Ω
10	36.0 + j128	12.0 + j8.80
25	20.0 + j64.0	12.4 + j6.40
50	16.0 + j41.6	11.6 + j14.4
100	8.00 + j24.8	9.00 + j9.80
200	3.00 + j12.8	7.20 + j6.40
300	1.52 + j7.92	6.00 + j5.00
400	1.08 + j5.04	4.20 + j4.00
500	1.04 + j3.16	3.32 + j2.72
600	0.88 + j1.76	2.72 + j1.68

1. Simulated performance at 1 dB gain compression.

Z_{source} = Source impedance presented from gate to gate.

Z_{load} = Load impedance presented from drain to drain.

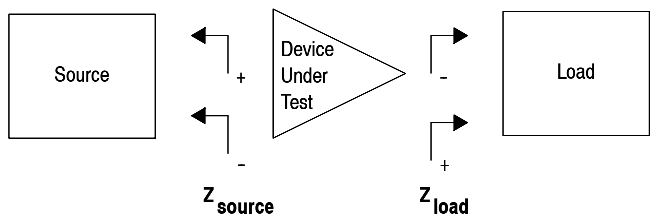
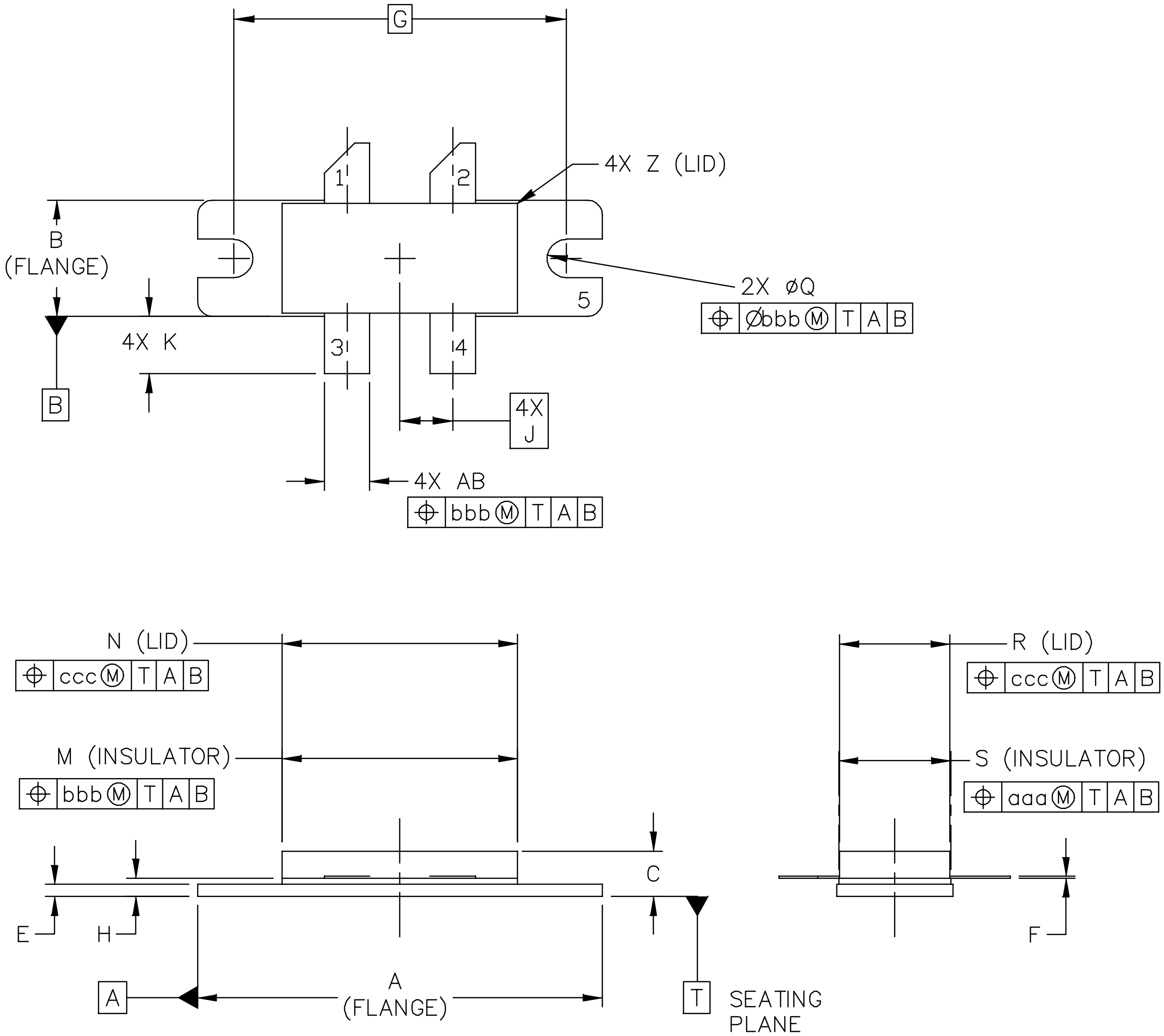


Figure 16. Simulated Source and Load Impedances Optimized for IRL, Output Power and Drain Efficiency — Push-Pull

PACKAGE DIMENSIONS



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	CASE NUMBER: 465M-01	27 MAR 2007
	STANDARD: NON-JEDEC	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.

2. CONTROLLING DIMENSION: INCH.

3. DIMENSION H IS MEASURED .030 (0.762) AWAY FROM PACKAGE BODY.

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16	R	.365	.375	9.27	9.53
B	.380	.390	9.65	9.91	S	.365	.375	9.27	9.52
C	.125	.170	3.18	4.32	U		.040		1.02
E	.035	.045	0.89	1.14	Z		.030		0.76
F	.003	.006	0.08	0.15	AB	.145	.155	3.68	3.94
G	1.100 BSC		27.94 BSC						
H	.057	.067	1.45	1.7	aaa	.005		0.127	
J	.175 BSC		4.44 BSC		bbb	.010		0.254	
K	.170	.210	4.32	5.33	ccc	.015		0.381	
M	.774	.786	19.61	20.02					
N	.772	.788	19.61	20.02					
Q	⌀.118	⌀.138	⌀3	⌀3.51					

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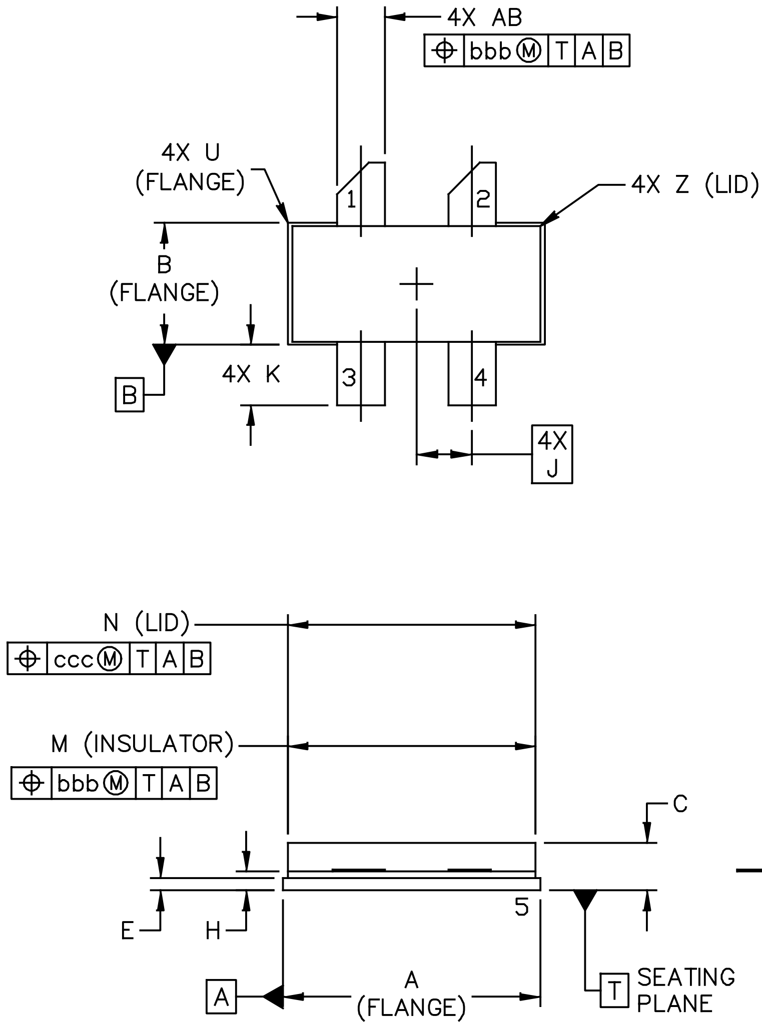

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	STANDARD: NON-JEDEC		

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED .030 (0.762) AWAY FROM PACKAGE BODY.

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.805	.815	20.45	20.7	U		.040		1.02
B	.380	.390	9.65	9.91	Z		.030		0.76
C	.125	.170	3.18	4.32	AB	.145	.155	3.68 –	3.94
E	.035	.045	0.89	1.14					
F	.003	.006	0.08	0.15	aaa	.005		0.127	
H	.057	.067	1.45	1.7	bbb	.010		0.254	
J	.175 BSC		4.44 BSC		ccc	.015		0.381	
K	.170	.210	4.32	5.33					
M	.774	.786	19.61	20.02					
N	.772	.788	19.61	20.02					
R	.365	.375	9.27	9.53					
S	.365	.375	9.27	9.52					

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	CASE NUMBER: 465H–02	27 MAR 2007
	STANDARD: NON–JEDEC	

PRODUCT DOCUMENTATION AND SOFTWARE

Refer to the following resources to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator

For Software, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	July 2014	• Initial Release of Data Sheet

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Rev. 0, 7/2014