

ADM8690/ADM8691/ADM8692/ADM8693/ADM8695

FEATURES

Upgrade for ADM690 to ADM695, MAX690 to MAX695
 Specified over temperature
 Low power consumption (0.7 mW)
 Precision voltage monitor
 Reset assertion down to 1 V V_{CC}
 Low switch on resistance 0.7 Ω normal, 7 Ω in backup
 High current drive (100 mA)
 Watchdog timer: 100 ms, 1.6 s, or adjustable
 400 nA standby current
 Automatic battery backup power switching
 Extremely fast gating of chip enable signals (3 ns)
 Voltage monitor for power fail
 Available in TSSOP package

APPLICATIONS

Microprocessor systems
 Computers
 Controllers
 Intelligent instruments
 Automotive systems

PRODUCT HIGHLIGHTS

The ADM8690 and ADM8692 are available in 8-lead, PDIP packages and provide:

1. Power-on reset output during power-up, power-down, and brownout conditions. The RESET output remains operational with V_{CC} as low as 1 V.
2. Battery backup switching for CMOS RAM, CMOS microprocessor, or other low power logic.
3. A reset pulse if the optional watchdog timer has not been toggled within a specified time.
4. A 1.3 V threshold detector for power-fail warning, low battery detection, or to monitor a power supply other than 5 V.

The ADM8691, ADM8693, and ADM8695 are available in 16-lead PDIP and small outline packages (including TSSOP) and provide three additional functions:

1. Write protection of CMOS RAM or EEPROM.
2. Adjustable reset and watchdog timeout periods.
3. Separate watchdog timeout, backup battery switchover, and low V_{CC} status outputs.

FUNCTIONAL BLOCK DIAGRAMS

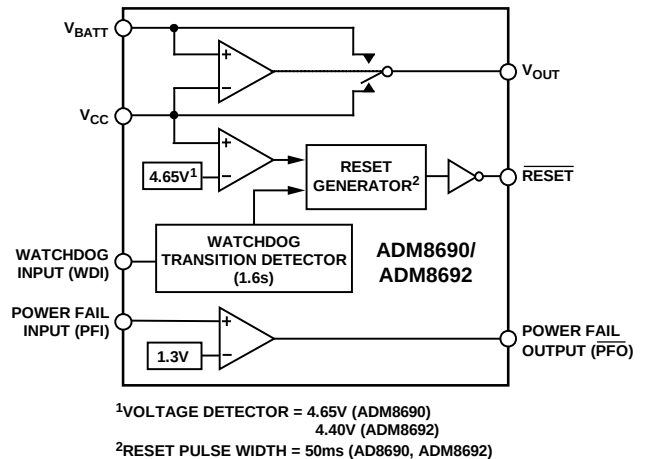


Figure 1. ADM8690/ADM8692

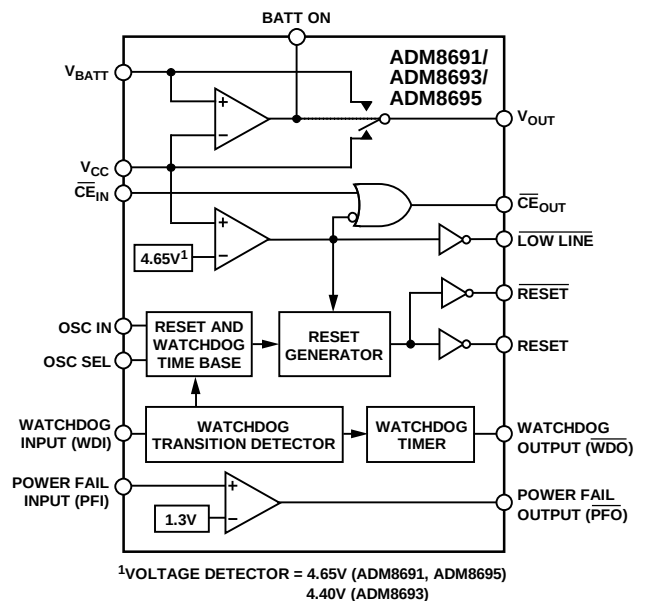


Figure 2. ADM8691/ADM8693/ADM8695

Rev. B

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TABLE OF CONTENTS

Features	1	Power-Fail Warning Comparator.....	13
Applications.....	1	Application Information.....	14
Product Highlights	1	Increasing the Drive Current.....	14
Functional Block Diagrams.....	1	Using a Rechargeable Battery for Backup	14
Revision History	2	Adding Hysteresis to the Power-Fail Comparator	14
General Description	3	Monitoring the Status of the Battery	14
Specifications.....	4	Alternate Watchdog Input Drive Circuits.....	15
Absolute Maximum Ratings.....	6	Typical Applications.....	16
ESD Caution.....	6	ADM8690 and ADM8692.....	16
Pin Configurations and Function Descriptions	7	ADM8691, ADM8693, and ADM8695	16
Typical Performance Characteristics	8	$\overline{\text{RESET}}$ Output	16
Circuit Information	10	Power-Fail Detector	17
Battery Switchover Section.....	10	RAM Write Protection.....	17
Power-Fail $\overline{\text{RESET}}$ Output.....	10	Watchdog Timer.....	17
Watchdog Timer $\overline{\text{RESET}}$	11	Outline Dimensions	18
Watchdog Output ($\overline{\text{WDO}}$)	12	Ordering Guide	19
$\overline{\text{CE}}$ Gating and RAM Write Protection (ADM8691/ADM8693/ADM8695).....	12		

REVISION HISTORY

6/11—Rev. A to Rev. B

Deleted ADM8694.....	Throughout
Updated Figure 11, Figure 12, and Figure 13.....	9
Updated Outline Dimensions	18

9/06—Rev. 0 to Rev. A

Updated Format.....	Universal
Changes to Absolute Maximum Ratings	6
Updated Ordering Guide.....	20

2/97—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADM869x family of supervisory circuits offers complete single-chip solutions for power supply monitoring and battery control functions in microprocessor systems. These functions include microprocessor reset, backup battery switchover, watchdog timer, CMOS RAM write protection, and power failure warning. The complete family provides a variety of configurations to satisfy most microprocessor system requirements.

The ADM869x family is fabricated using an advanced epitaxial CMOS process combining low power consumption (0.7 mW),

extremely fast chip enable gating (3 ns), and high reliability.

RESET assertion is guaranteed with V_{CC} as low as 1 V. In addition, the power switching circuitry is designed for minimal voltage drop thereby permitting increased output current drive of up to 100 mA without the need of an external pass transistor.

See Table 1 for a product selection guide listing the characteristics of each device in the ADM869x family. To place an order, use the Ordering Guide provided as the last section of this data sheet.

Table 1. Product Selection Guide

Part Number	Nominal Reset Time	Nominal V_{CC} Reset Threshold	Nominal Watchdog Timeout Period	Battery Backup Switching	Base Drive Ext PNP	Chip Enable Signals
ADM8690	50 ms	4.65 V	1.6 s	Yes	No	No
ADM8691	50 ms or ADJ	4.65 V	100 ms, 1.6 s, ADJ	Yes	Yes	Yes
ADM8692	50 ms	4.4 V	1.6 s	Yes	No	No
ADM8693	50 ms or ADJ	4.4 V	100 ms, 1.6 s, ADJ	Yes	Yes	Yes
ADM8695	200 ms or ADJ	4.65 V	100 ms, 1.6 s, ADJ	Yes	Yes	Yes

ADM8690/ADM8691/ADM8692/ADM8693/ADM8695

SPECIFICATIONS

V_{CC} = full operating range, $V_{BATT} = 2.8\text{ V}$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
BATTERY BACKUP SWITCHING					
V_{CC} Operating Voltage Range					
ADM8690, ADM8691, ADM8695	4.75		5.5	V	
ADM8692, ADM8693	4.5		5.5	V	
V_{BATT} Operating Voltage Range					
ADM8690, ADM8691, ADM8695	2.0		4.25	V	
ADM8692, ADM8693	2.0		4.0	V	
V_{OUT} Output Voltage	$V_{CC} - 0.005$	$V_{CC} - 0.0025$		V	$I_{OUT} = 1\text{ mA}$
	$V_{CC} - 0.2$	$V_{CC} - 0.125$		V	$I_{OUT} \leq 100\text{ mA}$
V_{OUT} in Battery Backup Mode	$V_{BATT} - 0.005$	$V_{BATT} - 0.002$		V	$I_{OUT} = 250\text{ }\mu\text{A}$, $V_{CC} < V_{BATT} - 0.2\text{ V}$
Supply Current (Excludes I_{OUT})		140	200	μA	$I_{OUT} = 100\text{ }\mu\text{A}$
Supply Current in Battery Backup Mode		0.4	1	μA	$V_{CC} = 0\text{ V}$, $V_{BATT} = 2.8\text{ V}$
Battery Standby Current					$5.5\text{ V} > V_{CC} > V_{BATT} + 0.2\text{ V}$
+ = Discharge, - = Charge	-0.1		+0.02	μA	$T_A = 25^\circ\text{C}$
Battery Switchover Threshold		70		mV	Power-up
$V_{CC} - V_{BATT}$		50		mV	Power-down
Battery Switchover Hysteresis		20		mV	
BATT ON Output Voltage			0.3	V	$I_{SINK} = 3.2\text{ mA}$
BATT ON Output Short-Circuit Current		55		mA	BATT ON = $V_{OUT} = 4.5\text{ V}$ sink current
	0.5	2.5	25	μA	BATT ON = 0 V source current
RESET AND WATCHDOG TIMER					
Reset Voltage Threshold					
ADM8690, ADM8691, ADM8695	4.5	4.65	4.73	V	
ADM8692, ADM8693	4.25	4.4	4.48	V	
Reset Threshold Hysteresis		40		mV	
Reset Timeout Delay					
ADM8690, ADM8691, ADM8692, ADM8693,	35	50	70	ms	OSC SEL = high
ADM8695	140	200	280	ms	OSC SEL = high
Watchdog Timeout Period, Internal Oscillator	1.0	1.6	2.25	s	Long period
	70	100	140	ms	Short period
Watchdog Timeout Period, External Clock	3840	4064	4097	cycles	Long period
	768	1011	1025	cycles	Short period
Minimum WDI Input Pulse Width	50			ns	$V_{IL} = 0.4$, $V_{IH} = 3.5\text{ V}$
RESET Output Voltage @ $V_{CC} = 1\text{ V}$		4	20	mV	$I_{SINK} = 10\text{ }\mu\text{A}$, $V_{CC} = 1\text{ V}$
RESET, LOW LINE Output Voltage		0.05	0.4	V	$I_{SINK} = 1.6\text{ mA}$, $V_{CC} = 4.25\text{ V}$
	3.5			V	$I_{SOURCE} = 1\text{ }\mu\text{A}$
RESET, WDO Output Voltage			0.4	V	$I_{SINK} = 1.6\text{ mA}$
	3.5			V	$I_{SOURCE} = 1\text{ }\mu\text{A}$
Output Short-Circuit Source Current	1	10	25	μA	
Output Short-Circuit Sink Current		25		mA	
WDI Input Threshold ¹					
Logic Low			0.8	V	
Logic High	3.5			V	
WDI Input Current		1	10	μA	WDI = V_{OUT}
	-10	-1		μA	WDI = 0 V

ADM8690/ADM8691/ADM8692/ADM8693/ADM8695

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER-FAIL DETECTOR					
PFI Input Threshold	1.25	1.3	1.35	V	$V_{CC} = 5\text{ V}$
PFI Input Current	-25	± 0.01	+25	nA	
PFO Output Voltage			0.4	V	$I_{SINK} = 3.2\text{ mA}$
	3.5			V	$I_{SOURCE} = 1\text{ }\mu\text{A}$
PFO Short-Circuit Source Current	1	3	25	μA	PFI = low, $\overline{\text{PFO}} = 0\text{ V}$
PFO Short-Circuit Sink Current		25		mA	PFI = high, $\overline{\text{PFO}} = V_{OUT}$
CHIP ENABLE GATING					
$\overline{\text{CE}}_{IN}$ Threshold			0.8	V	V_{IL}
	3.0			V	V_{IH}
$\overline{\text{CE}}_{IN}$ Pull-Up Current		3		μA	
$\overline{\text{CE}}_{OUT}$ Output Voltage			0.4	V	$I_{SINK} = 3.2\text{ mA}$
	$V_{OUT} - 1.5$			V	$I_{SOURCE} = 3.0\text{ mA}$
	$V_{OUT} - 0.05$			V	$I_{SOURCE} = 1\text{ }\mu\text{A}, V_{CC} = 0\text{ V}$
$\overline{\text{CE}}$ Propagation Delay		3	7	ns	
OSCILLATOR					
OSC IN Input Current		± 2		μA	
OSC SEL Input Pull-Up Current		5		μA	
OSC IN Frequency Range	0		500	kHz	OSC SEL = 0 V
OSC IN Frequency with External Capacitor		4		kHz	OSC SEL = 0 V, $C_{OSC} = 47\text{ pF}$

¹ WDI is a three-level input that is internally biased to 38% of V_{CC} and has an input impedance of approximately 5 M Ω .

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

Parameter	Rating
V_{CC}	–0.3 V to +6 V
V_{BATT}	–0.3 V to +6 V
All Other Inputs	–0.3 V to $V_{OUT} + 0.5\text{ V}$
Input Current	
V_{CC}	200 mA
V_{BATT}	50 mA
GND	20 mA
Digital Output Current	20 mA
Power Dissipation, N-8 PDIP	400 mW
θ_{JA} Thermal Impedance	120°C/W
Power Dissipation, R-8 SOIC	400 mW
θ_{JA} Thermal Impedance	120°C/W
Power Dissipation, N-16 PDIP	600 mW
θ_{JA} Thermal Impedance	135°C/W
Power Dissipation, RU-16 TSSOP	600 mW
θ_{JA} Thermal Impedance	158°C/W
Power Dissipation, R-16 SOIC_N	600 mW
θ_{JA} Thermal Impedance	110°C/W
Power Dissipation, RW-16 SOIC_W	600 mW
θ_{JA} Thermal Impedance	73°C/W
Operating Temperature Range	
Industrial (A Version)	–40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Storage Temperature Range	–65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

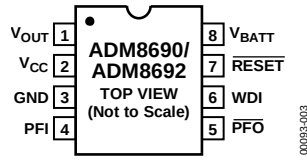


Figure 3. ADM8690 and ADM8692, Pin Configuration

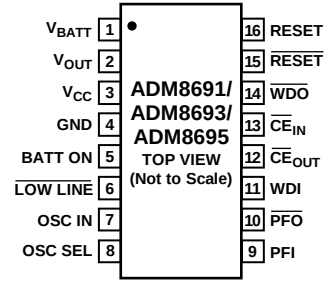


Figure 4. ADM8691, ADM8693, and ADM8695 Pin Configuration

Table 4. Pin Function Descriptions

Mnemonic	Function
V _{CC}	Power Supply Input. 5 V nominal.
V _{BATT}	Backup Battery Input.
V _{OUT}	Output Voltage. V _{CC} or V _{BATT} is internally switched to V _{OUT} , depending on which is at the highest potential. V _{OUT} can supply up to 100 mA to power CMOS RAM. Connect V _{OUT} to V _{CC} if V _{OUT} and V _{BATT} are not used.
GND	Ground. This is the 0 V ground reference for all signals.
RESET	Logic Output. RESET goes low if V _{CC} falls below the reset threshold, or the watchdog timer is not serviced within its timeout period. The reset threshold is typically 4.65 V for the ADM8690/ADM8691/ADM8695 and 4.4 V for the ADM8692 and ADM8693. RESET remains low for 50 ms (ADM8690/ADM8691/ADM8692/ADM8693) or 200 ms (ADM8695) after V _{CC} returns above the threshold. RESET also goes low for 50 ms (ADM8690/ADM8691/ADM8692/ADM8693) or 200 ms (ADM8695) if the watchdog timer is enabled but not serviced within its timeout period. The RESET pulse width can be adjusted on the ADM8691/ADM8693/ADM8695, as shown in Table 5. The RESET output has an internal 3 μ A pull-up, and can either connect to an open collector reset bus or directly drive a CMOS gate without an external pull-up resistor.
WDI	Watchdog Input. WDI is a three-level input. If WDI remains either high or low for longer than the watchdog timeout period, RESET pulses low and WDO goes low. The timer resets with each transition on the WDI line. The watchdog timer can be disabled if WDI is left floating or is driven to midsupply.
PFI	Power-Fail Input. PFI is the noninverting input to the power-fail comparator. When PFI is less than 1.3 V, PFO goes low. Connect PFI to GND or V _{OUT} when not used.
PFO	Power-Fail Output. PFO is the output of the power-fail comparator. It goes low when PFI is less than 1.3 V. The comparator is turned off and PFO goes low when V _{CC} is below V _{BATT} .
CE _{IN}	Logic Input. The input to the CE gating circuit. When not in use, connect this pin to GND or V _{OUT} .
CE _{OUT}	Logic Output. CE _{OUT} is a gated version of the CE _{IN} signal. CE _{OUT} tracks CE _{IN} when V _{CC} is above the reset threshold. If V _{CC} is below the reset threshold, CE _{OUT} is forced high. See Figure 21 and Figure 22.
BATT ON	Logic Output. BATT ON goes high when V _{OUT} is internally switched to the V _{BATT} input. It goes low when V _{OUT} is internally switched to V _{CC} . The output typically sinks 35 mA and can directly drive the base of an external PNP transistor to increase the output current above the 100 mA rating of V _{OUT} .
LOW LINE	Logic Output. LOW LINE goes low when V _{CC} falls below the reset threshold. It returns high as soon as V _{CC} rises above the reset threshold.
RESET	Logic Output. RESET is an active high output. It is the inverse of RESET.
OSC SEL	Logic Oscillator Select Input. When OSC SEL is unconnected (floating) or driven high, the internal oscillator sets the reset active time and watchdog timeout period. When OSC SEL is low, the external oscillator input, OSC IN, is enabled. OSC SEL has a 3 μ A internal pull-up (see Table 5).
OSC IN	Oscillator Logic Input. With OSC SEL low, OSC IN can be driven by an external clock signal or an external capacitor can be connected between OSC IN and GND. This sets both the reset active pulse timing and the watchdog timeout period (see Table 5 and Figure 17, Figure 18, Figure 19, and Figure 20). With OSC SEL high or floating, the internal oscillator is enabled and the reset active time is fixed at 50 ms typical (ADM8691/ADM8693) or 200 ms typical (ADM8695). In this mode, the OSC IN pin selects between fast (100 ms) and slow (1.6 s) watchdog timeout periods. In both modes, the timeout period immediately after a reset is 1.6 s typical.
WDO	Logic Output. The watchdog output, WDO, goes low if WDI remains either high or low for longer than the watchdog timeout period. WDO is set high by the next transition at WDI. If WDI is unconnected or at midsupply, the watchdog timer is disabled and WDO remains high. WDO also goes high when LOW LINE goes low.

TYPICAL PERFORMANCE CHARACTERISTICS

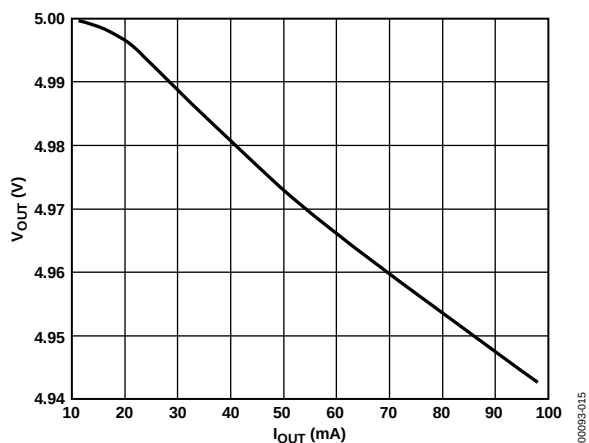


Figure 5. V_{OUT} vs. I_{OUT} Normal Operation

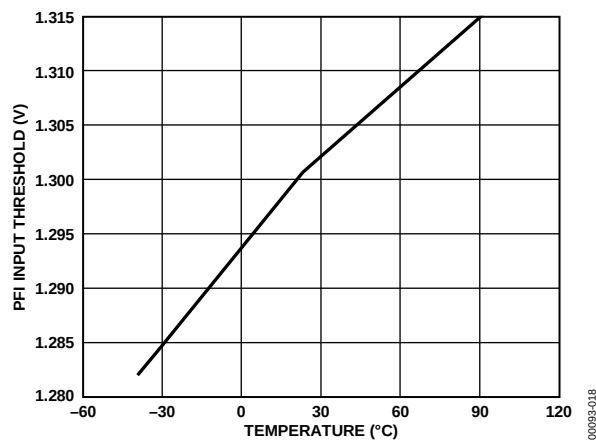


Figure 8. PFI Input Threshold vs. Temperature

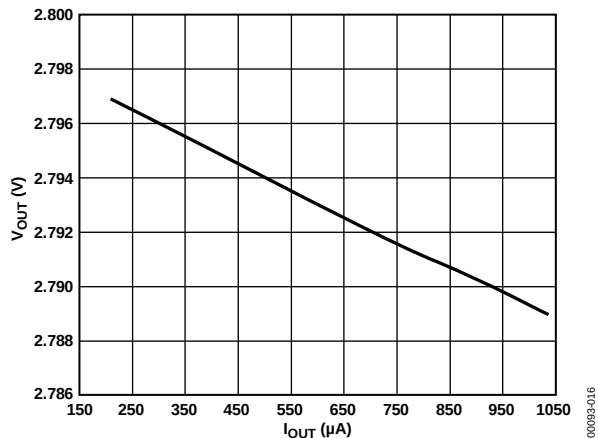


Figure 6. V_{OUT} vs. I_{OUT} Battery Backup

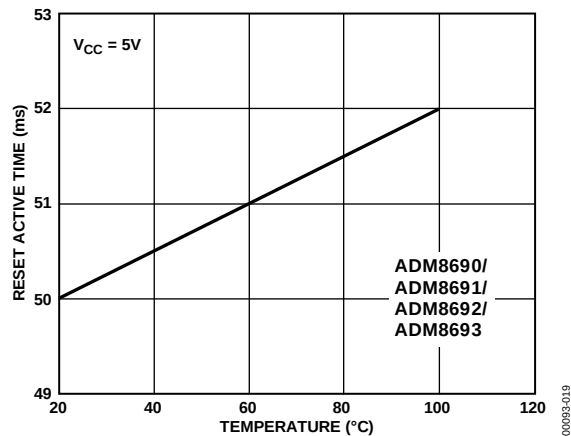


Figure 9. Reset Active Time vs. Temperature

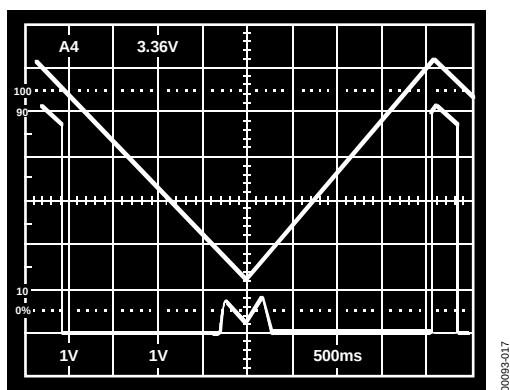


Figure 7. Reset Output Voltage vs. Supply Voltage

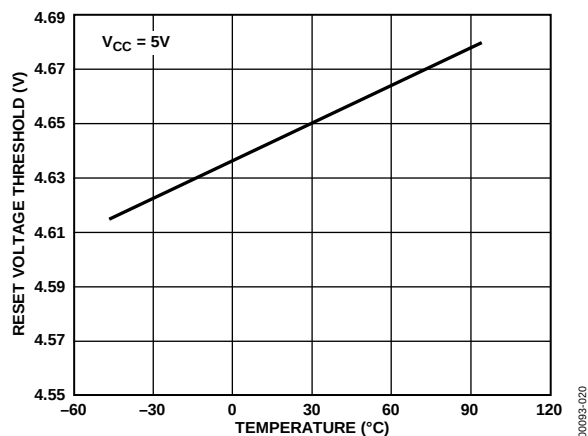


Figure 10. Reset Voltage Threshold vs. Temperature

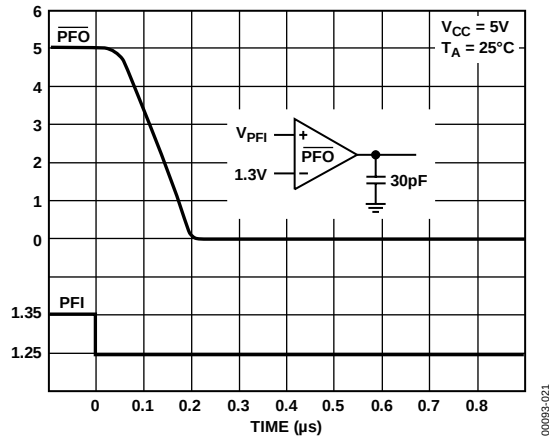


Figure 11. Power-Fail Comparator Response Time Falling

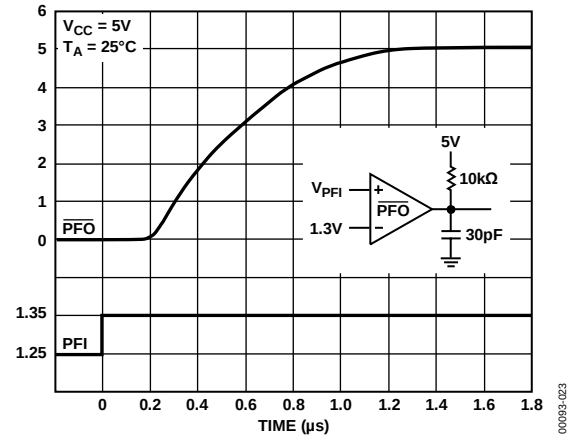


Figure 13. Power-Fail Comparator Response Time with Pull-Up Resistor

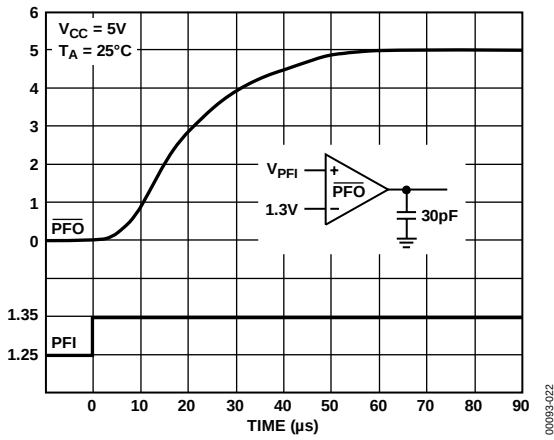


Figure 12. Power-Fail Comparator Response Time Rising

CIRCUIT INFORMATION

BATTERY SWITCHOVER SECTION

The battery switchover circuit compares V_{CC} to the V_{BATT} input, and connects V_{OUT} to whichever is higher. Switchover occurs when V_{CC} is 50 mV higher than V_{BATT} as V_{CC} falls, and when V_{CC} is 70 mV greater than V_{BATT} as V_{CC} rises. This 20 mV of hysteresis prevents repeated rapid switching if V_{CC} falls very slowly or remains nearly equal to the battery voltage.

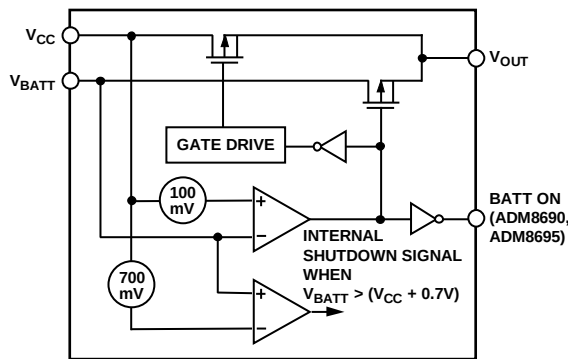


Figure 14. Battery Switchover Schematic

During normal operation, with V_{CC} higher than V_{BATT} , V_{CC} is internally switched to V_{OUT} through an internal PMOS transistor switch. This switch has a typical on resistance of 0.7Ω and can supply up to 100 mA at the V_{OUT} terminal. V_{OUT} is normally used to drive a RAM memory bank, requiring instantaneous currents of greater than 100 mA. If this is the case, a bypass capacitor should be connected to V_{OUT} . The capacitor provides the peak current transients to the RAM. A capacitance value of $0.1 \mu\text{F}$ or greater can be used.

If the continuous output current requirement at V_{OUT} exceeds 100 mA, or if a lower $V_{CC} - V_{OUT}$ voltage differential is desired, an external PNP pass transistor can be connected in parallel with the internal transistor. The BATT ON output (ADM8691/ADM8693/ADM8695) can directly drive the base of the external transistor.

A 7Ω MOSFET switch connects the V_{BATT} input to V_{OUT} during battery backup. This MOSFET has very low input-to-output differential (dropout voltage) at the low current levels required for battery back up of CMOS RAM or other low power CMOS circuitry. The supply current in battery back up is typically $0.4 \mu\text{A}$.

The ADM8690/ADM8691/ADM8695 operate with battery voltages from 2.0 V to 4.25 V, and the ADM8692/ADM8693 operate with battery voltages from 2.0 V to 4.0 V. High value capacitors, either standard electrolytic or the farad-size, double-layer capacitors, can also be used for short-term memory backup. A small charging current of typically 10 nA ($0.1 \mu\text{A}$ maximum) flows out of the V_{BATT} terminal. This current is useful for maintaining rechargeable batteries in a fully

charged condition. This extends the life of the backup battery by compensating for its self-discharge current. Also note that this current poses no problem when lithium batteries are used for backup because the maximum charging current ($0.1 \mu\text{A}$) is safe for even the smallest lithium cells.

If the battery switchover section is not used, V_{BATT} should be connected to GND and V_{OUT} should be connected to V_{CC} .

POWER-FAIL RESET OUTPUT

$\overline{\text{RESET}}$ is an active low output that provides a $\overline{\text{RESET}}$ signal to the microprocessor whenever V_{CC} is at an invalid level. When V_{CC} falls below the reset threshold, the $\overline{\text{RESET}}$ output is forced low. The nominal reset voltage threshold is 4.65 V (ADM8690/ADM8691/ADM8695) or 4.4 V (ADM8692/ADM8693).

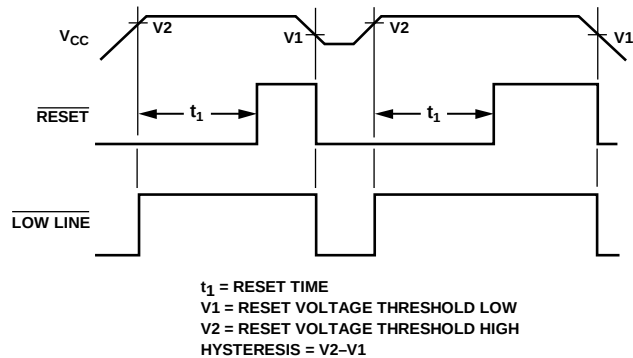


Figure 15. Power-Fail Reset Timing

On power-up, $\overline{\text{RESET}}$ remains low for 50 ms (200 ms for ADM8695) after V_{CC} rises above the appropriate reset threshold. This allows time for the power supply and microprocessor to stabilize. On power-down, the $\overline{\text{RESET}}$ output remains low with V_{CC} as low as 1 V. This ensures that the microprocessor is held in a stable shutdown condition.

This $\overline{\text{RESET}}$ active time is adjustable on the ADM8691/ADM8693/ADM8695 by using an external oscillator or by connecting an external capacitor to the OSC IN pin. Refer to Table 5 and Figure 17, Figure 18, Figure 19, and Figure 20.

The guaranteed minimum and maximum thresholds of the ADM8690/ADM8691/ADM8695 are 4.5 V and 4.73 V, and the guaranteed thresholds of the ADM8692/ADM8693 are 4.25 V and 4.48 V. The ADM8690/ADM8691/ADM8695 are, therefore, compatible with 5 V supplies with a +10%, -5% tolerance and the ADM8692/ADM8693 are compatible with $5 \text{ V} \pm 10\%$ supplies. The reset threshold comparator has approximately 50 mV of hysteresis. The response time of the reset voltage comparator is less than $1 \mu\text{s}$. If glitches are present on the V_{CC} line that could cause spurious reset pulses, V_{CC} should be decoupled close to the device.

In addition to $\overline{\text{RESET}}$, the ADM8691/ADM8693/ADM8695 contain an active high RESET output. This is the complement of $\overline{\text{RESET}}$ and is intended for processors requiring an active high reset signal.

WATCHDOG TIMER RESET

The watchdog timer circuit monitors the activity of the micro-processor to check that it is not stalled in an indefinite loop. An output line on the processor is used to toggle the watchdog input (WDI) line. If this line is not toggled within the selected timeout period, a RESET pulse is generated. The nominal watchdog timeout period is preset at 1.6 seconds on the ADM8690 and ADM8692. The ADM8691/ADM8693/ADM8695 can be configured for either a fixed short 100 ms, or a long 1.6 second timeout period, or for an adjustable timeout period. If the short period is selected, some systems are unable to service the watchdog timer immediately after a reset, so the ADM8691/ADM8693/ADM8695 automatically select the long timeout period directly after a reset is issued. The watchdog timer is restarted at the end of reset, whether the reset was caused by lack of activity on WDI or by V_{CC} falling below the reset threshold.

The normal (short) timeout period becomes effective following the first transition of WDI after $\overline{\text{RESET}}$ has gone inactive. The watchdog timeout period restarts with each transition on the WDI pin. To ensure that the watchdog timer does not time out, either a high-to-low or low-to-high transition on the WDI pin must occur at, or less than, the minimum timeout period. If WDI remains permanently either high or low, reset pulses are issued after each long (1.6 s) timeout period. The watchdog monitor can be deactivated by floating the watchdog input (WDI) or by connecting it to midsupply.

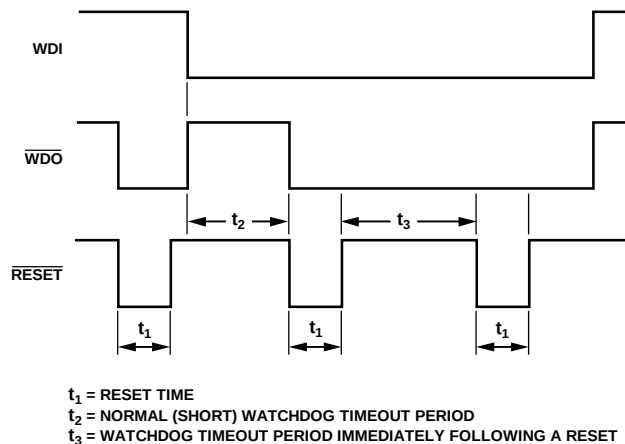


Figure 16. Watchdog Timeout Period and Reset Active Time

Table 5. ADM8691, ADM8693, ADM8695 Reset Pulse Width and Watchdog Timeout Selections

OSC SEL	OSC IN	Watchdog Timeout Period		Reset Active Period	
		Normal	Immediately After Reset	ADM8691/ADM8693	ADM8695
Low ¹	External clock input	1024 CLKs	4096 CLKs	512 CLKs	2048 CLKs
Low ¹	External capacitor	$400 \text{ ms} \times C/47 \text{ pF}$	$1.6 \text{ s} \times C/47 \text{ pF}$	$200 \text{ ms} \times C/47 \text{ pF}$	$520 \text{ ms} \times C/47 \text{ pF}$
Floating or high	Low	100 ms	1.6 s	50 ms	200 ms
Floating or high	Floating or high	1.6 s	1.6 s	50 ms	200 ms

¹ With the OSC SEL pin low, OSC IN can be driven by an external clock signal, or an external capacitor (C) can be connected between OSC IN and GND. The nominal internal oscillator frequency is 10.24 kHz. The nominal oscillator frequency with external capacitor is: $F_{\text{OSC}} (\text{Hz}) = 184,000/C (\text{pF})$.

ADM8690/ADM8691/ADM8692/ADM8693/ADM8695

On the ADM8690/ADM8692 the watchdog timeout period is fixed at 1.6 seconds and the reset pulse width is fixed at 50 ms. The ADM8691/ADM8693/ADM8695 allow these times to be adjusted, as shown in Table 5. Figure 17, Figure 18, Figure 19, and Figure 20 show the various oscillator configurations that can be used to adjust the reset pulse width and watchdog timeout period.

The internal oscillator is enabled when OSC SEL is high or floating. In this mode, OSC IN selects between the 1.6 second and 100 ms watchdog timeout periods. With OSC IN connected high or floating, the 1.6 second timeout period is selected; and with it connected low, the 100 ms timeout period is selected. In either case, the timeout period is 1.6 seconds immediately after a reset. This gives the microprocessor time to reinitialize the system. If OSC IN is low, the 100 ms watchdog period becomes effective after the first transition of WDI. The software should be written such that the input/output port driving WDI is left in its power-up reset state until the initialization routines are completed and the microprocessor is able to toggle WDI at the minimum watchdog timeout period of 70 ms.

WATCHDOG OUTPUT (WDO)

The Watchdog Output WDO (ADM8691/ADM8693/ADM8695) provides a status output that goes low if the watchdog timer times out and remains low until set high by the next transition on the watchdog input. WDO is also set high when V_{CC} goes below the reset threshold.

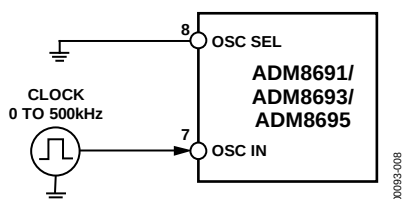


Figure 17. External Clock Source

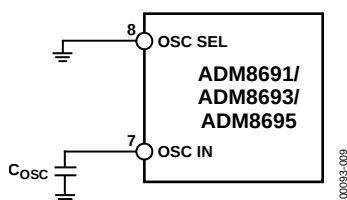


Figure 18. External Capacitor

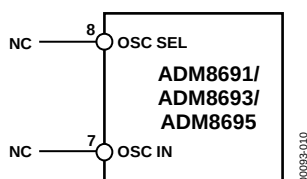


Figure 19. Internal Oscillator (1.6 Second Watchdog)

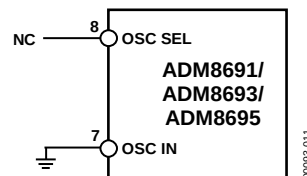


Figure 20. Internal Oscillator (100 ms Watchdog)

CE GATING AND RAM WRITE PROTECTION (ADM8691/ADM8693/ADM8695)

The ADM8691/ADM8693/ADM8695 products include memory protection circuitry that ensures the integrity of data in memory by preventing write operations when V_{CC} is at an invalid level. There are two additional pins ($\overline{CE}_{IN}$ and $\overline{CE}_{OUT}$) that can be used to control the chip enable or write inputs of CMOS RAM. When V_{CC} is present, $\overline{CE}_{OUT}$ is a buffered replica of $\overline{CE}_{IN}$, with a 3 ns propagation delay. When V_{CC} falls below the reset voltage threshold or V_{BATT} , an internal gate forces $\overline{CE}_{OUT}$ high, independent of $\overline{CE}_{IN}$.

$\overline{CE}_{OUT}$ typically drives the $\overline{CE}$, $\overline{CS}$, or write input of battery backed up CMOS RAM. This ensures the integrity of the data in memory by preventing write operations when V_{CC} is at an invalid level. Similar protection of EEPROMs can be achieved using the $\overline{CE}_{OUT}$ to drive the store or write inputs.

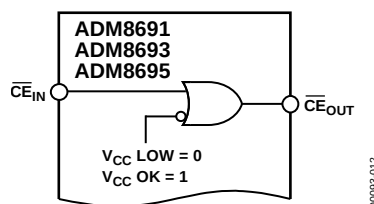


Figure 21. Chip Enable Gating

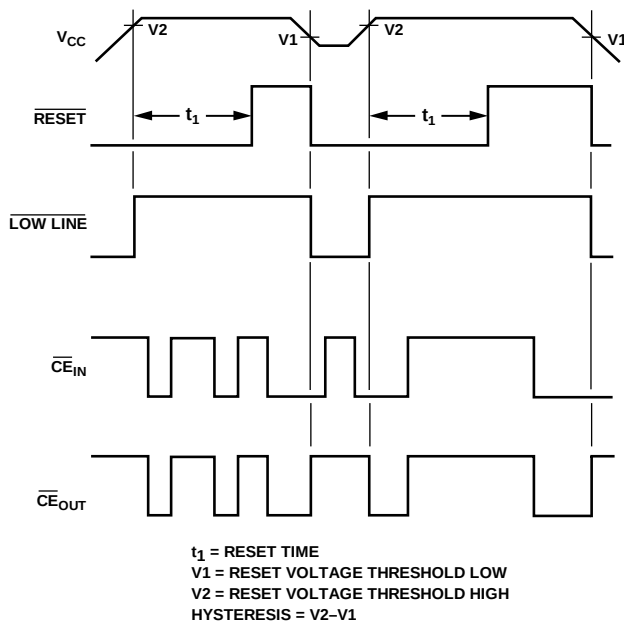


Figure 22. Chip Enable Timing

POWER-FAIL WARNING COMPARATOR

An additional comparator is provided for early warning of failure in the microprocessor power supply. The power-fail input (PFI) is compared to an internal 1.3 V reference. The power-fail output (PFO) goes low when the voltage at PFI is less than 1.3 V. Typically, PFI is driven by an external voltage divider that senses either the unregulated dc input to the system 5 V regulator or the regulated 5 V output. The voltage divider ratio can be chosen such that the voltage at PFI falls below 1.3 V several milliseconds before the 5 V power supply falls below the reset threshold. $\overline{\text{PFO}}$ is normally used to interrupt the microprocessor so that data can be stored in RAM and the shut-down procedure executed before power is lost.

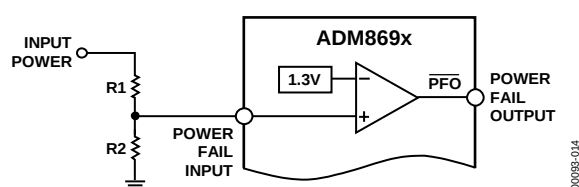


Figure 23. Power-Fail Comparator

Table 6. Input and Output Status in Battery Backup Mode

Signal	Status
V_{OUT}	V_{OUT} is connected to V_{BATT} via an internal PMOS switch.
$\overline{\text{RESET}}$	Logic low.
RESET	Logic high. The open-circuit output voltage is equal to V_{OUT} .
$\overline{\text{LOW LINE}}$	Logic low.
BATT ON	Logic high. The open-circuit voltage is equal to V_{OUT} .
WDI	WDI is ignored. It is internally disconnected from the internal pull-up resistor and does not source or sink current as long as its input voltage is between GND and V_{OUT} . The input voltage does not affect supply current.
$\overline{\text{WDO}}$	Logic high. The open circuit voltage is equal to V_{OUT} .
PFI	The power-fail comparator is turned off and has no effect on the power-fail output.
$\overline{\text{PFO}}$	Logic low.
$\overline{\text{CE}}_{\text{IN}}$	$\overline{\text{CE}}_{\text{IN}}$ is ignored. It is internally disconnected from its internal pull-up and does not source or sink current as long as its input voltage is between GND and V_{OUT} . The input voltage does not affect supply current.
$\overline{\text{CE}}_{\text{OUT}}$	Logic high. The open circuit voltage is equal to V_{OUT} .
OSC IN	OSC IN is ignored.
OSC SEL	OSC SEL is ignored.

ALTERNATE WATCHDOG INPUT DRIVE CIRCUITS

The watchdog feature can be enabled and disabled under program control by driving WDI with a three-state buffer (see Figure 28). When three-stated, the WDI input floats, thereby disabling the watchdog timer.

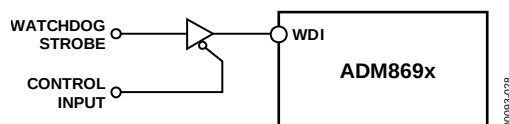


Figure 28. Programming the Watchdog Input

This circuit is not entirely foolproof, and it is possible for a software fault to erroneously three-state the buffer preventing the ADM869x from detecting that the microprocessor is no longer operating correctly. In most cases, a better method is to extend the watchdog period rather than disable the watchdog.

This can be done under program control using the circuit shown in Figure 29. When the control input is high, the OSC SEL pin is low and the watchdog timeout is set by the external capacitor. A 0.01 μF capacitor sets a watchdog time-out delay of 100 seconds. When the control input is low, the OSC SEL pin is driven high, selecting the internal oscillator. The 100 ms or the 1.6 s period is chosen, depending on which diode is used, as shown in Figure 29. With D1 inserted, the internal timeout is set at 100 ms; with D2 inserted, the timeout is set at 1.6 seconds.

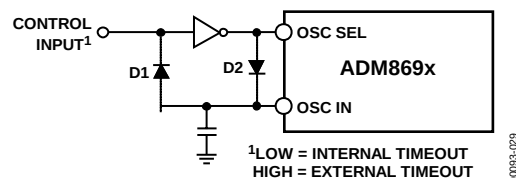


Figure 29. Programming the Watchdog Input

TYPICAL APPLICATIONS

ADM8690 AND ADM8692

Figure 30 shows the ADM8690/ADM8692 in a typical power monitoring, battery backup application. V_{OUT} powers the CMOS RAM. Under normal operating conditions with V_{CC} present, V_{OUT} is internally connected to V_{CC} . If a power failure occurs, V_{CC} decays and V_{OUT} is switched to V_{BATT} , thereby maintaining power for the CMOS RAM. A RESET pulse is also generated when V_{CC} falls below 4.65 V for the ADM8690 or 4.4 V for the ADM8692. RESET remains low for 50 ms after V_{CC} returns to 5 V.

The watchdog timer input (WDI) monitors an input/output line from the microprocessor system. This line must be toggled once every 1.6 seconds to verify correct software execution. Failure to toggle the line indicates that the microprocessor system is not correctly executing its program and can be tied up in an endless loop. If this happens, a reset pulse is generated to initialize the microprocessor.

If the watchdog timer is not needed, the WDI input should be left floating.

The power-fail input, PFI, monitors the input power supply via a resistive divider network. The voltage on the PFI input is compared with a precision 1.3 V internal reference. If the input voltage drops below 1.3 V, a power-fail output (PFO) signal is generated. This warns of an impending power failure and can be used to interrupt the processor so that the system can be shut down in an orderly fashion. The resistors in the sensing network are ratioed to give the desired power-fail threshold voltage (V_T).

$$V_T = (1.3 R1/R2) + 1.3 \text{ V}$$

$$R1/R2 = (V_T/1.3) - 1$$

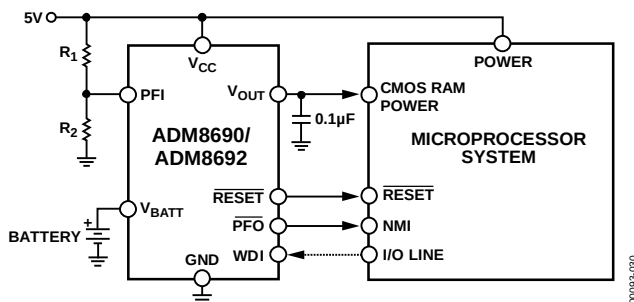


Figure 30. ADM8690/ADM8692 Typical Application Circuit A

Figure 31 shows a similar application, but in this case the PFI input monitors the unregulated input to the 7805 voltage regulator. This gives an earlier warning of an impending power failure. It is useful with processors operating at low speeds or where there are a significant number of housekeeping tasks to be completed before the power is lost.

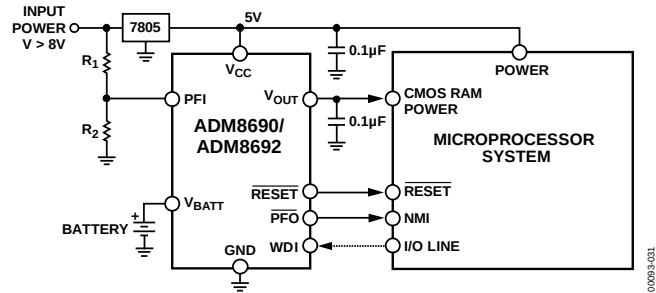


Figure 31. ADM8690/ADM8692 Typical Application Circuit B

ADM8691, ADM8693, AND ADM8695

A typical connection for the ADM8691/ADM8693/ADM8695 is shown in Figure 32. CMOS RAM is powered from V_{OUT} . When 5 V power is present, this is routed to V_{OUT} . If V_{CC} fails, V_{BATT} is routed to V_{OUT} . V_{OUT} can supply up to 100 mA from V_{CC} , but if more current is required, an external PNP transistor can be added. When V_{CC} is higher than V_{BATT} , the BATT ON output goes low, providing up to 25 mA of base drive for the external transistor. A 0.1 μ F capacitor is connected to V_{OUT} to supply the transient currents for CMOS RAM. When V_{CC} is lower than V_{BATT} , an internal 20 Ω MOSFET connects the backup battery to V_{OUT} .

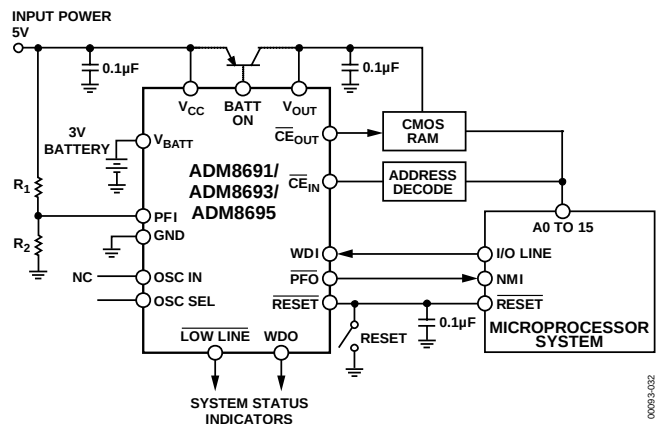


Figure 32. ADM8691/ADM8693/ADM8695 Typical Application

RESET OUTPUT

The internal voltage detector monitors V_{CC} and generates a RESET output to hold the microprocessor reset line low when V_{CC} is below 4.65 V (4.4 V for ADM8693). An internal timer holds RESET low for 50 ms (200 ms for the ADM8695) after V_{CC} rises above 4.65 V (4.4 V for the ADM8693). This prevents repeated toggling of RESET, even if the 5 V power drops out and recovers with each power line cycle.

The crystal oscillator normally used to generate the clock for microprocessors can take several milliseconds to stabilize. Because most microprocessors need several clock cycles to reset, RESET must be held low until the microprocessor clock oscillator has started. The power-up RESET pulse lasts 50 ms

(200 ms for the ADM8695) to allow for this oscillator start-up time. If a different reset pulse width is required, a capacitor should be connected to OSC IN, or an external clock can be used. Refer to Table 5 and Figure 17, Figure 18, Figure 19, and Figure 20. The manual reset switch and the 0.1 μ F capacitor connected to the reset line can be omitted if a manual reset is not needed. An inverted, active high, RESET output is also available.

POWER-FAIL DETECTOR

The 5 V V_{CC} power line is monitored via a resistive potential divider connected to the power-fail input (PFI). When the voltage at PFI falls below 1.3 V, the power-fail output ($\overline{PFO}$) drives the processor's NMI input low. If, for example, a power-fail threshold of 4.8 V is set with Resistor R_1 and Resistor R_2 , the microprocessor has the time when V_{CC} falls from 4.8 V to 4.65 V to save data into RAM. An earlier power-fail warning can be generated if the unregulated dc input to the 5 V regulator is available for monitoring. This allows more time for microprocessor housekeeping tasks to be completed before power is lost.

RAM WRITE PROTECTION

The ADM8691/ADM8693/ADM8695 $\overline{CE}_{OUT}$ line drives the chip select inputs of the CMOS RAM. $\overline{CE}_{OUT}$ follows $\overline{CE}_{IN}$ as long as V_{CC} is above the 4.65 V (4.4 V for the ADM8693) reset threshold.

If V_{CC} falls below the reset threshold, $\overline{CE}_{OUT}$ goes high, independent of the logic level at $\overline{CE}_{IN}$. This prevents the

microprocessor from writing erroneous data into RAM during power-up, power-down, brownouts, and momentary power interruptions.

WATCHDOG TIMER

The microprocessor drives the watchdog input (WDI) with an input/output line. When OSC IN and OSC SEL are unconnected, the microprocessor must toggle the WDI pin once every 1.6 seconds to verify proper software execution. If a hardware or software failure occurs such that WDI is not toggled, the ADM8691/ADM8693 issues a 50 ms (200 ms for the ADM8695) $\overline{RESET}$ pulse after 1.6 seconds. This typically restarts the microprocessor power-up routine. A new $\overline{RESET}$ pulse is issued every 1.6 seconds until WDI is again strobed. If a different watchdog timeout period is required, a capacitor should be connected to OSC IN or an external clock can be used. Refer to Table 5 and Figure 17, Figure 18, Figure 19, and Figure 20.

The watchdog output ($\overline{WDO}$) goes low if the watchdog timer is not serviced within its timeout period. Once $\overline{WDO}$ goes low, it remains low until a transition occurs at WDI. The watchdog timer feature can be disabled by leaving WDI unconnected.

The $\overline{RESET}$ output has an internal 3 μ A pull-up and can either connect to an open collector reset bus or directly drive a CMOS gate without an external pull-up resistor.

OUTLINE DIMENSIONS

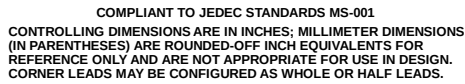


Figure 36. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-16)
Dimensions shown in millimeters and (inches)

Figure 1 is a mechanical drawing of the BSC package. It shows a top view and a side view. The top view includes dimensions for the package width (10.00 mm), pin pitch (1.27 mm), and pin width (0.25 mm). The side view shows the package height (6.20 mm) and the seating plane (1.35 mm). The package is labeled 'BSC' and 'SEATING PLANE'.

NOTES