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Team Nexperia



# PBRP113ZT

PNP 800 mA, 40 V BISS RET; R1 = 1 kΩ, R2 = 10 kΩ

Rev. 01 — 16 January 2008 Produc

Product data sheet

### **Product profile**

### 1.1 General description

800 mA PNP low V<sub>CEsat</sub> Breakthrough In Small Signal (BISS) Resistor-Equipped Transistor (RET) in a small SOT23 (TO-236AB) Surface-Mounted Device (SMD) plastic package.

NPN complement: PBRN113ZT.

### 1.2 Features

- 800 mA repetitive peak output current
- High current gain h<sub>FF</sub>
- Built-in bias resistors
- Simplifies circuit design
- Low collector-emitter saturation voltage
- Reduces component count
- Reduces pick and place costs
- ±10 % resistor ratio tolerance

### 1.3 Applications

- Digital application in automotive and industrial segments
- Medium current peripheral driver
- Switching loads

#### 1.4 Quick reference data

Table 1. **Quick reference data** 

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
$V_{\text{CEO}}$	collector-emitter voltage	open base		-	-	-40	V
Io	output current		[1][2]	-	-	-600	mA
I <sub>ORM</sub>	repetitive peak output current	$\begin{array}{l} t_p \leq 1 \text{ ms;} \\ \delta \leq 0.33 \end{array}$	[3]	-	-	-800	mA
R1	bias resistor 1 (input)			0.7	1	1.3	kΩ
R2/R1	bias resistor ratio			9	10	11	

<sup>[1]</sup> Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.



<sup>[2]</sup> Device mounted on a ceramic PCB, Al<sub>2</sub>O<sub>3</sub>, standard footprint.

<sup>[3]</sup> Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

PNP 800 mA, 40 V BISS RET; R1 = 1 k $\Omega$ , R2 = 10 k $\Omega$ 

## 2. Pinning information

Table 2. Pinning

Table 2.	riiiiiig		
Pin	Description	Simplified outline	Symbol
1	input (base)		
2	GND (emitter)	3	3
3	output (collector)	12	1 R1 R2
			evm003

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PBRP113ZT	-	plastic surface-mounted package; 3 leads	SOT23

### 4. Marking

Table 4. Marking codes

Type number	Marking code <sup>[1]</sup>
PBRP113ZT	*7M

[1] \* = -: made in Hong Kong

\* = p: made in Hong Kong

\* = t: made in Malaysia

\* = W: made in China

### 5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

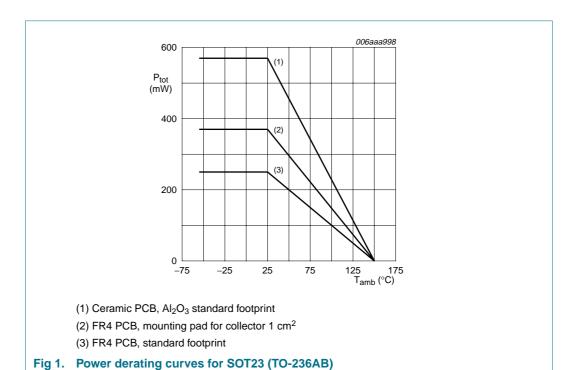
Symbol	Parameter	Conditions	Min	Max	Unit
$V_{\text{CBO}}$	collector-base voltage	open emitter	-	-40	V
$V_{CEO}$	collector-emitter voltage	open base	-	-40	V
$V_{EBO}$	emitter-base voltage	open collector	-	-5	V
VI	input voltage				
	positive		-	+5	V
	negative		-	-10	V
Io	output current		[1][2]	-600	mA
I <sub>ORM</sub>	repetitive peak output current	$t_p \le 1 \text{ ms};$ $\delta \le 0.33$	[3] -	-800	mA

#### PNP 800 mA, 40 V BISS RET; R1 = 1 k $\Omega$ , R2 = 10 k $\Omega$

**Table 5.** Limiting values ...continued
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
P <sub>tot</sub>	total power dissipation	$T_{amb} \le 25  ^{\circ}C$			
			[3] _	250	mW
			<u>[1]</u> -	370	mW
			[2] _	570	mW
Tj	junction temperature		-	150	°C
T <sub>amb</sub>	ambient temperature		-55	+150	°C
T <sub>stg</sub>	storage temperature		-65	+150	°C

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.
- [2] Device mounted on a ceramic PCB, Al<sub>2</sub>O<sub>3</sub>, standard footprint.
- [3] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.



PBRP113ZT\_1

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PNP 800 mA, 40 V BISS RET; R1 = 1 k $\Omega$ , R2 = 10 k $\Omega$ 

### 6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
$R_{th(j-a)}$	thermal resistance from	in free air					
	junction to ambient		<u>[1]</u>	-	-	500	K/W
			[2]	-	-	338	K/W
			[3]	-	-	219	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	-	105	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.
- [3] Device mounted on a ceramic PCB, Al<sub>2</sub>O<sub>3</sub>, standard footprint.

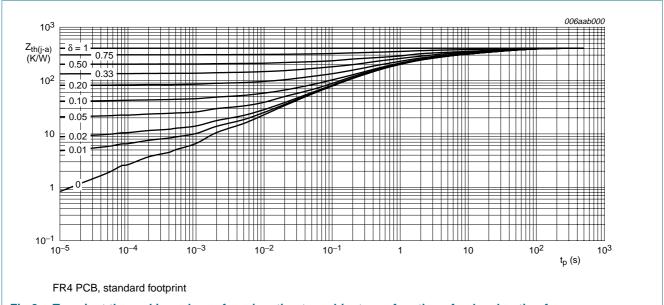
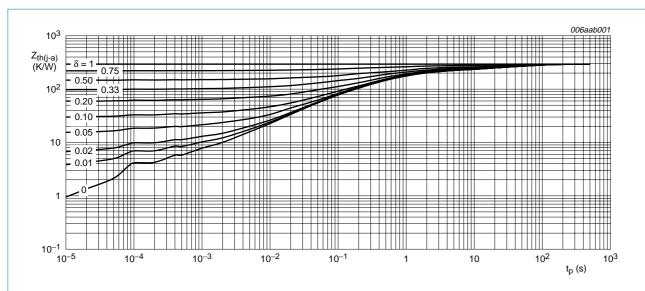


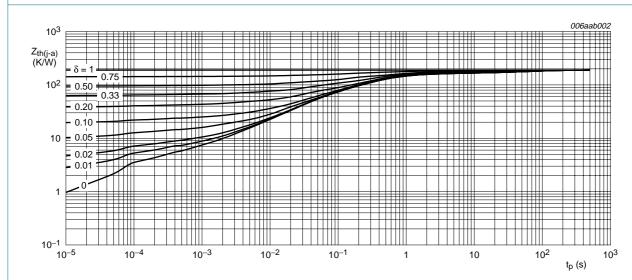
Fig 2. Transient thermal impedance from junction to ambient as a function of pulse duration for SOT23 (TO-236AB); typical values

PNP 800 mA, 40 V BISS RET; R1 = 1 k $\Omega$ , R2 = 10 k $\Omega$ 



FR4 PCB, mounting pad for collector 1 cm<sup>2</sup>

Fig 3. Transient thermal impedance from junction to ambient as a function of pulse duration for SOT23 (TO-236AB); typical values



Ceramic PCB, Al<sub>2</sub>O<sub>3</sub> standard footprint

Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration for SOT23 (TO-236AB); typical values

PNP 800 mA, 40 V BISS RET; R1 = 1 k $\Omega$ , R2 = 10 k $\Omega$ 

### 7. Characteristics

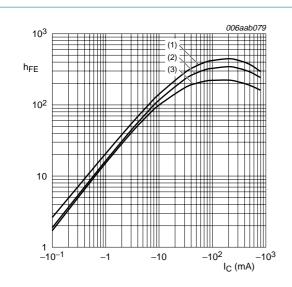
Table 7. Characteristics

 $T_{amb} = 25 \,^{\circ}C$  unless otherwise specified.

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
I <sub>CBO</sub>	collector-base cut-off current	$V_{CB} = -30 \text{ V};$ $I_E = 0 \text{ A}$		-	-	-100	nA
I <sub>CEO</sub>	collector-emitter cut-off current	$V_{CE} = -30 \text{ V};$ $I_{B} = 0 \text{ A}$		-	-	-0.5	μΑ
I <sub>EBO</sub>	emitter-base cut-off current	$V_{EB} = -5 \text{ V};$ $I_{C} = 0 \text{ A}$		-	-	-0.8	mA
h <sub>FE</sub> DC current gain	DC current gain	$V_{CE} = -5 \text{ V};$ $I_{C} = -50 \text{ mA}$		190	270	-	
		$V_{CE} = -5 \text{ V};$ $I_{C} = -300 \text{ mA}$	<u>[1]</u>	230	320	-	
		$V_{CE} = -5 \text{ V};$ $I_{C} = -600 \text{ mA}$	<u>[1]</u>	190	270	-	
V <sub>CEsat</sub>	collector-emitter saturation voltage	$I_C = -50 \text{ mA};$ $I_B = -2.5 \text{ mA}$		-	-35	<del>-4</del> 5	mV
		$I_C = -200 \text{ mA};$ $I_B = -10 \text{ mA}$		-	-70	-100	mV
		$I_C = -500 \text{ mA};$ $I_B = -10 \text{ mA}$	<u>[1]</u>	-	-200	-300	mV
		$I_{C} = -600 \text{ mA};$ $I_{B} = -6 \text{ mA}$	[1]	-	-450	-750	mV
$V_{I(off)}$	off-state input voltage	$V_{CE} = -5 \text{ V};$ $I_{C} = -100 \mu\text{A}$		-0.3	-0.5	-1	V
$V_{I(on)}$	on-state input voltage	$V_{CE} = -0.3 \text{ V};$ $I_{C} = -20 \text{ mA}$		-0.4	-0.7	-1.4	V
R1	bias resistor 1 (input)			0.7	1	1.3	kΩ
R2/R1	bias resistor ratio			9	10	11	
C <sub>c</sub>	collector capacitance	$V_{CB} = -10 \text{ V};$ $I_E = i_e = 0 \text{ A};$ $f = 1 \text{ MHz}$		-	11	-	pF

<sup>[1]</sup> Pulse test:  $t_p \le 300 \ \mu s$ ;  $\delta \le 0.02$ .

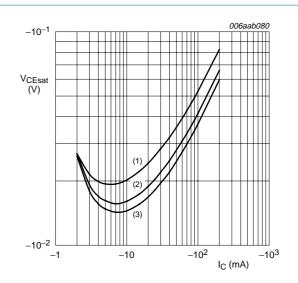
PNP 800 mA, 40 V BISS RET; R1 = 1 k $\Omega$ , R2 = 10 k $\Omega$ 



$$V_{CE} = -5 \text{ V}$$

- (1)  $T_{amb} = 100 \, ^{\circ}C$
- (2)  $T_{amb} = 25 \, ^{\circ}C$
- (3)  $T_{amb} = -40 \, ^{\circ}C$

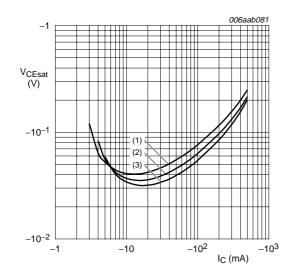
Fig 5. DC current gain as a function of collector current; typical values



$$I_{\rm C}/I_{\rm B} = 20$$

- (1)  $T_{amb} = 100 \, ^{\circ}C$
- (2)  $T_{amb} = 25 \, ^{\circ}C$
- (3)  $T_{amb} = -40 \, ^{\circ}C$

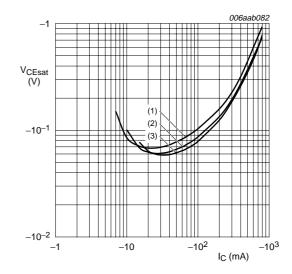
Fig 6. Collector-emitter saturation voltage as a function of collector current; typical values





- (1)  $T_{amb} = 100 \, ^{\circ}C$
- (2)  $T_{amb} = 25 \, ^{\circ}C$
- (3)  $T_{amb} = -40 \, ^{\circ}C$

Fig 7. Collector-emitter saturation voltage as a function of collector current; typical values

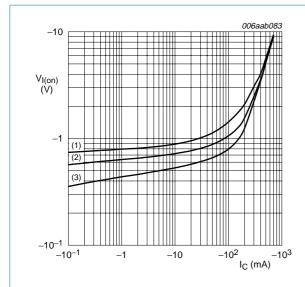


$$I_{\rm C}/I_{\rm B} = 100$$

- (1)  $T_{amb} = 100 \, ^{\circ}C$
- (2)  $T_{amb} = 25 \, ^{\circ}C$
- (3)  $T_{amb} = -40 \, ^{\circ}C$

Fig 8. Collector-emitter saturation voltage as a function of collector current; typical values

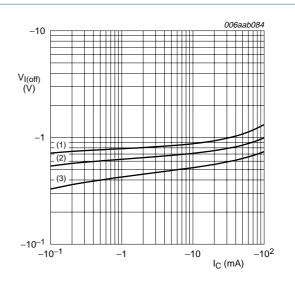
PNP 800 mA, 40 V BISS RET; R1 = 1 k $\Omega$ , R2 = 10 k $\Omega$ 





- (1)  $T_{amb} = -40 \, ^{\circ}C$
- (2)  $T_{amb} = 25 \, ^{\circ}C$
- (3)  $T_{amb} = 100 \, ^{\circ}C$

Fig 9. On-state input voltage as a function of collector current; typical values

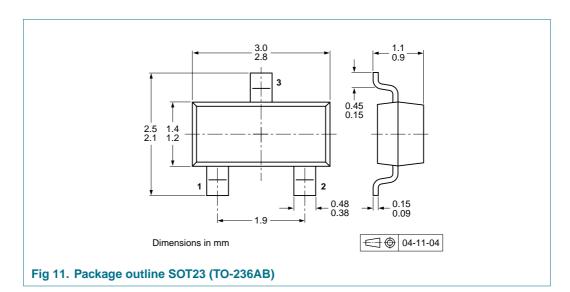


$$V_{CE} = -5 \text{ V}$$

- (1)  $T_{amb} = -40 \, ^{\circ}C$
- (2)  $T_{amb} = 25 \, ^{\circ}C$
- (3)  $T_{amb} = 100 \, ^{\circ}C$

Fig 10. Off-state input voltage as a function of collector current; typical values

### 8. Package outline



PNP 800 mA, 40 V BISS RET; R1 = 1 k $\Omega$ , R2 = 10 k $\Omega$ 

### 9. Packing information

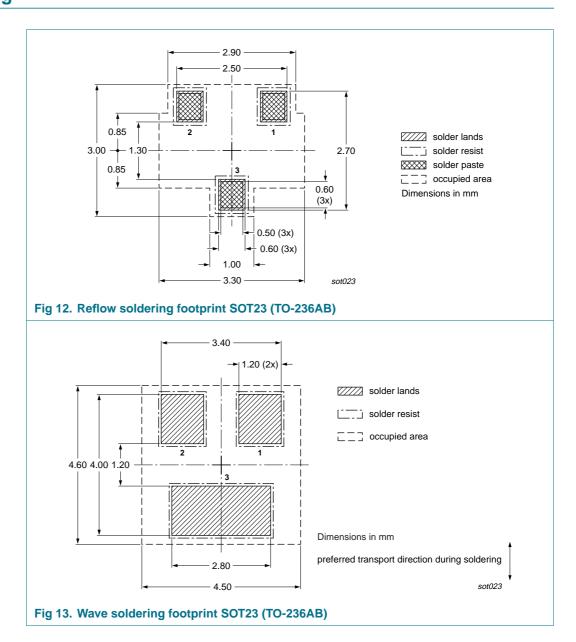
Table 8. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.[1]

Type number	Package Description		Packing of	quantity
			3000	10000
PBRP113ZT	SOT23	4 mm pitch, 8 mm tape and reel	-215	-235

<sup>[1]</sup> For further information and the availability of packing methods, see  $\underline{\text{Section 13}}$ .

### 10. Soldering



PNP 800 mA, 40 V BISS RET; R1 = 1 k $\Omega$ , R2 = 10 k $\Omega$ 

## 11. Revision history

### Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PBRP113ZT_1	20080116	Product data sheet	-	-

PNP 800 mA, 40 V BISS RET; R1 = 1 k $\Omega$ , R2 = 10 k $\Omega$ 

### 12. Legal information

#### 12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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NXP Semiconductors

## PBRP113ZT

### PNP 800 mA, 40 V BISS RET; R1 = 1 k $\Omega$ , R2 = 10 k $\Omega$

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