

R2A20166NP/SA

8-bit 6ch D/A Converter with Buffer Amplifiers

R03DS0018EJ0100 Rev.1.00 2011.09.05

Description

The R2A20166 is an integrated circuit semiconductor of CMOS structure with 6 channels of built in D/A unnecessary and enabling configuration of a system with few component parts.

Serial data transfer type input can easily be used through a combination of three lines: DI, CLK, and LD.

Outputs incorporate buffer op-amps that have a drive capacity of 1 mA or above for both sink source, and can operate over the entire voltage range from almost ground to Vcc (0 to 5V), making peripheral elements unnecessary and enabling configuration of a system with few component parts.

Very small QFN package is added to lineup. It is suitable for a small mounting and reduces the mounting area.

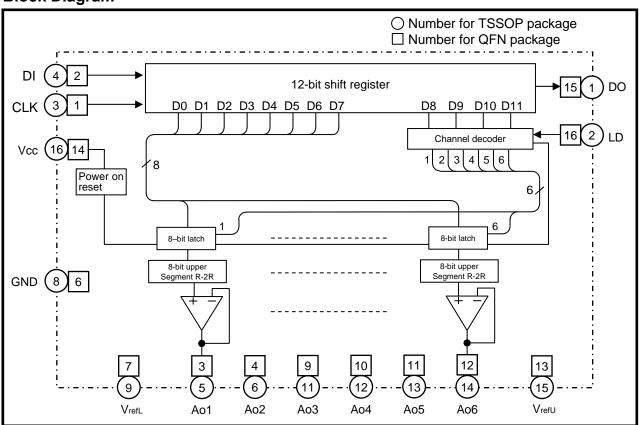
Features

- Guarantee Nonlinearity error : +/-1.0LSB, Differential nonlinearity error : +/-0.7LSB
- Data transfer format: 12-bit serial data input type by 3 wire (DI, SCK, LD)
- Output buffer op-amps: Operable over entire voltage range from almost ground to Vcc (0 to 5V)
- Very small size package line-up: QFN-16(pin pitch: 0.5mm), TSSOP-16 (pin pitch 0.65mm)

Application

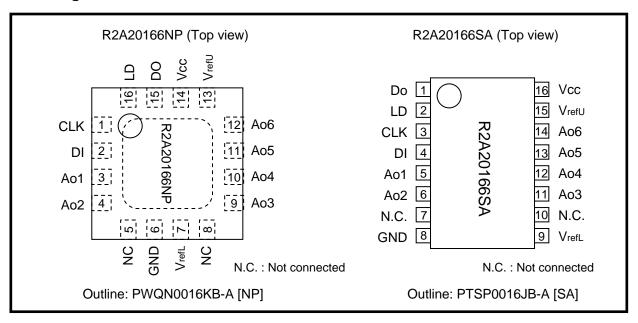
- Conversion from digital data to analog control data for home-use and industrial equipment.
- Signal gain control or automatic adjustment of LCD-TV, PDP-TV or LCD display-monitor.
- Blurring correction control or various control of the interchangeable lens of digital still camera.
- Automatic adjustment by combination with microcomputer and EEPROM. (substitution of half fixed resistance)

Block Diagram



New Product

Pin Arrangement



Pin Description

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Pir	Pin No.		Function						
[QFN]	[TSSOP]	Symbol	FUNCTION						
2	4	DI	Serial data input terminal. (Input serial data with a 12-bit data length)						
1	3	CLK	Serial clock input terminal (Input signal from DI terminal is input to 12-bit shift register at rise of serial clock.)						
16	2	LD	Load terminal (When High level is input to LD terminal, value in 12-bit shift register is loaded into decoder and 8-bit latch.)						
15	1	Do	Serial data output terminal (Data is sequentially output from the MSB bit.)						
3	5	Ao1							
4	6	Ao2							
9	11	Ao3	8-bit resolution D/A converter output terminals						
10	12	Ao4	(After power on, all channels are reset and DAC data 00h is output.)						
11	13	Ao5							
12	14	Ao6							
14	16	Vcc	Power supply terminal						
6	8	GND	GND terminal						
13	15	VrefU	D/A converter upper reference voltage input terminal						
7	9	VrefL	D/A converter lower reference voltage input terminal						
5	7	N.C.	Not connected						
8	10	N.C.	Not connected						

Absolute Maximum Ratings

(Ta= +25deg unless otherwise noted)

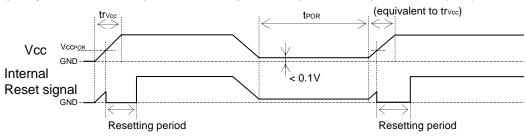
Item	Symbol	Conditions	Ratings	Unit
Supply voltage	Vcc		-0.3 to +6.5	V
D/A converter upper reference voltage	VrefU		-0.3 to +6.5	V
D/A converter lower reference voltage	VrefL		-0.3 to +6.5	V
Buffer amplifier output current	Iao	Continuous	-2.0 to +2.0	mA
Input voltage	Vin		-0.3 to Vcc+0.3 <+6.5	V
Output voltage	Vo		-0.3 to Vcc+0.3 <+6.5	V
Power dissipation	Pd	Ta= +85deg	290(NP) / 150(SA)	mW
Thermal derating factor	K theta	Ta> +25deg	7.25(NP) / 3.75(SA)	mW/deg
Operating temperature	Topr		-30 to +85	deg
Storage temperature	Tstg		-40 to +125	deg

Electrical Characteristics

« Digital Part » (Vcc, VrefU = +5V +/-10%, Vcc>VrefU, GND, VrefL =0V, Ta= -30 to +85deg, Unless otherwise noted)

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Item	Symbol	Test conditions	Min	Тур	Max	Unit
Supply voltage	Vcc		2.7	5.0	5.5	V
Supply current	Icc	CLK = 1MHz, Vcc =5V, Iao =0µA	-	0.35	1.1	mA
Input leak current	lilk	VIN = 0 to Vcc	-10	-	10	μΑ
Input low voltage	VIL		-	-	0.2Vcc	V
longt high voltage	Vıн	4.0V < Vcc	0.5Vcc	-	-	V
Input high voltage		Vcc ≤ 4.0V	0.8Vcc	-	-	V
Output low voltage	Vol	4.0V < Vcc, loL = 2.0 mA	-	-	0.4	V
Output low voltage	VOL	Vcc < 4.0V, loL = 1.5 mA	-	-	0.4	V
Output high voltage	Vон	Іон = -400 μА	Vcc - 0.4	-	-	V
Supply voltage rise time *1	trvcc	Vcc = 0 to 2.7V	100	-	-	μs
Internal reset VCCPOR operating voltage *1		Vcc = 0 to 2.7V	-	1.5	1.9	V
Power supply restart interval (Power supply OFF → ON) *1	t POR	Vcc < 0.1V	1	-	-	ms

^{*1 :} When power supply is turned on, internal circuit is initialized by power on reset circuit. But, if re-powered on quickly, initialize is not operate. So, keep the time period of re-powered on (tpor).



« Analog Part » (Vcc, VrefU = +5V +/-10%, Vcc>VrefU, GND, VrefL =0V, Ta= -30 to +85deg, unless otherwise noted)

Item	Symbol	Test conditions		Unit		
nem	Symbol	rest conditions	Min	Тур	Max	Unit
Current dissipation	lref∪	V _{refU} =5V, V _{refL} =0V, I _A 0=0μA, Data condition: at maximum current	-	0.8	1.6	mA
D/A converter upper reference voltage range *2	VrefU		0.7Vcc	-	Vcc	V
D/A converter lower reference voltage range *2	VrefL		GND	-	0.3Vcc	V
Buffer amplifier output	Vao	IAO = +/- 100 μA	0.1	-	Vcc - 0.1	V
voltage range		IAO = +/- 500 μA	0.2	-	Vcc - 0.2	V
Buffer amplifier output drive range		Upper side saturation voltage = 0.3V, Lower side saturation voltage = 0.2V	-1.0	-	1.0	mA
Differential nonlinearity	SDL	1/ 4.701/	-0.7	-	0.7	LSB
Nonlinearity	SL	$V_{refU} = 4.79V,$ $V_{refL} = 0.95V,$	-1.0	-	1.0	LSB
Zero code error	Szero	Vcc = 5.5V (15mV/LSB),	-2.0	-	2.0	LSB
Full scale error	SFULL	Without load (IAO =0μA)	-2.0	-	2.0	LSB
Output capacitive load	Co		-	-	0.1	μF
Buffer amplifier output impedance	Ro		-	5.0	-	ohm

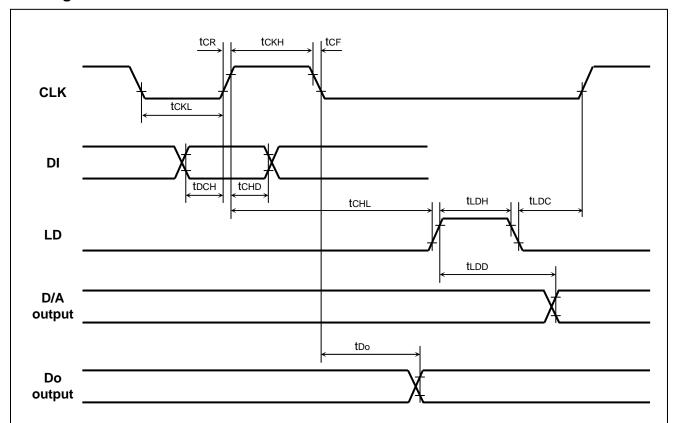
^{*2 :} The output does not necessary be the value with the reference voltage setting range. The output value is determined by the buffer amplifier output voltage range (VAO).

AC Characteristics

(Vcc, VrefU = +5V + /-10%, $Vcc \ge VrefU$, GND = VrefL = 0V, Ta = -30 to +85deg, unless otherwise noted)

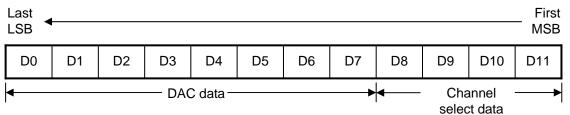
				11.24		
Item	Symbol Test conditions		Min	Тур	Max	Unit
Clock frequency	fclk		-	1.0	10	MHz
Clock low pulse width	tckl		40	-	-	ns
Clock high pulse width	tскн		40	-	-	ns
Clock rise time	tcr		-	-	200	ns
Clock fall time	tcf		-	-	200	ns
Data setup time	t DCH		4	-	-	ns
Data hold time	t CHD		30	-	-	ns
LD setup time	tchl		40	-	-	ns
LD hold time	tldc		40	-	-	ns
LD high pulse width	t LDH		40	-	-	ns
Data output delay time	tDO	CL < 100 pF	-10	-	50	ns
D/A output settling time	tldd	Ta=25deg, CL<100pF, Vao: 0.5←→4.5V, The time until the output becomes the final value of 1/2 LSB.	1	-	150	μs

Timing Chart



(Note) Timing chart above is a schematic representation of the timing of each signal type. CLK signal input is High or Low regardless, LD signal High input is enabled.

Digital Data Format



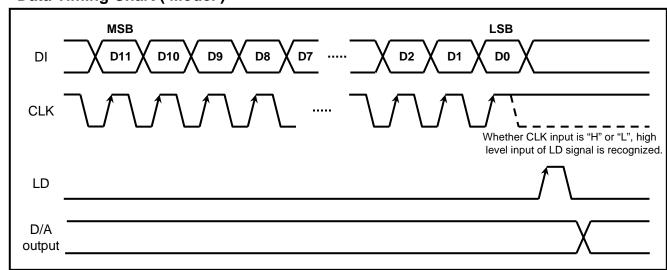
Channel select data

D8	D9	D10	D11	Chanel Selection
0	0	0	0	Don't care
0	0	0	1	Ao1 select
0	0	1	0	Ao2 select
0	0	1	1	Ao3 select
0	1	0	0	Ao4 select
0	1	0	1	Ao5 select
0	1	1	0	Ao6 select
0	1	1	1	Don't care
:	:	:	:	:
1	1	1	0	Don't care
1	1	1	1	Don't care

DAC data

D0	D1	D2	D3	D4	D5	D6	D7	D/A Output
0	0	0	0	0	0	0	0	(V _{refU} - V _{refL}) / 256 x 1 + V _{refL}
1	0	0	0	0	0	0	0	(V _{refU} - V _{refL}) / 256 x 2 + V _{refL}
0	1	0	0	0	0	0	0	(V _{refU} - V _{refL}) / 256 x 3 + V _{refL}
1	1	0	0	0	0	0	0	(V _{refU} - V _{refL}) / 256 x 4 + V _{refL}
:	:	:	:	:	:	:	:	:
0	1	1	1	1	1	1	1	(V _{ref} ∪ − V _{ref} L) / 256 x 255 + V _{ref} L
1	1	1	1	1	1	1	1	V _{ref} U

Data Timing Chart (Model)

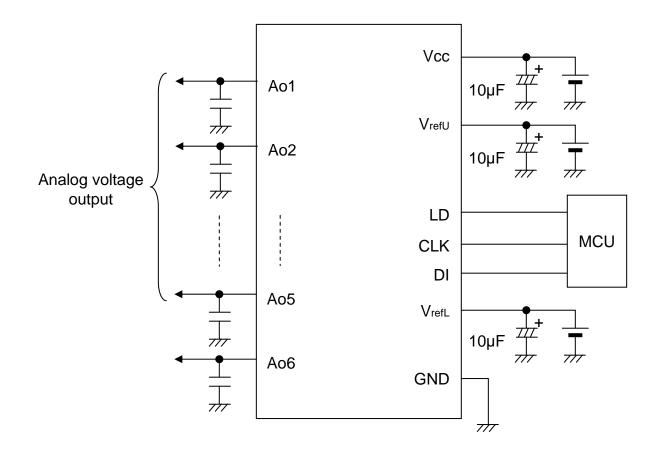


Precaution For Use

• There are three terminals (Vcc, V_{refU}, V_{refL}) that should be impressed a constant voltage. When ripple or spike noise is input to this terminal, there is fear that the accuracy of D/A conversion becomes lower and this IC malfunction. So, when use this IC, please connect capacitor between these terminals (Vcc, V_{refU}, V_{refL}) and GND for stable D/A conversion.

• This IC's output amplifier has an advantage to capacitive load, So, it's no problem at device action when connect capacitor (0.1µF Max) among output to GND for every noise elimination.

Standard Application Circuit

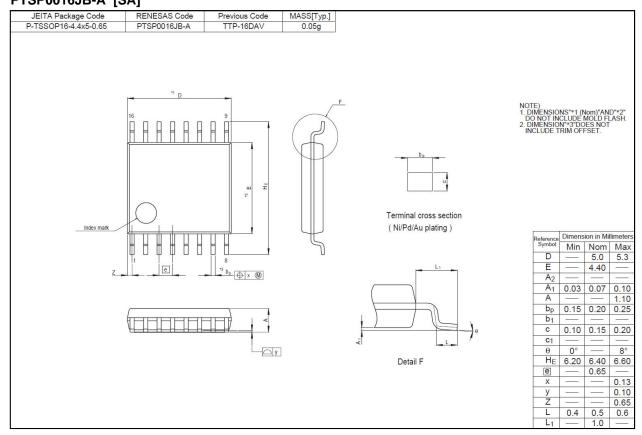


Ordering Information

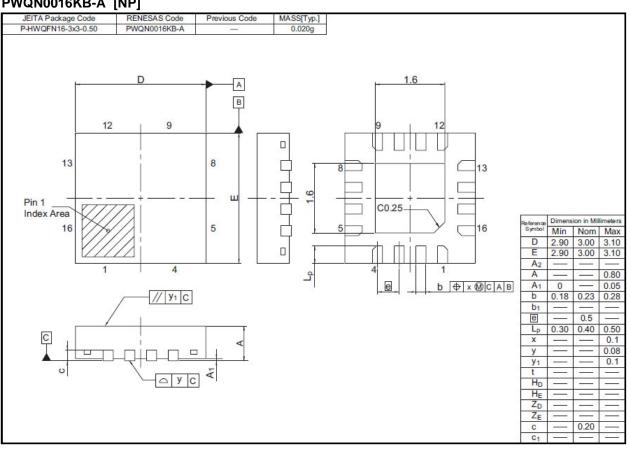
Order part No.	Order part No. Package Name		Package type No.	Packing/Quantity	
R2A20166SA	TSSOP-16	RTSP0016JB-A	SA	Embossed Taping/2,000 pcs.	
R2A20166NP	QFN-16	PWQN0016KB-A	NP	Embossed Taping/3,000 pcs.	

New Product

Package Dimensions PTSP0016JB-A [SA]



PWQN0016KB-A [NP]



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