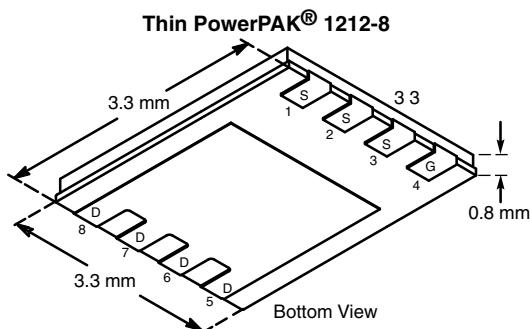


P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω) Max.	I_D (A) ^a	Q_g (Typ.)
- 20	0.0054 at $V_{GS} = - 4.5V$	- 30 ^a	57 nC
	0.0060 at $V_{GS} = - 3.7 V$	- 30 ^a	
	0.0083 at $V_{GS} = - 2.5 V$	- 30 ^a	
	0.0140 at $V_{GS} = - 1.8 V$	- 30 ^a	


Ordering Information:

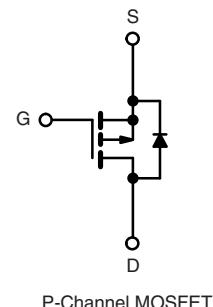
SiS435DNT-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

- TrenchFET[®] Gen III P-Channel Power MOSFET
- Thin 0.8 mm max. height
- 100 % R_g and UIS Tested
- Material categorization:
For definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT
HALOGEN
FREE
APPLICATIONS

- Smart Phones, Tablet PCs, and Mobile Computing
- Battery Switch
- Load Switch
- Power Management
- Battery Management



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	- 20	V
Gate-Source Voltage	V_{GS}	± 8	
Continuous Drain Current ($T_J = 150^\circ\text{C}$)	I_D	- 30 ^a	A
		- 30 ^a	
		- 22 ^{b, c}	
		- 17 ^{b, c}	
Pulsed Drain Current ($t = 300 \mu\text{s}$)	I_{DM}	- 80	
Continuous Source-Drain Diode Current	I_S	- 30 ^a	
		- 3.1 ^{b, c}	
Avalanche Current	I_{AS}	- 20	
Single Pulse Avalanche Energy	E_{AS}	20	
Maximum Power Dissipation	P_D	39	W
		25	
		3.7 ^{b, c}	
		2.4 ^{b, c}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	R_{thJA}	24	33	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	2.4	3.2	

Notes:

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- $t = 10 \text{ s}$.
- See solder profile (www.vishay.com/doc?73257). The Thin PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 81 °C/W.

SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)

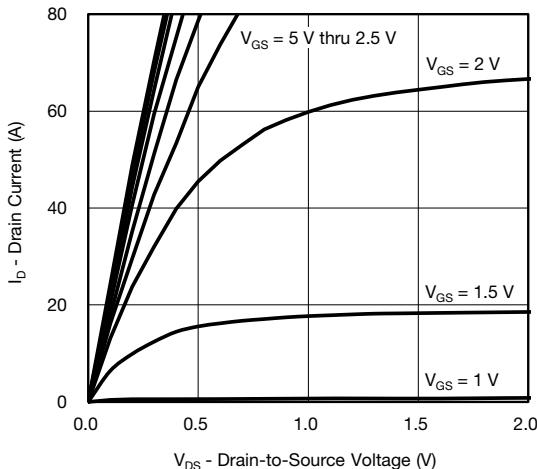
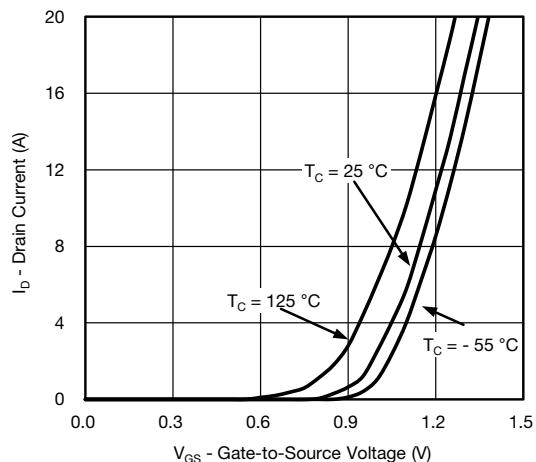
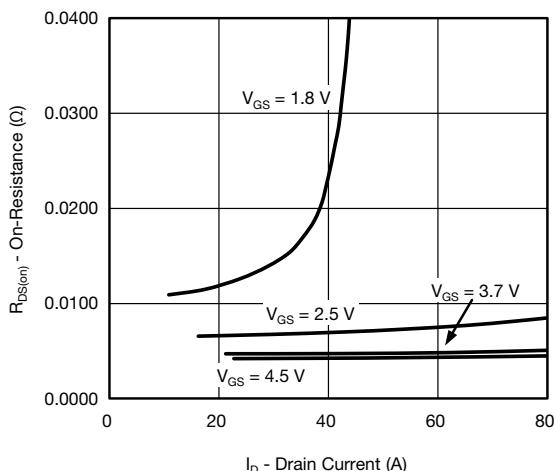
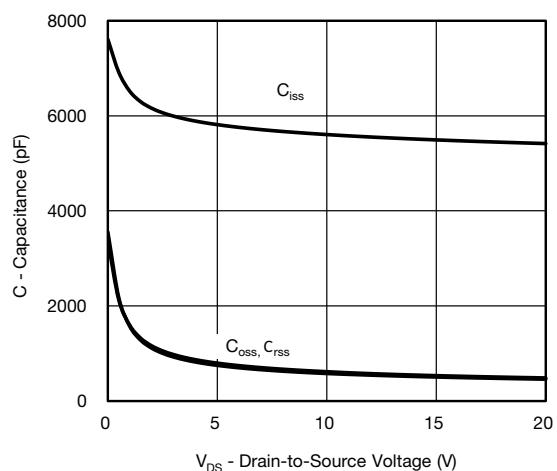
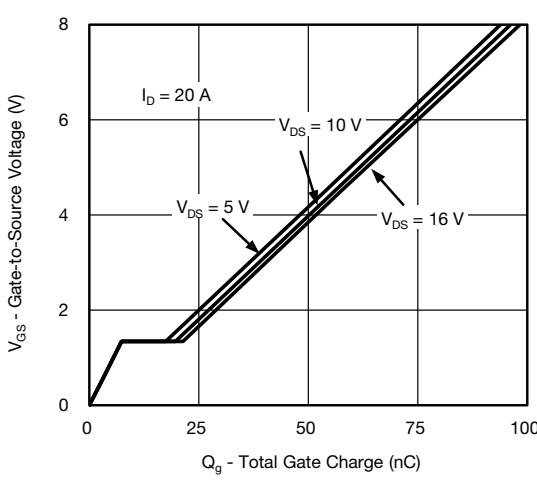
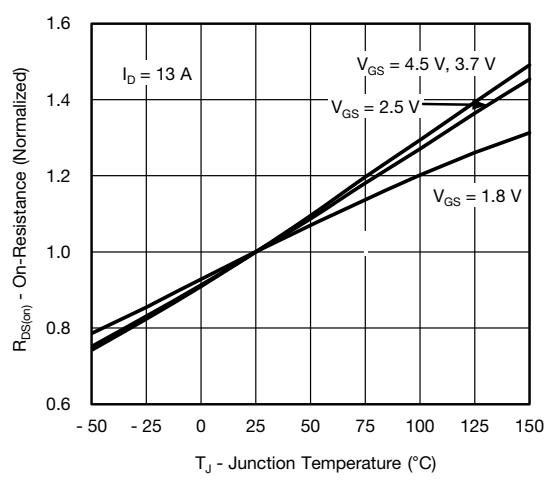
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}$, $I_D = -250 \mu\text{A}$	- 20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250 \mu\text{A}$		- 16		mV/ $^\circ\text{C}$
$V_{GS(\text{th})}$ Temperature Coefficient	$\Delta V_{GS(\text{th})}/T_J$			2.9		
Gate-Source Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$, $I_D = -250 \mu\text{A}$	- 0.4		- 0.9	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}$, $V_{GS} = \pm 8 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -20 \text{ V}$, $V_{GS} = 0 \text{ V}$			- 1	μA
		$V_{DS} = -20 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 55^\circ\text{C}$			- 10	
On-State Drain Current ^a	$I_{D(\text{on})}$	$V_{DS} \leq -5 \text{ V}$, $V_{GS} = -4.5 \text{ V}$	- 20			A
Drain-Source On-State Resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = -4.5 \text{ V}$, $I_D = -13 \text{ A}$		0.0044	0.0054	Ω
		$V_{GS} = -3.7 \text{ V}$, $I_D = -10 \text{ A}$		0.0048	0.0060	
		$V_{GS} = -2.5 \text{ V}$, $I_D = -10 \text{ A}$		0.0065	0.0083	
		$V_{GS} = -1.8 \text{ V}$, $I_D = -5 \text{ A}$		0.0110	0.0140	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -10 \text{ V}$, $I_D = -13 \text{ A}$		55		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = -10 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$		5700		pF
Output Capacitance	C_{oss}			620		
Reverse Transfer Capacitance	C_{rss}			585		
Total Gate Charge	Q_g	$V_{DS} = -10 \text{ V}$, $V_{GS} = -8 \text{ V}$, $I_D = -20 \text{ A}$		98	180	nC
		$V_{DS} = -10 \text{ V}$, $V_{GS} = -4.5 \text{ V}$, $I_D = -20 \text{ A}$		57	86	
Gate-Source Charge	Q_{gs}			7.4		
Gate-Drain Charge	Q_{gd}			13.1		
Gate Resistance	R_g	$f = 1 \text{ MHz}$	0.8	3.8	7.6	Ω
Turn-On Delay Time	$t_{d(\text{on})}$	$V_{DD} = -10 \text{ V}$, $R_L = 1 \Omega$ $I_D \cong -10 \text{ A}$, $V_{GEN} = -4.5 \text{ V}$, $R_g = 1 \Omega$		40	80	ns
Rise Time	t_r			30	60	
Turn-Off Delay Time	$t_{d(\text{off})}$			100	200	
Fall Time	t_f			30	60	
Turn-On Delay Time	$t_{d(\text{on})}$	$V_{DD} = -10 \text{ V}$, $R_L = 1 \Omega$ $I_D \cong -10 \text{ A}$, $V_{GEN} = -8 \text{ V}$, $R_g = 1 \Omega$		15	30	ns
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(\text{off})}$			110	220	
Fall Time	t_f			25	50	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$			- 30	A
Pulse Diode Forward Current	I_{SM}				- 80	
Body Diode Voltage	V_{SD}	$I_S = -10 \text{ A}$, $V_{GS} = 0 \text{ V}$		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -10 \text{ A}$, $dI/dt = 100 \text{ A}/\mu\text{s}$, $T_J = 25^\circ\text{C}$		19	40	ns
Body Diode Reverse Recovery Charge	Q_{rr}			10	20	
Reverse Recovery Fall Time	t_a			9		ns
Reverse Recovery Rise Time	t_b			10		

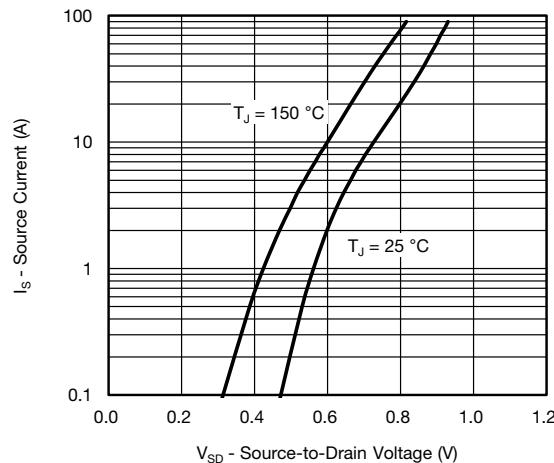
Notes:

a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.

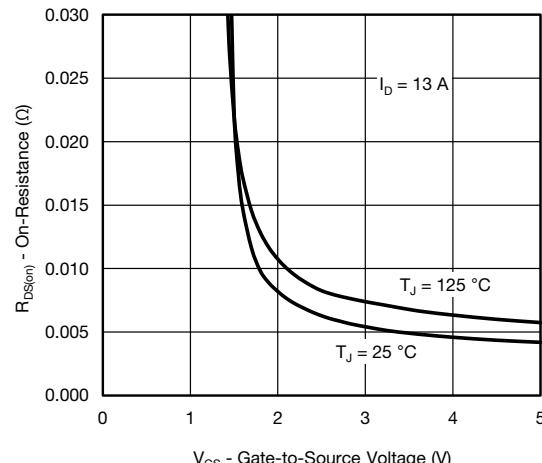
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

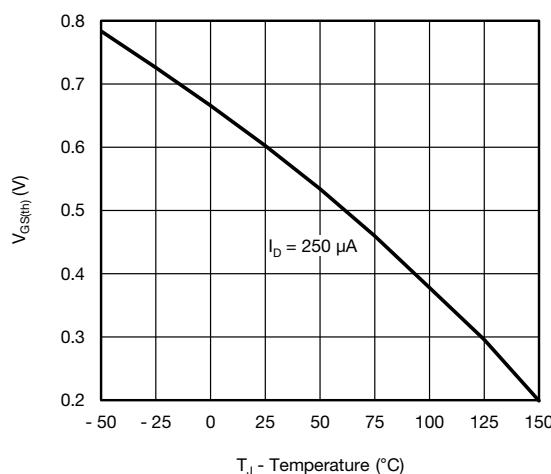
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current and Gate Voltage

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


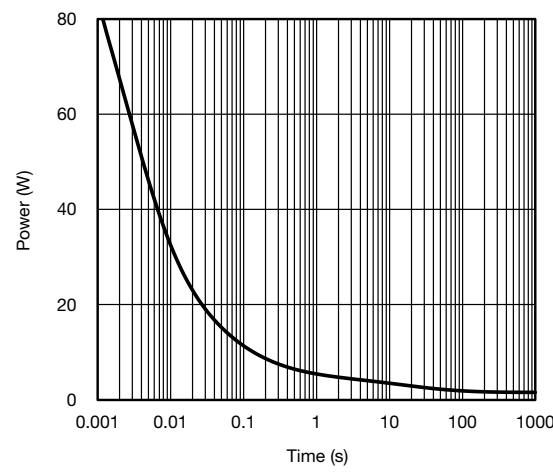
Source-Drain Diode Forward Voltage



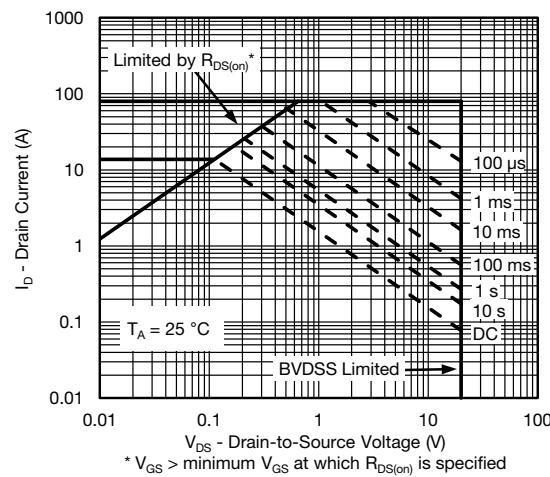
On-Resistance vs. Gate-to-Source Voltage



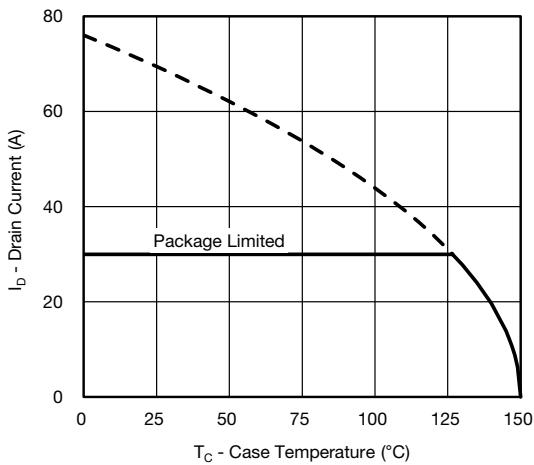
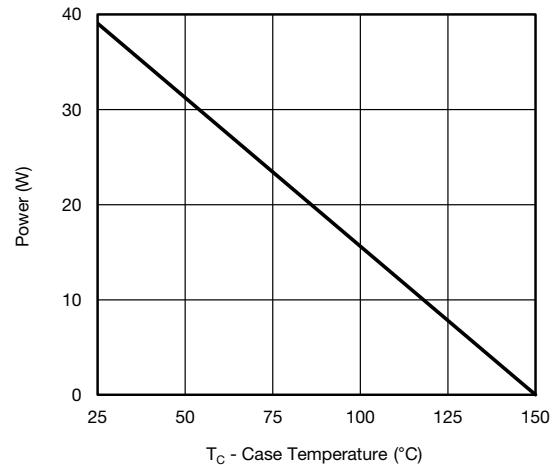
Threshold Voltage



Single Pulse Power, Junction-to-Ambient

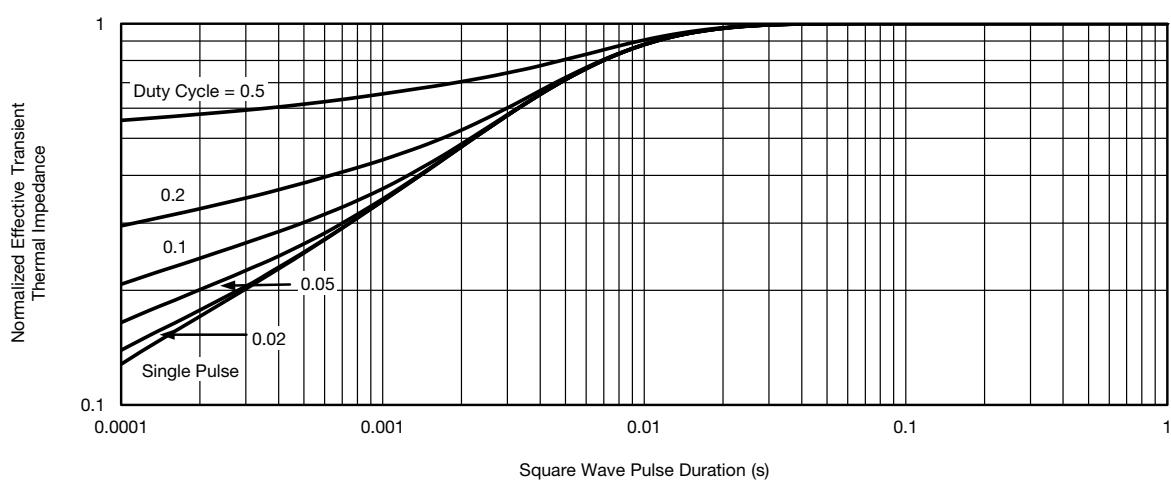
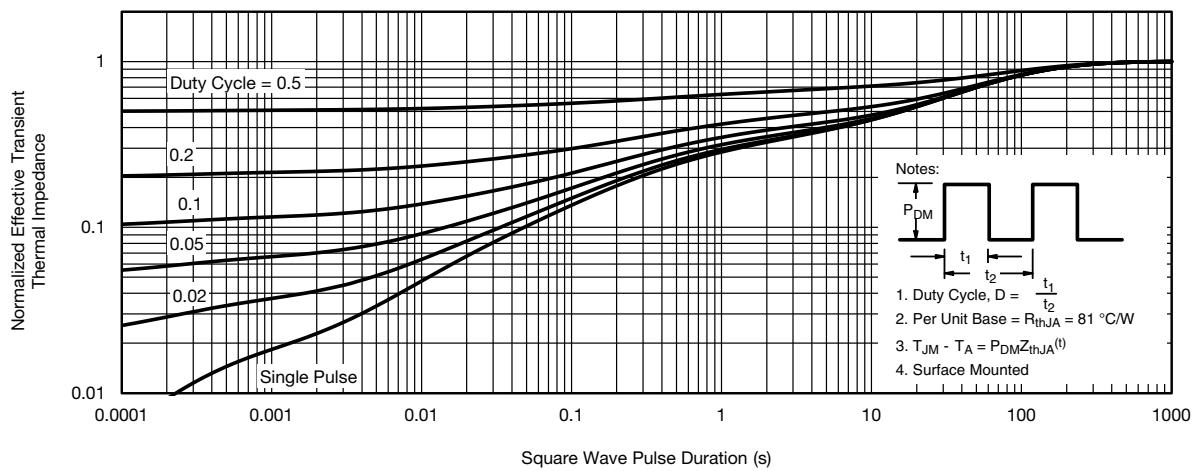


Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Current Derating*

Power Derating, Junction-to-Case

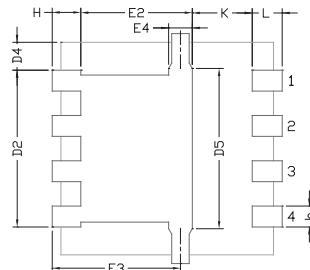
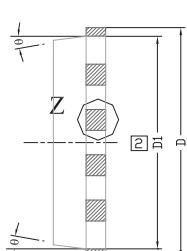
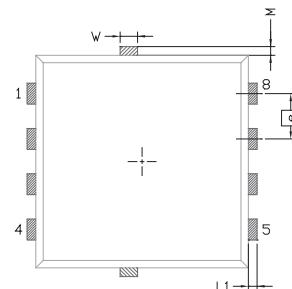
* The power dissipation P_D is based on T_{J(max.)} = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

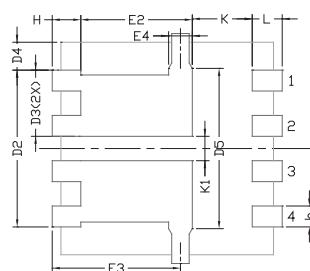


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PowerPAK® 1212-8T



BACKSIDE VIEW OF SINGLE PAD



BACKSIDE VIEW OF DUAL PAD

NOTE:
 1. MILLIMETER WILL GOVERN
 2. DIMENSIONS EXCLUSIVE OF MOLD
 FLASH AND CUTTING BURRS.
 3. DIMENSIONS EXCLUSIVE OF MOLD

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	-	0.05	0.000	-	0.002
b	0.23	0.30	0.41	0.009	0.012	0.016
c	0.23	0.28	0.33	0.009	0.011	0.013
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
D3	0.48	-	0.89	0.019	-	0.035
D4	0.47 TYP.			0.0185 TYP.		
D5	2.3 TYP.			0.090 TYP.		
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	1.75	1.85	1.98	0.069	0.073	0.078
E4	0.34 TYP.			0.013 TYP.		
e	0.65 BSC			0.026 BSC		
K	0.86 TYP.			0.034 TYP.		
K1	0.35	-	-	0.014	-	-
H	0.30	0.41	0.51	0.012	0.016	0.020
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 TYP.			0.005 TYP.		

ECN: T13-0056-Rev. A, 18-Feb-13

DWG: 6012

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