USB-910H

Embedded Systems Interface

FEATURES

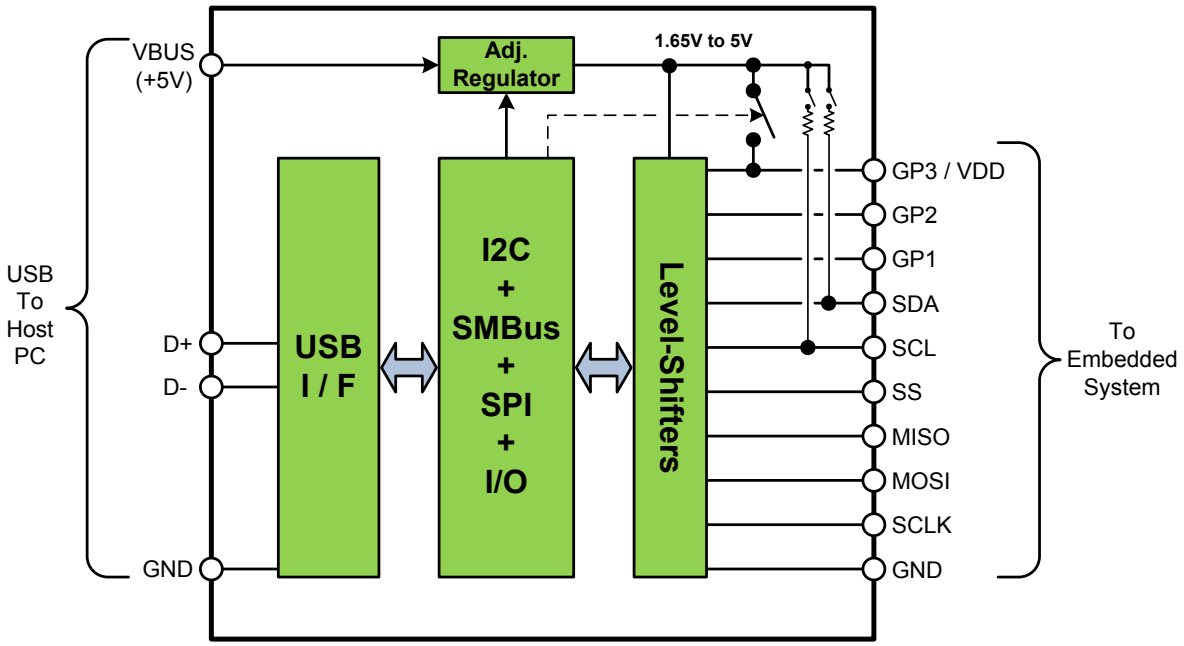
- SPI, I2C, SMBus Master or Slave
- Full I2C/SMBus Multi-Master Support
- Up to 9 General-Purpose I/O
- SMBus Timeouts and Bus-free Detect
- Supports PMBus Transport Layer
- Configurable I/O Levels from 1.65V to 5V
- SPI to 24MHz, I2C/SMBus to 1.5MHz
- Power the Target from the Adapter
- Responds to 16 Slave Addresses (or All)
- Up to 64kByte Transactions
- Powerful Scripting Feature
- Easy-to-use API for Software Development
- USB/HID - No User-Installed Device Drivers
- Built-in I2C Pull-ups with Enable

GENERAL DESCRIPTION

The Keterex USB-910H Embedded Systems Interface provides connectivity between a host PC and an embedded system requiring an I2C, SMBus, or SPI protocol. Other protocols can be supported by "bit-banging" up to 9 available general-purpose I/O. USB transactions are generated on the host PC using either the Keterex USB-900 Control Center application or calls to a provided API. The USB-910H Adapter converts these transactions to I2C, SMBus, SPI, or general-purpose I/O operations. Built-in scripting accommodates complex bus protocols, including combining bus transactions, timing, and general-purpose I/O operations.

The USB-910H Adapter provides configurable I/O voltage levels from 1.65V to 5V. In addition to setting the drive and sense logic levels, this voltage can be connected to the target hardware, providing up to 400mA to the target device.

FUNCTIONAL BLOCK DIAGRAM



1. RELATED DOCUMENTS

The following Keterex documents describe other components of the USB-910H Embedded Systems Interface:

1. Application Note AN2101 - The USB-910H API and Include File Reference Manual.
2. Application Note AN2102 - The USB-900 Control Center User's Guide.

2. REFERENCES

This datasheet assumes the reader is familiar with the I2C, SMBus, PMBus, SPI, and similar interfaces and standards. The following references are recommended:

1. *The I²C-Bus Specification*, Version 2.1, January 2000, Philips Semiconductors #939839340011.
2. *The I²C-Bus and How to Use it*, Philips Semiconductors #98808057501.
3. *System Management Bus (SMBus) Specification*, Version 2.0, August 3, 2000, SBS Implementers Forum.
4. *PMBus™ Power System Management Protocol Specification, Part I – General Requirements, Transport And Electrical Interface, Revision 1.0,* System Management Interface Forum, Inc., 28 March 2005.
5. *MICROWIRE™ Serial Interface,* National Semiconductor, Application Note 452, January 1992.

3. PERFORMANCE CHARACTERISTICS

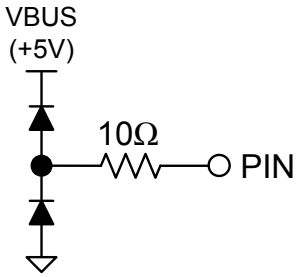
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Over-voltage Tolerance	except GP3	-0.3		VBUS+0.3	V
	GP3	-0.3		V_{IO}+0.3	V
Target I/O Voltage (V_{IO})	configurable mode	1.65		3.6	V
	USB 5V bypass mode		5.0		
Target I/O Voltage Error	configurable mode	-3		+3	%
Low-level Input Voltage (except SDA and SCL)				V_{IO} x 0.3	V
High-level Input Voltage (except SDA and SCL)		V_{IO} x 0.7			V
Low-level Input Voltage (SDA and SCL only)				0.8	V
High-level Input Voltage (SDA and SCL only)		2.0			V
Low-level Output Voltage	I_{OL}=4mA, V_{IO}=1.65V			0.5	V
	I_{OL}=8mA, V_{IO}=2.3V			0.4	
	I_{OL}=24mA, V_{IO}=3V			0.8	
	I_{OL}=32mA, V_{IO}=4.5V			0.9	
High-level Output Voltage	I_{OH}=-4mA, V_{IO}=1.65V	1.2			V
	I_{OH}=-8mA, V_{IO}=2.3V	1.8			
	I_{OH}=-24mA, V_{IO}=3V	2.8			
	I_{OH}=-32mA, V_{IO}=4.5V	4.2			
Input Leakage Current	0V ≤ V_{IN} ≤ 5V			±2	µA
SCL and SDA Pull-ups	when enabled		2.2		kΩ
I2C/SMBus Bit Rate		31.75		1500	kbits/sec
SPI Master Bit Rate		93.75		24000	kbits/sec
SPI Byte Throughput	Transactions < 4kbytes		170		kbytes/sec
SPI Slave Bit Rate			4000[†]		kbits/sec
SPI Slave SS Setup		3[Δ]			µsec
SCL Idle Bus Free Period	when enabled		3.3		SCL periods
SCL Low Timeout Period	when enabled (infinite timeout when disabled)			32.7	msec

[†] This value depends strongly on the electrical characteristics of a particular system design, such as bus capacitance, etc. The maximum bit-rate the SPI Slave can support in the user's system may be higher or lower than this value.

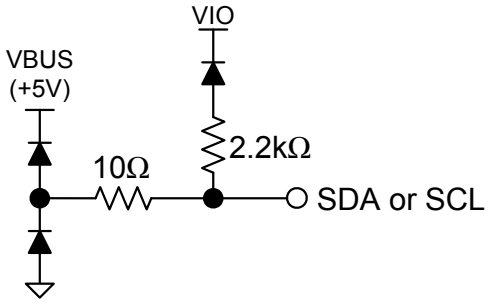
[Δ] This value assumes no additional USB traffic is sent to the adapter while the SPI slave is armed. Additional USB traffic can extend the required setup time by several microseconds.

4. EQUIVALENT PIN CIRCUITS

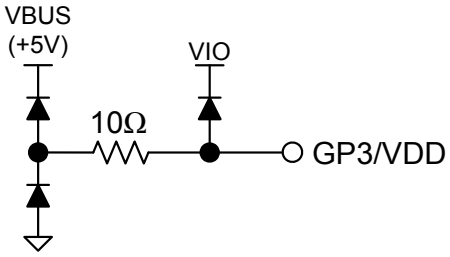
All non-USB pins of the USB-910H Adapter except GP3/VDD, SCL and SDA have the following equivalent input circuit:



The SDA and SCL pins have the following equivalent input circuit (assuming the built-in 2.2kΩ pull-up resistors are disabled):



VIO is the programmed Target I/O voltage of the Adapter. The GP3/VDD pin has the following equivalent input circuit, assuming the pin is operating as GP3:



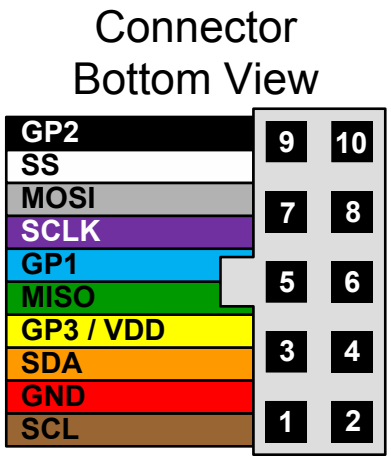
5. ADAPTER PINS

The USB-910H Adapter has nine pins plus GND to interface to a target embedded system. These pins provide functions ranging from I2C/SMBus and SPI signaling to general-purpose I/O and power. The following table describes the available pins, their functions, and their position and color-coding on the USB-910H Adapter connector.

Table 1. Adapter Pin-out and Color-coding.

Pin Name	Connector Pin Number	Connector Wire Color	Function
SCL	1	**BROWN**	Serves as either the clock for I2C/SMBus mode or as a general-purpose I/O.
GND	2	**RED**	Ground.
SDA	3	**ORANGE**	Serves as either the data for I2C/SMBus mode or as a general-purpose I/O.
GP3/VDD	4	**YELLOW**	Serves as either VDD to the target or as a general-purpose I/O.
MISO	5	**GREEN**	Serves as either master-in/slave-out data for SPI mode or as a general-purpose I/O.
GP1	6	**BLUE**	A general-purpose I/O.
SCLK	7	**VIOLET**	Serves as either the clock in SPI mode or as a general-purpose I/O.
MOSI	8	**GREY**	Serves as either master-out/slave-in data for SPI mode or as a general-purpose I/O.
SS	9	**WHITE**	A general-purpose I/O. Named SS only as a convenience.
GP2	10	**BLACK**	A general-purpose I/O.

Below is a color-coded diagram of a bottom-view of the standard connector for the USB-910H Adapter:



The table below shows the specific capabilities of each Adapter pin (beyond those associated with the I2C/SMBus and SPI interfaces).

Table 2. Adapter Pin Capabilities.

Pin	General-Purpose Input	General-Purpose Output	Master Mode Slave-Select	Slave Mode Slave-Select
SCLK	●	●		
MOSI	●	●		
MISO	●	●		
SDA	●	●	●	●
SCL	●	●	●	●
SS	●	●	●	●
GP1	●	●	●	●
GP2	●	●	●	●
GP3	●	●	●	

6. FUNCTIONAL DESCRIPTION

The USB-910H Embedded Systems Interface is a complete solution for providing connectivity between a host PC and a target system. The USB-910H provides this connectivity by converting USB transactions from the PC into I2C, SMBus, SPI, or "bit-banged" general-purpose I/O operations.

The USB-910H Adapter provides the following high-level capabilities:

- I2C/SMBus Master mode.
- I2C/SMBus Slave mode.
- SPI Master mode.
- SPI Slave mode.
- Up to 9 general-purpose I/O.
- I2C/SMBus Pull-up Resistors.
- Target VDD supply from 1.65V to 3.6V, or 5V @ 400mA.

At any given time, the USB-910H Adapter can act as any one of the four serial devices list above (an I2C/SMBus or SPI + Master or Slave), can be used strictly for general-purpose I/O operations, or can be both a serial device and perform "bit-banged" operations using the remaining I/O pins. The I2C Pull-up Resistors can be enabled in any combination with the other features, even if the Adapter is not acting as an I2C device.

All Adapter pins operate using a programmable I/O logic range[1]. This allows the Adapter to communicate with target systems running at a wide range of supply voltages. Regardless of the I/O voltage, all Adapter pins except GP3 can tolerate voltages up to VBUS+0.3V (GP3 is limited to V_{IO}+0.3V).

6.1. I/O Voltage and Powering the Target System

The USB-910H Adapter has the ability to level-shift the interface pins from a programmable I/O voltage to its own internal logic levels. This level-shifting is done using a true high-impedance method – the target system is not required to drive DC current into or out of the adapter pins. The I/O voltage at which the

[1] The SDA and SCL pins switch to fixed logic levels when in I2C/SMBus mode to accommodate the SMBus standard.

Adapter communicates with the target system is programmable from the host PC with supported values ranging from 1.65V to 3.6V, or 5V (see Section 1 for details).

The programmed I/O voltage sets the value the Adapter uses when driving an interface pin to a logic HIGH. The output drivers are true bi-directional, level-shifting, push-pull drivers. This prevents the target system from sinking high leakage current when driving a low voltage into an Adapter pin. The built-in I2C Pull-up Resistors are also switched to the I/O voltage when enabled.

The USB-910H Adapter can optionally connect the programmed I/O voltage directly to the GP3/VDD interface pin in order to supply power to the target system directly from the host PC. This VDD pin can provide up to 400mA and is both short-circuit and thermal-overload protected.

6.2. General-Purpose I/O

Any pin not claimed by an enabled feature of the USB-910 Adapter can be used as a general-purpose input/output signal. The following table shows which capabilities of the USB-910H claim which Adapter pins:

Table 3. Adapter Pins Claimed by Features.

Adapter Feature	Pins Claimed by the Adapter vs. Feature (not available as general-purpose I/O)								
	SCLK	MOSI	MISO	SDA	SCLK	SS	GP1	GP2	GP3
I2C/SMBus Master				X	X				
I2C/SMBus Slave				X	X				
SPI Master	X	X	X						
SPI Slave	X	X	X						
Target VDD									X

For example, when the Adapter is enabled as a SPI Master, the SCLK, MOSI, and MISO pins are not available as general-purpose I/O. Although one Adapter pin is named SS that is strictly for convenience. The SS pin in fact has no special significance. Any pin can be used as a Slave-Select during a SPI Master or SPI Slave operation. As such, it is up to the user to avoid using a chosen Slave-Select pin as a general-purpose I/O.

The USB-910H Adapter provides commands to set, clear, and tri-state any set of general-purpose I/O at any time, even during I2C or SPI operations. In addition, the Adapter allows all pins to be polled regardless of whether they are used by an enabled feature in the Adapter. Finally, both the I2C/SMBus and SPI script languages include commands to drive and poll I/O, allowing a mix of serial operations and I/O operations. For example, a SPI Master script can use I/O commands to handshake with a slave between or during serial transfers.

6.3. I2C / SMBus Modes

The USB-910H Adapter can operate as a fully-compliant I2C / SMBus master or slave device, supporting the following system requirements:

- Complete multi-master compliance.
- 7-bit and 10-bit addressing.
- Programmable SCL rates up to 1.5MHz.
- SMBus compliant setup/hold times.
- Shift data least-significant or most-significant bit first.
- SCL stretching compliance.
- Loss of arbitration detection and optional retry.
- SMBus PEC generation and checking.

- SCL low timeout and recovery.
- SCL high bus-free detection.
- Repeated STARTs.
- Group commands (master and slave).
- Bus fault detection.
- Built-in 2.2kΩ pull-up resistors to a programmable V_{IO} (with enables).
- Respond to up to 16 specific addresses or respond to all addresses.
- Generate arbitrary bus faults for use in system testing.

6.3.1. I2C/SMBus Master Operations

I2C/SMBus Master operations can be performed using three methods:

1. **Quick Write** – Perform a bus write to a specific slave device using 7-bit or 10-bit addressing.
2. **Quick Read** – Perform a bus read from a specific slave device using 7-bit or 10-bit addressing.
3. **Execute a Script** – Execute a script to perform any combination of configuration, reads, writes, delays, and general-purpose I/O operations.

Most simple data operations can be performed using a Quick Read or Quick Write. Both operations move a block of data to or from a slave device using the normal I2C/SMBus read or write protocol (i.e. a single START + Address + R/W bit + DATA + STOP).

However, the real power of the USB-910H Adapter is found in its ability to execute scripts supporting any combination of bus transactions, delays, and I/O operations. A script is a string of data and simple commands, each representing a low-level action to be performed, much like the list above (e.g. START + Address + R/W …). The I2C/SMBus master device can execute the following actions:

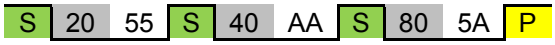
- Generate a START on the bus.
- Generate a STOP on the bus.
- Transmit a byte on the bus.
- Read a specified number of bytes from the bus.
- Delay a specified number of microseconds.
- Write an automatically-generated PEC byte to the bus.
- Read a PEC byte from the bus and compare to an automatically-generated value.
- Read a byte from the bus and compare to a specified value.
- Reconfigure the I2C Master settings (e.g. whether to retry if arbitration is lost, etc.).
- Drive a specified pin low, high, or to High-Z.
- Wait until a specified pin is high or low (with configurable timeout).

Using this simple script capability, complex protocols can be layered onto the I2C/SMBus bus, including handshaking using available general-purpose I/O.

6.3.2. I2C/SMBus Slave Operations

As an I2C/SMBus Slave device, the USB-910H Adapter can either respond to up to 16 specific 7-bit or 10-bit addresses, or can respond to all 7-bit or all 10-bit addresses. The slave device supports both read and write operations. For reads, the user sends the desired outgoing data to the Adapter prior to “arming” it as a slave. If a bus master attempts to read more data than provided by the user, the slave continues to transmit an internally-calculated PEC byte until a STOP is received. While addressed, the USB-910H stores all incoming data, including the address bytes, in its internal buffers. This allows the host PC to retrieve both the addresses and write data after the bus operation completes.

The USB-910H supports the PMBus Group Command Protocol. This protocol allows multiple devices to be addressed in the same operation, i.e. by using repeated STARTs. For example, consider the following bus operation:



This group operation writes 0x55 to device 0x10 (right-justified), 0xAA to device 0x20 and 0x5A to device 0x40. The USB-910H supports such protocols and will operate correctly as any of the addressed devices.

6.4. SPI Modes

The USB-910H Adapter can operate as a full-featured master or slave device compatible with SPI, MICROWIRE, and most other three-wire and four-wire synchronous serial interfaces. The following system requirements are supported:

- SCLK rates up to 24MHz.
- Active-high or active-low Slave-Selects.
- Shift data least-significant or most-significant bit first.
- Supports all standard “modes”.
- Clock data on leading or trailing edge.
- Idle with SCLK high or low.
- Transfer a configurable number of bytes per Slave-Select assertion.
- Up to 6 different Slave-Select pins available.
- Programmable Slave-Select setup/hold timing.
- Slave-Select pin can tri-state the MISO output to support multiple slaves.
- Operate with no Slave-Select (single-slave mode).

6.4.1. SPI Master Operations

SPI Master operations can be performed using two methods:

1. **Quick Transfer** – Perform a bus transfer using a specific Slave-Select pin.
2. **Execute a Script** – Execute a script to perform any combination of configurations, transfers, delays, and general-purpose I/O operations.

Most simple data transfers can be performed using a Quick Transfer. This operation transfers a block of data of a given size between the master and a slave using a single Slave-Select pin (or no Slave-Select pin). The number of bytes the master transfers each time it asserts the Slave-Select pin can be configured from 1 to 65536.

However, similar to I2C/SMBus mode, the SPI Master can execute scripts supporting any combination of configurations, bus transfers, delays, and I/O operations. The SPI Master device can execute the following actions:

- Transfer a byte on the bus.
- Transfer (i.e. repeat) a byte a given number of times.
- Delay a specified number of microseconds.
- Expect a specific byte from the slave.
- Reconfigure the SPI Master settings (e.g. change the Slave-Select, etc.).
- Drive a specific pin low, high, or to High-Z.
- Wait until a specific pin is high or low (with configurable timeout).

Using this simple script capability, complex protocols can be layered onto the SPI bus, including handshaking using available general-purpose I/O, communicating with multiple slaves, etc.

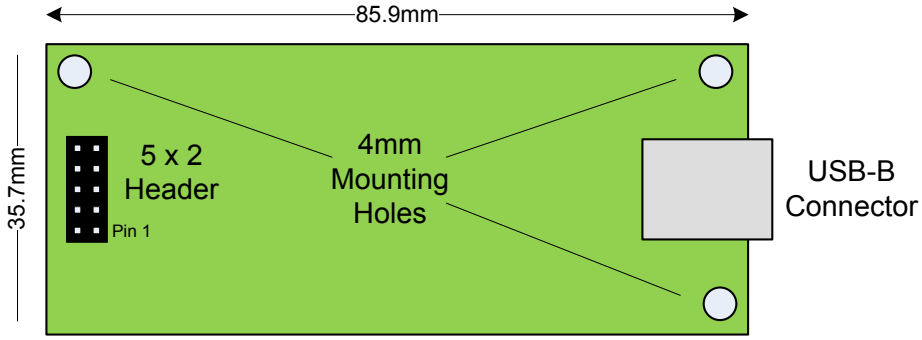
6.4.2. SPI Slave Operations

As a SPI Slave device, the USB-910H Adapter can be configured to respond to any one of 5 Slave-Select pins and can be configured to activate if that pin asserts either high or low. In addition, a slave device can operate with no Slave-Select – it will transfer data on all SCLK cycles.

Like a SPI Master, a slave device can transfer data either LSB or MSB first, and can support all standard SPI clocking modes. Slave operations are initiated by sending the desired outgoing data to the Adapter, then sending a command which "arms" the slave, causing it to start watching for its Slave-Select pin to assert. The slave will remain armed until its Slave-Select asserts and de-asserts (if it has a Slave-Select pin) or until it has transferred all outgoing data (if it has no Slave-Select pin). If a slave has a Slave-Select pin and a master requests more data than available in its outgoing buffer, the slave will enter loopback mode in which it transmits its incoming data back to the master. Once the slave disarms, the incoming data can be retrieved from the device and the next operation can be initiated by the host PC.

7. IN SYSTEM MOUNTING

Although generally the USB-910 Adapter will be used in its factory enclosure and connected to a target system via a ribbon connector or break-out cable, the Adapter PCB is equipped to be mounted directly into a target system when appropriate. The diagram below shows a simplified top-view of the Adapter PCB layout. For more information, contact Keterex at support@keterex.com.



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