Product Features

- Low current consumption: 0.4 μA typ. (V_{DD}=3.0 V, T_A = 25°C)
- Wide operating voltage range: 1.3 to 5.5 V
- Minimum time keeping operation voltage: 1.1 V
- Built-in clock adjustment function
- Built-in free user register
- 2-wire (I2C-BUS) CPU interface
- Built-in alarm interrupter
- Built-in flag generator at power down or power on
- Auto calendar up to the year 2099, automatic leap year calculation function
- Built-in constant voltage circuit
- Built-in 32 kHz crystal oscillator circuit (Cd built in, Cg external)
- Lead free and Green Package: 8-pin SOIC, 8-pin TSSOP

Ordering Information

Part Number	Package
PT7C43390WE	Lead free and Green 8-Pin SOIC
PT7C43390LE	Lead free and Green 8-Pin TSSOP

Product Description

The PT7C43390 is low-current consumption 2-wire CMOS real-time clock IC that features a wide operating voltage range(1.3V to 5.5V) and can be driven on a variety of supply voltages, from a main supply to a backup supply. The time keeping current consumption of 0.4μA and minimum time keeping operation voltage of 1.1V enable greatly increased battery duration.

In a system that operates on a backup battery, the free register incorporated in the real-time clock can be used for the user backup memory function. The user register can hold data on a supply voltage as low as 1.1V(min.), so the data stored in the register before the main power supply was cut can be called any time after the voltage is restored.

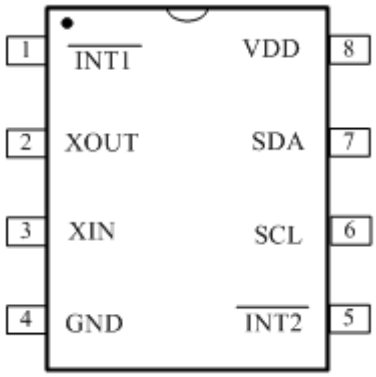
This product also includes a clock adjustment function that enables wide-ranging correction of deviation in the frequency of the crystal oscillator at a minimum resolution of 1 ppm. Also, by combining this function with a temperature sensor, the clock adjustment value can be set in accordance with changes in the temperature, which makes it possible to realize a clock function that retains a high degree of accuracy regardless of temperature variation.

Table 1 shows the basic functions of PT7C43390. More details are shown in section: Overview of Functions.

Table 1. Basic functions of PT7C43390

Item	Function			PT7C43390
1	Oscillator	Source	Crystal*	√
2	Time	Time display	12-hour	√
			24-hour	√
3	Interrupt	Alarm interrupt output		√2
4	Programmable square wave output (Hz)			1Hz,2Hz,4Hz,8Hz,16Hz,32kHz
5	Communication	2-wire I^2C bus		√
		Burst mode		√
6	Control	IC test mode		√
		Power-on detector		√
		Power supply voltage detector		√
7	Clock calibratoin			√
8	Free register acess			√

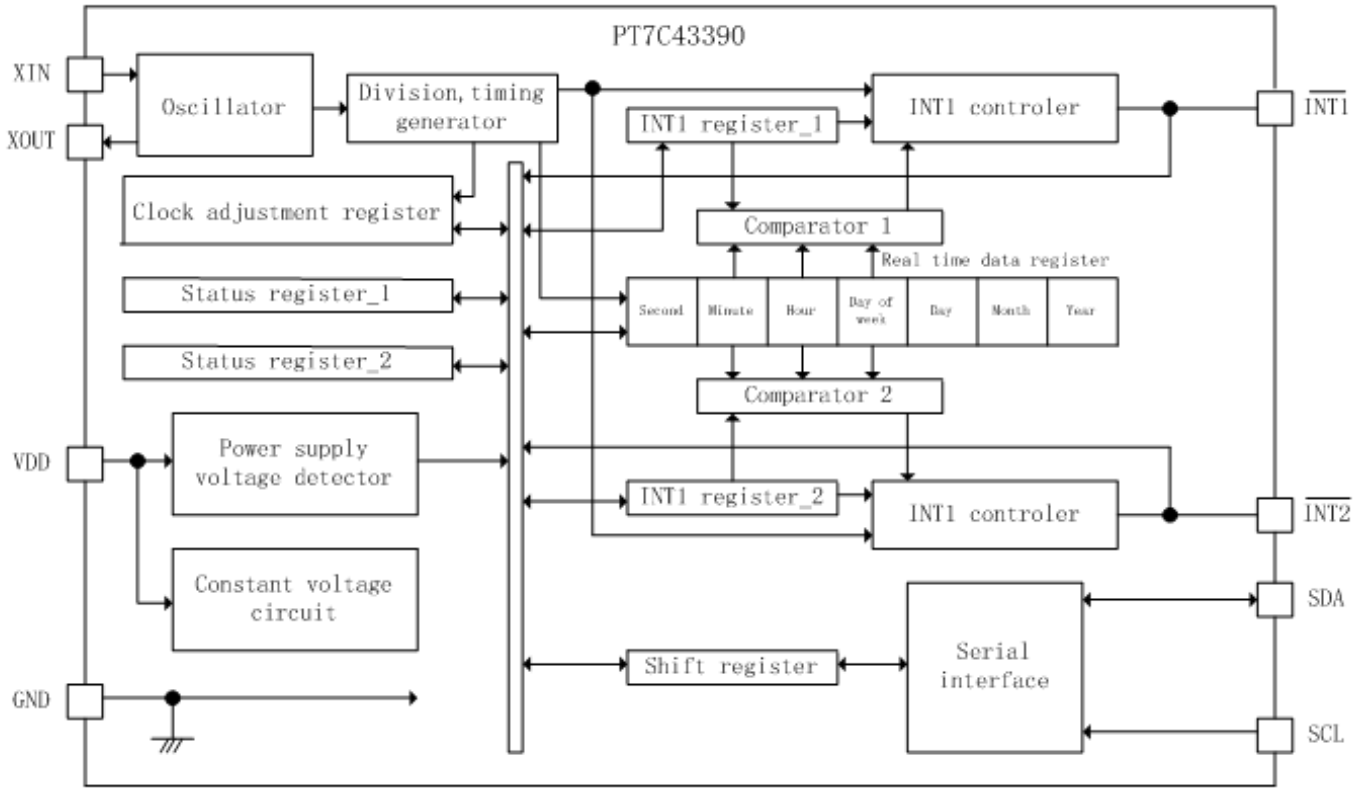
Pin Assignment



Pin Description

Pin no.	Pin	Description	Configuration
1	$\overline{\text{INT1}}$	**Interrupt 1 signal output pin** Depending on the mode set by INT1 register_1 and the status register, it outputs low or a clock when the time is reached. It is disabled by rewriting the status register.	Nch open-drain output (no protective diode on the side of VDD)
2	XOUT	**Crystal oscillator connect pin** (32,768 Hz) (Cd built in, Cg external)	-
3	XIN		
4	GND	**Negative power supply pin** (GND)	-
5	$\overline{\text{INT2}}$	**Interrupt 2 signal output pin** Depending on the mode set by INT1 register_2 and the status register, it outputs low or clock when time is reached. It is disabled by rewriting the status register.	Nch open-drain output (no protective diode on the side of VDD)
6	SCL	**Serial clock input pin** Since signal processing is done on the SCL signal rising/ falling edge, give great care to the rising/falling time and comply strictly with the specifications.	CMOS input (no protective diode on the side of VDD)
7	SDA	**Serial data I/O pin** Normally, it is pulled up to the VDD voltage by a resistor and connected with another open-drain output or open-collector output device via a wired-OR connection.	Nch open-drain output (no protective diode on the side of VDD) CMOS input
8	VDD	**Positive power supply pin**	-

Function Block



Function Description

Overview of Functions

Clock function

CPU can read or write data including the year (last two digits), month, date, day, hour, minute, and second. Any (two-digit) year that is a multiple of 4 is treated as a leap year and calculated automatically as such until the year 2099.

Alarm function

This device has two alarm system (Alarm 1 and Alarm 2) that outputs interrupt signals from $\overline{INT1}$ or $\overline{INT2}$ to CPU when the date, day of the week, hour, minute or second correspond to the setting. Each of them may output interrupt signal separately at a specified time. The alarm is be selectable between on and off for matching alarm or repeating alarm.

Programmable square wave output

Square wave output at pin 1 or pin 5. Six frequencies are selectable: 1, 2, 4, 8, 16, 32.768kHz.

Interface with CPU

For PT7C43390: 2-wire I^2C interface.

Calibration function

With the calibration bits properly set, the accuracy can be improved to better than ±2 ppm at 25°C.

■ Registers

Allocation of registers

Command				Data							
C2	C1	C0	Description	B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	Status register_1 access	POC*4	BLD*4	INT2*3	INT1*3	SC1*2	SC0*2	12/24	RESET*1
0	0	1	Status register_2 access	TEST*5	INT2AE	INT2ME	INT2FE	32kE	INT1AE	INT1ME	INT1FE
0	1	0	Real-time data 1 access (year data to second data)	Y80 —*6 —*6 —*6 —*6 —*6 —*6	Y40 —*6 —*6 —*6 AM/PM m40 s20	Y20 —*6 D20 —*6 H20 m20 s20	Y10 M10 D10 —*6 H10 m10 s10	Y8 M8 D8 —*6 H8 m8 s8	Y4 M4 D4 W4 H4 m4 s4	Y2 M2 D2 W2 H2 m2 s2	Y1 M1 D1 W1 H1 m1 s1
0	1	1	Real-time data 2 access (hour data to second data)	—*6 —*6 —*6	AM/PM m40 s20	H20 m20 s20	H10 m10 s10	H8 m8 s8	H4 m4 s4	H2 m2 s2	H1 m1 s1
1	0	0	INT1 register_1 access (alarm time 1) (INT1AE=1,INT1ME=0 INT1FE=0)	A1WE A1HE A1mE	—*6 AM/PM m40	—*6 H20 m20	—*6 H10 m10	—*6 H8 m8	W4 H4 m4	W2 H2 m2	W1 H1 m1
			INT1 register_1 access (frequency duty setting) (INT1ME=0,INT1FE=1)	SC*7	SC*7	SC*7	16Hz	8Hz	4Hz	2Hz	1Hz
1	0	1	INT1 register_2 access (alarm time 2) (INT2AE=1,INT2ME=0 INT2FE=0)	A2WE A2HE A2mE	—*6 AM/PM m40	—*6 H20 m20	—*6 H10 m10	—*6 H8 m8	W4 H4 m4	W2 H2 m2	W1 H1 m1
			INT1 register_2 access (frequency duty setting) (INT2ME=0,INT2FE=1)	SC*7	SC*7	SC*7	16Hz	8Hz	4Hz	2Hz	1Hz
1	1	0	Clock adjustment register access	V7	V6	V5	V4	V3	V2	V1	V0
1	1	1	Free register access	F7	F6	F5	F4	F3	F2	F1	F0

Caution:

*1. Write-only flag. By writing "1" to this register, the IC is reset.

*2. Scratch bit. R/W-enabled register that can be freely used by users.

*3. Read-only flag. It is cleared when read. It is valid only when the alarm is set.

*4. Read-only flag. "POC" is set to "1" when power is applied. It is cleared when read. For the "BLD", refer to "Power Supply Voltage Detector".

*5. For IC testing. Normally set this register to "0".

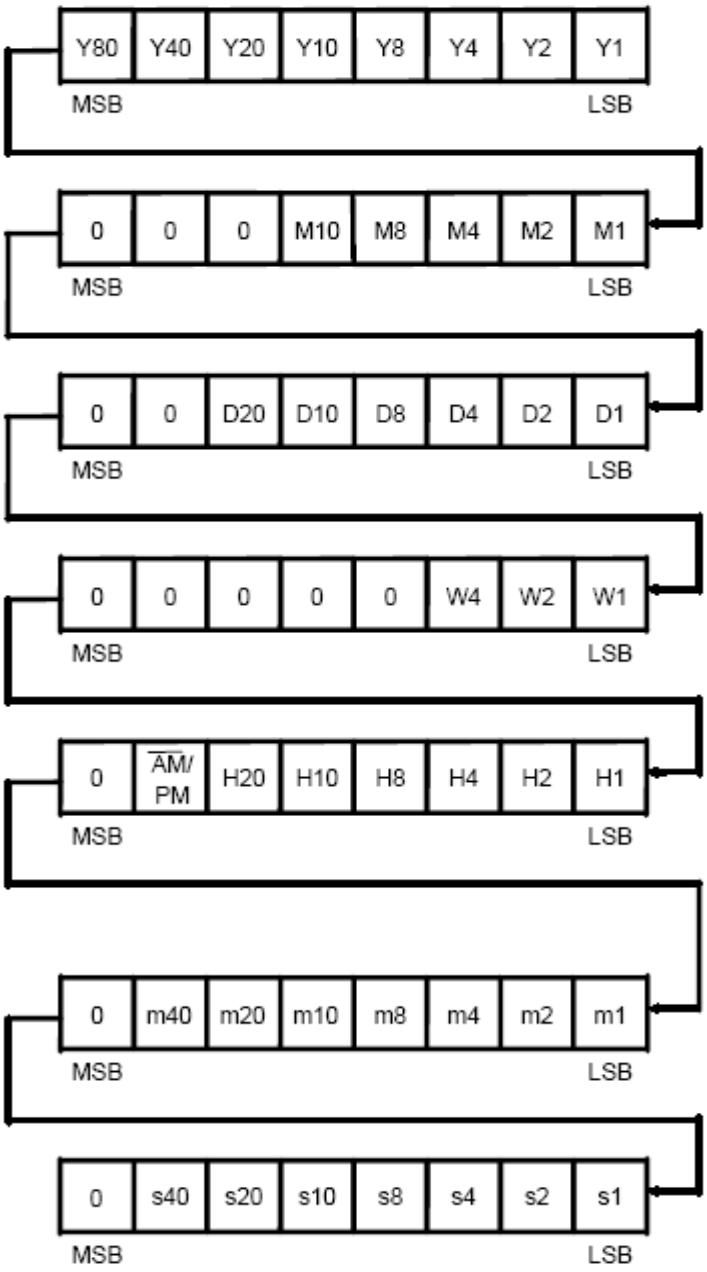
*6. No effect by writing. It is "0" when read.

*7. This is a R/W-enabled register that does not affect interrupts.

■ Register configuration

1. Real-time data register

The real-time data register is a 56-bit register that stores the BCD code of the year, month, day, day of week, hour, minute, and second data. Any read/write operation performed by the real-time data access command transmits or receives the data from the LSB which is the first digit of the year.



Year data (00 to 99)

Sets the lower two digits of the Western Calendar Year (00 to 99) and links together with the auto calendar feature until 2099.

Month data (01 to 12)

The count value is automatically changed by the auto calendar feature.

1 to 31: 31-day months (1, 3, 5, 7, 8, 10, 12)
1 to 30: 30-day months (4, 6, 9, 11)
1 to 29: Feb. (leap year)
1 to 28: Feb. (common year)

Day data (01 to 31)

Day of week data (00 to 06)

A septenary counter. Set it so that it corresponds to the day of the week.

Hour data (00 to 23 or 00 to 11)

$\overline{\text{AM}}$/PM

For a 12-hour expression, write 0 and 1 for AM and PM, respectively.

For a 24-hour expression, either 0 or 1 can be written. 0 is read when the hour data is from 00 to 11, and 1 is read when from 12 to 23.

Minute data (00 to 59)

Second data (00 to 59)

2. Status register_1

Status register_1 is an 8-bit register that is used to display and set various modes. The bit configuration is shown below.

	B7	B6	B5	B4	B3	B2	B1	B0	
MSB	POC	BLD	INT2	INT1	SC1	SC0	12/$\overline{24}$	RESET	LSB
	R	R	R	R	R/$\overline{W}$	R/$\overline{W}$	R/$\overline{W}$	W	

R: Read-enabled W: Write-enabled R/$\overline{W}$: Read/Write-enabled

B7: POC

This flag is set to "1" at power-on. Once this flag is set to "1", it is not set to "0" even when the power supply voltage reaches or exceeds the detection voltage (VDET). This flag is read-only and can be read by the status register_1 access command. Once it is read, it is automatically set to "0". When the flag is "1", it must be initialized. For the method of initialization, refer to "**Initialization at Power-on and Power-on Detector**".

B6: BLD

If the power supply voltage detector detects a voltage of detection voltage (VDET) or less this flag is set to "1", which enables the detection of a power supply voltage drop. Once this flag is set to "1", it is not set to "0" even when the power supply voltage reaches or exceeds the detection voltage (VDET). This flag is read-only and can be read by the status register_1 access command. Once it is read, it is automatically set to "0". When the flag is "1", it must be initialized. For the method of initialization, refer to "**Initialization at Power-on and Power-on Detector**". and for the operation of the power supply voltage detector, refer to "**Power Supply Voltage Detector**".

B5, B4: INT2, INT1

When the interrupt signal is output from the $\overline{INT1}$ or $\overline{INT2}$ pin using the alarm interrupt function, for an interrupt signal output from the $\overline{INT1}$ pin, the INT1 flag is set to "1", and for an interrupt signal output from the $\overline{INT2}$ pin, the INT2 flag is set to "1".

B3, B2: SC1, SC0

These flags configure a 2-bit SRAM type register that can be freely set by users. They are read and written within the operating voltage range (1.3 to 5.5 V).

B1: $\overline{12}$/24

This flag is used to set 12-hour or 24-hour expression.

0: 12-hour expression

1: 24-hour expression

B0: RESET

By setting this bit to "1", the internal IC is initialized. This is a write-only bit and is always "0" when it is read. Be sure to write "1" to the reset flag when applying the power supply voltage to the IC.

3. Status register_2

Status register_2 is an 8-bit register that is used to display and set various modes. The bit configuration is shown below.

	B7	B6	B5	B4	B3	B2	B1	B0	
MSB	TEST	INT2AE	INT2ME	INT2FE	32kE	INT1AE	INT1ME	INT1FE	LSB
	R/$\overline{W}$	R/$\overline{W}$	R/$\overline{W}$	R/$\overline{W}$	R/$\overline{W}$	R/$\overline{W}$	R/$\overline{W}$	R/$\overline{W}$	

R/$\overline{W}$: Read/Write-enabled

B7: TEST

The TEST flag is a bit for testing the IC. If the TEST flag is set to "1", the IC is switched to the TEST mode. If this flag is "1", it is necessary to initialize it to "0" by setting the reset flag of status register_1 to "1".

B5, B4: SC

These flags configure a 2-bit SRAM type register that can be freely set by users. They are read and written within the operating voltage range (1.3 to 5.5 V).

B6: INT2AE, B5: INT2ME, B4: INT2FE

These flags are used to select the output mode from the $\overline{INT2}$ pin. Mode selections are shown below. When using the alarm 2 function, after setting the alarm interrupt mode, access INT1 register_2.

Interrupt Modes ($\overline{INT2}$)

INT2AE	INT2ME	INT2FE	$\overline{INT2}$ Pin Output Mode
0	0	0	No interrupt
*1	0	1	Selected frequency steady interrupt
*1	1	0	Per-minute edge interrupt
*1	1	1	Per-minute steady interrupt 1 (50% duty)
1	0	0	Alarm interrupt

***1.** Don't care (Both of 0 and 1 are acceptable).

B3: 32kE, B2: INT1AE, B1: INT1ME, B0: INT1FE

These flags are used to select the output mode from the $\overline{INT1}$ pin. Mode selections are shown below. When using the alarm 1 function, after setting the alarm interrupt mode, access INT1 register_1.

Interrupt Modes ($\overline{INT1}$)

32kE	INT1AE	INT1ME	INT1FE	$\overline{INT1}$ Pin Output Mode
0	0	0	0	No interrupt
1	*1	*1	*1	32 kHz output
0	*1	0	1	Selected frequency steady interrupt
0	*1	1	0	Per-minute edge interrupt
0	0	1	1	Per-minute steady interrupt 1 (50% duty)
0	1	0	0	Alarm interrupt
0	1	1	1	Per-minute steady interrupt 2

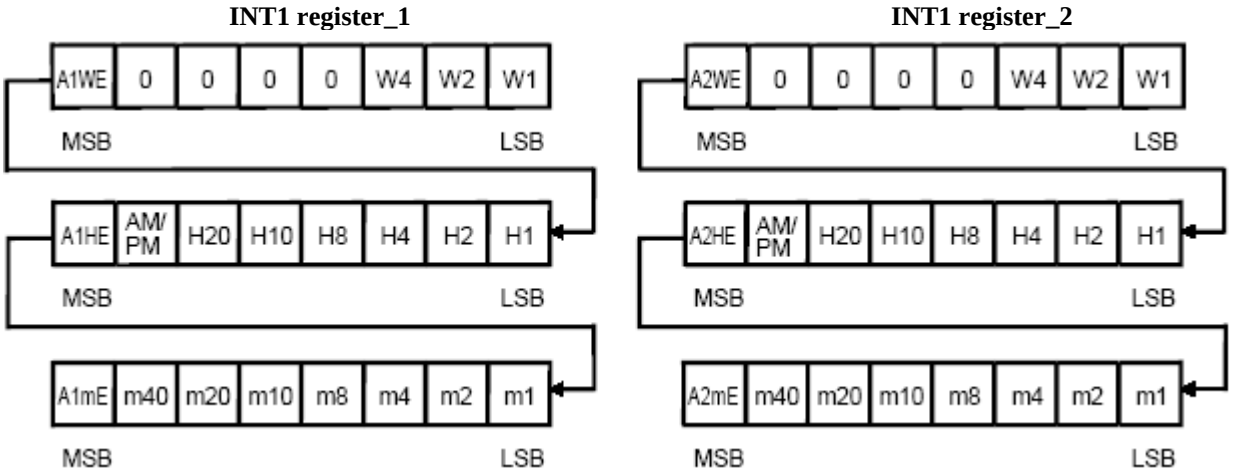
***1.** Don't care (Both of 0 and 1 are acceptable).

4. INT1 register_1 and INT1 register_2

INT1 register_1 and INT1 register_2 are interrupt setting registers that can be set independently. The interrupts are output from the $\overline{INT1}$ pin and $\overline{INT2}$ pin. The function is switched by using status register_2.

1) Alarm interrupt

Data set in INT1 register_1 and INT1 register_2 is considered as alarm time data. Having the same configuration as the hour and minute registers of the real-time data register, these registers represent hours and minutes with BCD codes. When setting these registers, do not set any nonexistent day. Data to be set must be in accordance with the 12-hour or 24-hour expression that is set in status register_1.



In INT1 register_1, A1WE, A1HE, and A1mE are respectively in the MSB of each byte. By setting each bit to "1", the setting of the day of week data, hour data, and minute data in the corresponding byte becomes valid. A2WE, A2HE, and A2mE of INT1 register_2 are the same.

The example of setting In case of the setting alarm time "PM 7:00" in INT1 register_1

a) 12-hour expression (status register_1 B1 = 0)

: set up 7:00 PM

Writing in INT1 register_1

Day of week data	0	*1	*1	*1	*1	*1	*1	*1
Hour data	1	1	0	0	0	1	1	1
Minute data	1	0	0	0	0	0	0	1
	MSB							LSB

***1.** Don't care (Both of 0 and 1 are acceptable).

b) 24-hour expression (status register_1 B1 = 1)

: set up 19:00 PM

Writing in INT1 register_1

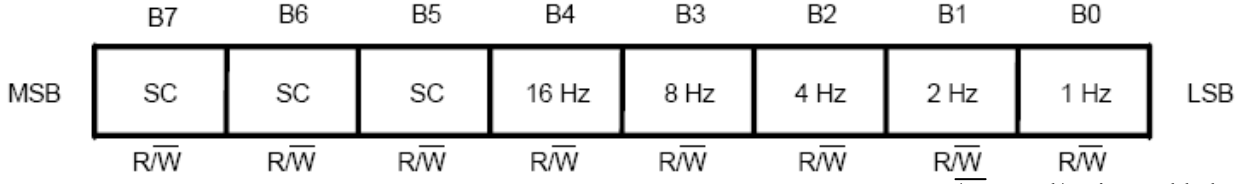
Day of week data	0	*1	*1	*1	*1	*1	*1	*1
Hour data	1	1*2	0	1	1	0	0	1
Minute data	1	0	0	0	0	0	0	0
	MSB							LSB

*1. Don't care (Both of 0 and 1 are acceptable).

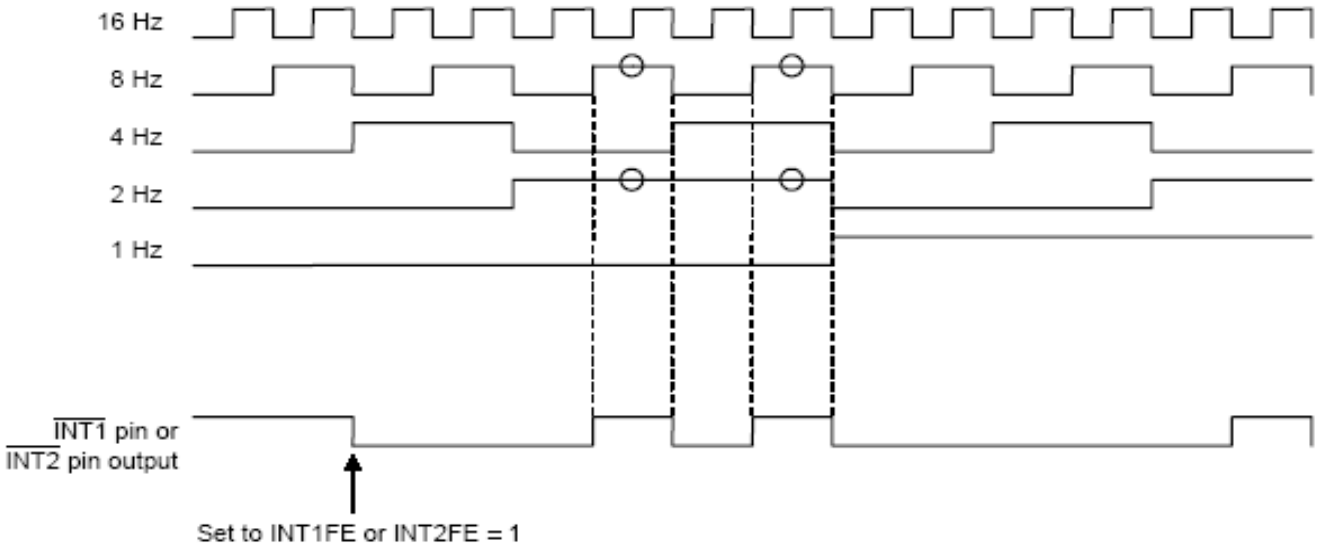
*2. Set up AM/PM flag along with the time setting.

2) Selected frequency steady interrupt

Data set in INT1 register_1 and INT1 register_2 is considered as frequency duty data. By setting each bit from B4 to B0 of the register to "1", the frequency corresponding to each bit is selected in an ANDed form. The SC bits configure a 3-bit SRAM type register that can be set freely by users. These bits can be read and written within the operating voltage range (1.3 to 5.5 V). There is no impact on the duty function.



R/$\overline{W}$: Read/Write-enabled



5. Clock adjustment register

The clock adjustment register is a 1-byte register that is used to logically correct real-time data. When not using the clock adjustment register, set this register to 00h using the clock adjustment register write command.
For the "register value", refer to "**Clock Adjustment Function**".

	B7	B6	B5	B4	B3	B2	B1	B0	
MSB	V7	V6	V5	V4	V3	V2	V1	V0	LSB
	R/$\overline{W}$	R/$\overline{W}$	R/$\overline{W}$	R/$\overline{W}$	R/$\overline{W}$	R/$\overline{W}$	R/$\overline{W}$	R/$\overline{W}$	

R/$\overline{W}$: Read/Write-enabled

6. Free register

The free register is a 1-byte SRAM type register that can be set freely by users. It can be read and written within the operating voltage range (1.3 to 5.5 V).

	B7	B6	B5	B4	B3	B2	B1	B0	
MSB	F7	F6	F5	F4	F3	F2	F1	F0	LSB
	R/$\overline{W}$	R/$\overline{W}$	R/$\overline{W}$	R/$\overline{W}$	R/$\overline{W}$	R/$\overline{W}$	R/$\overline{W}$	R/$\overline{W}$	

R/$\overline{W}$: Read/Write-enabled

■ Initialization at Power-on and Power-on Detector

When power is applied to this IC, status register_1 is set to "80h" (bit 7 (POC flag) of status register_1 is set to "1") by the power-on detector and a 1 Hz clock is output from the INT pin. This function is provided to adjust the oscillation frequency. In normal use, the IC must be initialized at power-on. Initialization is performed by writing "1" to bit 0 (RESET flag) of status register_1. Also, the IC must be initialized when the POC flag is set to "1". After initialization, the POC flag is set to "0". For normal operation of the power-on detector, first hold the IC power supply voltage at 0 V and then increase it.

■ Register State After Initialization

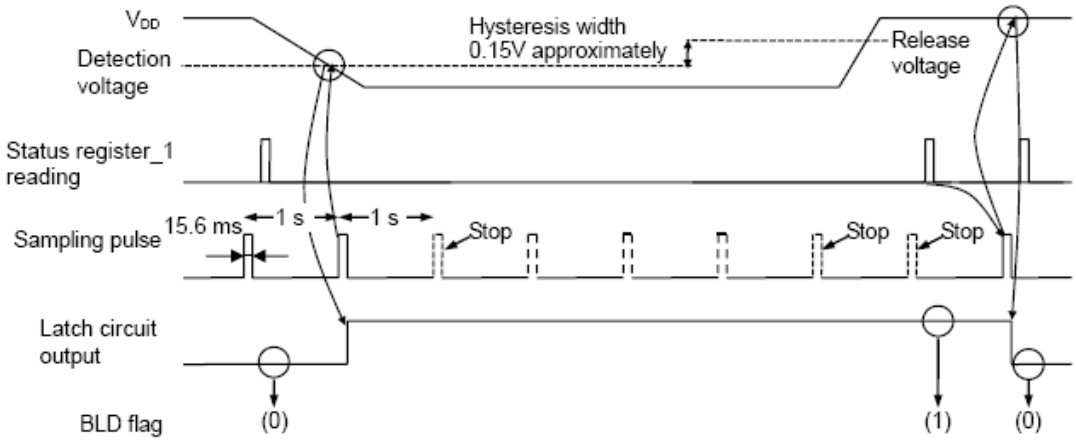
The state of each register after initialization is as follows.

Real-time data register: 00 (year), 01 (month), 01 (day), 0 (day of week), 00 (hour), 00 (minute), 00 (second)
Status register_1: "0 h * * * 0 b"(B3, B2, and B1 are user setting data.)
Status register_2: "00h"
INT1 register_1: "00h"
INT1 register_2: "00h"
Clock adjustment register: "00h"
Free register: "00h"

■ Power Supply Voltage Detector

PT7C43390 has an internal power supply voltage detector, which monitors drops in the power supply voltage by reading the BLD flag. This circuit samples the voltage for only 15.6 ms per second. If the power supply voltage drops below the detection voltage (V_{DET}), the BLD latch circuit latches the "H" level, bit 6 (BLD flag) of internal status register_1 is set to "1", and sampling stops. Detection voltage and release voltage have approximate 0.15V(Typ.) of hysteresis width respectively (Refer to "**Characteristics**"). Once "1" is detected in the BLD flag, no detection operation is performed unless initialization is performed or the BLD flag is read by the status register_1 access command, and "1" is held in the BLD flag. Sampling resumes only when the subsequent communication action is initialization or BLD flag read.
In addition, if this BLD flag is "1" after the power supply voltage is recovered, it must be initialized.

Caution In case the power supply voltage falls and returns after the latch circuit latches "H", the BLD flag can be read as "1" by a status register_1 accsess command first. After that the sampling is resumed and the read-out of the next BLD flag is performed, the BLD flag is reset and read as "0". Refer to the timing chart below.



■ Processing of Nonexistent Data and End-of-Month

When real-time data is written, the data is checked for validity, invalid data is processed, and the end-of month is corrected.

[Processing of nonexistent data]

Register	Normal Data	Error Data	Result
Year data	00 to 99	XA to XF, AX to FX	00
Month data	01 to 12	00, 13 to 19, XA to XF	01
Day data	01 to 31	00, 32 to 39, XA to XF	01
Day of week data	0 to 6	7	0
Hour data ***1** (24-hour)	0 to 23	24 to 29, 3X, XA to XF	00
(12-hour)	0 to 11	12 to 19, 2X, 3X, XA to XF	00
Minute data	00 to 59	60 to 79, XA to XF	00
Second data ***2**	00 to 59	60 to 79, XA to XF	00

***1.** For 12-hour expression, write the $\overline{AM}$/PM flag.
The $\overline{AM}$/PM flag is ignored in 24-hour expression, but "0" for 0 to 11 hours and "1" for 12 to 23 hours are read in a read operation.
***2.** Processing of nonexistent data for second data is performed by a carry pulse one second after the end of writing. At this point, the carry pulse is sent to the minute counter.

[Processing of end-of-month]
A nonexistent day is set to the first day of the next month. If February 30th is written, March 1st is set. Leap year correction is also performed at this time.

■ Interrupts

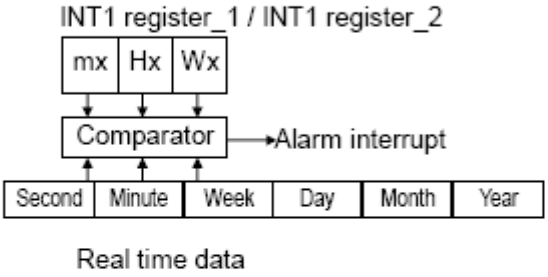
The $\overline{INT1}$ pin output mode is selected by the INT1AE, INT1ME, and INT1FE flags of status register_2. Similarly, the $\overline{INT2}$ pin output mode is selected by the INT2AE, INT2ME, and INT2FE flags of status register_2.

1. Alarm interrupt output

When the $\overline{INT1}$ or $\overline{INT2}$ pin output mode is set as the alarm setting using status register_2 and the day of week, hour, and minute data is set in INT1 register_1 (or INT1 register_2), low is output from the $\overline{INT1}$or $\overline{INT2}$ pin when the set hour is reached. Since the output is held, rewrite INT1AE of status register_2 to "0" (or INT2AE to "0") using serial communication to set the output to high (OFF state).

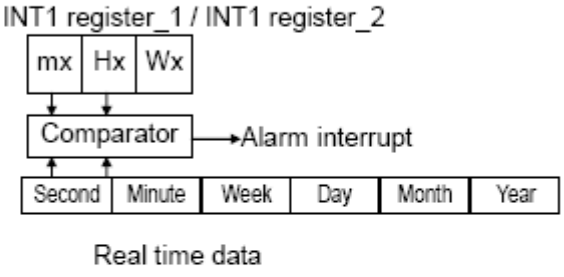
32kE = 0, INT1ME = INT1FE = 0
($\overline{INT1}$ pin output mode)
INT2ME = INT2FE = 0
($\overline{INT2}$ pin output mode)

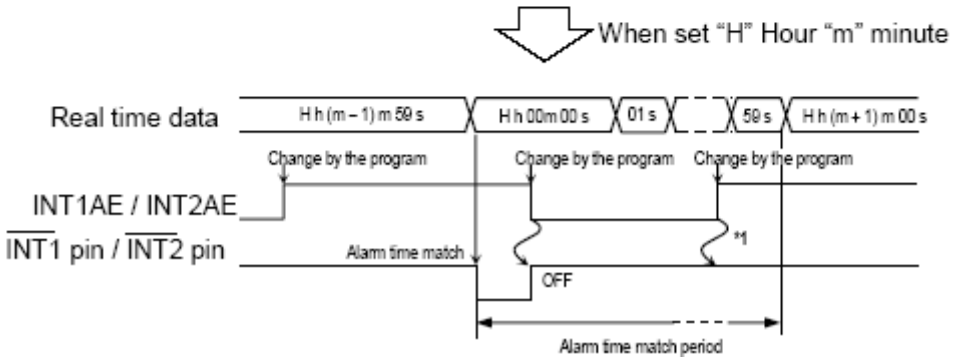
Alarm enable flag
In case of AxWE = AxHE = AxmE = "1"



32kE = 0, INT1ME = INT1FE = 0
($\overline{INT1}$ pin output mode)
INT2ME = INT2FE = 0
($\overline{INT2}$ pin output mode)

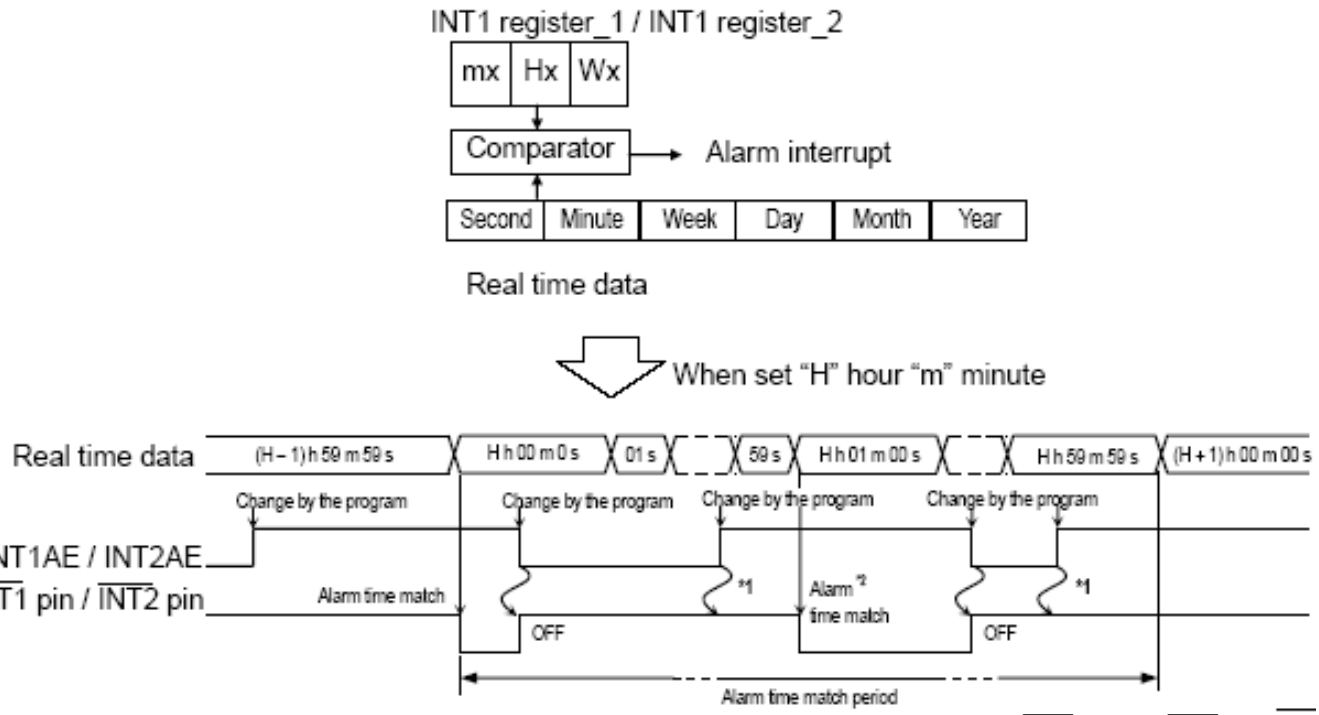
Alarm enable flag
In case of AxWE = "0", AxHE = AxmE = "1"





32kE = 0, INT1ME = INT1FE = 0
(INT1 pin output mode)
INT2ME = INT2FE = 0
(INT2 pin output mode)

Alarm enable flag
In case of AxWE = AxmE = "0", AxHE = "1"

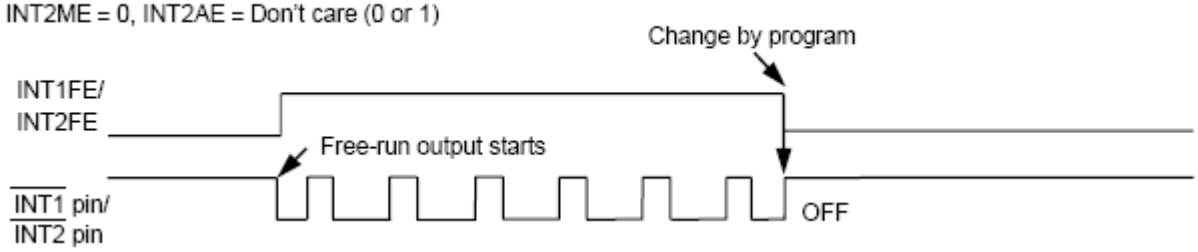


***1.** Once it clears, even if it enables again within a coincidene period, "L" will not be output from an INT1 pin (or INT2 pin).
***2.** When an alarm output is turned on by change by the program within a concidence period, "L" is again output from an INT pin at th time of change of the following part.

2. Selected frequency steady interrupt output

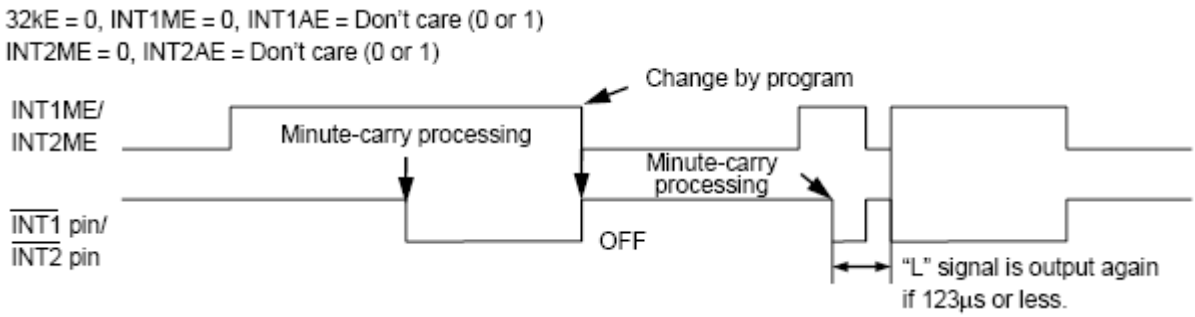
When the INT1 (or INT2) pin output mode is set as the selected frequency steady interrupt setting using status register_2 and the frequency/duty data is set in INT1 register_1 (or INT1 register_2), the set clock is output.

32kE = 0, INT1ME = 0, INT1AE = Don't care (0 or 1)
INT2ME = 0, INT2AE = Don't care (0 or 1)



3. Per-minute edge interrupt output

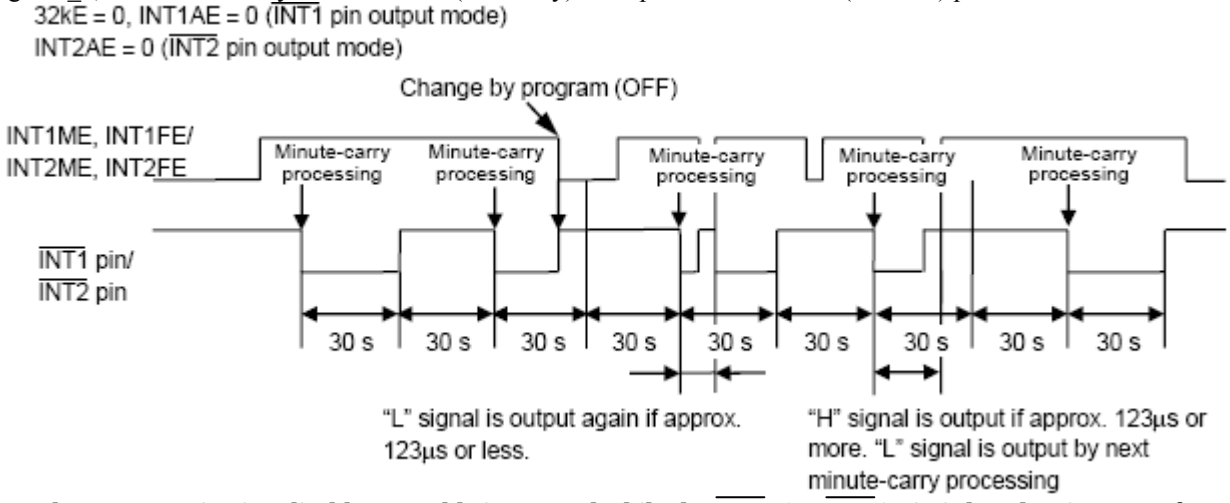
When the first minute carry is performed after the INT1 (or INT2) pin output mode is set as the per-minute edge interrupt using status register_2, low is output from the INT1 (or INT2) pin. Since the output is held, in the INT1 pin output mode, rewrite 32kE, INT1AE, INT1ME, and INT1FE of status register_2 to "0", and in the INT2 pin output mode, rewrite INT2AE, INT2ME, and INT2FE of status register_2 to "0" using serial communication to set the output to high (OFF state).



Caution Since the minute carry processing signal is retained for 123 µs, if communication disable or enable is executed during this period, low is output from the INT1 (or INT2) pin again.

4. Per-minute steady interrupt output 1

When the first minute carry is performed after the INT1 (or INT2) pin output mode is set as per-minute steady interrupt 1 using status register_2, a clock whose cycle is 1 minute (50% duty) is output from the INT1 (or INT2) pin.

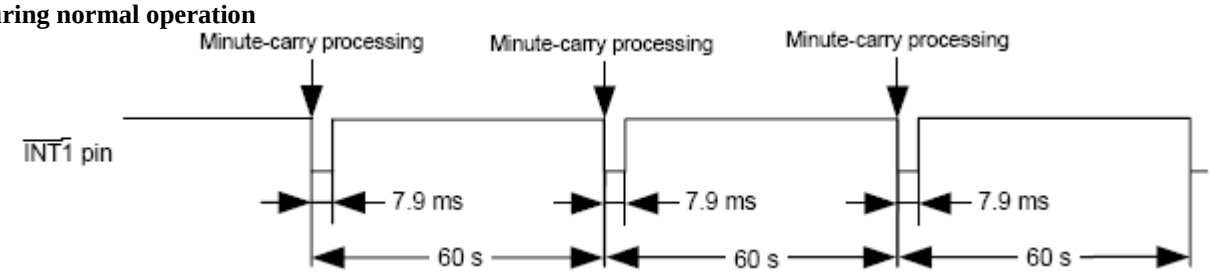


Caution When communication disable or enable is execued while the INT1 (or INT2) pin is low, low is output from the INT1 (or INT2) pin again.

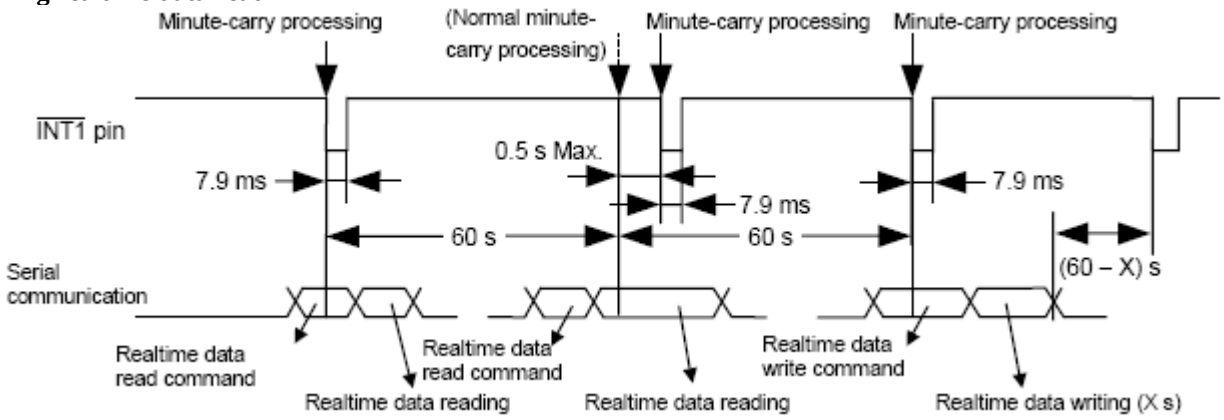
5. Per-minute steady interrupt output 2(INT1 output mode only)

When the first minute carry is performed after the INT1 pin output mode is set as per-minute steady interrupt 2 using status register_2, low is output from the INT1 pin for a period of 7.9 ms in synchronization with the minute carry processing inside the IC. However, when real-time data is read, the minute carry processing is delayed by a maximum of 0.5 s and accordingly low output from the INT1 pin is also delayed by a maximum of 0.5 s. When the second data is rewritten by a real-time data write command, counting starts from the rewritten second data and as a result, the output interval during that period may become either longer or shorter.

1) During normal operation



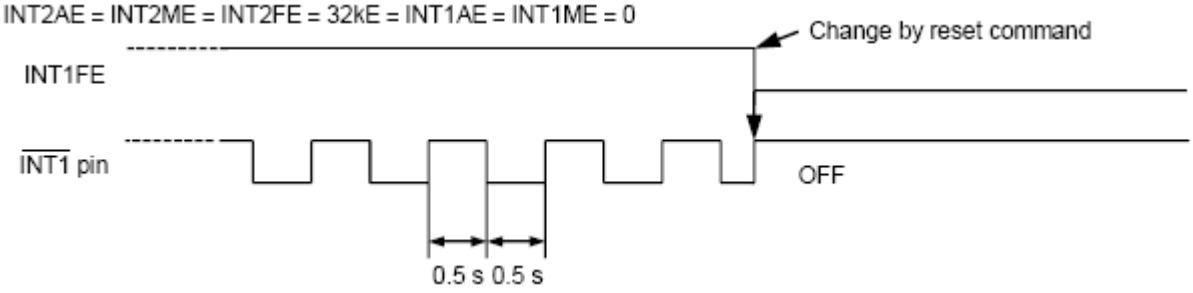
2) During realtime data read



Caution 1. When changing an output mode, give care to the state of INT1 register_1 (or INT1 register_2) and the output.
2. If per-minute edge interrupt output or per-minute steady interrupt output is chosen, INT1 register_1 (or INT1 register_2) has no meaning.

6. During power-on detector operation

When power is applied to this IC, power-on detection circuit operates, status register_1 is set to "80h" (bit 7 (POC flag) of status register_1 is set to 1) via the power-on detection circuit, and a 1Hz clock is output from the $\overline{INT1}$ pin.



■ Clock adjustment function

A clock adjustment function is provided to logically perform slow/fast adjustment of the 32kHz clock and correct a slow/fast clock with high accuracy. Use the clock adjustment register to set this function. When not using this function, be sure to set it to 00h.

The clock adjustment register value is calculated by the following expression.

1. If current oscillation frequency > target frequency (in case the clock is fast)

$$\text{Register value}^{*1} = 128 - \text{Integral value}\left[\frac{(\text{Current oscillation frequency actual measurement value}^{*2}) - (\text{Target oscillation frequency}^{*3})}{(\text{Current oscillation frequency actual measurement value}^{*2}) \times (\text{Minimum resolution}^{*4})}\right]$$

Caution The figure range which can be corrected is that the calculated value is from 0 to 64.

***1.** The register value is the value set to the clock adjustment register. Set the binarized value of this value to the clock adjustment register.

***2.** This is the measurement value of the signal that is output to the $\overline{INT1}$ (PT7C43390) or $\overline{INT2}$ pin when 1Hz clock output setting is made.

32kE = 0, INT1ME = 0, INT1FE = 1, INT1 register_1 is 01h (for the $\overline{INT1}$ pin)

INT2ME = 0, INT2FE = 1, INT1 register_2 is 01h (for the $\overline{INT2}$ pin)

***3.** This is the frequency to be adjusted by using the clock adjustment function.

***4.** For the minimum resolution, 3.052 ppm or 1.017 ppm can be set using B7 of the clock adjustment register. When B7 is 0, 3.052 ppm is set and logical slow/fast adjustment is performed every 20 seconds. When B7 is 1, 1.017 ppm is set and logical slow/fast adjustment is performed every 60 seconds.

	B7 =0	B7 =1
Slow/fast adjustment	Every 20 seconds	Every 60 seconds
Minimum resolution	3.052 ppm	1.017 ppm
Correction range	−195.3 ppm to +192.2 ppm	−65.1 ppm to +64.1 ppm

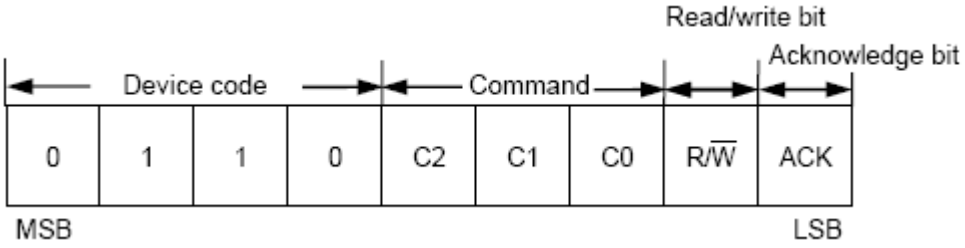
2. If current oscillation frequency < target frequency (in case the clock is slow)

$$\text{Register value} = \text{Integral value}\left[\frac{(\text{Target oscillation frequency}) - (\text{Current oscillation frequency actual measurement value})}{(\text{Current oscillation frequency}) \times (\text{Minimum resolution})}\right] + 1$$

Caution The figure range which can be corrected is that the calculated value is from 0 to 62.

■ I2C Bus's Basic Transfer Format

The master device on the system generates a start condition to the slave device to communicate. Then it transmits a 4-bit device address, 3-bit command, and 1-bit read/write command on the SDA bus. The higher 4 bits that indicate the device address are called the device code and are fixed to "0110".



1. Data reading

After detecting the start condition from outside, a device code and command are received. If the read/write bit is "1" at this point, the data read mode is entered. The data output sequence is output from the LSB.

2. Data writing

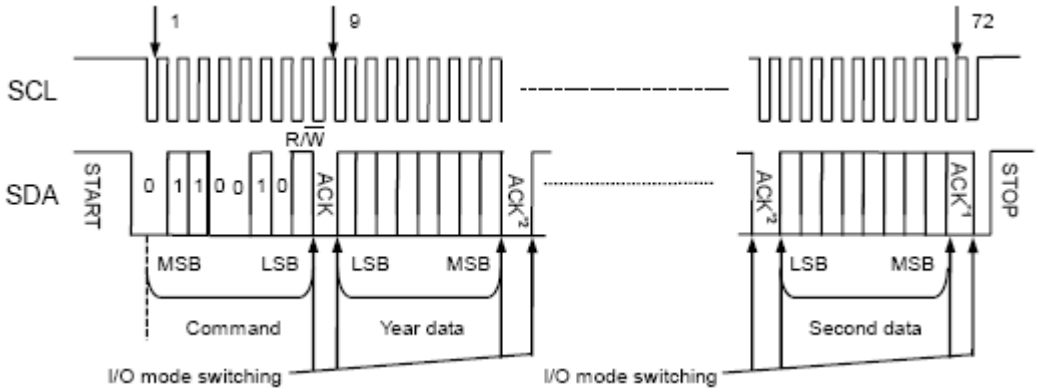
After detecting the start condition from outside, a device code and command are received. If the read/write bit is "0" at this point, the real-time data write mode or another register write mode is entered. Input the data input sequence for both the real-time data write mode and status register write mode from the LSB.

In real-time data writing, the calendar and time counter is reset by the rising of the ACK signal after the real-time write command and update operations are then prohibited. Subsequently, when minute data reception is completed, an end-of-month correction is performed while the second data is loaded.

Counting up is started from the rising of the ACK signal after the second data reception.

3. Basic Transfer Format

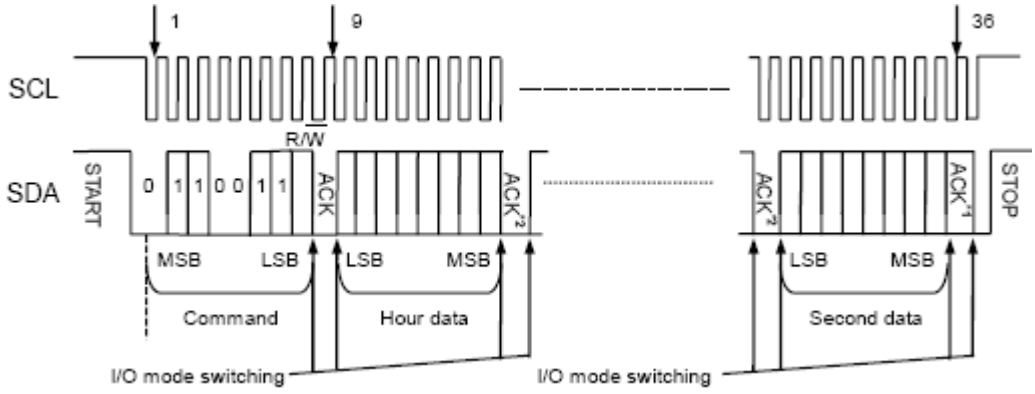
1) Real-time data access 1



***1.** During reading, set NO_ACK to 1.

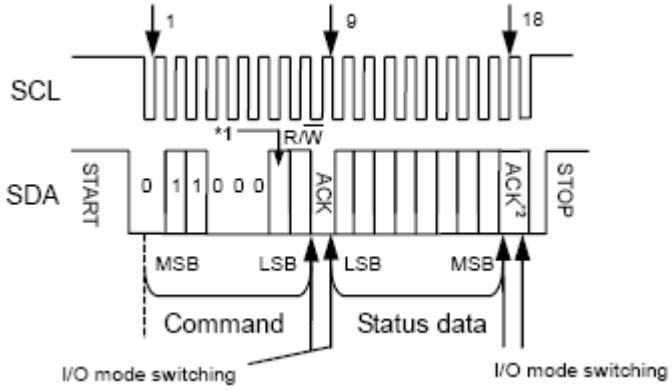
***2.** During reading, transmit ACK = 0 to PT7C43390 from the master device.

2) Real-time data access 2



***1.** During reading, set NO_ACK to 1.
***2.** During reading, transmit ACK = 0 to PT7C43390 from the master device.

3) Status register_1 access and status register_2 access



***1.** 0: Status register_1 selected, 1: Status register_2 selected
***2.** During reading, set NO_ACK to 1.

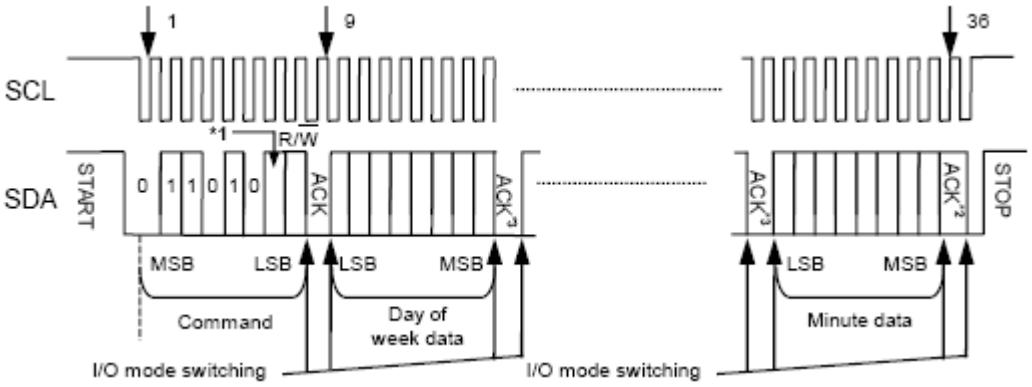
4) INT1 register_1 access and INT1 register_2 access

Since data written to and read from INT1 register_1 varies according to the setting of status register_2, be sure to set status register_2 before reading/writing INT1 register_1. When an alarm is set using status register_2, these registers function as 3-byte alarm time data registers, and other than that, they function as 1-byte registers. When the selected frequency steady interrupt setting is set, the data in these registers is frequency duty setting data.

Caution Alarm data and frequency duty data cannot be operated simultaneously.

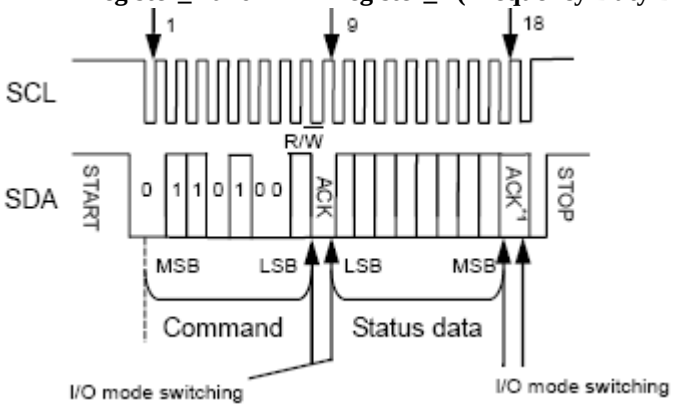
Since data written to and read from INT1 register_2 varies according to the setting of status register_2, be sure to set status register_2 before reading/writing INT1 register_1. When an alarm is set using status register_2, these registers function as 3-byte alarm time data registers, and other than that, they function as 1-byte registers. When the selected frequency steady interrupt setting is set, the data in these registers is frequency duty setting data.
For details of each data, refer to "**Status register_1**" and "**Status register_2**".

INT1 Register_1 Access and INT1 Register_2 Access



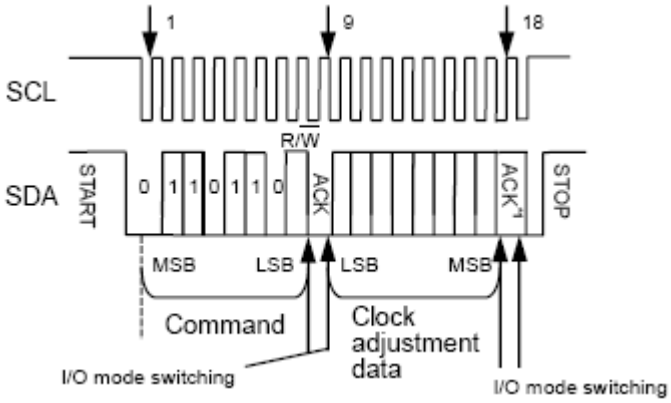
***1.** 0: INT1 register_1 selected, 1:INT1 register_2 selected
***2.** During reading, set NO_ACK to 1.
***3.** During reading, transmit ACK = 0 to PT7C43390 from the master device.

INT1 Register_1 and INT1 Register_2 (Frequency Duty Data)



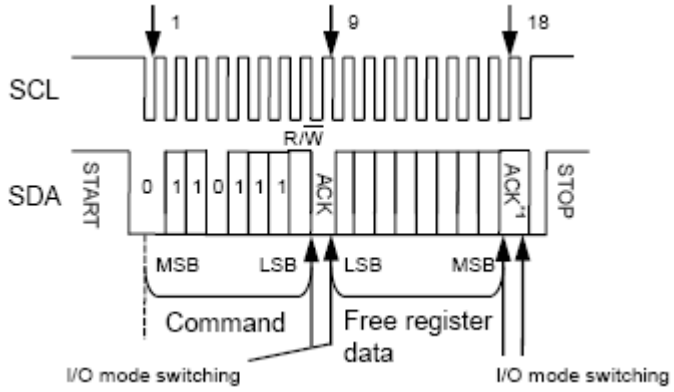
***1.** During reading, set NO_ACK to 1.

5) Clock adjustment register access



***1.** During reading, set NO_ACK to 1.

6) Free register access



***1.** During reading, set NO_ACK to 1.

Maximum Ratings

Storage Temperature	- 55°C to +125°C
Ambient Temperature with Power Applied	-40 °C to +85 °C
Supply Voltage to Ground Potential (Vcc to GND)	- 0.3 to +6.5V
DC Input (SCL, SDA)	- 0.3 to +6.5V
DC Output Voltage (SDA, $\overline{INT1}$, $\overline{INT2}$ pin)	- 0.3 to +6.5V
Power Dissipation	320mW (depend on package)

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Symbol	Description	Test Conditions	Min	Type	Max	Unit
V_{DD}	Power voltage	T_A=-40 to + 85ºC	1.3	3.0	5.5	V
V_{DH}	Time keeping voltage range	T_A=-40 to + 85ºC	V_{DDTm}	-	5.5	V
V_{DDT}	Register hold voltage	T_A=-40 to + 85ºC	V_{DDTm}	-	5.5	V
V_{DDTm}	Minimum time keeping voltage range	T_A=-40 to + 85ºC	0.9***1**	-	1.1	V
C_L	Crystal oscillator C_L value	-	-	-	7.0	pF
T_A	Operating temperature	V_{DD}=1.3 to 5.5V	-40	+25	+85	ºC

***1.** Reference value

DC Electrical Characteristics

T_A = -40 to +85°C, V_{DD} = 3.0 V, DS-VT-200 crystal oscillator (C_L = 6 pF, 32,768 Hz, Cg = 9.1 pF)

Parameter	Symbol	Applicable Pin	Conditions	Min.	Typ.	Max.	Unit
Current consumption 1	I_{DD1}	-	Out of communication	-	0.40	0.65	µA
Current consumption 2	I_{DD2}	-	During communication (SCK =100 kHz)	-	6.0	14.0	µA
Input current leakage 1	I_{IZH}	SCL, SDA	$V_{IN} = V_{DD}$	−0.5	-	0.5	µA
Input current leakage 2	I_{IZL}	SCL, SDA	$V_{IN} = V_{SS}$	−0.5	-	0.5	µA
Output current leakage 1	I_{OZH}	SDA,$\overline{INT1}$,$\overline{INT2}$	$V_{OUT} = V_{DD}$	−0.5	-	0.5	µA
Output current leakage 2	I_{OZL}	SDA,$\overline{INT1}$,$\overline{INT2}$	$V_{OUT} = V_{SS}$	−0.5	-	0.5	µA
Input voltage 1	V_{IH}	SCL, SDA	-	$0.8\times V_{DD}$	-	-	V
Input voltage 2	V_{IL}	SCL, SDA	-	-	-	$0.2\times V_{DD}$	V
Output current 1	I_{OL1}	$\overline{INT1}$	V_{OUT} =0.4 V	1.0	1.4	-	mA
		$\overline{INT2}$	V_{OUT} =0.4 V	3.0	5.0		
Output current 2	I_{OL2}	SDA	V_{OUT} =0.4 V	5	10	-	mA
Power supply voltage detection voltage *1	V_{DET}	-	Ta = −40 to +85°C	V_{DDTm} + 0.15 *2	-	V_{DDTm} + 0.4	V

***1.** Power supply voltage detection voltage: Constantly maintains the relation of $V_{DET} > V_{DDTm}$ (minimum time keeping voltage).
***2.** Reference value

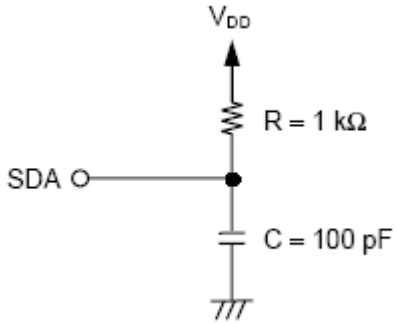
T_A = -40 to +85°C, V_{DD} = 5.0 V, DS-VT-200 crystal oscillator (C_L = 6 pF, 32,768 Hz, Cg = 9.1 pF)

Parameter	Symbol	Applicable Pin	Conditions	Min.	Typ.	Max.	Unit
Current consumption 1	I_{DD1}	-	Out of communication	-	0.45	0.7	µA
Current consumption 2	I_{DD2}	-	During communication (SCK =100 kHz)	-	14	30	µA
Input current leakage 1	I_{IZH}	SCL, SDA	$V_{IN} = V_{DD}$	−0.5	-	0.5	µA
Input current leakage 2	I_{IZL}	SCL, SDA	$V_{IN} = V_{SS}$	−0.5	-	0.5	µA
Output current leakage 1	I_{OZH}	SDA,$\overline{INT1}$,$\overline{INT2}$	$V_{OUT} = V_{DD}$	−0.5	-	0.5	µA
Output current leakage 2	I_{OZL}	SDA,$\overline{INT1}$,$\overline{INT2}$	$V_{OUT} = V_{SS}$	−0.5	-	0.5	µA
Input voltage 1	V_{IH}	SCL, SDA	-	$0.8\times V_{DD}$	-	-	V
Input voltage 2	V_{IL}	SCL, SDA	-	-	-	$0.2\times V_{DD}$	V
Output current 1	I_{OL1}	$\overline{INT1}$	V_{OUT} =0.4 V	1.0	1.4	-	mA
		$\overline{INT2}$	V_{OUT} =0.4 V	3.0	5.0		
Output current 2	I_{OL2}	SDA	V_{OUT} =0.4 V	6	13	-	mA
Power supply voltage detection voltage *1	V_{DET}	-	Ta = −40 to +85°C	V_{DDTm} + 0.15 *2	-	V_{DDTm} + 0.4	V

***1.** Power supply voltage detection voltage: Constantly maintains the relation of $V_{DET} > V_{DDTm}$ (minimum time keeping voltage).
***2.** Reference value

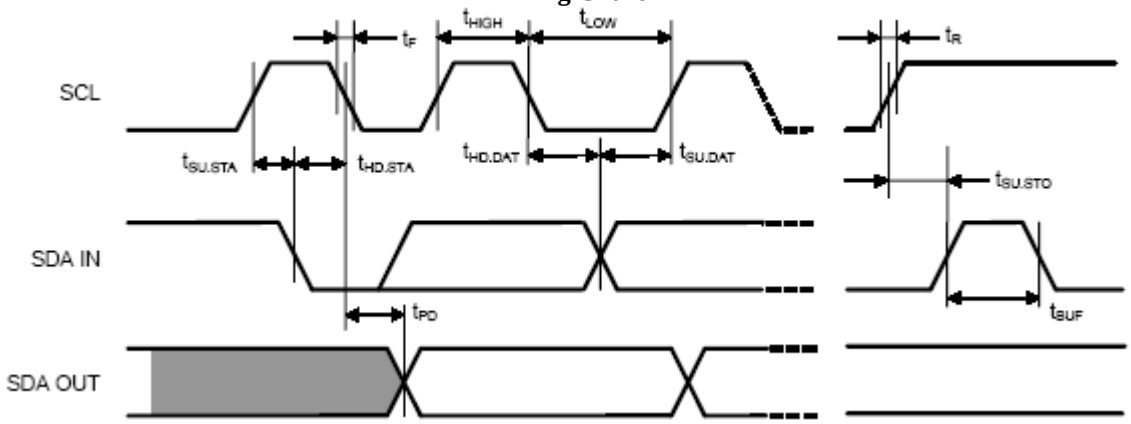
AC Electrical Characteristics

Input pulse voltage	0.1 ×V_{DD} to 0.9 ×V_{DD}
Input pulse rise/fall time	20 ns
Output determination voltage	0.5 ×V_{DD}
Output load	100 pF +pull-up resistor 1 kΩ



Output Load Citcuit

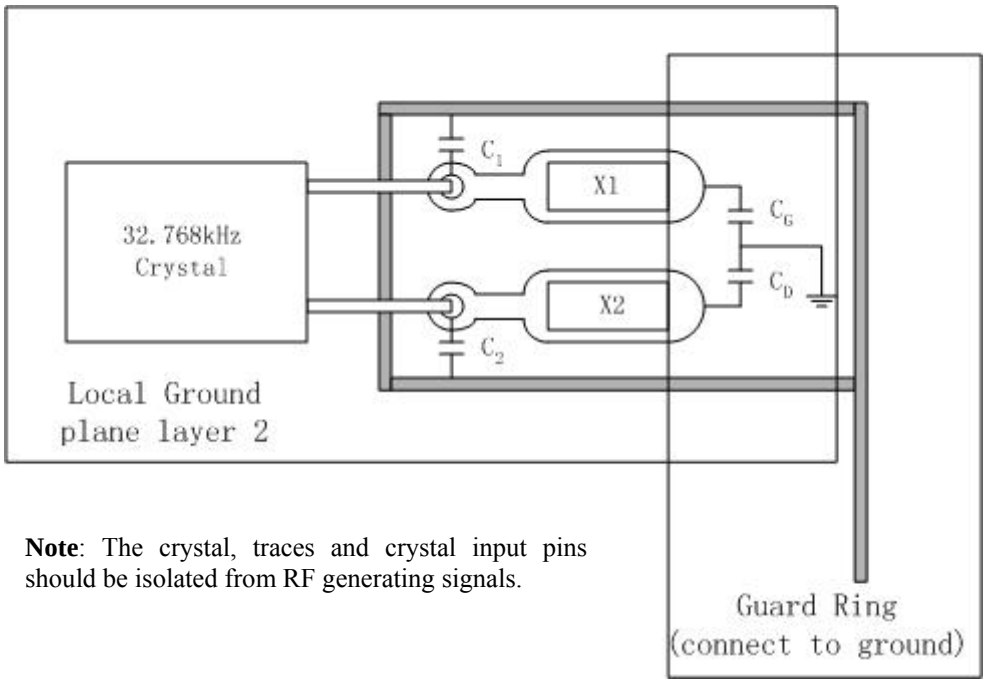
Timing Chart



Parameter	Symbol	V_{DD} = 1.3 to 5.5 V			V_{DD} = 3.0 to 5.5 V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	0	-	100	0	-	400	kHz
SCL clock “L” time	t_{LOW}	4.7	-	-	1	-	-	µs
SCL clock “H” time	t_{HIGH}	4	-	-	0.9	-	-	µs
SDA output delay time*1	t_{PD}	-	-	3.5	-	-	0.9	µs
Start condition setup time	$t_{SU.STA}$	4.7	-	-	0.6	-	-	µs
Start condition hold time	$t_{HD.STA}$	4	-	-	0.6	-	-	µs
Data input setup time	$t_{SU.DAT}$	250	-	-	100	-	-	ns
Data input hold time	$t_{HD.DAT}$	0	-	-	0	-	-	ns
Stop condition setup time	$t_{SU.STO}$	4.7	-	-	-	-	-	µs
SCL and SDA rise time	t_R	-	-	1	-	-	0.3	µs
SCL and SDA fall time	t_F	-	-	0.3	-	-	0.3	µs
Bus release time	t_{BUF}	4.7	-	-	1.3	-	-	µs
Noise suppression time	t_I	-	-	100	-	-	50	ns

***1.** Since the output format of the SDA pin is Nch open-drain output, the SDA output delay time is determined by the values of the load resistance (R_L) and load capacity (C_L) outside the IC. Therefore, use this value only as a reference value.

Recommended Layout for Crystal



Note: The crystal, traces and crystal input pins should be isolated from RF generating signals.

Built-in Capacitors Specifications and Recommended External Capacitors

Parameter		Symbol	Typ	Unit
Build-in capacitors	X1 to GND	C_G	5	pF
	X2 to GND	C_D	5	pF
Recommended External capacitors for crystal C_L=12.5pF	X1 to GND	C_1	18	pF
	X2 to GND	C_2	18	pF
Recommended External capacitors for crystal C_L=6pF	X1 to GND	C_1	7	pF
	X2 to GND	C_2	7	pF

Note: The frequency of crystal can be optimized by external capacitor C_1 and C_2, for frequency=32.768Hz, C_1 and C_2 should meet the equation as below:

$Cpar + [(C_1+C_G)*(C_2+C_D)]/ [(C_1+C_G)+(C_2+C_D)] = C_L$

Cpar is all parasitical capacitor between X1 and X2.

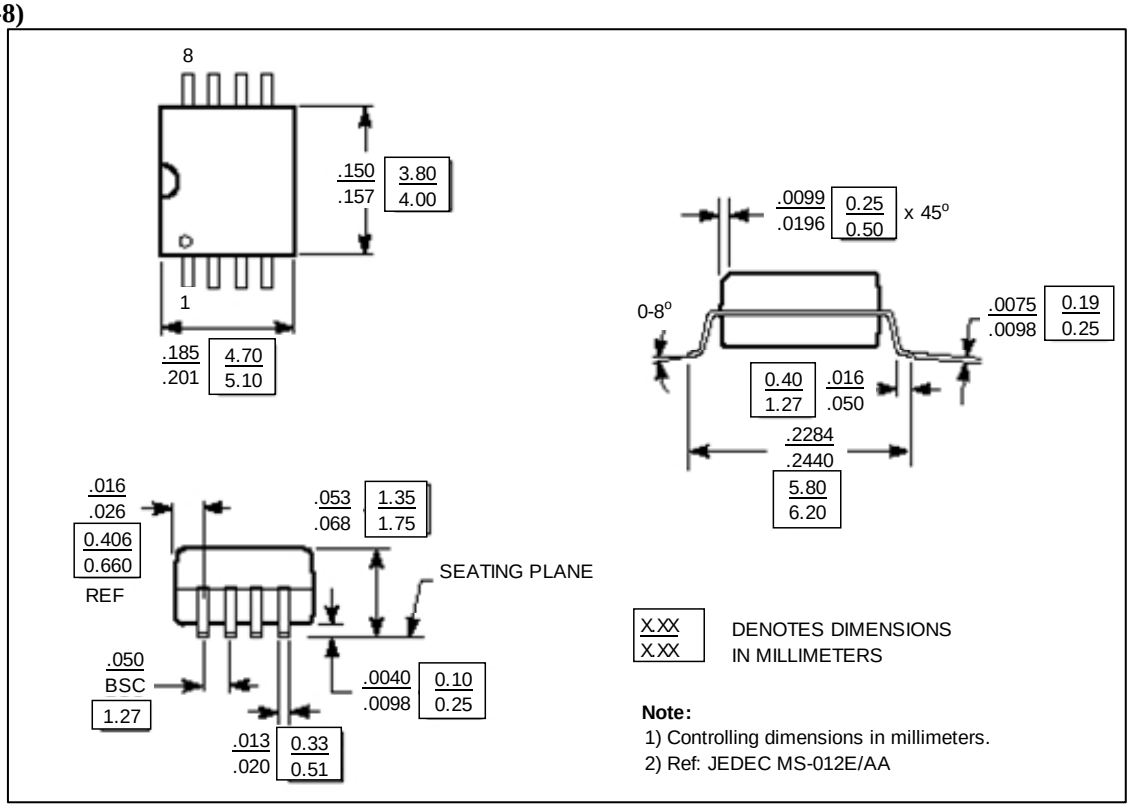
C_L is crystal's load capacitance.

Crystal Specifications

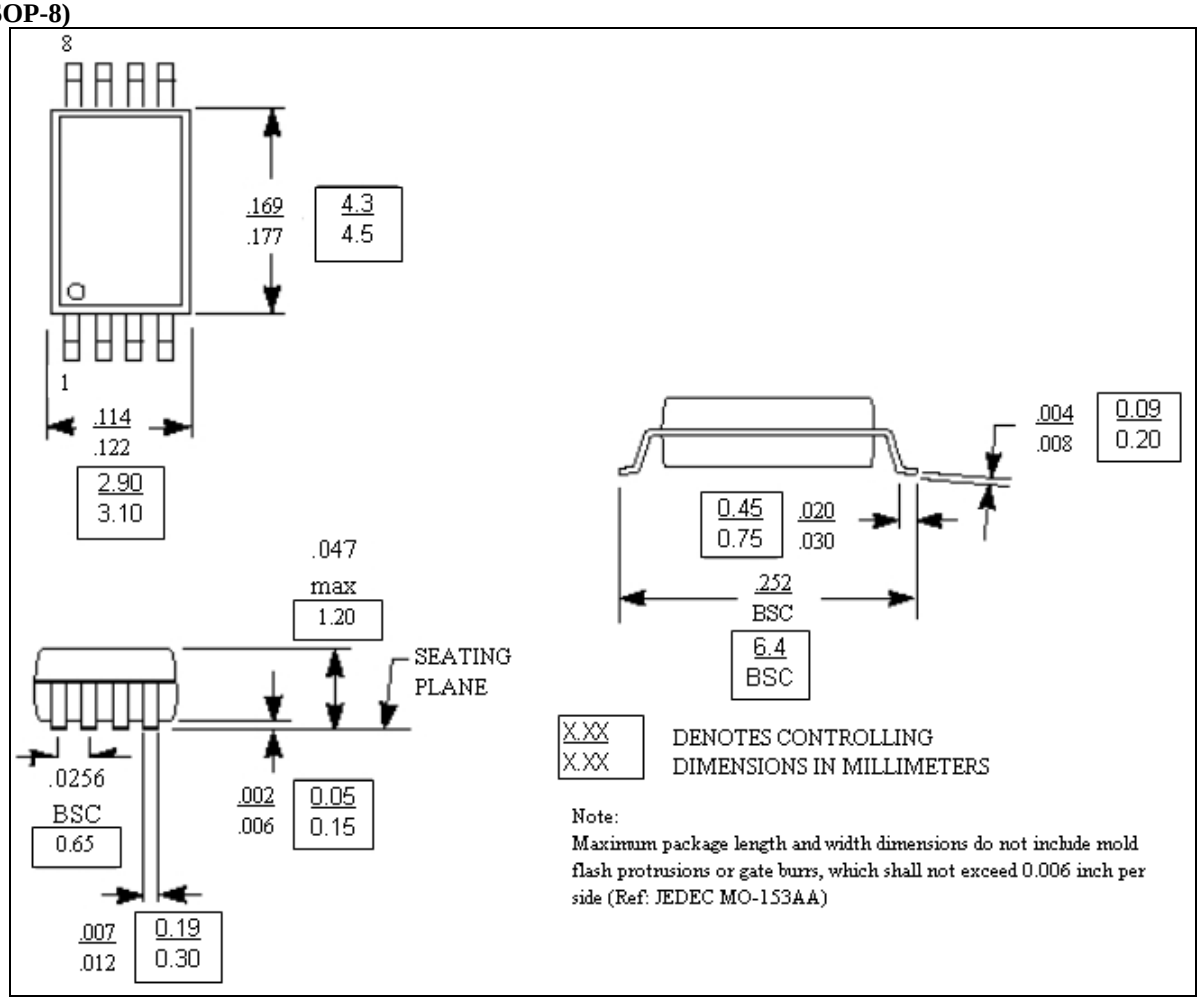
Parameter	Symbol	Min	Typ	Max	Unit
Nominal Frequency	f_O	-	32.768	-	kHz
Series Resistance	ESR	-	-	70	kΩ
Load Capacitance	C_L	-	6/12.5	-	pF

Mechanical Information

WE (SOIC-8)



LE (TSSOP-8)



Notes

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