

USB2GPIOISO# Adapter Board

Evaluates: USB2GPIOISO

General Description

The USB2GPIOISO# adapter board, shown in [Figure 1](#), is designed to work with Maxim's USB2GPIO# adapter board to provide galvanic isolation between the 'master' USB adapter board and a 'slave' EV kit or Pmod™ board. Four MAX14483 6-channel digital isolators are used to provide 3.75kV_{RMS} isolation.

USB2GPIOISO# block diagram is shown in [Figure 2](#). The two power domains are on the 'master' side (VDD_M and GNDM), and the 'slave' side (VDD_S and GNDS). The two independent power supplies are provided from the master board and the slave board with each VDD_ between 1.71V and 5.5V. The two connectors on the 'master' side are male connectors and plug into the female connectors on the USB2GPIO# adapter, as shown in [Figure 3](#).

USB2GPIOISO# is also designed to work with legacy USB2PMB1# and USM2PMB2# adapters; connectors XMA and XSA are 12-pin connectors which support either SPI with 4 GPIO pins and are fully compatible with previous adapters and low-pin count EV kit or Pmod boards. These connectors are controlled from the Munich GUI or relevant EV kit GUIs. Note that the isolator ICs have unidirectional channels (in or out). Full bidirectional I²C communication is not supported by this board.

The other connectors, XMB and XSB, are 20-pin connectors supporting extra GPIO connections. These 20-pin connectors are NOT controlled by the Munich GUI but are for use with future EV kits and will be controlled by the relevant EV kit GUIs.

USB2GPIOISO# adapter board can be used to enable isolated USB-to-SPI/GPIO interface for any Pmod-compatible plug-in peripheral modules such as the Maxim MAX14001PMB, and MAXREFDES12-Corona reference design.

Features

- 24 Isolated Channels with 3.75kV_{RMS} Robust Galvanic Isolation
- Low Propagation Delay 10ns, Typical
- Flexible System Design with Wide 1.71V to 5.5V Voltage Range on Each Side
- Small PCB area
- Pmod-Compatible Form Factor

[Ordering Information](#) appears at end of data sheet.

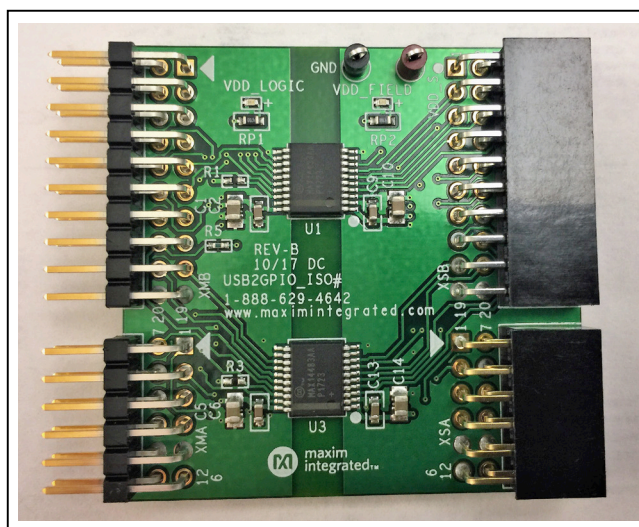


Figure 1. USB2GPIOISO# Board

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Detailed Description of Hardware

Figure 2 shows the USB2GPIOISO# connector block diagram (taken from the schematic). Note that the 'arrow' on each connector indicates the flow of data. For example, pin 1 on XMA shows that the signal (CS_AM) comes from the master, passes through the male connector, and onto USB2GPIOISO# board to the isolator channel for CS. Then, on the slave side of the isolator, this signal routes to pin 1 on XSA connector (CS_AS) and the 'arrow' shows the direction is from the isolator, through the female connector and to the slave board.

The two power domains are on the 'master' side (VDD_M and GNDM), and the 'slave' side (VDD_S and GNDS). The two independent power supplies are provided from the master board and the slave board with each VDD_ between 1.71V and 5.5V. The two connectors on the 'master' side are male connectors and plug into the female connectors on the USB2GPIO# adapter, as shown in Figure 3.

MAX14483 has unidirectional data channels and USB2GPIOISO# is configured in a 14/10 mode rather than a bidirectional I/O mode, meaning there are 14 channels communicating from the master to the slave, and 10 channels communicating from the slave to the master. Refer to the [USB2GPIOISO# Adapter Board Schematic](#) for each channel's communication direction. The digital channels on the slave Pmods or EV kits should follow the same communication directions as on the USB2GPIOISO# board. The Munich GUI and the EV kit GUI automatically configure the channel directions based on this and no jumpers are required for configuration.

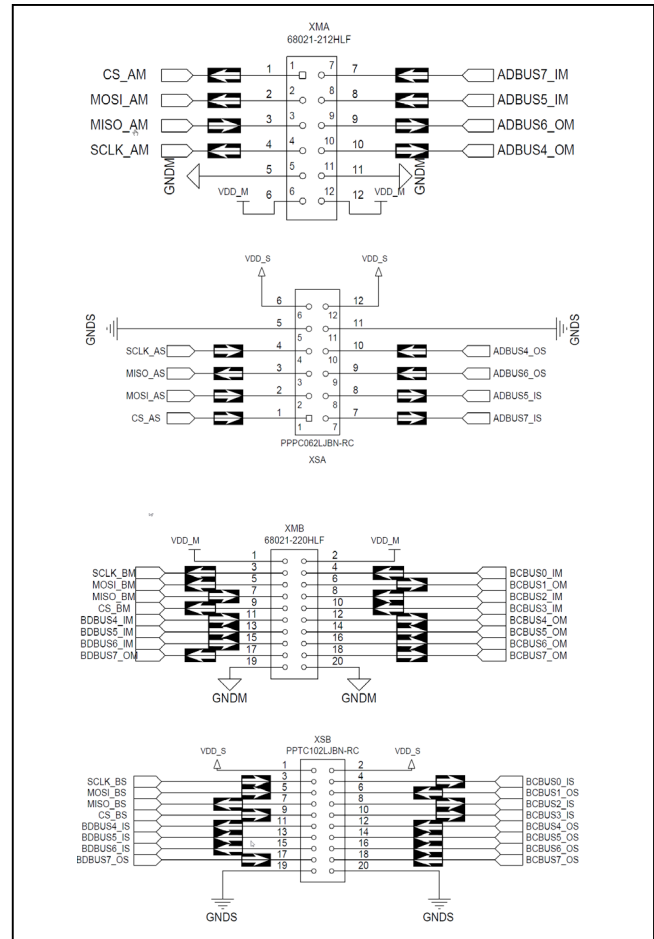


Figure 2. USB2GPIOISO# Subsystem Block Diagram

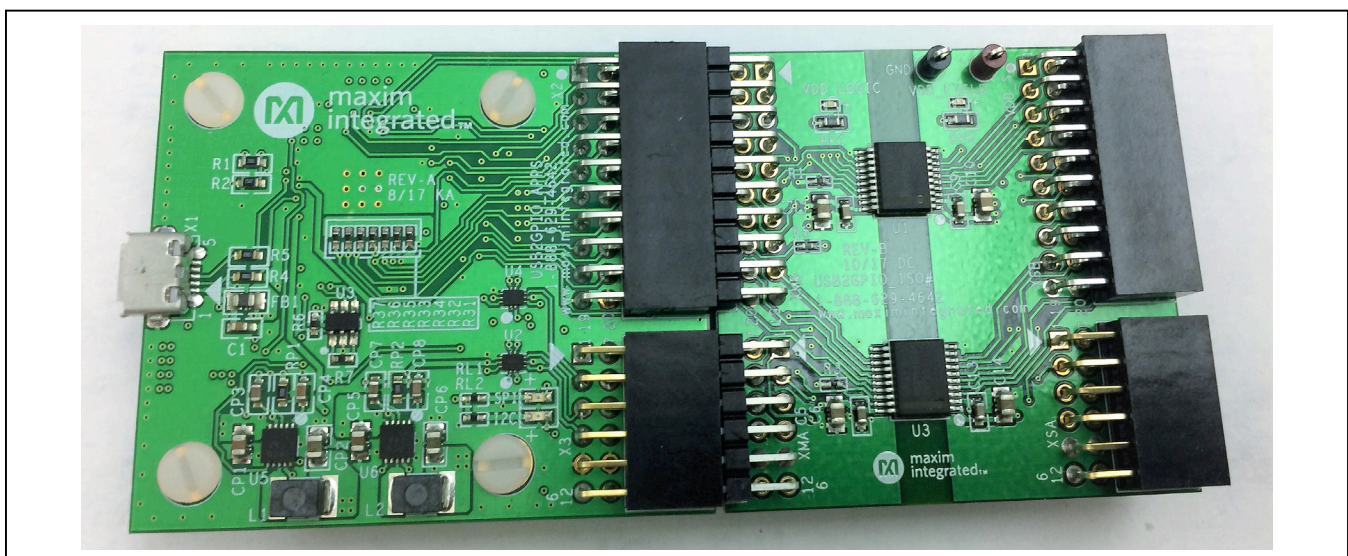


Figure 3. USB2GPIOISO# Board Connected with USB2GPIO# Adapter

Master and Slave Connectors

The USB2GPIOISO# is designed to receive power (VDD_M, GNDM and VDD_S, GNDS) from external boards through the connectors XMA, XMB, XSA and XSB. VDD_S is defined by the type of board connected to the slave connectors. When the user selects certain tab in the Munich GUI, VDD_M is automatically set to certain level, either 1.8V, 2.5V, 3.3V, or 5.0V. Note that USB2GPIOISO# does NOT provide power using VDD_S to the Pmod or EV kit board, but instead expects to receive power from those boards. Test points VDD_S and GND are provided to allow powering the USB2GPIOISO# slave side and Pmod or EV kit boards with external power supply.

Figure 4 shows the top view of the USB2GPIOISO# board, with the different connectors and the pin 1 identifiers. Note there are no jumpers or shunts on this board, all configuration is done under software control. Care should be taken to only insert the boards in the correct way as the connectors are not keyed to avoid false insertions. Reversing the connections (by turning the Pmod board upside down for example) may result in damage to the USB2GPIOISO# Pmod or EV kit board. Two LEDs are included to indicate if VDD_M and VDD_S are powered.

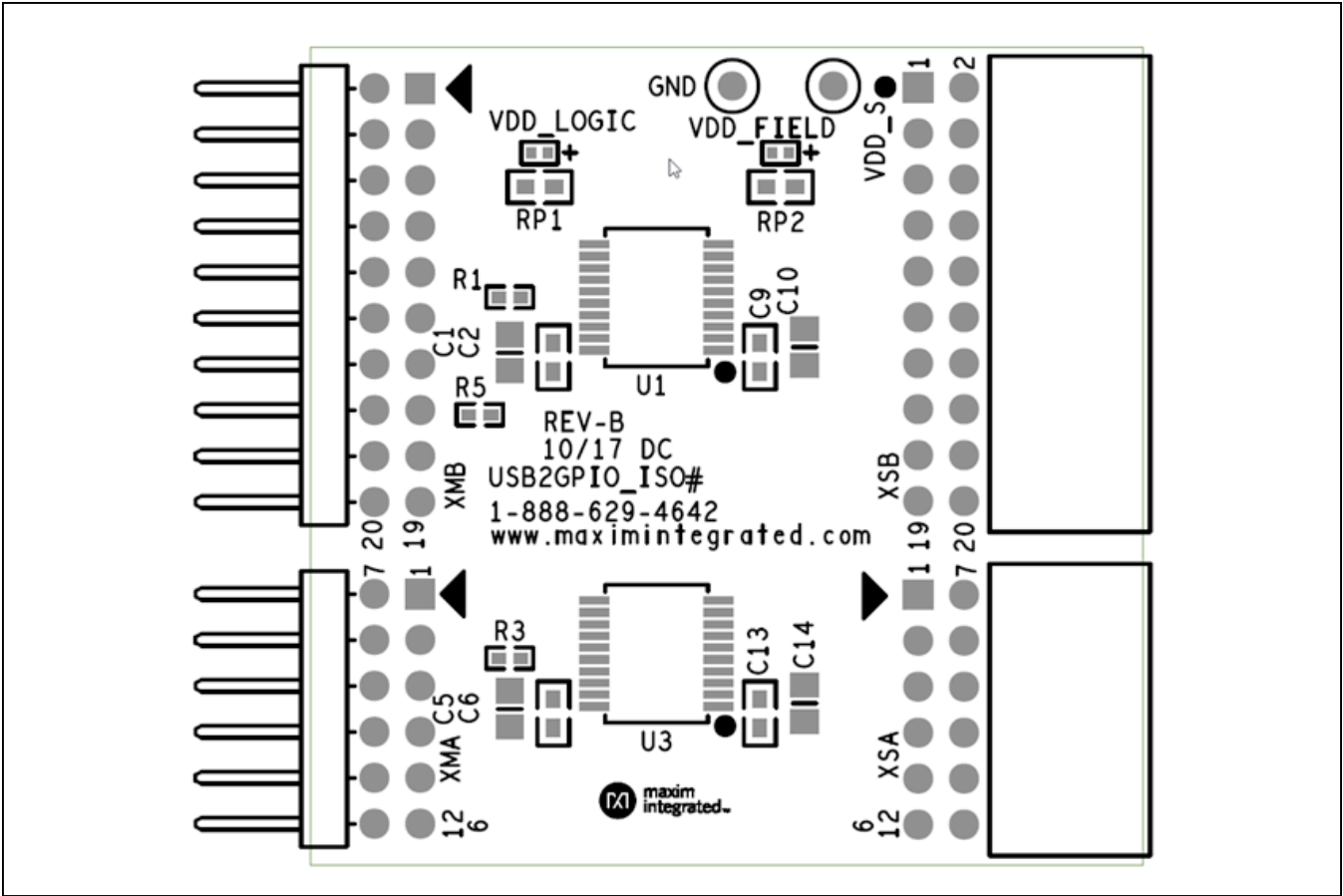


Figure 4. USB2GPIOISO# Orientation and Pinouts

Ordering Information

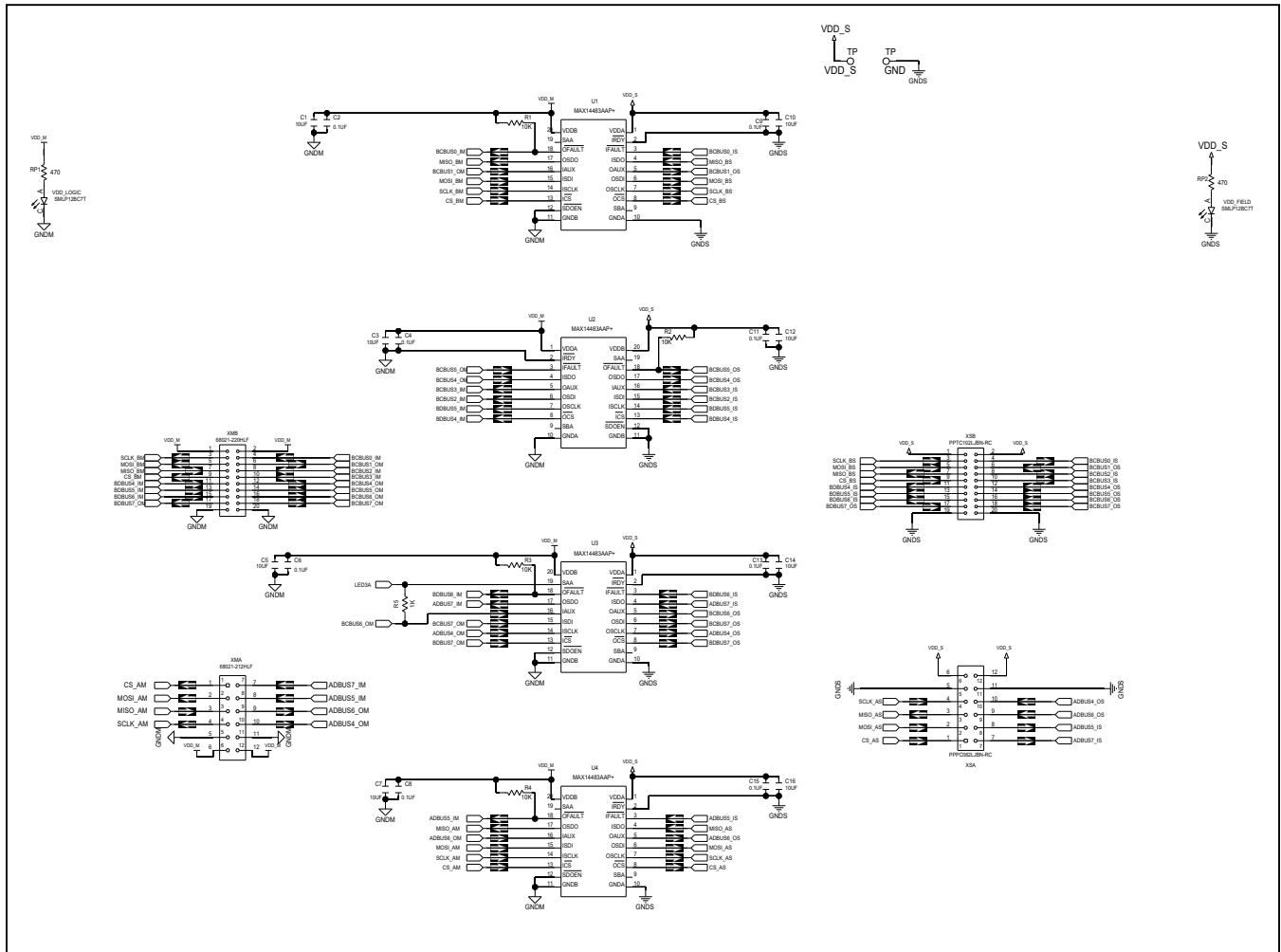
PART	TYPE
USB2GPIOISO#	Adapter Board

#Denotes RoHS compliant

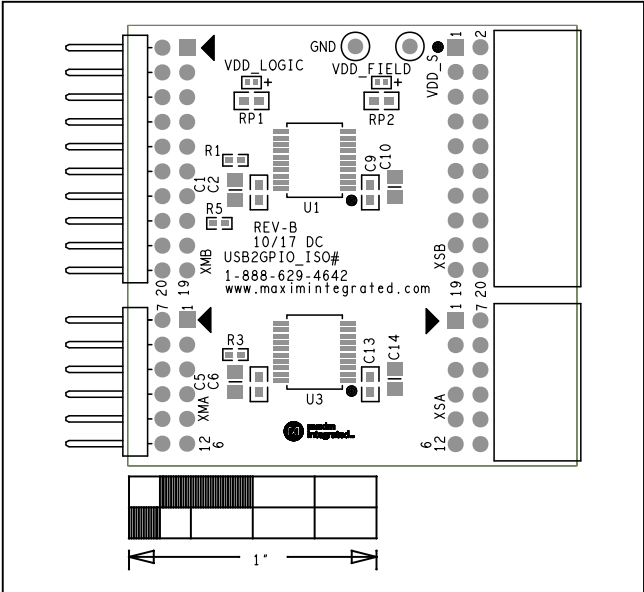
USB2GPIOISO# Adapter Board Bill of Materials

ITEM	REF DES	DNI/ DNP	QTY	MFG PART #	MANUFACTURER	VALUE	DESCRIPTION
1	C1, C3, C5, C7, C10, C12, C14, C16	-	8	CL21B106KQNNN	SAMSUNG ELECTRONICS	10UF	CAPACITOR; SMT (0805); CERAMIC CHIP; 10UF; 16V; TOL=10%; TG=-55 DEGC TO +125 DEGC; TC=X7R
2	C2, C4, C6, C8, C9, C11, C13, C15	-	8	GCJ188R71H104KA12; GCM188R71H104K; CGA3EZ7R1H104K080AA	MURATA; TDK	0.1UF	TOL=10%; TG=-55 DEGC TO +125 DEGC; TC=X7R; AUTO
3	GND	-	1	5001	KEYSTONE	N/A	BOARD HOLE=0.04IN; BLACK; PHOSPHOR BRONZE FILM
4	R1-R4	-	4	CRCW040210K0FK; RC0402FR-0710K	VISHAY DALE; YAGEO PHICOMP	10K	RESISTOR; 0402; 10K; 1%; 100PPM; 0.0625W; THICK FILM
5	R5	-	1	TNPW04021K00BE	VISHAY DALE	1K	RESISTOR; 0402; 1K; 1%; 100PPM; 0.10W, THICK FILM
6	RP1, RP2	-	2	CRCW0603470RFK; ERJ-3EKF-4700	VISHAY DALE/PANASONIC	470	RESISTOR; 0603; 470 OHM; 1%; 100PPM; 0.10W, THICK FILM
7	U1-U4	-	4	MAX14483AAP+	MAXIM	+	POWER; 3.75KV RMS; SPI DIGITAL ISOLATOR; DIODE; LED; SML-P1 SERIES; PICOLED; BLUE; SMT (0402); VF=2.9V; IF=0.005A
8	VDD_FIELD, VDD_LOGIC	-	2	SMLP12BC7T	ROHM	SMLP12BC7T	DIODE; LED; SML-P1 SERIES; PICOLED; BLUE; SMT (0402); VF=2.9V; IF=0.005A
9	VDD_S	-	1	5000	KEYSTONE	N/A	BOARD HOLE=0.04IN; RED; PHOSPHOR BRONZE
10	XMA	-	1	68021-212HLF	FCI CONNECT	68021-212HLF	BREAKAWAY HEADER; RIGHT ANGLE; 12PINS; BERGSTIK II BREAKAWAY HEADER; RIGHT ANGLE; 12PINS; CONNECTOR; FEMALE; THROUGH HOLE; 0.1IN CC; HEADER; 2 ROW; RIGHT ANGLE; 12PINS
11	XMB	-	1	68021-220HLF	AMPHENOL ICC	68021-220HLF	BREAKAWAY HEADER; RIGHT ANGLE; 12PINS; BERGSTIK II BREAKAWAY HEADER; RIGHT ANGLE; 12PINS; CONNECTOR; FEMALE; THROUGH HOLE; 0.1IN CC; HEADER; 2 ROW; RIGHT ANGLE; 12PINS
12	XSA	-	1	PPPC062LJBN-RC	ELECTRONICS CORP.	PPPC062LJBN-RC	CONNECTOR; FEMALE; THROUGH HOLE; 0.1IN CC; HEADER; 2 ROW; RIGHT ANGLE; 12PINS
13	XSB	-	1	PPTC102LJBN-RC	ELECTRONICS CORP.	PPTC102LJBN-RC	CONNECTOR; FEMALE; THROUGH HOLE; 0.1IN CC; HEADER; 2 ROW; RIGHT ANGLE; 12PINS
14	PCB	-	1	USB2GPIO_ISO_APPS_B	MAXIM	PCB	BREAKAWAY HEADER; RIGHT ANGLE; 20PINS; PCB:USB2GPIO_ISO_APPS_B
TOTAL			36				
NOTE: DNI--> DO NOT INSTALL(PACKOUT) ; DNP--> DO NOT PROCURE							

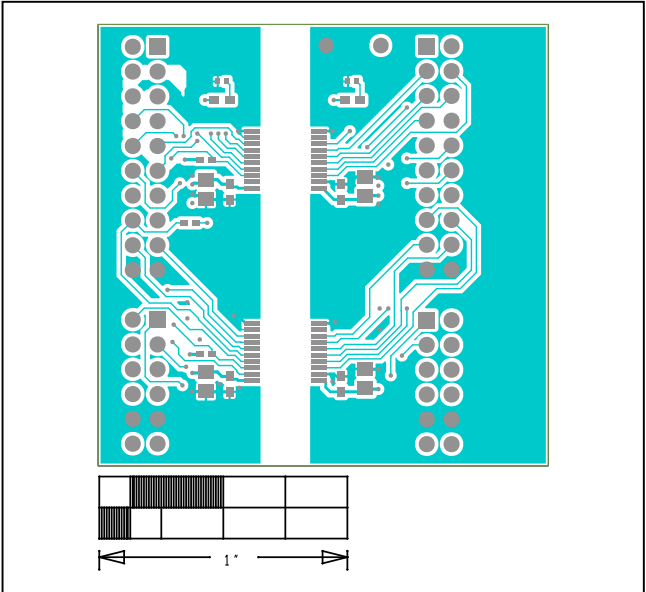
USB2GPIOISO# Adapter Board Schematic



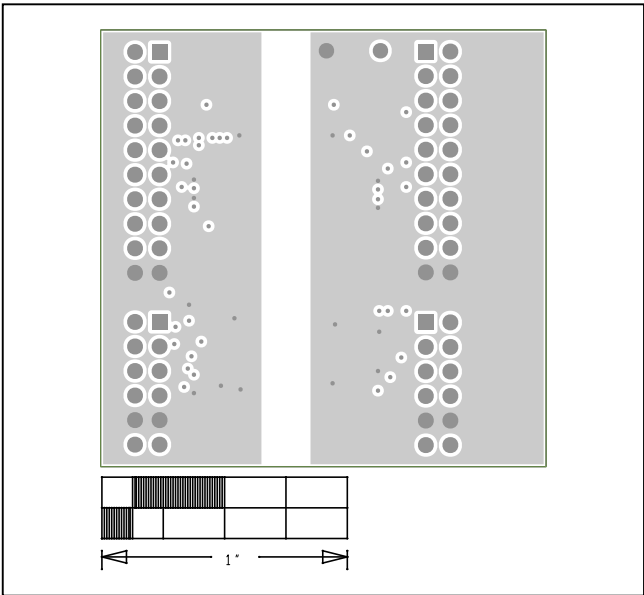
USB2GPIOISO# Adapter Board PCB Layout Diagrams



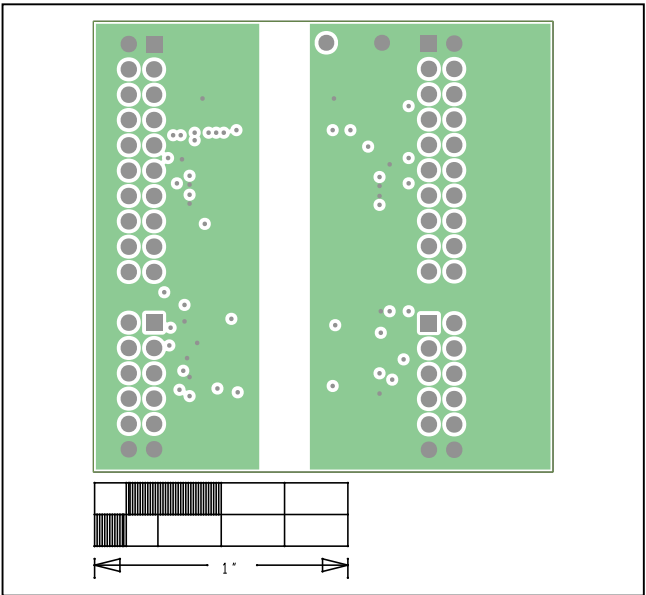
USB2GPIOISO# Adapter Board—Top Silkscreen



USB2GPIOISO# Adapter Board—Top

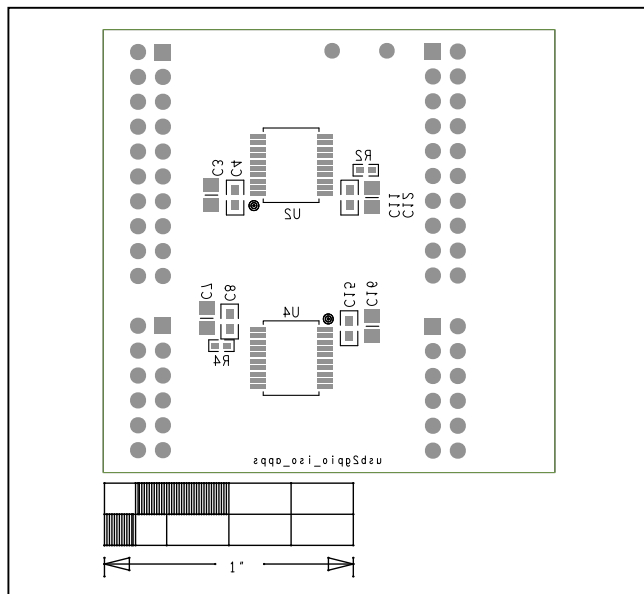


USB2GPIOISO# Adapter Board—Internal 2

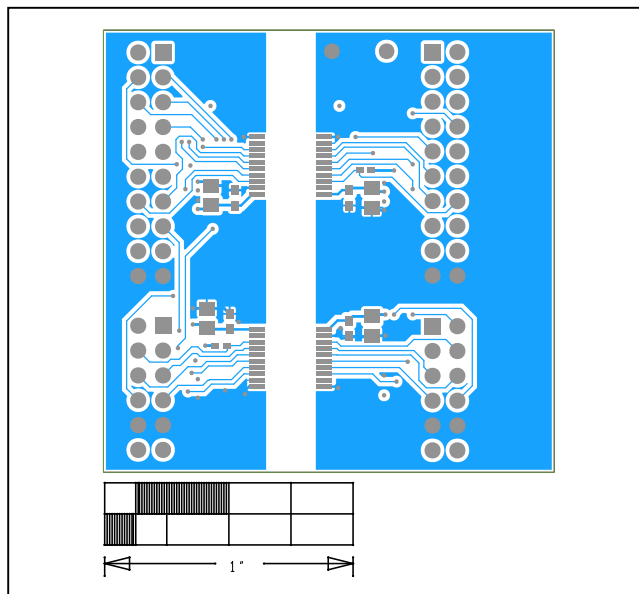


USB2GPIOISO# Adapter Board—Internal 3

USB2GPIOISO# Adapter Board PCB Layout Diagrams (continued)



USB2GPIOISO# Adapter Board—Bottom Silkscreen



USB2GPIOISO# Adapter Board—Bottom

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	04/18	Initial release	—

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