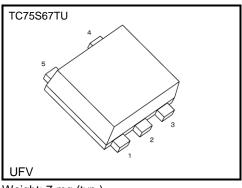
TOSHIBA CMOS Linear Integrated Circuit Silicon Monolithic

TC75S67TU

Single Operational Amplifier (Ultra Low Noise Operational Amplifier)

Features

- Ultra Low Noise. $V_{NI} = 6.0 \text{ nV/}\sqrt{\text{Hz}}$ (typ.) @ $V_{DD} = 2.5 \text{ V}$
- Low-current supply. 430 μA (typ.) @ V_{DD} = 2.5 V
- Ultra-compact package.



Weight: 7 mg (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage	V _{DD} , V _{SS}	6	V
Differential input voltage	DVIN	±6	V
Input voltage	VIN	V _{DD} to V _{SS}	V
Output current	lout	±4	mA
Power dissipation (Note 1)	PD	450	mW
Operating temperature	Topr	-40 to 85	°C
Storage temperature	T _{stg}	-55 to 125	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on a glass epoxy circuit board of 30 mm × 30 mm. Pad dimension of 35mm²

Operating Ratings (Ta = 25°C)

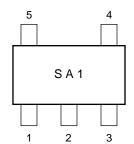
Characteristics	Symbol	Rating	Unit
Supply voltage	V _{DD} , V _{SS}	2.2 to 5.5	V

Note2: Do not use this product in a voltage follower circuit or outside the range of the common mode input voltage. (For the common mode input voltage, see DC Characteristics on Page 2). Failure to follow this instruction may cause voltage oscillation.

A higher load capacitance will increase the risk of voltage oscillation, even if this product is used within the range of the common mode input voltage. Allow sufficient capacitance value margin when designing your circuit and using this product to prevent voltage oscillation.

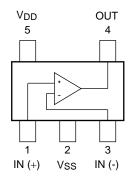
Start of commercial production 2017-08

Marking (top view)



Pin Connection (top view)

TC75S67TU



Electrical Characteristics

DC Characteristics (VDD = 2.5 V, Vss = GND, Ta = 25°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Тур.	Max	Unit
Input offset voltage	Vio	1	$R_S = 1 \text{ k}\Omega, R_F = 100 \text{ k}\Omega$	-	0.5	3	mV
Input offset voltage drift	V _{IO} drift	1	$R_S = 1 \text{ k}\Omega, R_F = 100 \text{ k}\Omega$	-	2	-	μV/°C
Input offset current	lio	-	-	-	1	-	pA
Input bias current	lį	-	-	-	1	-	pA
Common mode input voltage	CMVIN	2	$R_S = 1 \text{ k}\Omega, R_F = 100 \text{ k}\Omega$	0	-	1.4	V
Voltage gain (open loop)	GV	-	-	80	100	-	dB
Maximum output voltage	Voн	3	R _L ≥ 100 kΩ	2.4	-	-	V
	VoL	4	R _L ≥ 100 kΩ	-	-	0.1	
Common mode input signal rejection ratio	CMRR	2	V _{IN} = 0 to 1.4 V	70	100	-	dB
Supply voltage rejection ratio	SVRR	1	V _{DD} = 2.2 to 5.5V	70	100	-	dB
Supply current	I _{DD}	5	-	-	430	700	μA
Source current	Isource	6	-	2000	2500	-	μA
Sink current	Isink	7	-	2000	3500	-	μA

AC Characteristics (VDD = 2.5 V, Vss = GND, Ta = 25°C)

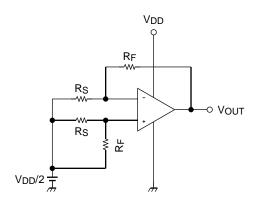
Characteristics	Symbol	Test Circuit	Test Condition	Min	Тур.	Max	Unit
Equivalent input Noise Voltage	.,	-	$f = 10 \text{ Hz}, \text{ GV} = 40 \text{ dB},$ RS = 100 Ω , Rf = 10 $k\Omega$	-	16	40	- nV/√Hz
	VNI		$f = 1 \text{ kHz}, G_V = 40 \text{ dB},$ RS = 100 Ω , Rf = 10 $k\Omega$	-	6	10	
Unity Gain Cross Frequency	fT	9	-	3.0	3.5	-	MHz
Phase delay	φD	8	f = 10 kHz	-	-10.5	-	degrees
Phase margin	φm	9	G _V = 6 dB (A _V = 2)	-	55	-	degrees

AC Characteristics (VDD = 1.25 V, Vss = -1.25 V, Ta = 25°C)

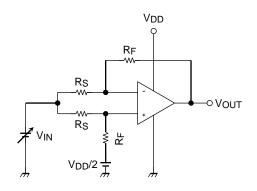
Characteristics	Symbol	Test Circuit	Test Condition	Min	Тур.	Max	Unit
Slew Rate	SR	10	G _V = 12 dB, V _{IN} = 0.25 Vp-p	ı	1.0	-	V/µs

Test Circuit

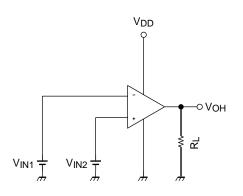
1. SVRR, Vio



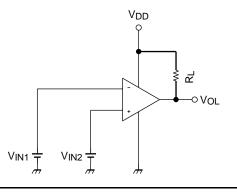
2. CMRR, CMVIN



3. Voh



4. Vol



SVRR

 For each of the two VDD values, measure the VOUT value, as indicated below, and calculate the value of SVRR using the equation shown.

When V_{DD} = 2.2 V, V_{DD} = V_{DD} 1 and V_{OUT} = V_{OUT} 1 When V_{DD} = 5.5 V, V_{DD} = V_{DD} 2 and V_{OUT} = V_{OUT} 2

$$SVRR = 20 \ log \left(\left| \frac{V_{OUT}1 - V_{OUT}2}{V_{DD}1 - V_{DD}2} \right| \times \frac{R_S}{R_F + R_S} \right)$$

Vio

Measure the value of V_{OUT} and calculate the value of V_{IO} using the following equation.

$$V_{IO} = \left(V_{OUT} - \frac{V_{DD}}{2}\right) \times \frac{R_S}{R_F + R_S}$$

CMRR

Measure the V_{OUT} value, as indicated below, and calculate the value of the CMRR using the equation shown.

When $V_{IN} = 0$ V, $V_{IN} = V_{IN}1$ and $V_{OUT} = V_{OUT}1$ When $V_{IN} = 1.4$ V, $V_{IN} = V_{IN}2$ and $V_{OUT} = V_{OUT}2$

$$CMRR = 20 \ log \left(\frac{\left| V_{OUT}1 - V_{OUT}2 \right|}{V_{IN}1 - V_{IN}2} \right| \times \frac{R_S}{R_F + R_S} \right)$$

CMV_{IN}

Input range within which the CMRR specification guarantees V_{OUT} value (as varied by the V_{IN} value).

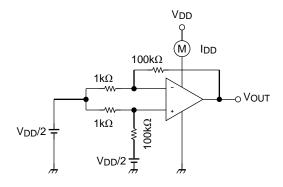
$$V_{IN1} = \frac{V_{DD}}{2} - 0.1 V$$

$$V_{IN2} = \frac{V_{DD}}{2}$$

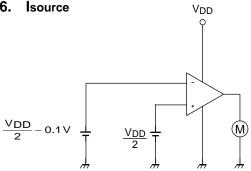
$$V_{IN1} = \frac{V_{DD}}{2}$$

$$V_{IN2} = \frac{V_{DD}}{2} - 0.1 V$$

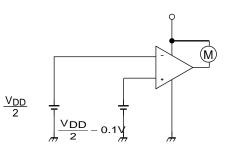
5. IDD



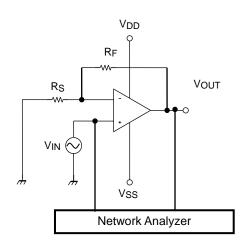
6. Isource

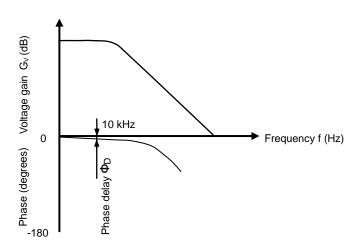


7. Isink

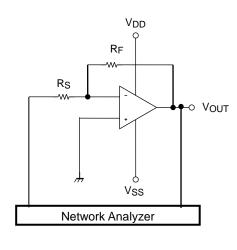


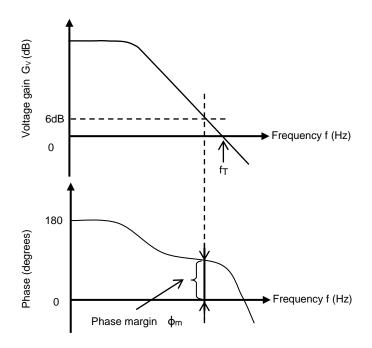
8. фр



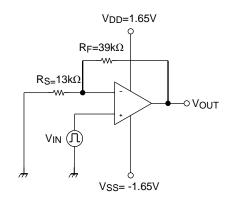


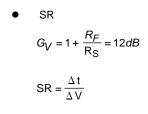
9. fT, **фm**

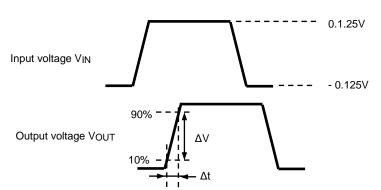




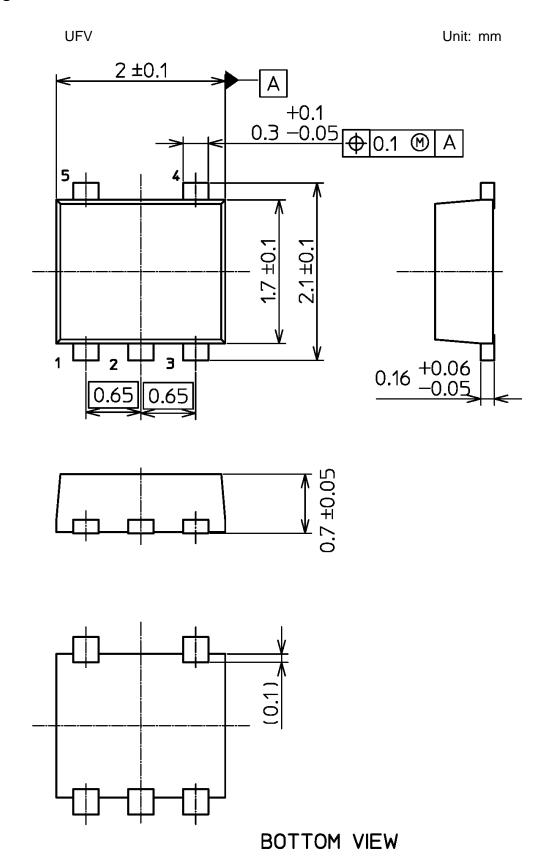
10. SR







Package Dimensions



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Weight: 7 mg (typ.)

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