### 3.3 VOLT TIME SLOT INTERCHANGE

 DIGITAL SWITCH $512 \times 512$
## FEATURES:

- $512 \times 512$ channel non-blocking switching at $2.048 \mathrm{Mb} / \mathrm{s}$
- Per-channel variable or constant throughput delay
- Automatic identification of ST-BUS ${ }^{\circledR} / G C I$ interfaces
- Accept 16 serial data streams of $2.048 \mathrm{Mb} / \mathrm{s}$
- Automatic frame offset delay measurement
- Per-stream frame delay offset programming
- Per-channel high impedance output control
- Per-channel Processor Mode
- Control interface compatible to Intel/Motorola CPUs
- Connection memory block programming
- IEEE-1149.1 (JTAG) Test Port
- Available in 100-pin Thin Quad Flatpack (TQFP)
- 3.3V Power Supply
- Operating Temperature Range $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$


## DESCRIPTION:

The IDT72V70200 is a non-blocking digital switch that has a capacity of $512 \times 512$ channels at $2.048 \mathrm{Mb} / \mathrm{s}$. Some of the main features are: programmable stream and channel control, ProcessorMode, inputoffsetdelay and highimpedanceoutputcontrol.

Per-stream input delay control is provided for managing large multi-chip switches thattransportboth voice channel and concatenated datachannels. In addition, input streams can be individually calibrated for input frame offset.


## PIN CONFIGURATIONS



NOTES:

1. DNC - Do Not Connect

PLCC: 0.05in. pitch, 1.15in. x 1.15in. (PL84-1, order code: J)
2. IC - Internal Connection, tie to GROUND for normal operation.

TOP VIEW
3. All I/O pins are 5 V tolerant except for TMS, TDI and TRST.

## PIN CONFIGURATIONS (CONTINUED)



## PIN DESCRIPTION

| SYMBOL | NAME | I/O | DESCRIPTION |
| :---: | :---: | :---: | :---: |
| GND | Ground. |  | Ground Rail. |
| Vcc | Vcc |  | +3.3 Volt Power Supply. |
| TX0-15 ${ }^{(1)}$ | TX Output 0 to 15 (Three-state Outputs) | 0 | Serial data output stream. These streams have a data rate of $2.048 \mathrm{Mb} / \mathrm{s}$. |
| RX0-15 ${ }^{(1)}$ | RX Input 0 to 15 | I | Serial data input stream. These streams have a data rate of $2.048 \mathrm{Mb} / \mathrm{s}$. |
| F0i ${ }^{(1)}$ | Frame Pulse | I | This input accepts and automatically identifies frame synchronization signals formatted according to ST-BUS ${ }^{\circledR}$ and GCI specifications. |
| $\mathrm{FE}^{(1)}$ | Frame Evaluation | 1 | This pin is the frame measurement input. |
| CLK ${ }^{(1)}$ | Clock | I | Serial clock for shifting data in/out on the serial streams (RX/TX 0-15). This input accepts a 4.096 MHz clock. |
| TMS | Test Mode Select | 1 | JTAG signal that controls the state transitions of the TAP controller. This pin is pulled HIGH by an internal pullup when not driven. |
| TDI | Test Serial Data In | 1 | JTAG serial test instructions and data are shifted in on this pin. This pin is pulled HIGH by an internal pull-up when not driven. |
| TDO | Test Serial Data Out | 0 | JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high-impedance state when JTAG scan is not enabled. |
| TCK ${ }^{(1)}$ | Test Clock | 1 | Provides the clock to the JTAG test logic. |
| TRST | Test Reset | 1 | Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-reset state. This pin is pulled by an internal pull-up when not driven. This pin should be pulsed LOW on power-up, or held LOW, to ensure that the IDT72V70200 is in the normal functional mode. |
| IC ${ }^{(1)}$ | Internal Connection | I | Connect to GND for normal operation. This pin must be LOW for the IDT72V70200 to function normally and to comply with IEEE 1114 (JTAG) boundary scan requirements. |
| $\overline{\mathrm{RESET}}{ }^{(1)}$ | Device Reset (Schmitt Trigger Input) | I | This input (active LOW) puts the IDT72V70200 in its reset state that clears the device internal counters, registers and brings TX0-15 and microport data outputs to a high-impedance state. The time constant for a power up reset circuit must be a minimum of five times the rise time of the power supply. In normal operation, the RESET pin must be held LOW for a minimum of 100 ns to reset the device. |
| A0-7 ${ }^{(1)}$ | Address 0-7 | 1 | When non-multiplexed CPU bus operation is selected, these lines provide the A0-A7 address lines to the internal memories. |
| $\mathrm{DS} / \overline{R D}^{(1)}$ | Data Strobe/Read | I | For Motorola multiplexed bus operation, this input is DS. This active HIGH DS input works in conjunction with $\overline{\mathrm{CS}}$ to enable the read and write operations. For Motorola non-multiplexed CPU bus operation, this input is DS. This active LOW input works in conjunction with $\overline{\mathrm{CS}}$ to enable the read and write operations. For Intel multiplexed bus operation, this input is $\overline{\mathrm{RD}}$. This active LOW input sets the data bus lines (AD0-7, D8-15) as outputs. |
| $\mathrm{R} / \overline{\mathrm{W}} / \overline{\mathrm{WR}}^{(1)}$ | Read/Write / Write | 1 | In the cases of Motorola non-multiplexed and multiplexed bus operations, this input is $R / \bar{W}$. This input controls the direction of the data bus lines (AD0-7, D8-15) during a microprocessor access. For Intel multiplexed bus operation, this input is $\overline{W R}$. This active LOW input is used with $\overline{R D}$ to control the data bus (ADO-7) lines as inputs. |
| $\overline{\mathrm{CS}}{ }^{(1)}$ | Chip Select | 1 | Active LOW input used by a microprocessor to activate the microprocessor port of IDT72V70200. |
| AS/ALE ${ }^{(1)}$ | Address Strobe or Latch Enable | I | This input is used if multiplexed bus operation is selected via the IM input pin. For Motorola non-multiplexed bus operation, connect this pin to ground. |
| $\mathrm{IM}^{(1)}$ | CPU Interface Mode | I | When IM is HIGH, the microprocessor port is in the multiplexed mode. When IM is LOW, the microprocessor port is in non-multiplexed mode. |
| AD0-7 ${ }^{(1)}$ | Address/Data Bus 0 to 7 | I/0 | These pins are the eight least significant data bits of the microprocessor port. In multiplexed mode, these pins are also the input address bits of the microprocessor port. |
| D8-15 ${ }^{(1)}$ | Data Bus 8-15 | I/0 | These pins are the eight most significant data bits of the microprocessor port. |
| $\overline{\mathrm{DTA}}{ }^{(1)}$ | Data Transfer Acknowledgment | 0 | This active LOW output signal indicates that a data bus transfer is complete. When the bus cycle ends, this pin drives HIGH and then goes high-impedance, allowing for faster bus cycles with a weaker pull-up resistor. A pull-up resistor is required to hold a HIGH level when the pin is in high-impedance. |
| $\mathrm{CCO}^{(1)}$ | Control Output | 0 | This is a $4.096 \mathrm{Mb} / \mathrm{s}$ output containing 512 bits per frame respectively. The level of each bit is determined by the CCO bit in the connection memory. See External Drive Control Section. |
| ODE ${ }^{(1)}$ | Output Drive Enable | I | This is the output enable control for the TX0 to TX15 serial outputs. When ODE input is LOW and the OSB bit of the IMS register is LOW, TXO-15 are in a high-impedance state. If this input is HIGH, the TXO-15 output drivers are enabled. However, each channel may still be put into a high-impedance state by using the per channel control bit in the connection memory. |

NOTE:

1. These pins are 5 V tolerant.

## FUNCTIONAL DESCRIPTION

The IDT72V70200 is capable of switching $512 \times 512,64 \mathrm{Kbit} / \mathrm{PCM}$ or $\mathrm{N} \times 64$ Kbit/s channel data. The device maintains frame integrity in data applications and minimum throughput delay for voice applications on a per channel basis.

The serial input streams of the IDT72V70200 can have a bit rate of $2.048 \mathrm{Mb} / \mathrm{s}$ and are arranged in $125 \mu \mathrm{~s}$ wide frames, which contain 32 channels respectively. The data rates on input and output streams are identical.

In Processor Mode, the microprocessor can access inputand outputimeslots on a perchannel basis allowing fortransfer of control andstatus information. The IDT72V70200 automatically yidentifies the polarity of the frame synchronization inputsignal and configures the serial streams to eitherST-BUS ${ }^{\circledR}$ or GCI formats.

With the variety ofdifferentmicroprocessor interfaces, IDT72V70200 has provided an Input Mode pin (IM) to help integrate the device into different microprocessorbased environments: Non-multiplexed or Multiplexed. These interfaces provide compatibility with multiplexed and Motorolanon-multiplexed buses. Thedevice can also resolvedifferent control signalseliminating the use of glue logic necessary to convert the signals ( $R / \bar{W} / \overline{W R}, ~ D S / \overline{R D}, A S / A L E)$.

Theframe offsetcalibrationfunctionallowsuserstomeasuretheframeoffset delay using a frame evaluation pin (FE). The input offset delay can be programmedforindividual streams using internal frameinputoffsetregisters, see Table 8.

The internal loopback allows the TX outputdata to be looped around to the RXinputs for diagnostic purposes.

A functional Block Diagram of the IDT72V70200 is shown in Figure 1.

## DATA ANDCONNECTIONMEMORY

The received serial data is converted to parallel format by internal serial-to-parallel converters and stored sequentially in the data memory. The 8 KHz input frame pulse (드i) is used to generate channel and frame boundaries of the inputserial data. Depending on the interface mode select(IIS) register, the usable data memory may be as large as 512 bytes.

Data to be outputon the serial streams (TX0-15) may come from eitherthe data memory or connection memory. For data output from data memory (connection mode), addresses in the connection memory are used. For data to be outputfrom connection memory, the connection memory control bits must setthe particularTXoutputin Processor Mode. Onetime-slotbefore the data is to be output, data from either connection memory or data memory is read internally. This allows enoughtime for memory access and parallel-to-serial conversion.

## CONNECTION AND PROCESSOR MODES

Inthe Connection Mode, the addresses of the inputsource dataforall output channels are stored in the connection memory. The connection memory is mapped in such a way thateach location corresponds to an output channel on the outputstreams. Fordetails on the use ofthe source address data (CAB and SAB bits), see Table 10. Once the source address bits are programmed by the microprocessor, the contents of the data memory at the selected address are transferredto the parallel-to-serial converters and then ontoa TX outputstream.

By having the each location in the connection memory specify an input channel, multiple outputs can specify the same input address. This can be a powerful tool used for broadcasting data.

In Processor Mode, the microprocessor writes data to the connection memory. Eachlocation in the connection memory corresponds to a particular outputstream and channel numberand is transferred directly to the parallel-to-
serial converter one time-slot before itis to be output. This data will be output onthe TXstreamsineveryframeuntil the datais changed bythemicroprocessor.

Asthe IDT72V70200 can beused in a wide variety of applications, the device also has memory locations to control the outputs based on operating mode. Specifically, the IDT72V70200 provides five per-channel control bits for the following functions: processor orconnection mode, constantorvariabledelay, enables/three-state the TX output drivers and enables/disable the loopback function. In addition, one of these bits allows the userto control the CCO output.

Ifan outputchannel is setto ahigh-impedance statethrough the connection memory, the TX outputwill be in a high-impedance state for the duration of that channel. In addition to the per-channel control, all channels on the ST-BUS ${ }^{\circledR}$ outputs can be placed in a high impedance state byeitherpulling the ODE input pin low or programming the Output Stand-By (OSB) bitin the interface mode selection register. This action overrides the per-channel programming in the connection memory bits.

The connection memory data can be accessed via the microprocessor interface. The addressing ofthe devices internal registers, dataand connection memories is performed through the address inputpins and the Memory Select (MS) bit ofthe control register. Fordetails on device addressing, see Software Control and Control Register bits description (Table 3 and 5).

## SERIAL DATA INTERFACE TIMING

The master clock frequency mustalways be twice the datarate. For serial data rates of $2.048 \mathrm{Mb} / \mathrm{s}$, the master clock (CLK) must be at 4.096 MHz . The input and output stream data rates will always be identical.

The input 8 KHz frame pulse can be in eitherST-BUS ${ }^{\ominus}$ or GCI format. The IDT72V70200 automatically detects the presence of an inputframe pulse and identifies itas eitherST-BUS ${ }^{\circledR}$ or GCI.InST-BUS ${ }^{\circledR}$ format, every second falling edge ofthe master clock marks abitboundary and the data is clocked in on the rising edge of CLK, three quarters of the way into the bit cell, see Figure 7. In GCI format, every second rising edge ofthe master clock marks the bitboundary and data is clocked in on the falling edge of CLK at three quarters of the way into the bit cell, see Figure 8.

## INPUT FRAME OFFSET SELECTION

Inputframe offsetselection allows the channel alignment of individual input streams tobe offsetwithrespectto the outputstream channel alignment (i.e. $\overline{\text { Fii) }}$ ). Although all input data comes in at the same speed, delays can be caused by variable path serial backplanes and variable path lengths which may be implemented inlarge centralized and distributed switching systems. Because data is often delayed, thisfeature is useful in compensatingforthe skewbetween clocks.

Each input stream can have its own delay offsetvalue by programming the frame inputoffsetregisters (FOR). The maximumallowable skew is +4.5 master clock(CLK) periods forward with resolution of $1 / 2$ clock period. The outputframe offsetcannotbe offsetor adjusted. See Figure 5, Table 8 and 9 fordelay offset programming.

## SERIAL INPUT FRAME ALIGNMENT EVALUATION

The IDT72V70200 provides the frame evaluation (FE) inputto determine different data inputdelays with respect to the frame pulse FOi.

A measurement cycle is started by setting the startframe evaluation(SFE) bitlow for at leastone frame. When the SFE bitin the IMS register is changed from low to high, the evaluation starts. Two frames later, the complete frame evaluation (CFE) bit of the frame alignmentregister(FAR) changes from low to high to signal thata valid offsetmeasurementis ready to be read from bits 0
to 11 of the FAR register. The SFE bit must be set to zero before a new measurementcycle started.

InST-BUS ${ }^{\circledR}$ mode, the falling edge of the frame measurement signal(FE) is evaluated againstthe falling edge oftheST-BUS ${ }^{\circledR}$ frame pulse. In CCImode , the risingedge ofFE is evaluated againstthe rising edge of the GCI frame pulse. See Table 7 and Figure 4 for the description of the frame alignment register.

## MEMORY BLOCK PROGRAMMING

The IDT72V70200 provides users with the capability of initializing the entire connection memory blockintwo frames. To setbits 11 to 15 of every connection memorylocation, firstprogramthe desired patterninbits 5 to9 ofthe IMS register.

The block programming mode is enabled by setting the memory block program (MBP) bit of the control register high. When the block programming enable(BPE) bitofthe IMS register is setto high, the block programming data will be loaded into the bits 11 to 15 of every connection memory location. The other connection memory bits (bit0 to bit 10) are loaded with zeros. When the memory block programming is complete, the device resets the BPE bittozero.

## LOOPBACK CONTROL

The loopback control (LPBK) bitofeach connectionmemory locationallows the TX output data to be looped backed internally to the RXinputfor diagnostic purposes.

If the LPBK bitis high, the associated TX output channel data is internally looped back to the RX inputchannel (i.e., data from TX n channel m routes to the RX $n$ channel m internally); if the LPBK bit is low, the loopback feature is disabled. For proper per-channel loopback operation, the contents of frame delay offset registers mustbe setto zero.

## DELAY THROUGH THE IDT72V70200

The switching of information from the inputserial streams to theoutputserial streams results in a throughput delay. The device can be programmed to performtime-slotinterchangefunctionswith differentthroughputdelay capabilities on the per-channel basis. Forvoice applications, variable throughputdelay is bestasitensuresminimum delay betweeninputand outputdata. In wideband data applications, constant throughputdelay is bestas the frame integrity of the information is maintained through the switch.

The delay through the device varies according to the type of throughput delay selected in the $\overline{\mathrm{V}} / \mathrm{C}$ bit of the connection memory.

## VARIABLE DELAY MODE (VI/C BIT $=0$ )

In this mode, the delay is dependentonly on the combination of source and destination channels and is independent of input and output streams. The minimum delay achievable in the IDT72V70200 is three time-slots. If the input channel data is switched to the same outputchannel (channeln, framep), it will beoutputinthe following frame (channeln, framep+1). The same istrue if input channel $n$ is switched to output channel $n+1$ or $n+2$. If the input channel $n$ is switched to outputchannel $n+3, n+4, \ldots$, the new output data will appear in the same frame. Table 1 shows the possible delays for the IDT72V70200 in the variable delay mode.

## CONSTANT DELAY MODE (V̄/C BIT = 1 )

Inthis mode, frame integrity is maintained in all switching configurations by making use of a multiple data memory buffer. Inputchannel data is written into the data memory buffers during frame $n$ will be read out during frame $n+2$. In the IDT72V70200, the minimum throughputdelay achievable in the constant
delay mode will be one frame. For example, when inputtime-slot31 is switched to outputtime-slot 0 . The maximum delay of 94 time-slots of delay occurs when time-slot 0 in a frame is switched to time-slot 31 in the frame. See Table 2.

## MICROPROCESSORINTERFACE

The IDT72V70200 provides a parallel microprocessor interface for multiplexed or non-multiplexed bus structures. This interface is compatible with Motorolanon-multiplexed and multiplexed buses.

Ifthe IM pin is low a Motorolanon-multiplexed bus should be connected to the device. Ifthe IM pin is high, the device monitors the AS/ALE and DS/依to determine what mode the IDT72V70200 should operate in.

IfDS/RD is low at the rising edge of AS/ALE, then the mode 1 multiplexed timing is selected. IfDS/ $\overline{R D}$ is high atthe rising edge of AS/ALE, then the mode 2 multiplexed bustiming is selected.

For multiplexed operation, the required signals are the 8-bit data and address (AD0-AD7), 8-bit Data (D8-D15), Address strobe/Address latch
 Chip select $(\overline{\mathrm{CS}})$ and Data transfer acknowledge ( $\overline{\mathrm{DTA})}$. See Figure 11 and Figure 12 formultiplexed parallel microporttiming.

For the Motorola non-multiplexed bus, the required signals are the 16-bit data bus (AD0-AD7, D8-D15), 8-bit address bus (A0-A7) and 4 control lines ( $\overline{\mathrm{CS}}, \mathrm{DS}, \mathrm{R} / \overline{\mathrm{W}}$ and $\overline{\mathrm{DTA}}$ ). See Figure 13 and 14 for Motorola non-multiplexed microportiming.

The IDT72V70200 microport provides access to the internal registers, connection and data memories. All locations provide read/write access except for the data memory and the frame alignment register which are read only.

## MEMORY MAPPING

The address bus on the microprocessor interface selects the internal registers and memories of the IDT72V70200.

If the A7 address input is low, then A6 through A0 are used to address the interface mode selection(IMS), control(CR), framealignment(FAR) and frame input offset(FOR) registers(Table4). If the A7 is high, A6 and A5 are low, then A4 through A0 are used to select 32 locations corresponding to data rate of the ST-BUS ${ }^{\circledR}$. The address input lines and the stream address bits (STA) of the control register allow access to the entire data and connection memories. The control and IMS registers together control all the major functions of the device, see Figure 3.

As explained in the Serial Data Interface Timing and Switching Configurations sections, after system power-up, the IMS registershould be programmed immediately toestablishthe desired switching configuration.

The data in the control register consists ofthe memory block programming bit(MBP), the memory selectbit(MS) and the stream address bits (STA). As explained in the Memory Block Programming section, the MBP bitallows the entire connection memory block to be programmed. The memory select bitis used to designate the connection memory or the data Memory. The stream address bits selectinternal memory subsections corresponding toinputoroutput serial streams.

The data in the IMS register consists of block programming bits (BPDOBPD4), block programming enablebit(BPE), outputstand bybit(OSB) and start frameevaluation bit(SFE). Theblock programming and the block programming enablebitsallows usersto programtheentire connection memory (seeMemory Block Programming section). Ifthe ODE pinislow, the OSB bitenables(ifhigh) ordisables(iflow) all ST-BUS ${ }^{\text {® }}$ outputdrivers. IftheODE pin ishigh, the contents of the OSB bit is ignored and all TX output drivers are enabled.

## CONNECTION MEMORY CONTROL

The CCO pin is a $4.096 \mathrm{Mb} /$ s output, which carries 512 bits. The contents of the CCO bit of each connection memory location are output on the CCO pin once every frame. The contents of theCCO bits of the connection memory are transmitted sequentially on to the CCO pin and are synchronous with the data rates on the other serial streams.

The CCO bit is output one channel before the corresponding channel on the serial streams. Forexample, the contents of the CCO bitin position 0 (TXO, CHO ) of the connection memory is output on the first clock cycle of channel 31 through CCO pin. The contents of theCCO bitin position 32(TX1,CH0) of the connection memory is outputon the second clock cycle of channel 31 viaCCO pin.

IftheODE pin or the OSB bitis high, the OE bit of each connection memory location controls the output drivers-enables (if high) or disables (iflow). See Table 4 for detail.

The processor channel(PC) bitof the connection memory selects between ProcessorMode and Connection Mode. Ifhigh, the contents ofthe connection memory are output on the TX streams. Iflow, the stream address bit(SAB) and the channel address bit (CAB) of the connection memory defines the source
information(streamandchannel) ofthe time-slotthatwill be switched totheoutput from datamemory.

The $\bar{V} / C$ (Variable/ConstantDelay) bitineach connectionmemory location allows the per-channel selection between variable and constant throughput delay modes.

If the LPBK bit is high, the associated TX output channel data is internally looped back to the RXinputchannel (i.e., RXnchannel m data comes from the TX $n$ channel $m$ ). If the LPBK bit is low, the loopback feature is disabled. For proper per-channel loopback operation, the contents ofthe frame delay offset registers mustbe settozero.

## INITIALIZATION OF THE IDT72V70200

After power up, the state of the connection memory is unknown. As such, the outputs should be putinhigh impedance by holding the ODE low. While the ODE is low, the microprocessor can initialize the device, program the active paths, and disable unused outputs by programming the OE bit in connection memory. Once the device is configured, the ODE pin (or OSB bit depending on initialization) can be switched.

The Control Register is only accessed when A7-A0 are all zeroed. When $\mathrm{A} 7=1$, up to 32 bytes are randomly accessable via A0-A4 at any one instant. Of which stream these bytes (channels) are accessed is determined by the state of CRb3-CRb0.



Figure 3. Addressing Internal Memories

## TABLE 1 -VARIABLE THROUGHPUT

 DELAY VALUE| Input Rate | Delay for Variable Throughput Delay Mode <br> $(m-$ output channel number) <br> $(n-$ input channel number) |  |  |
| :---: | :---: | :---: | :---: |
|  | $m<n$ | $m=n, n+1, n+2$ | $m>n+2$ |
|  | $32-(n-m)$ time-slots | $m-n+32$ time-slots | $m-n$ time-slots |

TABLE 2 -CONSTANT THROUGHPUT DELAY VALUE

| Input Rate | Delay for Constant Throughput Delay Mode <br> $(\mathrm{m}-$ output channel number) <br> $(\mathrm{n}-$ input channel number) |
| :---: | :---: |
| $2.048 \mathrm{Mb} / \mathrm{s}$ | $32+(32-\mathrm{n})+\mathrm{m}$ time-slots |

TABLE 3 -INTERNAL REGISTER AND ADDRESS MEMORY MAPPING

| A7 ${ }^{(1)}$ | A6 | A5 | A4 | A3 | A2 | A1 | A0 | Location |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Control Register, CR |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | InterfaceModeSelection Register, IMS |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | FrameAlignmentRegister, FAR |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | Frame Input OffsetRegister0,FOR0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | Frame Input OffsetRegister 1,FOR1 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | Frame InputOffsetRegister2,FOR2 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | Frame InputOffsetRegister3,FOR3 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Ch0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Ch1 |
| 1 | 0 | 0 | . | . | . | . | . | . |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | Ch30 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | Ch31 |

NOTE:

1. Bit A7 must be high for access to data and connection memory positions. Bit A7 must be low for access to registers.

## TABLE 4 -OUTPUT HIGH IMPEDANCE CONTROL

| OE bit in Connection <br> Memory | ODE pin | OSB bit in IMS <br> Register | TX Output Driver <br> Status |
| :---: | :---: | :---: | :---: |
| 0 | Don'tCare | Don'tCare | Per Channel <br> High-Impedance |
| 1 | 0 | 0 | High-Impedance |
| 1 | 0 | 1 | Enable |
| 1 | 1 | 1 | Enable |
| 1 | 1 | 0 | Enable |

TABLE 5 - CONTROL REGISTER (CR) BITS


TABLE 6 - INTERFACE MODE SELECTION (IMS) REGISTER BITS

| $\begin{array}{ll}\text { Read/Write Address: } & 01 \mathrm{H}, \\ \text { Reset Value: } & 0000 \mathrm{H} .\end{array}$ |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | BPD4 | BPD3 | BPD2 | BPD1 | BPDO | BPE | OSB | SFE | 0 | 0 |
| Bit | Name |  |  |  | Description |  |  |  |  |  |  |  |  |  |  |
| 15-10 | Unused |  |  |  | Must be zero for normal operation. |  |  |  |  |  |  |  |  |  |  |
| 9-5 | BPD4-0 <br> (BlockProgramming Data) |  |  |  | These bits carry the value to be loaded into the connection memory block whenever the memory block programming feature is activated. After the MBP bit in the control register is setto 1 and the BPE bit is set to 1 , the contents of the bits BPD4-0 are loaded into bit 15 and 11 of the connection memory. Bit 10 to bit 0 of the connection memory are set to 0 . |  |  |  |  |  |  |  |  |  |  |
| 4 | BPE <br> (BeginBlock Programming Enable) |  |  |  | A zero to one transition of this bit enables the memory block programming function. The BPE and BPD4-0 bits in the IMS register have to be defined in the same write operation. Once the BPE bit is set HIGH, the device requires two frames to complete the block programming. After the programming function has finished, the BPE bit returns to zero to indicate the operation is completed. When the BPE $=1$, the BPE or MBP can be set to 0 to ensure proper operation. When $B P E=1$, the other bit in the IMS register must not be changed for two frames to ensure proper operation. |  |  |  |  |  |  |  |  |  |  |
| 3 | OSB <br> (OutputStand By) |  |  |  | When ODE $=0$ and $O S B=0$, the output drivers of TX0 to TX15 are in high impedance mode. When $O D E=0$ and $O S B=1$, the output driver of TX0 to TX15 function normally. When ODE $=1$, TX0 to TX15 outputdrivers function normally. |  |  |  |  |  |  |  |  |  |  |
| 2 | SFE <br> (StartFrameEvaluation) |  |  |  | A zero to one transition in this bit starts the frame evaluation procedure. When the CFE bit in the FAR register changes from zero to one, the evaluation procedure stops. To start another fame evaluation cycle, set this bitto zero for at least one frame. |  |  |  |  |  |  |  |  |  |  |
| 1-0 | Unused |  |  |  | Must be zero for normal operation. |  |  |  |  |  |  |  |  |  |  |

TABLE 7 -FRAME ALIGNMENT REGISTER (FAR) BITS



Figure 4. Example for Frame Alignment Measurement

TABLE 8 - FRAME INPUT OFFSET REGISTER (FOR) BITS


NOTE:

1. n denotes an input stream number from 0 to 15 .

TABLE 9 - OFFSET BITS (OFn2, OFn1, OFn0, DLEn) \& FRAME DELAY BITS (FD11,FD2-0)

| InputStream Offset | MeasurementResultfrom Frame Delay Bits |  |  |  | Corresponding OffsetBits |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | FD11 | FD2 | FD1 | FDO | OFn2 | OFn1 | OFn0 | DLEn |
| Noclock period shift(Default) | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| +0.5 clock period shift | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| + 1.0 clock period shift | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| + 1.5 clock period shift | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| +2.0 clock period shift | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| +2.5 clock period shift | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| +3.0 clock period shift | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| +3.5 clock period shift | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| +4.0 clock period shift | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| +4.5 clock period shift | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |



Figure 5. Examples for Input Offset Delay Timing

## TABLE 10 - CONNECTION MEMORY BITS



NOTE:

1. If bit $13(\mathrm{PC})$ of the corresponding connection memory location is 1 (device in processor mode), then these entire 8 bits (SAB0, bits $6-5, \mathrm{CAB} 4-\mathrm{CAB}$ ) are output on the output channel and stream associated with this location.

## J TAG SUPPORT

The IDT72V70200 JTAG interface conforms to the Boundary-Scan standard IEEE-1149.1. This standard specifies a design-for-testability technique called Boundary-Scan Test (BST). The operation of the boundary-scan circuitry is controlled by an external test access port (TAP) Controller.

## TEST ACCESS PORT (TAP)

The Test Access Port (TAP) provides access to the test functions of the IDT72V70200. It consists of three input pins and one output pin.

- Test Clock Input (TCK)

TCK provides the clock for the test logic. The TCK does not interfere with any on-chip clock and thus remainindependent. TheTCK permits shifting oftest data into or out of the Boundary-Scan register cells concurrently with the operation of the device and without interfering with the on-chip logic.
-Test Mode Select Input(TMS)
The logic signals received at the TMS input are interpreted by the TAP Controller to control the test operations. The TMS signals are sampled at the rising edge of the TCK pulse. This pin is internally pulled to Vcc when it is not driven from an external source.

- Test Data Input (TDI)

Serial input data applied to this port is fed either into the instruction register or into a test data register, depending on the sequence previously applied to the TMS input. Both registers are described in a subsequent section. The received input data is sampled at the rising edge of TCK pulses. This pin is internally pulled to Vcc when it is not driven from an external source.
-TestData Output(TDO)
Depending on the sequence previously applied to the TMS input, the contents of either the instruction registeror data register are serially shifted out towards the TDO. The data out of the TDO is clocked on the falling edge of the TCK pulses. When no data is shifted throughthe boundary scan cells, the TDO driver is set to a high impedance state.

- Test Reset (TRST)

Reset the JTAG scan structure. This pin is internally pulled to VCC.

## INSTRUCTION REGISTER

In accordance with the IEEE 1149.1 standard, the IDT72V70200 uses public instructions. The IDT72V70200 JTAG Interface contains a two-bit instruction register. Instructions are serially loaded into the instruction register from the TDI when the TAP Controller is in its shifted-IR state. Subsequently, theinstructions are decodedtoachievetwo basicfunctions: toselectthetestdata register that may operate while the instruction is current, and to define the serial testdataregisterpath, which is used to shift data between TDI and TDO during data register scanning. See Table below for Instruction decoding.

| Value | Instruction | Function |
| :---: | :--- | :--- |
| 000 | EXTEST | SelectBoundary Scan Register |
| 001 | EXTEST | SelectBoundary Scan Register |
| 010 | Sample/preload | SelectBoundary Scan Register |
| 011 | Sample/preload | SelectBoundary Scan Register |
| 100 | Sample/preload | SelectBoundary Scan Register |
| 101 | Sample/preload | SelectBoundary Scan Register |
| 110 | Bypass | SelectBypass Register |
| 111 | Bypass | SelectBypass Register |

JTAG Instruction Register Decoding

## TESTDATAREGISTER

As specified in IEEE 1149.1, the IDT72V70200 JTAG Interface contains two testdata registers:
-The Boundary-Scan register
The Boundary-Scan register consists of a series of Boundary-Scan cells arranged to form a scan path around the boundary of the IDT72V70200 core logic.
-The Bypass Register
The Bypass register is a single stage shift register that provides a one-bit path from TDI to its TDO. The IDT72V70200 boundary scan register contains 118 bits. Bit 0 in Table 11 Boundary Scan Register is the first bit clocked out. All three-state enable bits are active high.

TABLE 11 - BOUNDARY SCAN REGISTER BITS

| Device Pin | Boundary Scan Bit 0 to bit 117 |  |  |
| :---: | :---: | :---: | :---: |
|  | Three-State Control | Output Scan Cell | Input <br> Scan Cell |
| TX7 | 0 | 1 |  |
| TX6 | 2 | 3 |  |
| TX5 | 4 | 5 |  |
| TX4 | 6 | 7 |  |
| TX3 | 8 | 9 |  |
| TX2 | 10 | 11 |  |
| TX1 | 12 | 13 |  |
| TX0 | 14 | 15 |  |
| ODE |  |  | 16 |
| CCO | 17 | 18 |  |
| $\overline{\text { DTA }}$ |  | 19 |  |
| D15 | 20 | 21 | 22 |
| D14 | 23 | 24 | 25 |
| D13 | 26 | 27 | 28 |
| D12 | 29 | 30 | 31 |
| D11 | 32 | 33 | 34 |
| D10 | 35 | 36 | 37 |
| D9 | 38 | 39 | 40 |
| D8 | 41 | 42 | 43 |
| AD7 | 44 | 45 | 46 |
| AD6 | 47 | 48 | 49 |
| AD5 | 50 | 51 | 52 |
| AD4 | 53 | 54 | 55 |
| AD3 | 56 | 57 | 58 |
| AD2 | 59 | 60 | 61 |
| AD1 | 62 | 63 | 64 |
| AD0 | 65 | 66 | 67 |
| IM |  |  | 68 |
| AD/ALE |  |  | 69 |
| $\overline{\mathrm{CS}}$ |  |  | 70 |
| $\mathrm{R} / \overline{\mathrm{W}} / \overline{\mathrm{WR}}$ |  |  | 71 |
| DS/ $\overline{R D}$ |  |  | 72 |
| A7 |  |  | 73 |
| A6 |  |  | 74 |
| A5 |  |  | 75 |


| Device Pin | Boundary Scan Bit 0 to bit 117 |  |  |
| :---: | :---: | :---: | :---: |
|  | Three-State Control | Output Scan Cell | Input Scan Cell |
| A4 |  |  | 76 |
| A3 |  |  | 77 |
| A2 |  |  | 78 |
| A1 |  |  | 79 |
| A0 |  |  | 80 |
| IC |  |  | 81 |
| $\overline{\text { RESET }}$ |  |  | 82 |
| CLK |  |  | 83 |
| FE |  |  | 84 |
| $\overline{\mathrm{F} 0}$ |  |  | 85 |
| RX15 |  |  | 86 |
| RX14 |  |  | 87 |
| RX13 |  |  | 88 |
| RX12 |  |  | 89 |
| RX11 |  |  | 90 |
| RX10 |  |  | 91 |
| RX9 |  |  | 92 |
| RX8 |  |  | 93 |
| RX7 |  |  | 94 |
| RX6 |  |  | 95 |
| RX5 |  |  | 96 |
| RX4 |  |  | 97 |
| RX3 |  |  | 98 |
| RX2 |  |  | 99 |
| RX1 |  |  | 100 |
| RX0 |  |  | 101 |
| TX15 | 102 | 103 |  |
| TX14 | 104 | 105 |  |
| TX13 | 106 | 107 |  |
| TX12 | 108 | 109 |  |
| TX11 | 110 | 111 |  |
| TX10 | 112 | 113 |  |
| TX9 | 114 | 115 |  |
| TX8 | 116 | 117 |  |

## ABSOLUTE MAXIMUM RATINGS ${ }^{(1)}$

| Symbol | Parameter | Min. | Max. | Unit |
| :---: | :--- | :---: | :---: | :---: |
| Vcc | Supply Voltage | -0.3 | 5.0 | V |
| Vi | Voltageon Digital Inputs | $\mathrm{GND}-0.3$ | 5.5 | V |
| IO | CurrentatDigital Outputs |  | 20 | mA |
| Ts | Storage Temperature | -65 | +125 | ${ }^{\circ} \mathrm{C}$ |
| PD | Package PowerDissapation | - | 1 | W |

NOTE:

1. Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

## RECOMMENDEDDC OPERATING CONDITIONS

| Symbol | Parameter | Min. | Typ. | Max. | Units |
| :---: | :--- | :---: | :---: | :---: | :---: |
| Vcc | Positive Supply | 3.0 | - | 3.6 | V |
| $\mathrm{~V}_{\mathrm{IH}}$ | Input HIGH Voltage (3.3V) | 2.0 | - | Vcc | V |
| $\mathrm{V}_{\mathrm{IH}}$ | Input HIGH Voltage (5.0V) | 2.0 | - | 5.5 | V |
| $\mathrm{~V}_{\mathrm{IL}}$ | InputLOW Voltage | GND | - | 0.8 | V |
| ToP | OperatingTemperature <br> Commercial | -40 | - | +85 | ${ }^{\circ} \mathrm{C}$ |

NOTE:

1. Voltages are with respect to ground unless other wise stated.

DCELECTRICAL CHARACTERISTICS

| Symbol | Characteristics | Min. | Typ. | Max. | Units |
| :---: | :--- | :---: | :---: | :---: | :---: |
| ICc $^{(1)}$ | Supply Current $@ 2.048 \mathrm{Mb} / \mathrm{s}$ | - | 7 | 10 | mA |
| IIL $^{(2)}$ | InputLeakage(inputpins) | - | - | 15 | $\mu \mathrm{~A}$ |
| IBL | InputLeakage(I/Opins) | - | - | 50 | $\mu \mathrm{~A}$ |
| CI | InputPinCapacitance | - | - | 10 | pF |
| Ioz | High-impedanceLeakage | - | - | 5 | $\mu \mathrm{~A}$ |
| VoH | OutputHIGH Voltage | 2.4 | - | - | V |
| VoL | OutputLOWVoltage | - | - | 0.4 | V |
| Co | OutputPinCapacitance | - | - | 10 | pF |

## NOTE:

1. Outputs Unloaded
2. For TDI, TMS, and TRST pins, the maximum leakage current is $50 \mu \mathrm{~A}$.

S1 is open circuitexceptwhen testing output levels or high impedance states.
S2 is switched to Vcc or GND when testing outputlevels orhighimpedance states.


5711 drw09

Figure 6. Output Load

## AC ELECTRICAL CHARACTERISTICS -FRAME PULSE AND CLK

| Symbol | Characteristics | Min. | Typ. | Max. | Units |
| :---: | :---: | :---: | :---: | :---: | :---: |
| tFPW | Frame Pulse Width (ST-BUS ${ }^{\text {® }}$, GCI) ——Bit rate $=2.048 \mathrm{Mb} / \mathrm{s}$ | 26 | - | 295 | ns |
| tFPS | Frame Pulse Setup time before CLK falling (ST-BUS® or GCI) | 5 | - | - | ns |
| tFPH | Frame Pulse Hold Time from CLK falling (ST-BUS ${ }^{\text {® }}$ or GCI) | 10 | - | - | ns |
| tCP | CLK Period - Bit rate $=2.048 \mathrm{Mb} / \mathrm{s}$ | 190 | - | 300 | ns |
| tch | CLK Pulse Width HIGH - Bit rate $=2.048 \mathrm{Mb} / \mathrm{s}$ | 85 | - | 150 | ns |
| tCL | CLK Pulse Width LOW - Bit rate $=2.048 \mathrm{Mb} / \mathrm{s}$ | 85 | - | 150 | ns |
| tr, tf | Clock Rise/Fall Time | - | - | 10 | ns |

AC ELECTRICAL CHARACTERISTICS - SERIAL STREAMS ${ }^{(1)}$

| Symbol | Characteristics | Min. | Typ. | Max. | Unit | Test Conditions |
| :---: | :--- | :---: | :---: | :---: | :---: | :---: |
| tsIS | RXSetup Time | 0 | - | - | ns |  |
| tSIH | RXHold Time | 10 | - | - | ns |  |
| tsod | TX Delay - Active to Active | - | - | 30 | ns | $\mathrm{C}_{\mathrm{L}}=30 \mathrm{pF}$ |
|  |  | - | - | 40 | ns | $\mathrm{C}_{\mathrm{L}}=200 \mathrm{pF}$ |
| tDZ | TXDelay-Active to High-Z | - | - | 32 | ns | $\mathrm{R}_{\mathrm{L}}=1 \mathrm{~K} \Omega, \mathrm{C}_{\mathrm{L}}=200 \mathrm{pF}$ |
| tZD | TX Delay -High-Z to Active | - | - | 32 | ns | $\mathrm{R}_{\mathrm{L}}=1 \mathrm{~K} \Omega, \mathrm{C}_{\mathrm{L}}=200 \mathrm{pF}$ |
| toDE | Output Driver Enable (ODE) Delay | - | - | 32 | ns | $\mathrm{R}_{\mathrm{L}}=1 \mathrm{~K} \Omega, \mathrm{C}_{\mathrm{L}}=200 \mathrm{pF}$ |
| txCD | CCO Output Delay | - | - | 30 | ns | $\mathrm{C}_{\mathrm{L}}=30 \mathrm{pF}$ |
|  |  | - | - | 40 | ns | $\mathrm{C}_{\mathrm{L}}=200 \mathrm{pF}$ |

NOTE:

1. High Impedance is measured by pulling to the appropriate rail with $R_{L}$, with timing corrected to cancel time taken to discharge $C_{L}$.


NOTE:
Figure 7. ST-BUS ${ }^{\circledR}$ Timing

1. last channel $=\operatorname{ch} 31$.


NOTE:
Figure 8. GCI Timing

1. last channel $=\operatorname{ch} 31$.


Figure 9. Serial Output and External Control


Figure 10. Output Driver Enable (ODE)

## AC ELECTRICAL CHARACTERISTICS - MULTIPLEXED BUS TIMING (INTEL)

| Symbol | Parameter | Min. | Typ. | Max. | Units | Test Conditions |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| taLw | ALE Pulse Width | 20 |  |  | ns |  |
| tADS | Address Setup fromALE falling | 3 |  |  | ns |  |
| tadH | Address Hold from ALE falling | 3 |  |  | ns |  |
| tALRD | $\overline{\mathrm{RD}}$ Active after ALE falling | 3 |  |  | ns |  |
| to R | Data Setup from DTAALOW on Read | 5 |  |  | ns | $\mathrm{CL}=150 \mathrm{pF}$ |
| tCSRW | $\overline{\text { CS }}$ Hold after $\overline{\mathrm{RD}} / \overline{\mathrm{WR}}$ | 5 |  |  | ns |  |
| tRW | $\overline{\mathrm{RD}}$ Pulse Width (Fast Read) | 45 |  |  | ns |  |
| tCSR | $\overline{\mathrm{CS}}$ Setup from $\overline{\mathrm{RD}}$ | 0 |  |  | ns |  |
| tDHR ${ }^{(1)}$ | Data Hold after $\overline{\mathrm{RD}}$ | 10 |  | 20 | ns | $\mathrm{CL}_{\mathrm{L}}=150 \mathrm{pF}, \mathrm{RL}=1 \mathrm{~K}$ |
| twn | WRPulse Width (FastWrite) | 45 |  |  | ns |  |
| talwr | WR Delay after ALE falling | 3 |  |  | ns |  |
| tcsw |  | 0 |  |  | ns |  |
| tDSW | DataSetup from $\overline{\mathrm{WR}}$ (FastWrite) | 20 |  |  | ns |  |
| tSWD | Valid Data Delay on Write (Slow Write) |  |  | 122 | ns |  |
| DHW | Data Hold after $\overline{\text { WR }}$ Inactive | 5 |  |  | ns |  |
| takD | AcknowledgmentDelay: <br> Reading/WritingRegisters <br> Reading/Writing Memory |  |  | $\begin{gathered} 43 / 43 \\ 760 / 750 \end{gathered}$ | $\begin{aligned} & \text { ns } \\ & \text { ns } \end{aligned}$ | $\begin{aligned} & C L=150 \mathrm{pF} \\ & C L L=150 \mathrm{pF} \end{aligned}$ |
| takH ${ }^{(1)}$ | Acknowledgment Hold Time |  |  | 22 | ns | $\mathrm{CL}_{\mathrm{L}}=150 \mathrm{pF}, \mathrm{RL}=1 \mathrm{~K}$ |

## NOTE:

1. High Impedance is measured by pulling to the appropriate rail with $R_{l}$, with timing corrected to cancel time taken to discharge $C_{L}$.


Figure 11. Multiplexed Bus Timing (Intel Mode)

## AC ELECTRICAL CHARACTERISTICS -MULTIPLEXED BUS TIMING (MOTOROLA)

| Symbol | Parameter | Min. | Typ. | Max. | Units | Test Conditions |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| tasw | ALE Pulse Width | 20 |  |  | ns |  |
| tads | Address Setup from AS falling | 3 |  |  | ns |  |
| tadH | Address Hold from AS falling | 3 |  |  | ns |  |
| tod | Data Setup from DTA LOW on Read | 5 |  |  | ns | $C L=150 \mathrm{pF}$ |
| tCSH | $\overline{\mathrm{CS}}$ Hold after DS falling | 0 |  |  | ns |  |
| tcss | $\overline{\mathrm{CS}}$ Setup from DS rising | 0 |  |  | ns |  |
| thew | Data Hold afterWrite | 5 |  |  | ns |  |
| tDWS | Data Setup from DS-Write (FastWrite) | 20 |  |  | ns |  |
| tswd | Valid Data Delay on Write (Slow Write) |  |  | 122 | ns |  |
| tRWS | R/W Setup from DS Rising | 60 |  |  | ns |  |
| trWH | R/W Hold from DS Rising | 5 |  |  | ns |  |
| tDHR ${ }^{(1)}$ | Data Hold after Read | 10 |  | 20 | ns | $C_{L}=150 \mathrm{pF}, \mathrm{RL}=1 \mathrm{~K}$ |
| tDSH | DS Delay after AS falling | 10 |  |  | ns |  |
| takD | AcknowledgmentDelay: <br> Reading/Writing Registers <br> Reading/Writing Memory |  |  | $\begin{gathered} 43 / 43 \\ 760 / 750 \end{gathered}$ | $\begin{aligned} & \text { ns } \\ & \text { ns } \end{aligned}$ | $\begin{aligned} & C L=150 \mathrm{pF} \\ & C L=150 \mathrm{pF} \end{aligned}$ |
| tAKH ${ }^{(1)}$ | Acknowledgment Hold Time |  |  | 22 | ns | $C_{L}=150 \mathrm{pF}, \mathrm{RL}=1 \mathrm{~K}$ |

## NOTE:

1. High Impedance is measured by pulling to the appropriate rail with $R_{L}$, with timing corrected to cancel time taken to discharge $C_{L}$.


Figure 12. Multiplexed Bus Timing (Motorola Mode)

## AC ELECTRICAL CHARACTERISTICS-MOTOROLA NON-MULTIPLEXEDBUS MODE

| Symbol | Parameter | Min. | Typ. | Max. | Units | Test Conditions |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| tcss | CS Setup from DS falling | 0 |  |  | ns |  |
| tRWS | R/W Setup from DS falling | 10 |  |  | ns |  |
| tADS | Address Setup from DS falling | 2 |  |  | ns |  |
| tcSH | CS Hold after DS rising | 0 |  |  | ns |  |
| tRWH | R/W Hold after DS Rising | 2 |  |  | ns |  |
| taDH | Address Hold after DS Rising | 2 |  |  | ns |  |
| DDR | Data Setup from DTALOW on Read | 2 |  |  | ns | $\mathrm{CL}_{\mathrm{L}}=150 \mathrm{pF}$ |
| ©HR | Data Hold on Read | 10 |  | 20 | ns | $C L=150 \mathrm{pF}, \mathrm{RL}=1 \mathrm{~K}$ |
| tDSW | Data Setup onWrite (FastWrite) | 0 | - |  | ns |  |
| tswD | Valid Data Delay on Write (Slow Write) |  |  | 122 | ns |  |
| DHW | Data Hold onWrite | 5 |  |  | ns |  |
| takD | AcknowledgmentDelay: <br> Reading/WritingRegisters <br> Reading/WritingMemory |  |  | $\begin{gathered} 43 / 43 \\ 760 / 750 \\ \hline \end{gathered}$ | $\begin{aligned} & \text { ns } \\ & \text { ns } \end{aligned}$ | $\begin{aligned} & C L=150 \mathrm{pF} \\ & C L=150 \mathrm{pF} \end{aligned}$ |
| takH ${ }^{(1)}$ | AcknowledgmentHold Time |  |  | 22 | ns | $C_{L}=150 \mathrm{pF}, \mathrm{RL}=1 \mathrm{~K}$ |

NOTE:

1. High Impedance is measured by pulling to the appropriate rail with $R_{L}$, with timing corrected to cancel time taken to discharge $C_{L}$.


Figure 13. Motorola Non-Multiplexed Asyncrounous Bus Timing


Figure 14. Motorola Non-Multiplexed Syncrounous Bus Timing

## ORDERINGINFORMATION



DATASHEET DOCUMENT HISTORY
$5 / 19 / 2000 \quad$ pgs. 1, 3, 17 and 23 . 12/16/14 Pg 1 and 24 removed JG, BGG and PQFG packages.
8/15/2000
9/22/2000
1/04/2001
1/25/2001
pgs. 1, 2, 3, 5, 12 and 23.
pgs. 3, 12 and 17.
pgs. 6, 11, 17, 19, 20, 21 and 22.
pgs. 17 and 22.
08/06/2001
pgs. 4, 10, 15, and 22.

