



PBL2001D

20 V PNP BISS loadswitch

Rev. 02 — 27 August 2009

Product data sheet

1. Product profile

1.1 General description

PNP low V_{CEsat} Breakthrough in Small Signal (BISS) transistor and NPN Resistor-Equipped Transistor (RET) in a SOT457 (SC-74) small Surface Mounted Device (SMD) plastic package.

1.2 Features

- Low V_{CEsat} (BISS) and resistor-equipped transistor in one package
- Low threshold voltage (< 1 V) compared to MOSFET
- Low drive power required
- Space-saving solution
- Reduction of component count

1.3 Applications

- Supply line switches
- Battery charger switches
- High-side switches for LEDs, drivers and backlights
- Portable equipment

1.4 Quick reference data

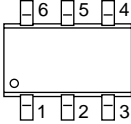
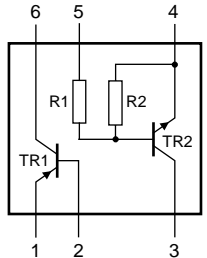
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TR1; PNP low V_{CEsat} transistor						
V_{CEO}	collector-emitter voltage	open base	-	-	-20	V
I_C	collector current (DC)		-	-	-1	A
R_{CEsat}	collector-emitter saturation resistance	$I_C = -1$ A; $I_B = -100$ mA	[1]	185	280	m Ω
TR2; NPN resistor-equipped transistor						
V_{CEO}	collector-emitter voltage	open base	-	-	50	V
I_O	output current		-	-	100	mA
R1	bias resistor 1 (input)		1.54	2.2	2.86	k Ω
R2/R1	bias resistor ratio		0.8	1	1.2	

[1] Pulse test: $t_p \leq 300$ μ s; $\delta \leq 0.02$

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Symbol
1	emitter TR1		
2	base TR1		
3	output (collector) TR2		
4	GND (emitter) TR2		
5	input (base) TR2		
6	collector TR1		

sym036

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PBLS2001D	SC-74	plastic surface mounted package; 6 leads	SOT457

4. Marking

Table 4. Marking codes

Type number	Marking code
PBLS2001D	F6

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

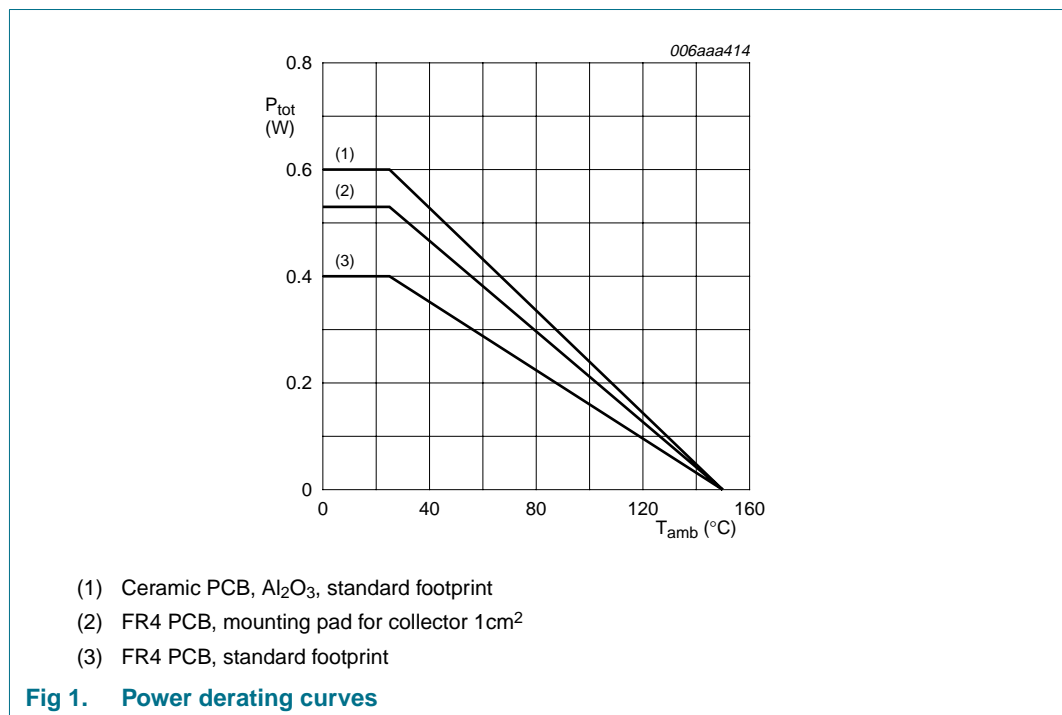
Symbol	Parameter	Conditions	Min	Max	Unit	
TR1; PNP low V_{CEsat} transistor						
V_{CBO}	collector-base voltage	open emitter	-	-20	V	
V_{CEO}	collector-emitter voltage	open base	-	-20	V	
V_{EBO}	emitter-base voltage	open collector	-	-5	V	
I_C	collector current (DC)		-	-1	A	
I_{CM}	peak collector current	$t_p \leq 300 \mu s$	-	-2	A	
I_B	base current (DC)		-	-0.3	A	
I_{BM}	peak base current	$t_p \leq 300 \mu s$	-	-0.6	A	
P_{tot}	total power dissipation	$T_{amb} \leq 25 \text{ }^\circ\text{C}$	[1]	-	250	mW
			[2]	-	350	mW
			[3]	-	400	mW

Table 5. Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
TR2; NPN resistor-equipped transistor					
V_{CBO}	collector-base voltage	open emitter	-	50	V
V_{CEO}	collector-emitter voltage	open base	-	50	V
V_{EBO}	emitter-base voltage	open collector	-	10	V
V_I	input voltage				
	positive		-	+12	V
	negative		-	-10	V
I_O	output current		-	100	mA
I_{CM}	peak collector current	$t_p \leq 300 \mu s$	-	100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25 \text{ }^\circ\text{C}$	[1]	-	200 mW
Per device					
P_{tot}	total power dissipation		[1]	-	400 mW
			[2]	-	530 mW
			[3]	-	600 mW
T_{stg}	storage temperature		-65	+150	$^\circ\text{C}$
T_j	junction temperature		-	150	$^\circ\text{C}$
T_{amb}	ambient temperature		-65	+150	$^\circ\text{C}$

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1cm².
- [3] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.



6. Thermal characteristics

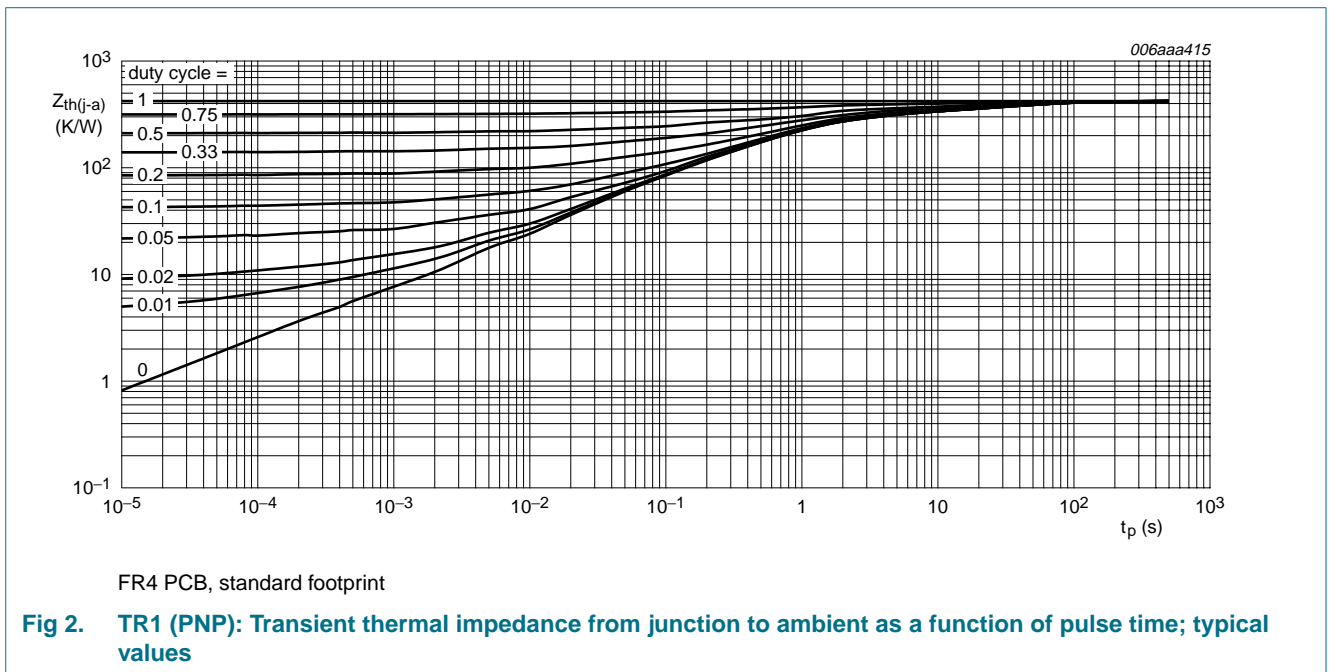
Table 6. Thermal characteristics

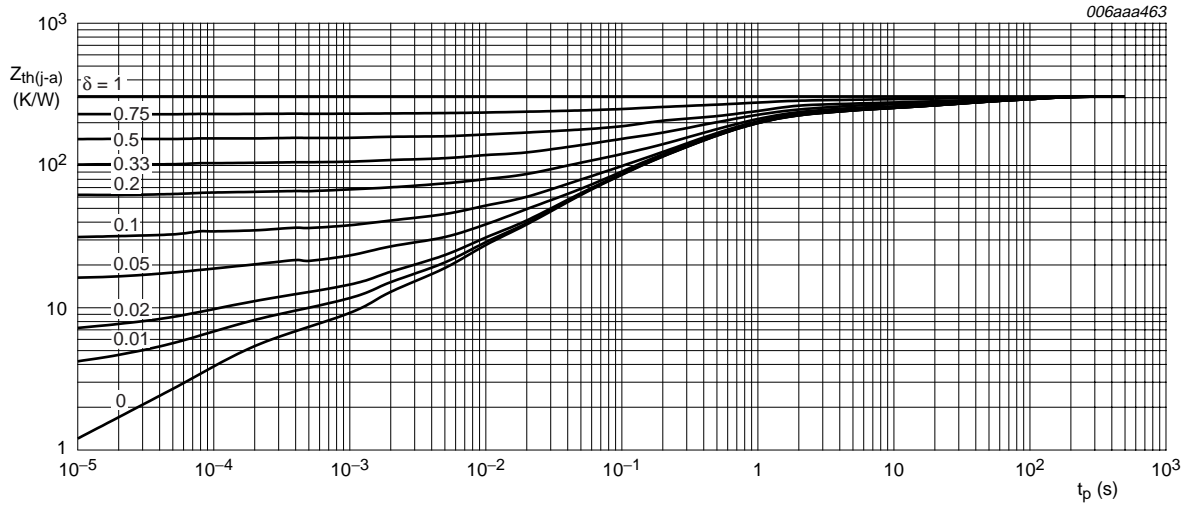
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	315	K/W
			[2]	-	-	236	K/W
			[3]	-	-	210	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm².

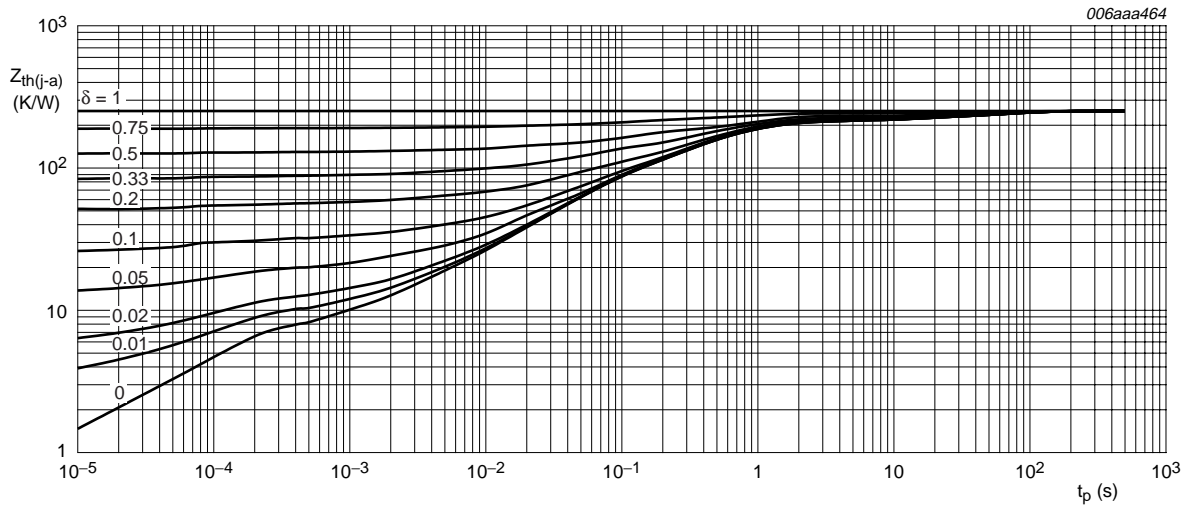
[3] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.





FR4 PCB, mounting pad for collector 1cm²

Fig 3. TR1 (PNP): Transient thermal impedance from junction to ambient as a function of pulse time; typical values



Ceramic PCB, Al₂O₃, standard footprint

Fig 4. TR1 (PNP): Transient thermal impedance from junction to ambient as a function of pulse time; typical values

7. Characteristics

Table 7. Characteristics

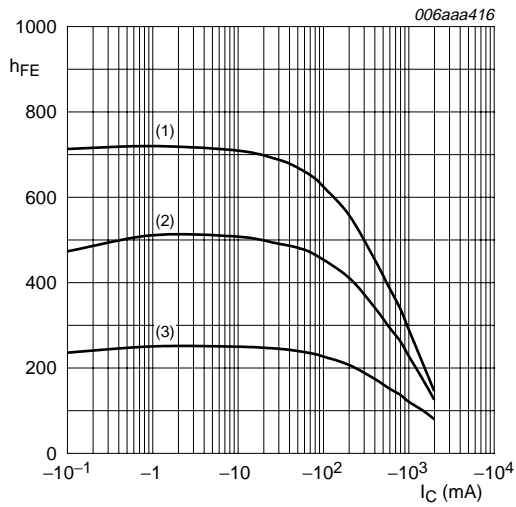
$T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TR1; PNP low V_{CEsat} transistor						
I_{CBO}	collector-base cut-off current	$V_{CB} = -20\text{ V}; I_E = 0\text{ A}$	-	-	-0.1	μA
		$V_{CB} = -20\text{ V}; I_E = 0\text{ A}; T_j = 150\text{ }^{\circ}\text{C}$	-	-	-50	μA
I_{CES}	collector-emitter cut-off current	$V_{CE} = -20\text{ V}; V_{BE} = 0\text{ V}$	-	-	-0.1	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = -5\text{ V}; I_C = 0\text{ A}$	-	-	-0.1	μA
h_{FE}	DC current gain	$V_{CE} = -2\text{ V}; I_C = -1\text{ mA}$	220	495	-	
		$V_{CE} = -2\text{ V}; I_C = -100\text{ mA}$	220	440	-	
		$V_{CE} = -2\text{ V}; I_C = -500\text{ mA}$	[1] 220	310	-	
		$V_{CE} = -2\text{ V}; I_C = -1\text{ A}$	[1] 155	220	-	
		$V_{CE} = -2\text{ V}; I_C = -2\text{ A}$	[1] 60	120	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = -100\text{ mA}; I_B = -1\text{ mA}$	-	-55	-90	mV
		$I_C = -500\text{ mA}; I_B = -50\text{ mA}$	[1] -	-100	-150	mV
		$I_C = -1\text{ A}; I_B = -50\text{ mA}$	[1] -	-200	-300	mV
		$I_C = -1\text{ A}; I_B = -100\text{ mA}$	[1] -	-185	-280	mV
R_{CEsat}	collector-emitter saturation resistance	$I_C = -1\text{ A}; I_B = -100\text{ mA}$	[1] -	185	280	m Ω
V_{BEsat}	base-emitter saturation voltage	$I_C = -1\text{ A}; I_B = -50\text{ mA}$	[1] -	-0.95	-1.1	V
		$I_C = -1\text{ A}; I_B = -100\text{ mA}$	[1] -	-1	-1.1	V
V_{BEon}	base-emitter turn-on voltage	$V_{CE} = -5\text{ V}; I_C = -1\text{ A}$	[1] -	-0.85	-1.1	V
t_d	delay time	$I_C = -1\text{ A}; I_{Bon} = -50\text{ mA}; I_{Boff} = 50\text{ mA}$	-	8	-	ns
t_r	rise time		-	34	-	ns
t_{on}	turn-on time		-	42	-	ns
t_s	storage time		-	140	-	ns
t_f	fall time		-	45	-	ns
t_{off}	turn-off time		-	185	-	ns
f_T	transition frequency	$I_C = -50\text{ mA}; V_{CE} = -10\text{ V}; f = 100\text{ MHz}$	150	185	-	MHz
C_c	collector capacitance	$V_{CB} = -10\text{ V}; I_E = I_e = 0\text{ A}; f = 1\text{ MHz}$	-	15	20	pF

Table 7. Characteristics ...continued
 $T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

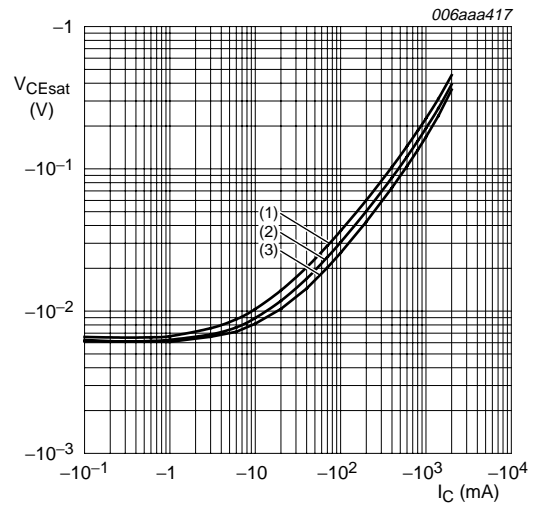
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TR2; NPN resistor-equipped transistor						
I_{CBO}	collector-base cut-off current	$V_{CB} = 50\text{ V}; I_E = 0\text{ A}$	-	-	100	nA
I_{CEO}	collector-emitter cut-off current	$V_{CE} = 30\text{ V}; I_B = 0\text{ A}$	-	-	1	μA
		$V_{CE} = 30\text{ V}; I_B = 0\text{ A}; T_j = 150\text{ }^{\circ}\text{C}$	-	-	50	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5\text{ V}; I_C = 0\text{ A}$	-	-	2	mA
h_{FE}	DC current gain	$V_{CE} = 5\text{ V}; I_C = 20\text{ mA}$	30	-	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 10\text{ mA}; I_B = 0.5\text{ mA}$	-	-	150	mV
$V_{I(off)}$	off-state input voltage	$V_{CE} = 5\text{ V}; I_C = 1\text{ mA}$	-	1.2	0.5	V
$V_{I(on)}$	on-state input voltage	$V_{CE} = 0.3\text{ V}; I_C = 20\text{ mA}$	2	1.6	-	V
R1	bias resistor 1 (input)		1.54	2.2	2.86	k Ω
R2/R1	bias resistor ratio		0.8	1	1.2	
C_c	collector capacitance	$V_{CB} = 10\text{ V}; I_E = i_e = 0\text{ A}; f = 1\text{ MHz}$	-	-	2.5	pF

[1] Pulse test: $t_p \leq 300\text{ }\mu\text{s}; \delta \leq 0.02$



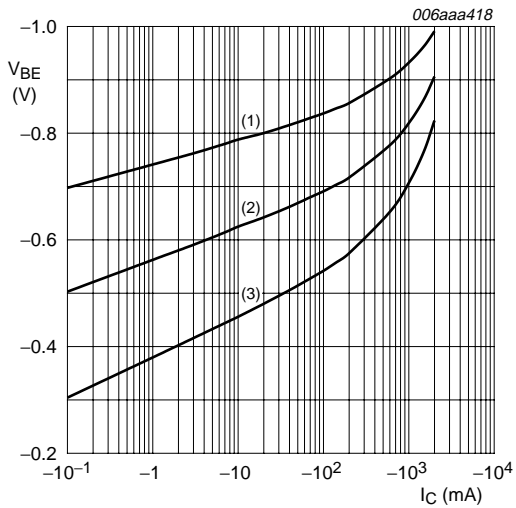
$V_{CE} = -2 \text{ V}$
 (1) $T_{amb} = 100 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = -55 \text{ }^\circ\text{C}$

Fig 5. TR1 (PNP): DC current gain as a function of collector current; typical values



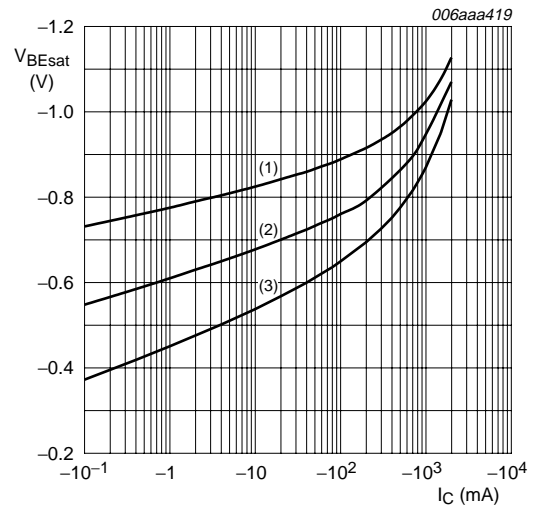
$I_C/I_B = 20$
 (1) $T_{amb} = 100 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = -55 \text{ }^\circ\text{C}$

Fig 6. TR1 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



$V_{CE} = -5 \text{ V}$
 (1) $T_{amb} = -55 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = 100 \text{ }^\circ\text{C}$

Fig 7. TR1 (PNP): Base-emitter voltage as a function of collector current; typical values



$I_C/I_B = 20$
 (1) $T_{amb} = -55 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = 100 \text{ }^\circ\text{C}$

Fig 8. TR1 (PNP): Base-emitter saturation voltage as a function of collector current; typical values

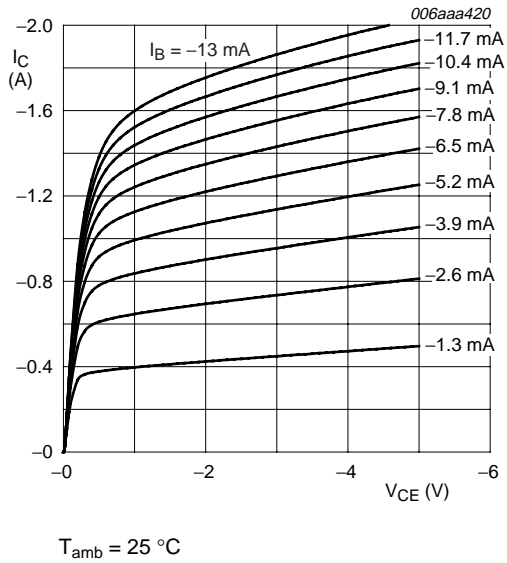


Fig 9. TR1 (PNP): Collector current as a function of collector-emitter voltage; typical values

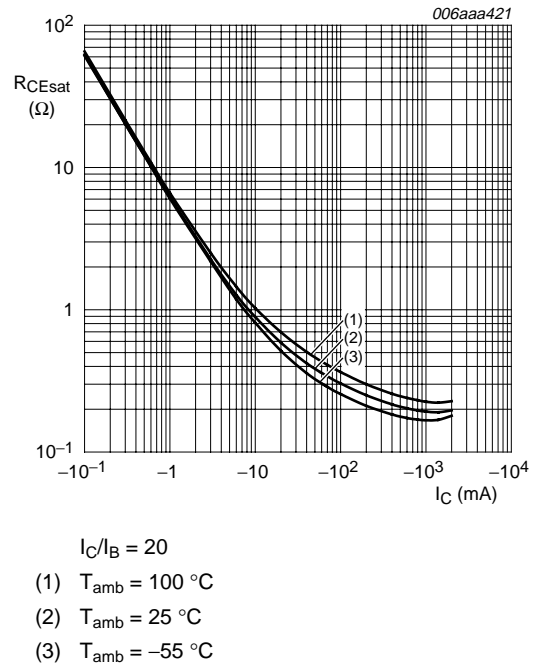


Fig 10. TR1 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values

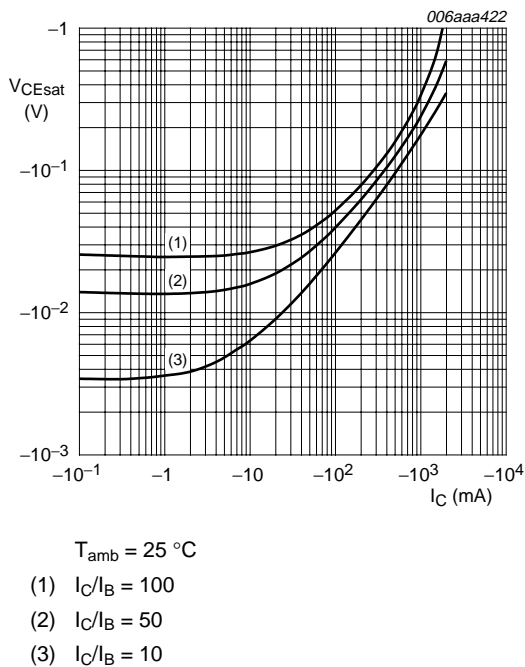


Fig 11. TR1 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values

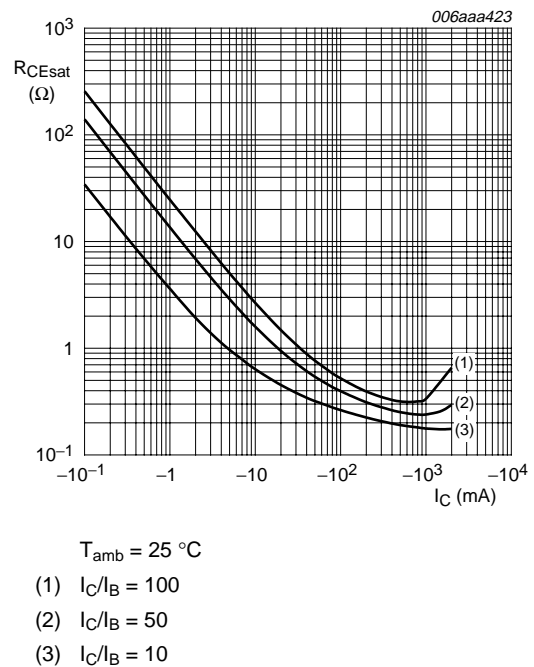
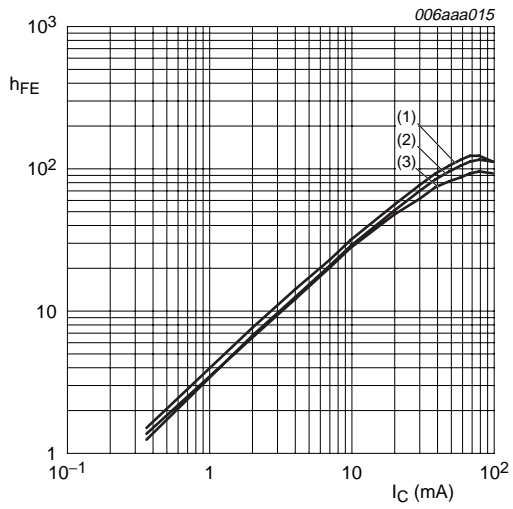
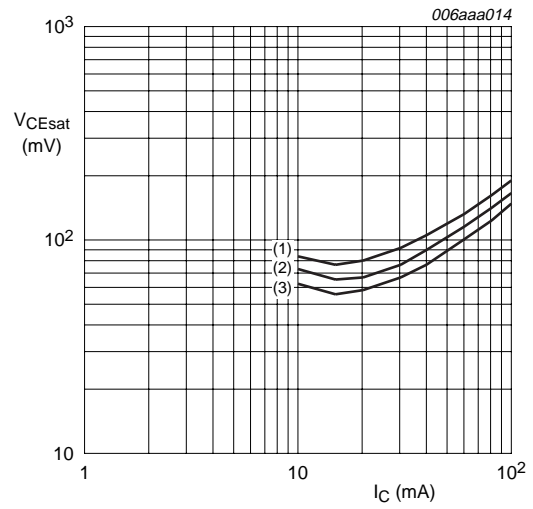


Fig 12. TR1 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values



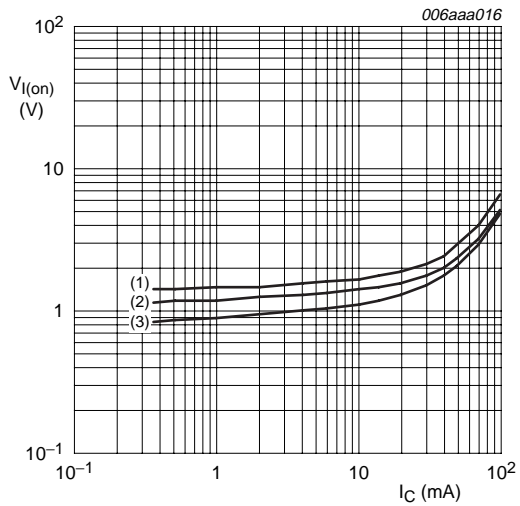
$V_{CE} = 5 \text{ V}$
 (1) $T_{amb} = 150 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = -40 \text{ }^\circ\text{C}$

Fig 13. TR2 (NPN): DC current gain as a function of collector current; typical values



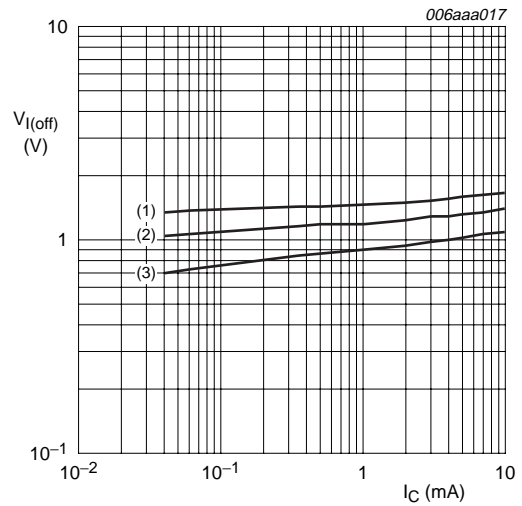
$I_C/I_B = 20$
 (1) $T_{amb} = 100 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = -40 \text{ }^\circ\text{C}$

Fig 14. TR2 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values



$V_{CE} = 0.3 \text{ V}$
 (1) $T_{amb} = -40 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = 100 \text{ }^\circ\text{C}$

Fig 15. TR2 (NPN): On-state input voltage as a function of collector current; typical values



$V_{CE} = 5 \text{ V}$
 (1) $T_{amb} = -40 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = 100 \text{ }^\circ\text{C}$

Fig 16. TR2 (NPN): Off-state input voltage as a function of collector current; typical values

8. Test information

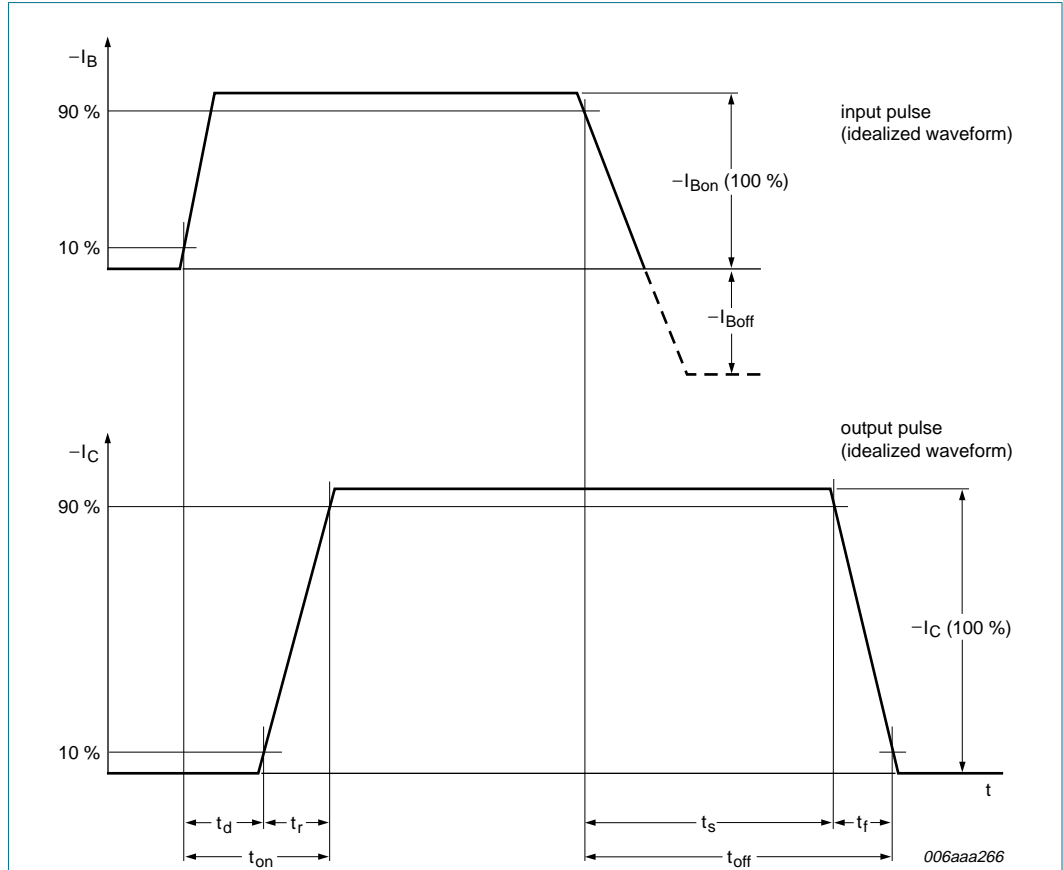
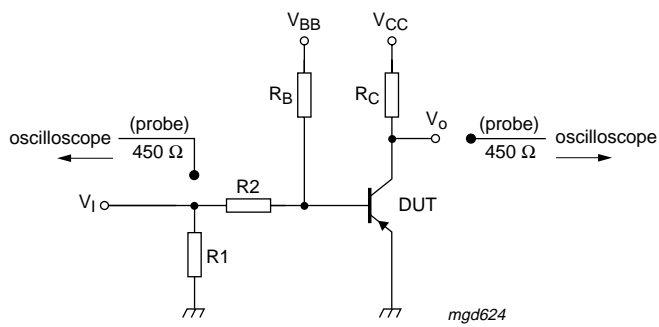


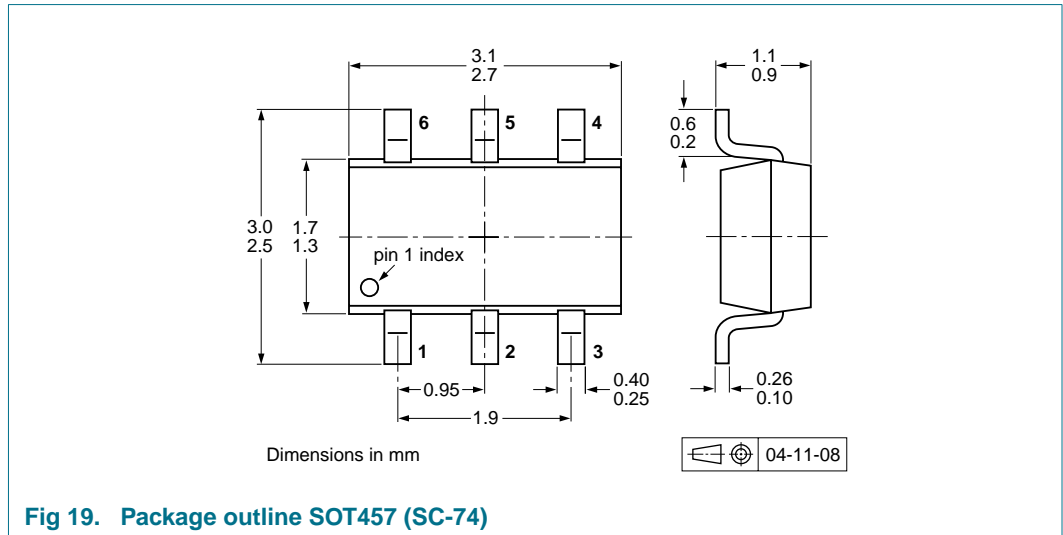
Fig 17. BISS transistor switching time definition



$I_C = -1$ A; $I_{Bon} = -50$ mA; $I_{Boff} = 50$ mA; $R_1 =$ open; $R_2 = 45$ Ω ; $R_B = 145$ Ω ; $R_C = 10$ Ω

Fig 18. Test circuit for switching times

9. Package outline



10. Packing information

Table 8. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.^[1]

Type number	Package	Description	Packing quantity	
			3000	10000
PBLS2001D	SOT457	4 mm pitch, 8 mm tape and reel; T1	^[2] -115	-135
		4 mm pitch, 8 mm tape and reel; T2	^[3] -125	-165

[1] For further information and the availability of packing methods, see [Section 14](#).

[2] T1: normal taping

[3] T2: reverse taping

11. Soldering

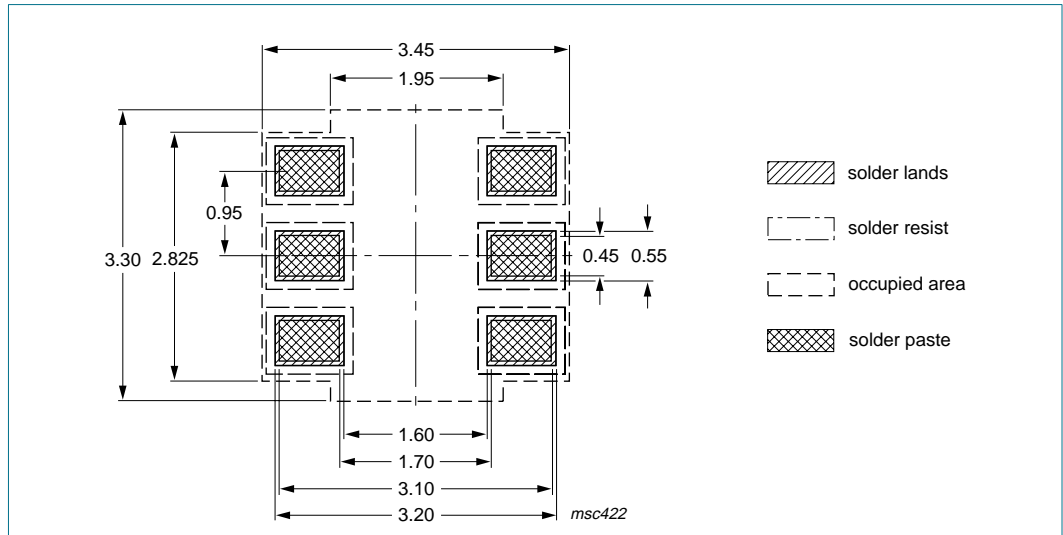


Fig 20. Reflow soldering footprint

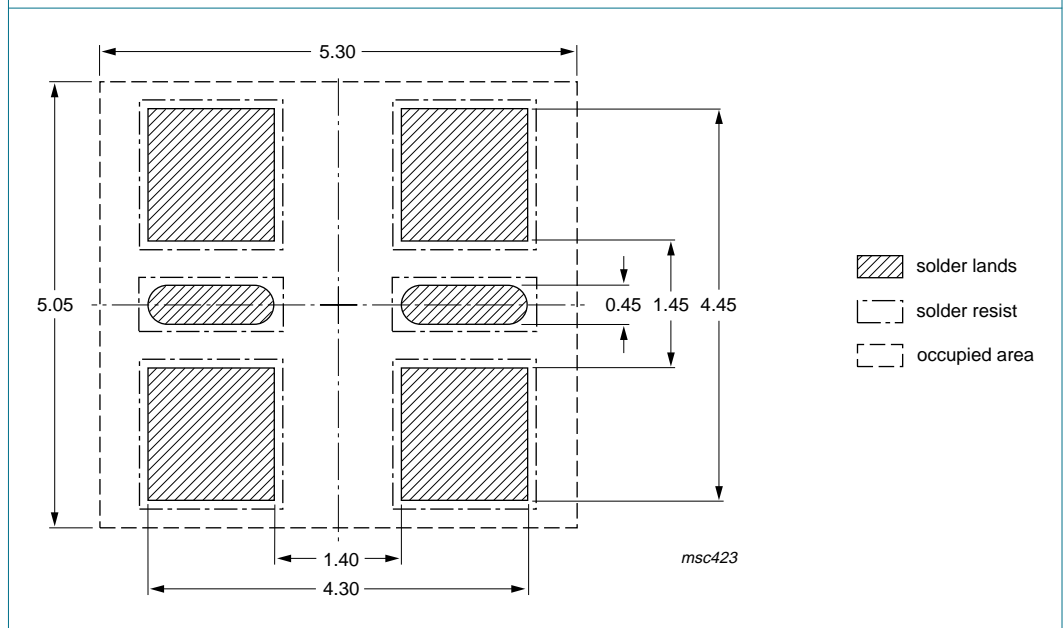


Fig 21. Wave soldering footprint

12. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PBL2001D_2	20090827	Product data sheet	-	PBL2001D_1
Modifications:	<ul style="list-style-type: none">• This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content.• Figure 21 "Wave soldering footprint": updated			
PBL2001D_1	20050705	Product data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

13.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

13.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental

damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

13.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

14. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

15. Contents

1	Product profile	1
1.1	General description	1
1.2	Features	1
1.3	Applications	1
1.4	Quick reference data	1
2	Pinning information	2
3	Ordering information	2
4	Marking	2
5	Limiting values	2
6	Thermal characteristics	4
7	Characteristics	6
8	Test information	11
9	Package outline	12
10	Packing information	12
11	Soldering	13
12	Revision history	14
13	Legal information	15
13.1	Data sheet status	15
13.2	Definitions	15
13.3	Disclaimers	15
13.4	Trademarks	15
14	Contact information	15
15	Contents	16

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.



© NXP B.V. 2009.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 27 August 2009

Document identifier: PBLS2001D_2