

## Automotive integrated H-bridge

### Features

Type	$R_{DS(on)}$	$I_{out}$	$V_{CCmax}$
VNH7013XP-E	13 m $\Omega$ typ (per leg)	40 A	72 V <sup>(1)</sup>

1. Per leg: sum of the two  $BV_{dss}$  (HSD + LSD);  
 $V_{CC} > 36$  V whole bridge must be switched off;

- Maximum  $V_{CC}$  voltage: 72 V
- 10 V compatible inputs
- $R_{DS(on)}$  per leg: 13 m $\Omega$  typical
- Embedded thermal sensor: -8.1 mV/ $^{\circ}$ K
- Very low stray inductance in power line



### Description

The VNH7013XP-E is an automotive integrated H-bridge intended for a wide range of automotive applications driving DC motors. The device incorporates a dual channel and two single channel MOSFETs. All the devices are designed using STMicroelectronics<sup>®</sup> well known and proven proprietary VIPower<sup>®</sup> M0-S7 technology that allows to integrate in a package four different channels in H-bridge topology.

This package, specifically designed for the harsh automotive environment offers improved thermal performance thanks to exposed die pads. Moreover, its fully symmetrical mechanical design allows superior manufacturability at board level.

**Table 1. Device summary**

Package	Order codes	
	Tube	Tape and reel
PowerSSO-36 TP	VNH7013XP-E	VNH7013XPTR-E

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# 1 Block diagram and pin description

Figure 1. Block diagram

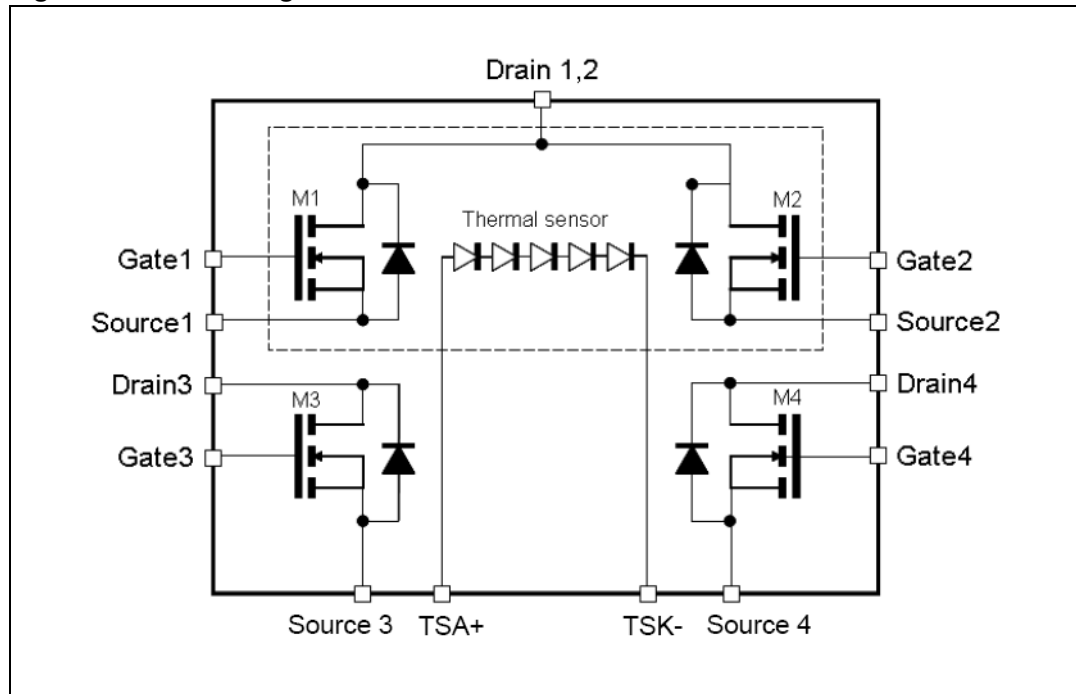
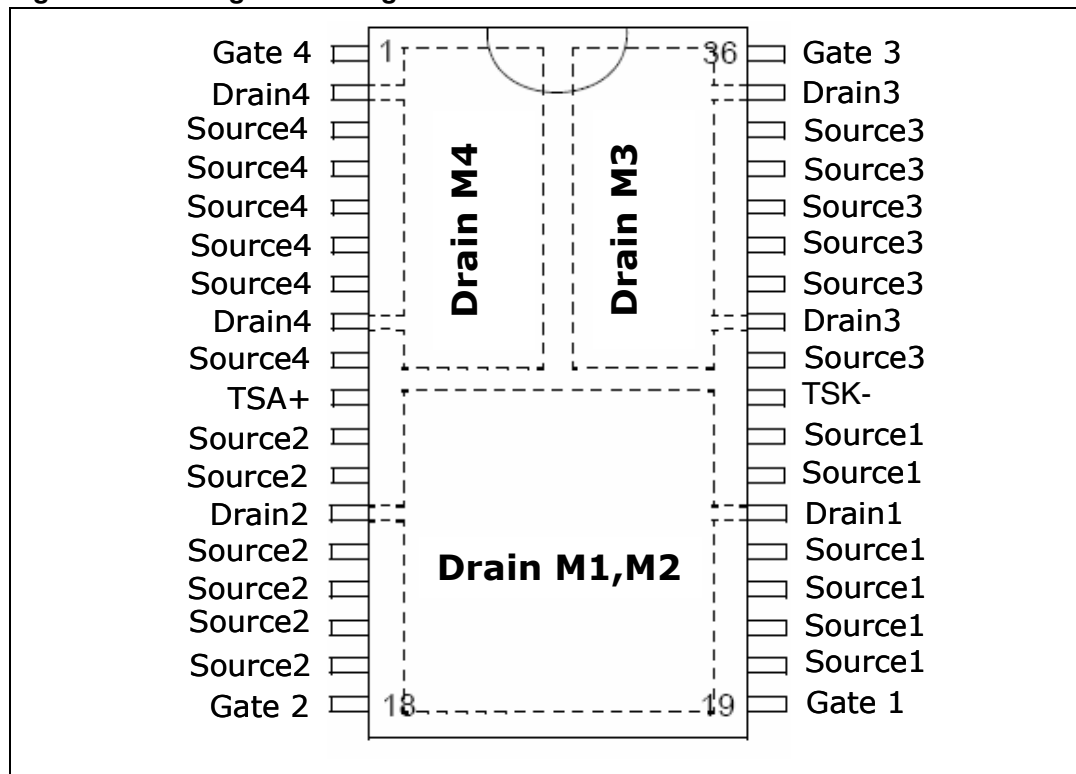


Figure 2. Configuration diagram



**Table 2. Pin definitions and functions**

Pin number	Symbol	Function
1	Gate 4	Gate of the LSD 4
2, 8	Drain 4	Drain of the LSD 4
3, 4, 5, 6, 7, 9	Source 4	Source of the LSD 4
10	TSA+	Thermal sensor anode
11, 12, 14, 15, 16, 17	Source 2	Source of the HSD 2
13	Drain 2	Drain of the HSD 2
18	Gate 2	Gate of the HSD 2
19	Gate 1	Gate of the HSD 1
20, 21, 22, 23, 25, 26	Source 1	Source of the HSD 1
24	Drain 1	Drain of the HSD 1
27	TSK-	Thermal sensor cathode
28, 30, 31, 32, 33, 34	Source 3	Source of the LSD 3
29, 35	Drain 3	Drain of the LSD 3
36	Gate 3	Gate of the LSD 3

## 2 Electrical specifications

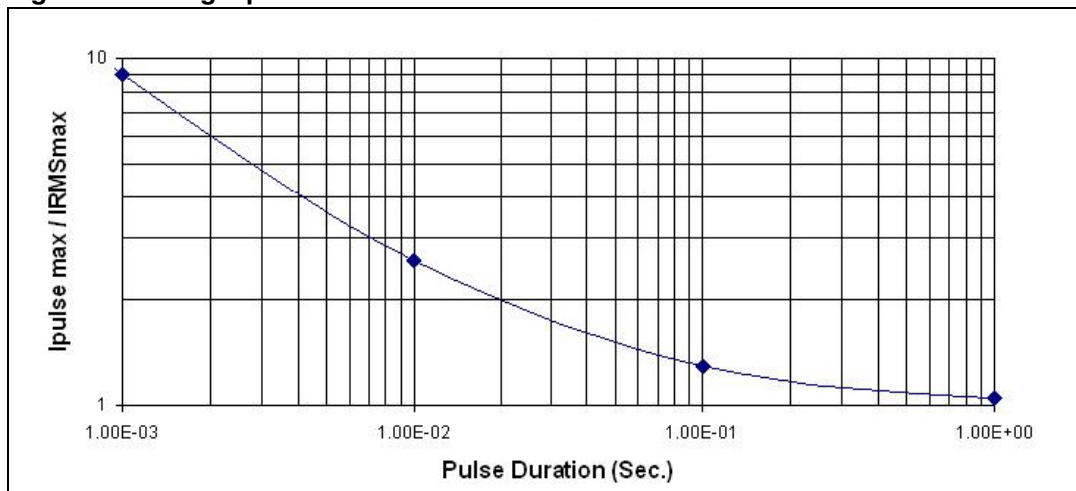
### 2.1 Absolute maximum rating

Table 3. Absolute maximum rating

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply voltage (whole bridge switched off)	72	V
I <sub>max</sub>	Maximum output current (continuous)	40	A
V <sub>GS_max</sub>	Maximum gate source voltage	18	V
I <sub>pulse_max</sub>	Maximum Single Pulse output current	80 <sup>(1)</sup>	A
T <sub>j</sub>	Junction operating temperature	175	°C
T <sub>c</sub>	Case operating temperature	-40 to 150	°C
T <sub>STG</sub>	Storage temperature	-55 to 150	°C
I <sub>S</sub>	Diode continuous forward current	40	A

1. Pulse duration = 20 ms (see [Figure 3](#)).

Figure 3. Single pulse maximum current



## 2.2 Electrical characteristics

$T_j = 25\text{ °C}$ , unless otherwise specified.

**Table 4. Power off**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 10\text{ mA}$ , $V_{GS} = 0\text{ V}$	36	—		V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS}=0V$ )	$V_{DS} = 28\text{ V}$ ; $-40\text{ °C} < T_j < 150\text{ °C}$		—	100	$\mu\text{A}$
		$V_{DS} = 28\text{ V}$ ; $T_j = 25\text{ °C}$		—	10	$\mu\text{A}$
$I_{GSS}$	Gate-source leakage current ( $V_{DS}=0V$ )	$V_{GS} = \pm 10\text{ V}$		—	$\pm 100$	nA

**Table 5. Power on**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ ; $I_D = 1\text{ mA}$	2		4	V
$dV_{GS(th)}/dT$	Gate threshold voltage temperature derating	$V_{DS} = V_{GS}$ ; $I_D = 1\text{ mA}$		7.5		$\text{mV}/\text{°C}$
$R_{DS(on)HS}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 5\text{ A}$ ; $T_j = 25\text{ °C}$		5.7		$\text{m}\Omega$
		$V_{GS} = 10\text{ V}$ ; $I_D = 5\text{ A}$ ; $T_j = 150\text{ °C}$			11.9	$\text{m}\Omega$
$R_{DS(on)LS}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 5\text{ A}$ ; $T_j = 25\text{ °C}$		7.3		$\text{m}\Omega$
		$V_{GS} = 10\text{ V}$ ; $I_D = 5\text{ A}$ ; $T_j = 150\text{ °C}$			15.1	$\text{m}\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$G_{fs\_HS}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{ V}$ ; $I_D = 20\text{ A}$ ; $T_j = 25\text{ °C}$	—	20	—	S
$G_{fs\_LS}^{(1)}$	Forward transconductance		—	17.5	—	S
$C_{iss\_HS}$	Input capacitance	$V_{DS} = 25\text{ V}$ ; $f = 1\text{ MHz}$ ; $V_{GS} = 0\text{ V}$ (see <a href="#">Figure 6</a> )	—	1836	—	pF
$C_{oss\_HS}$	Output capacitance		—	426	—	pF
$C_{rss\_HS}$	Reverse transfer capacitance		—	55	—	pF
$C_{iss\_LS}$	Input capacitance	$V_{DS} = 25\text{ V}$ ; $f = 1\text{ MHz}$ ; $V_{GS} = 0\text{ V}$ (see <a href="#">Figure 7</a> )	—	1250	—	pF
$C_{oss\_LS}$	Output capacitance		—	311	—	pF
$C_{rss\_LS}$	Reverse transfer capacitance		—	49	—	pF

1. Pulsed: pulse duration = 300 $\mu\text{s}$ , duty cycle 1.5%.



**Table 7. Gate resistance**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
R <sub>G_HS</sub>	Gate resistance HS	V <sub>DD</sub> = 15 V; f <sub>gate</sub> = 1 MHz	—	20	—	Ω
R <sub>G_LS</sub>	Gate resistance LS		—	13	—	Ω

**Table 8. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>SD</sub> <sup>(1)</sup>	Forward on voltage	I <sub>SD</sub> = 20 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	—	0.9	1.1	V
t <sub>rr</sub>	Reverse recovery time	I <sub>SD</sub> = 20 A; di/dt = 100 A/μs; V <sub>DD</sub> = 20 V; T <sub>j</sub> = 150 °C (see <a href="#">Figure 10</a> )	—	50		ns
Q <sub>rr</sub>	Reverse recovery charge		—	28		nC
I <sub>RRM</sub>	Reverse recovery current		—	0.8		A

1. Pulse width limited by safe operating area.

**Table 9. Switching on HSD**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t <sub>d(on)</sub>	Turn on delay time	V <sub>DD</sub> = 15 V; I <sub>D</sub> = 20 A; R <sub>G</sub> = 4.7 Ω; V <sub>GS</sub> = 10 V	—	53	—	ns
t <sub>r</sub>	Rise time		—	319	—	ns
Q <sub>g</sub>	Total gate charge	V <sub>DD</sub> = 15 V; I <sub>D</sub> = 20 A; V <sub>GS</sub> = 10 V (see <a href="#">Figure 4</a> and <a href="#">Figure 9</a> )	—	36	—	nC
Q <sub>gs</sub>	Gate-source charge		—	8.5	—	nC
Q <sub>gd</sub>	Gate-drain charge		—	5	—	nC

**Table 10. Switching on LSD**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t <sub>d(on)</sub>	Turn on delay time	V <sub>DD</sub> = 15 V; I <sub>D</sub> = 20 A; R <sub>G</sub> = 4.7 Ω; V <sub>GS</sub> = 10 V	—	53	—	ns
t <sub>r</sub>	Rise time		—	430	—	ns
Q <sub>g</sub>	Total gate charge	V <sub>DD</sub> = 15 V; I <sub>D</sub> = 20 A; V <sub>GS</sub> = 10 V (see <a href="#">Figure 5</a> and <a href="#">Figure 9</a> )	—	23	—	nC
Q <sub>gs</sub>	Gate-source charge		—	6	—	nC
Q <sub>gd</sub>	Gate-drain charge		—	2.5	—	nC

**Table 11. Switching off HSD**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t <sub>d(off)</sub>	Turn-off delay time	V <sub>DD</sub> = 15 V; I <sub>D</sub> = 20 A; R <sub>G</sub> = 4.7 Ω; V <sub>GS</sub> = 10 V (see <a href="#">Figure 11</a> )	—	253	—	ns
t <sub>f</sub>	Fall time		—	169	—	ns

**Table 12. Switching off LSD**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off delay time	$V_{DD} = 15\text{ V}; I_D = 20\text{ A};$ $R_G = 4.7\ \Omega; V_{GS} = 10\text{ V}$ (see <a href="#">Figure 11</a> )	—	124	—	ns
$t_f$	Fall time		—	293	—	ns

**Table 13. Thermal sensor<sup>(1)</sup>**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_F$	Chain diode forward voltage	$T_j = 25\text{ }^\circ\text{C}; I_F = 250\ \mu\text{A}$ (see <a href="#">Figure 8</a> )	3.72	3.88	4.04	V
$S_F$	Chain temperature coefficient	$-40\text{ }^\circ\text{C} < T_j < 175\text{ }^\circ\text{C}; I_F = 250\ \mu\text{A}$		-8.1		mV/°K

1. See [Figure 8](#).

**Figure 4. Gate charge vs gate-source voltage HS**

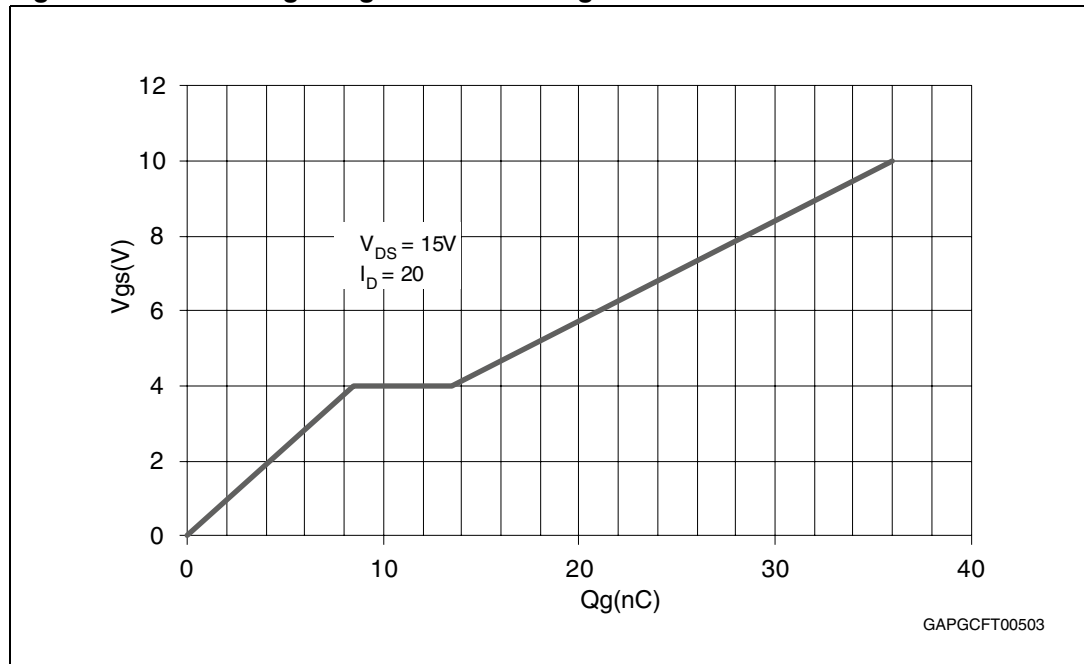


Figure 5. Gate charge vs gate-source voltage LS

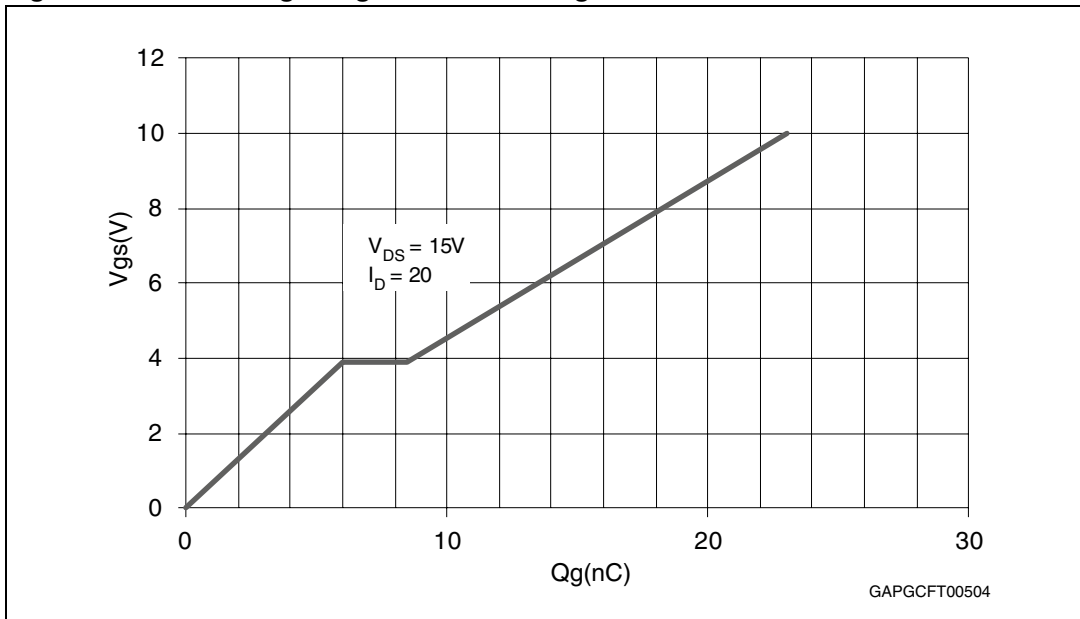


Figure 6. Capacitance variations HS

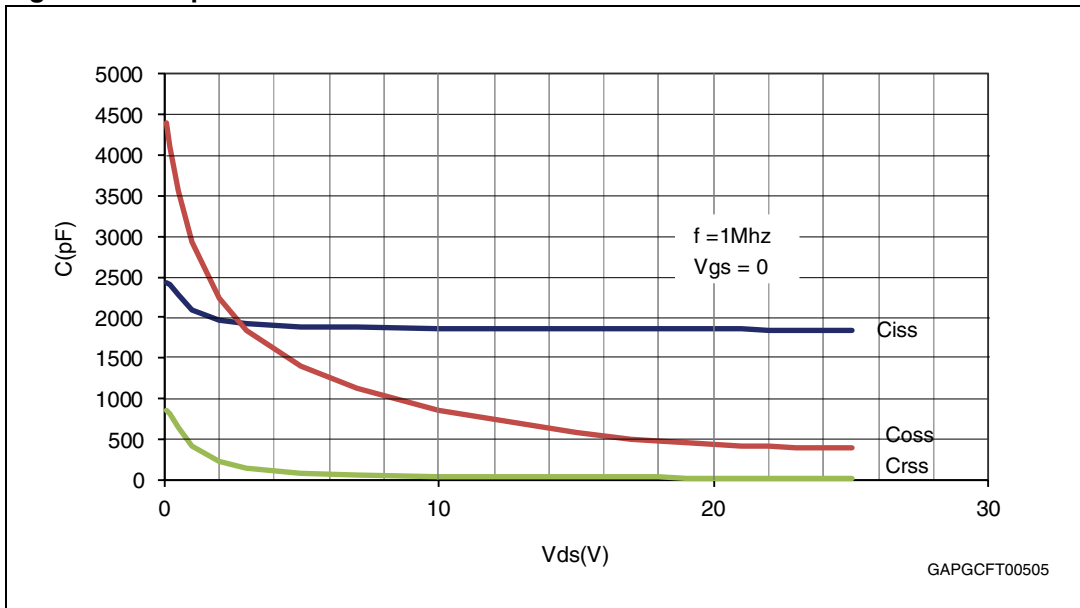


Figure 7. Capacitance variations LS

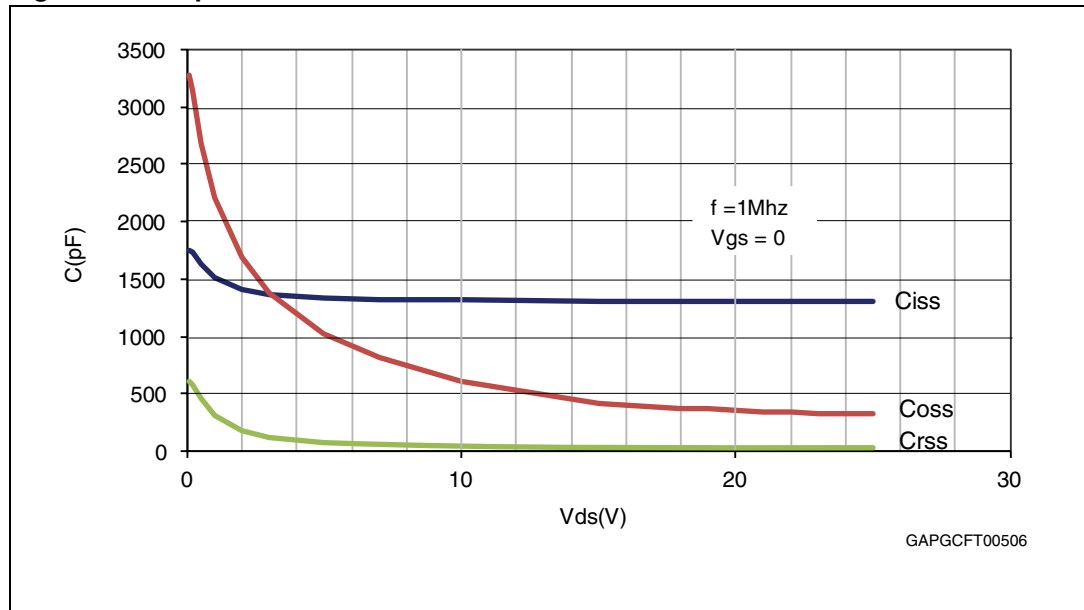


Figure 8. Thermal sensor voltage vs temperature

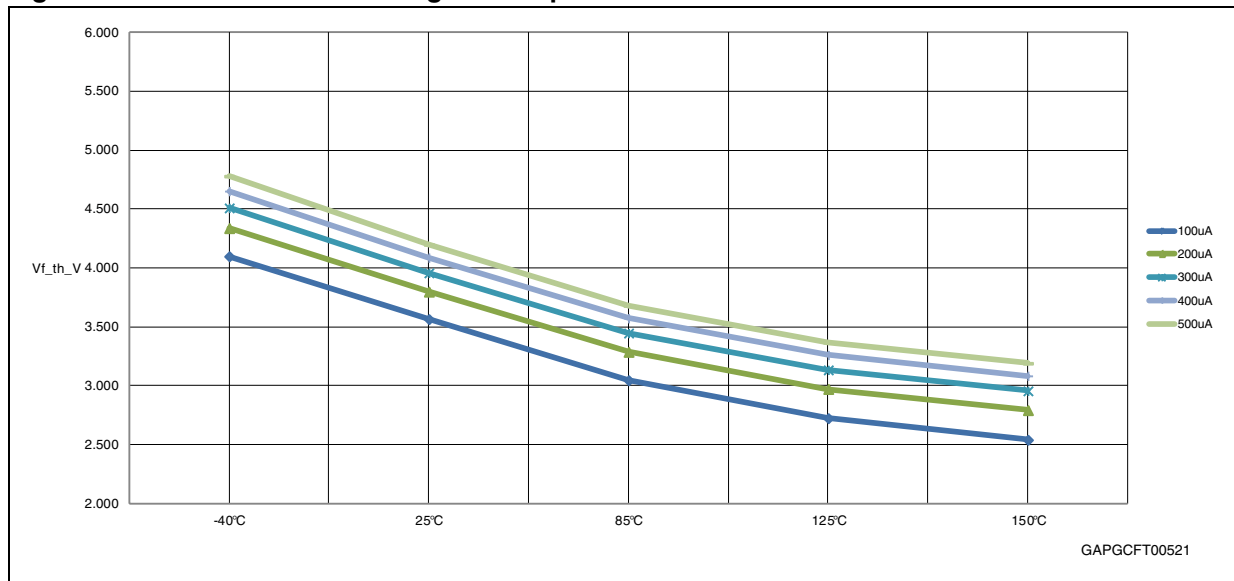


Figure 9. Gate charge test circuit

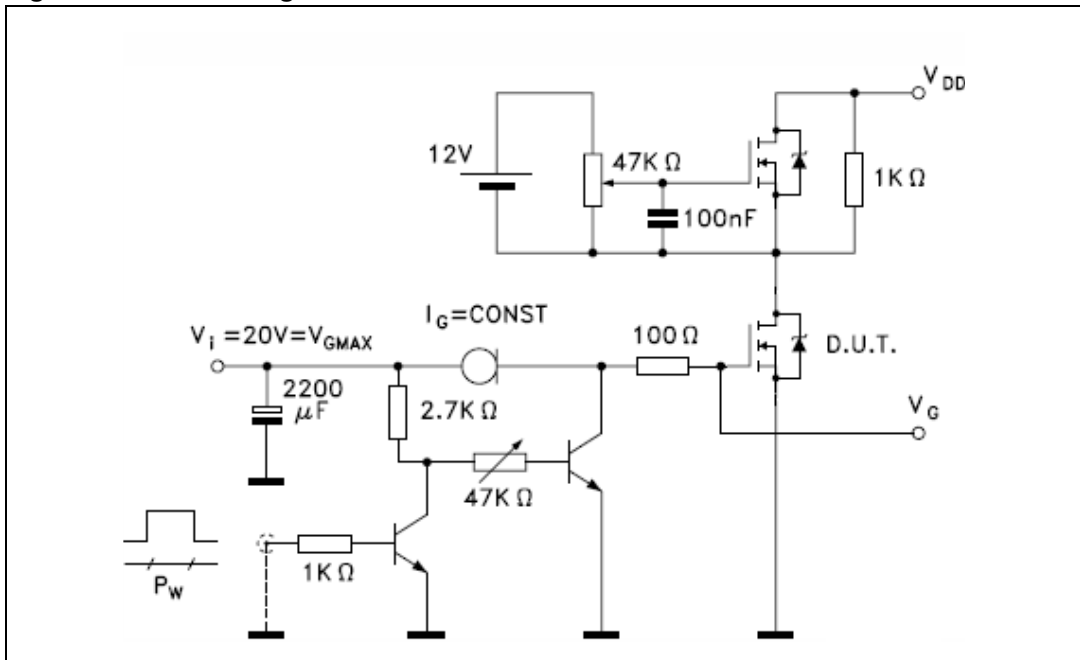


Figure 10. Test circuit for inductive load switching and diode recovery times

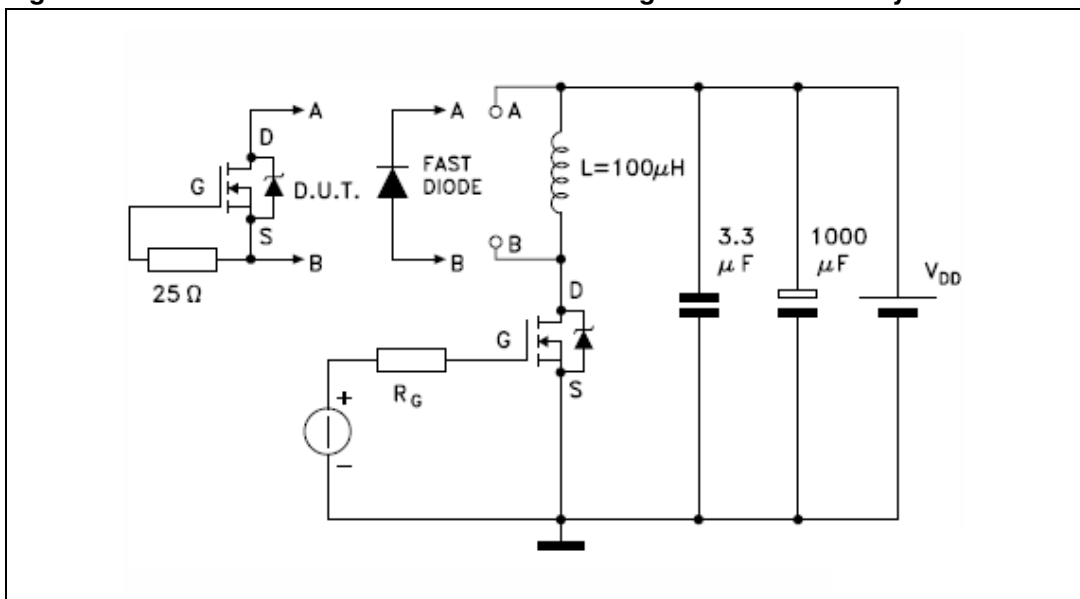
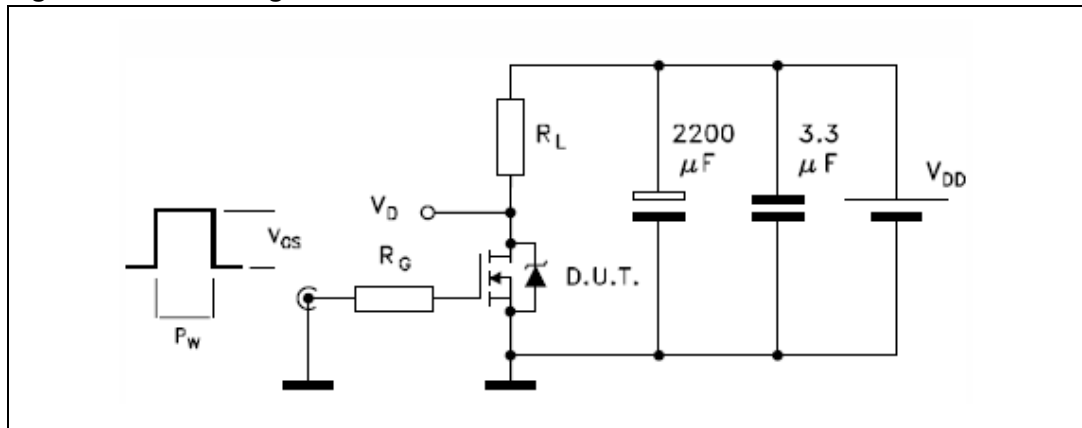


Figure 11. Switching times test circuit for resistive load



### 3 Package and PCB thermal data

#### 3.1 PowerSSO-36 thermal data

Figure 12. PowerSSO-36 PC board

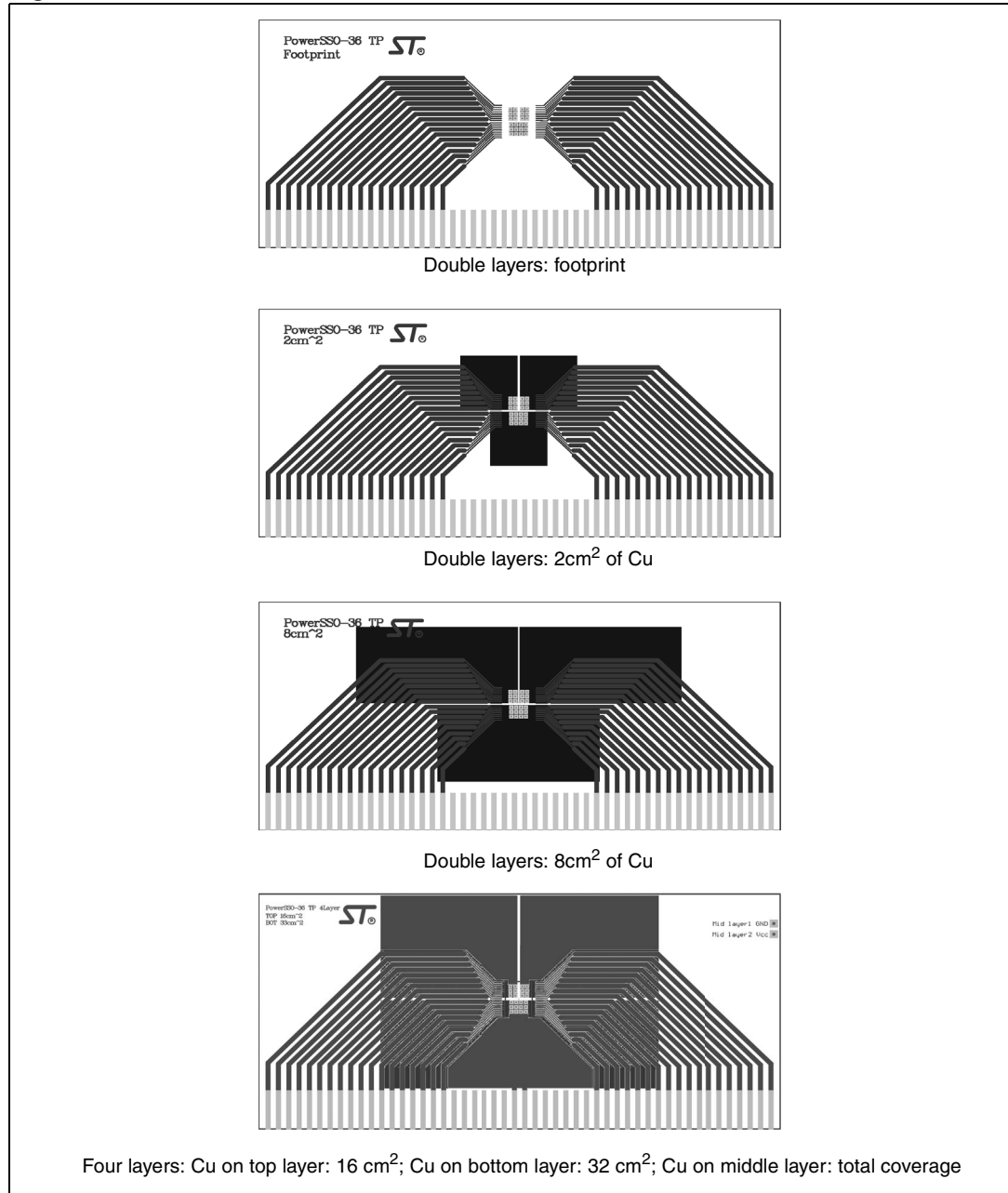


Figure 13. Chipset configuration

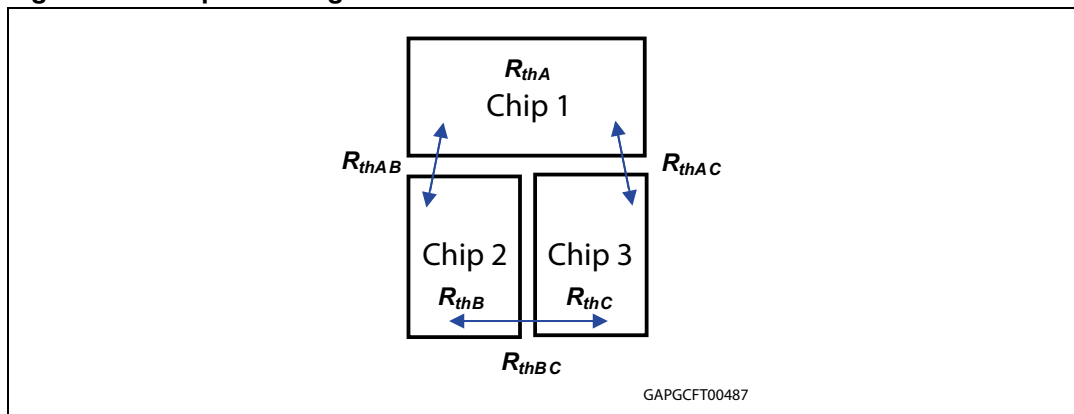
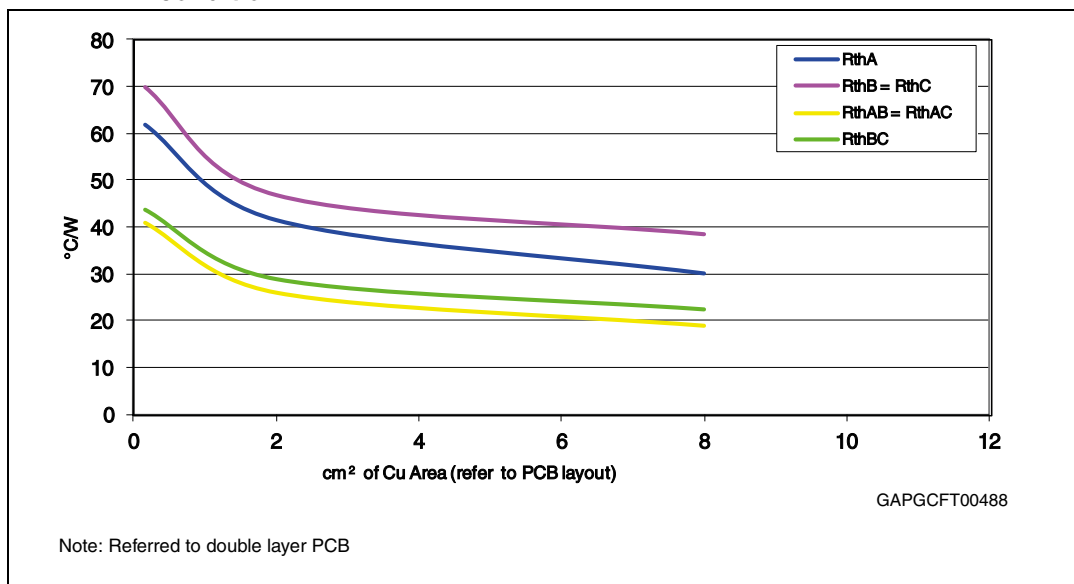


Figure 14. Auto and mutual  $R_{thj-amb}$  vs PCB copper area in open box free air condition



### 3.1.1 Thermal calculation in clockwise and anti-clockwise operation in steady-state mode

Table 14. Thermal calculation in clockwise and anti-clockwise operation in steady-state mode

HS <sub>A</sub>	HS <sub>B</sub>	LS <sub>A</sub>	LS <sub>B</sub>	T <sub>jHSAB</sub>	T <sub>jLSA</sub>	T <sub>jLSB</sub>
ON	OFF	OFF	ON	$P_{dHSA} \times R_{thHS} + P_{dLSB} \times R_{thHLS} + T_{amb}$	$P_{dHSA} \times R_{thHLS} + P_{dLSB} \times R_{thLSL} + T_{amb}$	$P_{dHSA} \times R_{thHLS} + P_{dLSB} \times R_{thLS} + T_{amb}$
OFF	ON	ON	OFF	$P_{dHSB} \times R_{thHS} + P_{dLSA} \times R_{thHSL} + T_{amb}$	$P_{dHSB} \times R_{thHSL} + P_{dLSA} \times R_{thLS} + T_{amb}$	$P_{dHSB} \times R_{thHSL} + P_{dLSA} \times R_{thLSL} + T_{amb}$



**3.1.2 Thermal resistances definition (values according to the PCB heatsink area)**

$R_{thHS} = R_{thHSA} = R_{thHSB}$  = High Side Chip Thermal Resistance Junction to Ambient ( $HS_A$  or  $HS_B$  in ON state)

$R_{thLS} = R_{thLSA} = R_{thLSB}$  = Low Side Chip Thermal Resistance Junction to Ambient

$R_{thHSLS} = R_{thHSALS} = R_{thHSBLS}$  = Mutual Thermal Resistance Junction to Ambient between High Side and Low Side Chips

$R_{thLSLS} = R_{thLSALS}$  = Mutual Thermal Resistance Junction to Ambient between Low Side Chips

**3.1.3 Thermal calculation in transient mode<sup>(a)</sup>**

$$T_{jHSAB} = Z_{thHS} \times P_{dHSAB} + Z_{thHSLS} \times (P_{dLSA} + P_{dLSB}) + T_{amb}$$

$$T_{jLSA} = Z_{thHSLS} \times P_{dHSAB} + Z_{thLS} \times P_{dLSA} + Z_{thLSLS} \times P_{dLSB} + T_{amb}$$

$$T_{jLSB} = Z_{thHSLS} \times P_{dHSAB} + Z_{thLSLS} \times P_{dLSA} + Z_{thLS} \times P_{dLSB} + T_{amb}$$

**3.1.4 Single pulse thermal impedance definition (values according to the PCB heatsink area)**

$Z_{thHS}$  = High Side Chip Thermal Impedance Junction to Ambient

$Z_{thLS} = Z_{thLSA} = Z_{thLSB}$  = Low Side Chip Thermal Impedance Junction to Ambient

$Z_{thHSLS} = Z_{thHSALS} = Z_{thHSBLS}$  = Mutual Thermal Impedance Junction to Ambient between High Side and Low Side Chips

$Z_{thLSLS} = Z_{thLSALS}$  = Mutual Thermal Impedance Junction to Ambient between Low Side Chips

**Equation 1: pulse calculation formula**

$$Z_{TH\delta} = R_{TH} \times \delta + Z_{THtp} \times (1 - \delta)$$

where  $\delta = t_p / T$

a. Calculation is valid in any dynamic operating condition.  $P_d$  values set by user.

Figure 15. PowerSSO-36 HSD thermal impedance junction ambient single pulse

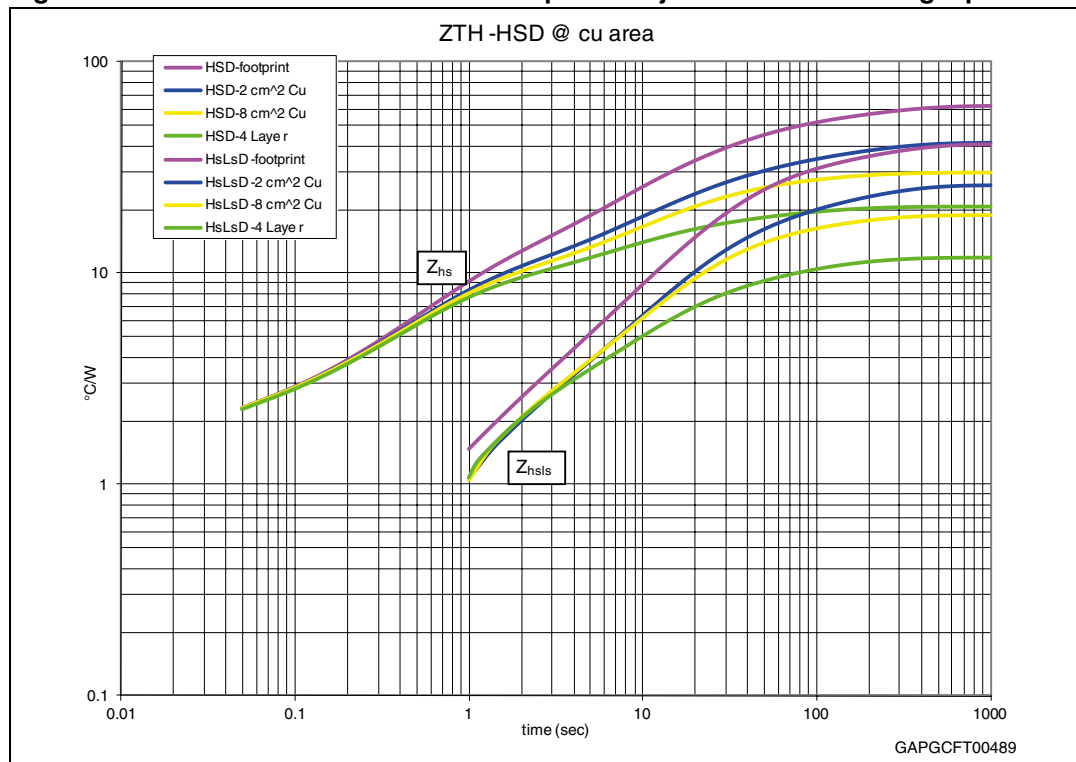


Figure 16. PowerSSO-36 LSD thermal impedance junction ambient single pulse

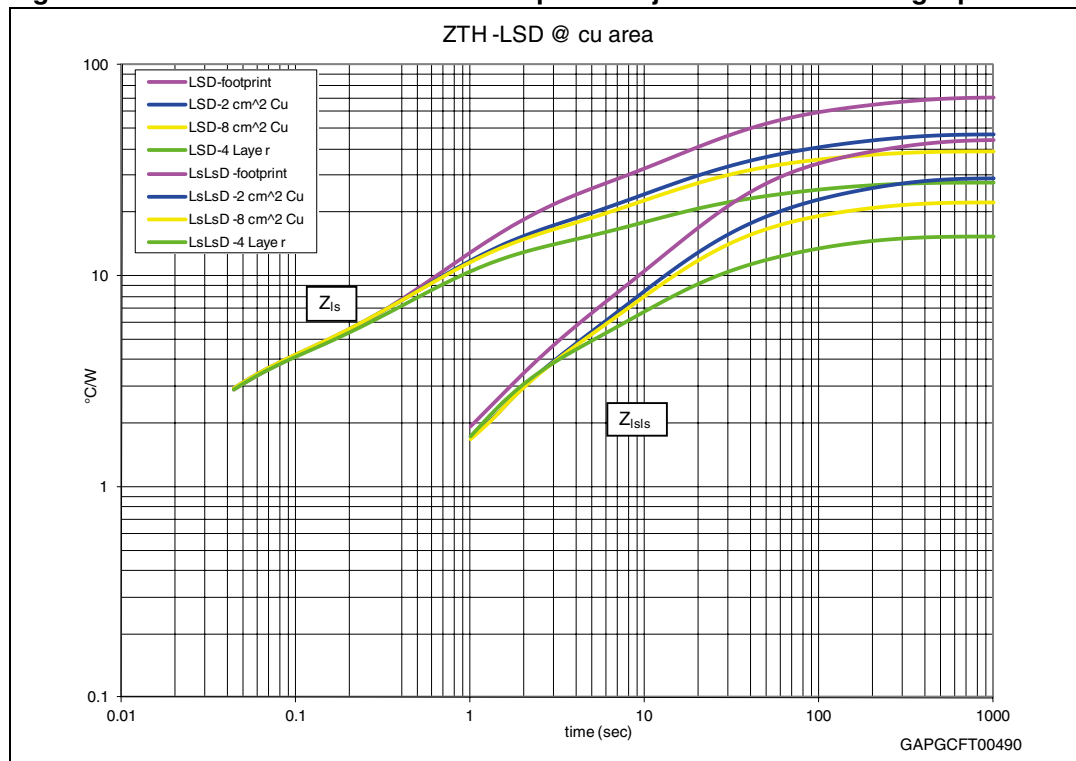


Figure 17. Thermal fitting model of an H-bridge in PowerSSO-36

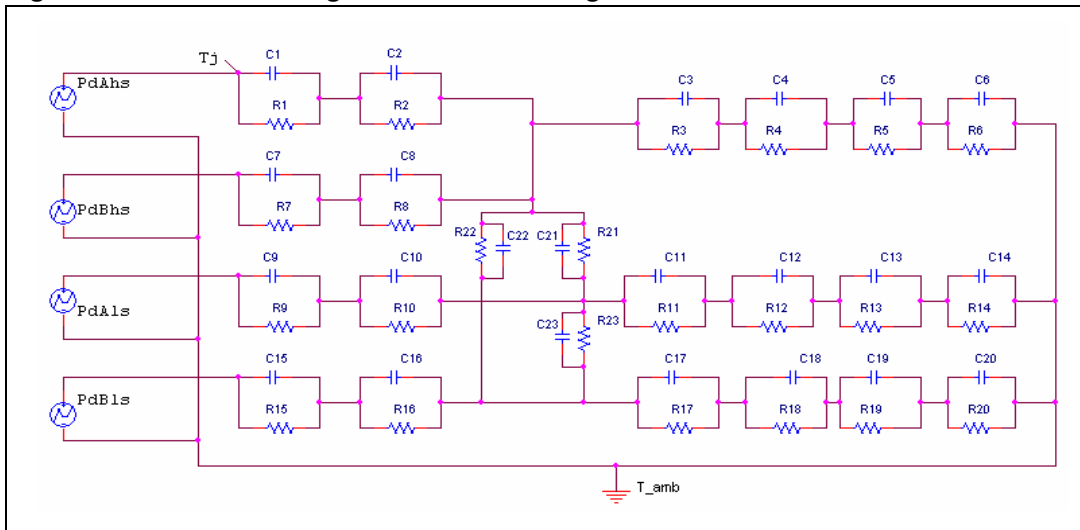


Table 15. Thermal parameters<sup>(1)</sup>

Area/island (cm <sup>2</sup> )	Footprint	2	8	4L
R1 = R7 (°C/W)	0.2			
R2 = R8 (°C/W)	1.6			
R3 (°C/W)	8			
R4 (°C/W)	30	16	16	10
R5 (°C/W)	40	22	12	5
R6 (°C/W)	36	28	10	6
R9 = R15 (°C/W)	0.1			
R10 = R16 (°C/W)	2.8			
R11 = R17 (°C/W)	22	14	14	14
R12 = R18 (°C/W)	49	30	30	20
R13 = R19 (°C/W)	52	36	28	16
R14 = R20 (°C/W)	50	32	26	18
R21 = R22 (°C/W)	80	60	50	40
R23 (°C/W)	80	50	45	30
C1 = C7 = C9 = C15 (W.s/°C)	0.001			
C2 = C8 (W.s/°C)	0.009			
C3 (W.s/°C)	0.09			
C4 (W.s/°C)	0.5	0.8	0.8	0.8
C5 (W.s/°C)	0.8	1.4	2	3
C6 (W.s/°C)	5	6	8	10
C10 = C16 (W.s/°C)	0.1			
C11 = C17 (W.s/°C)	0.07			
C12 = C18 (W.s/°C)	0.45	0.45	0.45	0.6
C13 = C19 (W.s/°C)	0.8	1	1.2	2.5
C14 = C20 (W.s/°C)	4	5	6	8
C21 = C22 = C23 (W.s/°C)	0.01	0.006	0.005	0.005

1. The blank space means that the value is the same as the previous one.

## 4 Package and packing information

### 4.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com).

ECOPACK® is an ST trademark.

### 4.2 PowerSSO-36 TP package information

Figure 18. PowerSSO-36 TP package dimensions

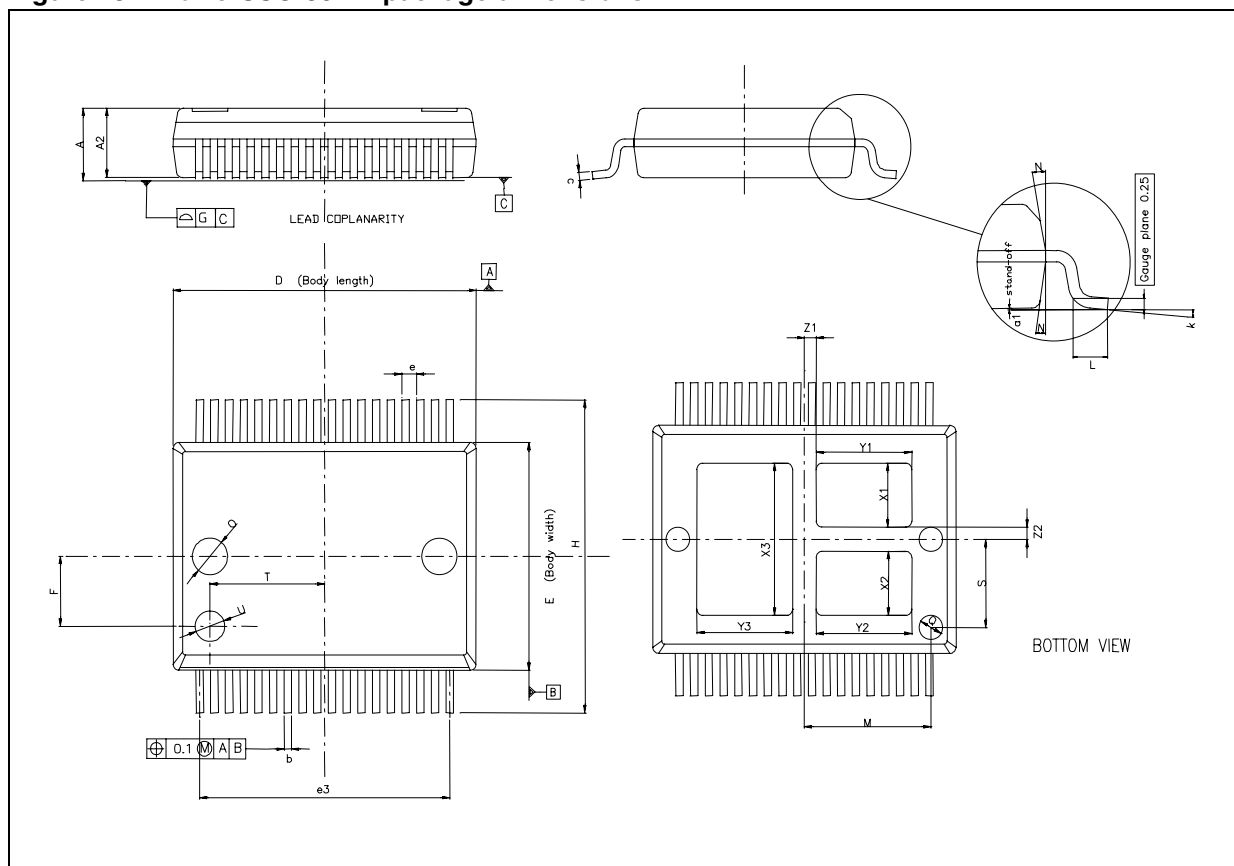


Table 16. PowerSSO-36 TP mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	2.15		2.47
A2	2.15		2.40
a1	0		0.1
b	0.18		0.36
c	0.23		0.32
D	10.10		10.50
E	7.4		7.6
e		0.5	
e3		8.5	
F		2.3	
G			0.1
H	10.1		10.5
h			0.4
k	0 deg		8 deg
L	0.6		1
M		4.3	
N			10 deg
O		1.2	
Q		0.8	
S		2.9	
T		3.65	
U		1.0	
X1	1.85		2.35
Y1	3		3.5
X2	1.85		2.35
Y2	3		3.5
X3	4.7		5.2
Y3	3		3.5
Z1		0.4	
Z2		0.4	

### 4.3 PowerSSO-36 TP packing information

Figure 19. PowerSSO-36 TP tube shipment (no suffix)

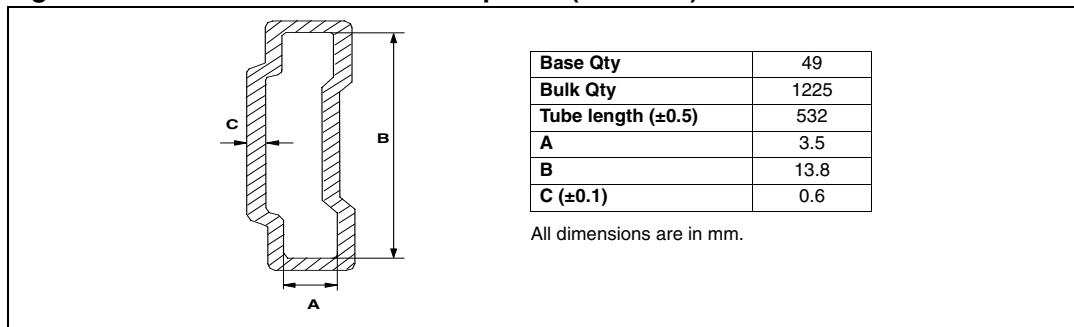
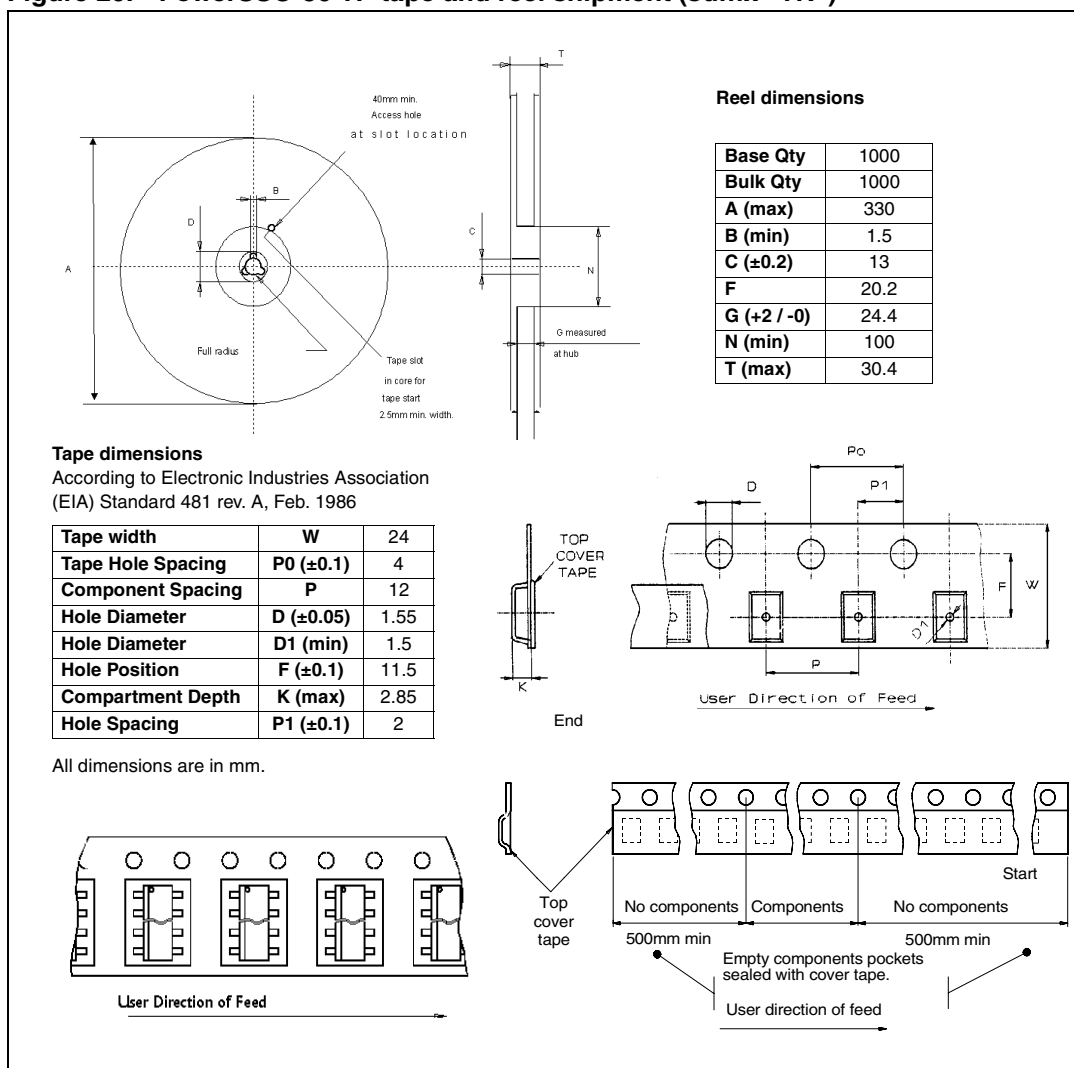


Figure 20. PowerSSO-36 TP tape and reel shipment (suffix “TR”)



## 5 Revision history

**Table 17. Document revision history**

<b>Date</b>	<b>Revision</b>	<b>Changes</b>
07-Nov-2011	1	Initial release
18-Jan-2012	2	Changed document status from preliminary data to datasheet.
20-Jan-2012	3	Updated features list.

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