

Low-Cost, Ultra-Small, 3μA Single-Supply Comparators

General Description

The MAX9075/MAX9077 single/dual comparators are optimized for 3V and 5V single-supply applications. These comparators have a 580ns propagation delay and consume just 3μA per comparator. The combination of low-power, single-supply operation down to 2.1V, and ultra-small footprint makes these devices ideal for all portable applications.

The MAX9075/MAX9077 have a common-mode input voltage range of -0.2V to $V_{CC} - 1.2V$. Unlike many comparators, there is no differential clamp between the inputs, allowing the differential input voltage range to extend rail-to-rail. All inputs and outputs tolerate a continuous short-circuit fault condition to either rail.

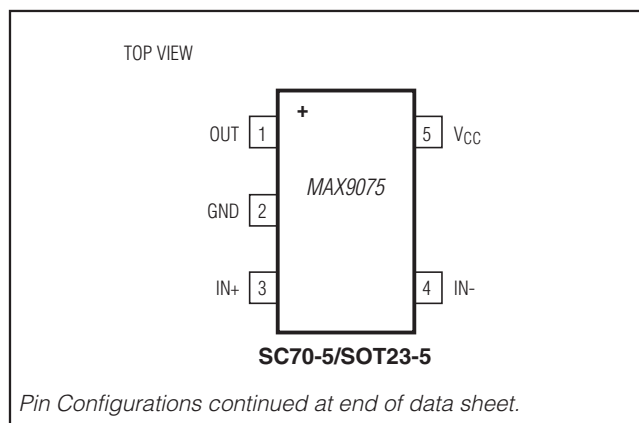
The design of the output stage limits supply-current surges while switching (typical of many other comparators), minimizing power consumption under dynamic conditions. Large internal push-pull output drivers allow rail-to-rail output swing with loads up to 2mA, making these devices ideal for interface with TTL/CMOS logic.

The MAX9075 single comparator is available in 5-pin SC70 and SOT23 packages, while the MAX9077 dual comparator is available in 8-pin SOT23, μMAX®, and SO packages.

Applications

Battery-Powered Systems
 Threshold Detectors/Discriminators
 Keyless Entry Systems
 IR Receivers
 Digital Line Receivers

Pin Configurations



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Features

- ◆ 580ns Propagation Delay from Only 3μA
- ◆ 2.1V to 5.5V Single-Supply Operation
- ◆ Ground-Sensing Inputs
- ◆ Rail-to-Rail Outputs
- ◆ No Output Phase Inversion for Overdriven Inputs
- ◆ No Differential Clamp Across Inputs
- ◆ Available in Ultra-Small Packages
 - 5-Pin SC70 (MAX9075)
 - 8-Pin SOT23 (MAX9077)

Ordering Information

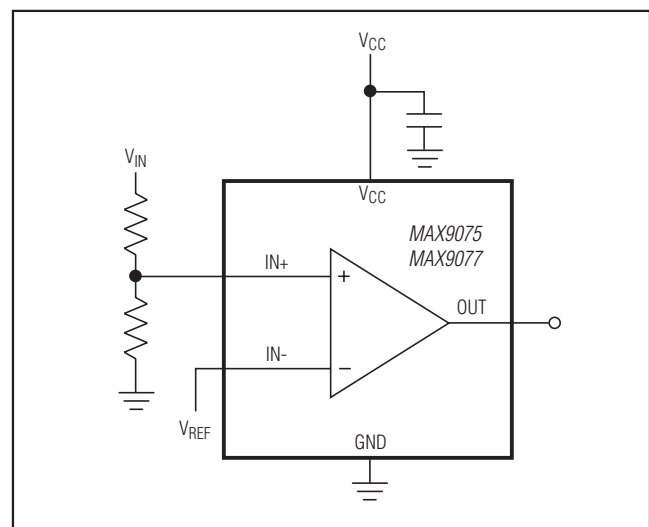
| PART* | TEMP RANGE | PIN-PACKAGE | TOP MARK |
|----------------|-----------------|-------------|----------|
| MAX9075EXK+T | -40°C to +85°C | 5 SC70 | AAC+ |
| MAX9075EUK+T | -40°C to +85°C | 5 SOT23 | ADLX+ |
| MAX9077EKA+T | -40°C to +85°C | 8 SOT23 | AAAD+ |
| MAX9077EUA+ | -40°C to +85°C | 8 μMAX | — |
| MAX9077ESA+ | -40°C to +85°C | 8 SO | — |
| MAX9077MSA/PR2 | -55°C to +125°C | 8 SO | — |

+Denotes a lead(Pb)-free/RoHS-compliant package.

*Denotes a package containing lead(Pb).

T = Tape and reel.

Typical Operating Circuit



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ABSOLUTE MAXIMUM RATINGS

| | |
|--|---|
| Supply Voltage | 8-Pin μ MAX (derate 4.5mW/°C above +70°C)362mW |
| V _{CC} to GND6V | 8-Pin SO (derate 5.88mW/°C above +70°C)471mW |
| All Other Pins to GND-0.3V to (V _{CC} + 0.3V) | Operating Temperature Range-40°C to +85°C |
| Current into Input Pins \pm 20mA | Military Operating Temperature Range-55°C to +125°C |
| Duration of Output Short-Circuit to GND or V _{CC}Continuous | Storage Temperature Range-65°C to +150°C |
| Continuous Power Dissipation (T _A = +70°C) | Lead Temperature (soldering, 10s)+300°C |
| 5-Pin SC70 (derate 3.1mW/°C above +70°C)247mW | Soldering Temperature (reflow) |
| 5-Pin SOT23 (derate 3.1mW/°C above +70°C)247mW | Lead (Pb)-free+260°C |
| 8-Pin SOT23 (derate 5.2mW/°C above +70°C)412mW | Containing lead (Pb)+240°C |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, V_{CM} = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------|------------------|---|-----------------------|---------|-----------------------|---------|
| Operating Supply Voltage Range | V _{CC} | Inferred from PSRR | 2.1 | | 5.5 | V |
| Supply Current per Comparator | I _{CC} | V _{CC} = 5V | | 3 | 5.2 | μ A |
| | | T _A = T _{MIN} to T _{MAX} | | | 7.5 | |
| | | V _{CC} = 3V | | 2.4 | | |
| Power-Supply Rejection Ratio | PSRR | 2.1V \leq V _{CC} \leq 5.5V | 54 | 77 | | dB |
| Common-Mode Voltage Range | V _{CMR} | (Note 2) | 0 | | V _{CC} - 1.2 | V |
| Input Offset Voltage | V _{OS} | | | \pm 1 | \pm 8 | mV |
| Input Offset Current | I _{OS} | | | 1 | | nA |
| Input Bias Current | I _B | V _{CM} = 0.2V (Note 3) | | -5 | -20 | nA |
| Input Capacitance | C _{IN} | | | 3 | | pF |
| Common-Mode Rejection Ratio | CMRR | 0V \leq V _{CM} \leq (V _{CC} - 1.2V) | 60 | 82 | | dB |
| OUT_ Output-Voltage High | V _{OH} | I _{SOURCE} = 2mA | V _{CC} - 0.4 | | | V |
| OUT_ Output-Voltage Low | V _{OL} | I _{SINK} = 2mA | | | 0.4 | V |
| Propagation Delay Low to High | t _{PD+} | C _{LOAD} = 10pF, overdrive = 100mV | | 580 | | ns |
| Propagation Delay High to Low | t _{PD-} | C _{LOAD} = 10pF, overdrive = 100mV | | 250 | | ns |
| Rise/Fall Time | | C _{LOAD} = 10pF | | 1.6 | | ns |

Note 1: All devices are 100% production tested at T_A = +25°C. All temperature limits are guaranteed by design.

Note 2: Inferred from CMRR. Either input can be driven to the absolute maximum limit without output inversion, as long as the other input is within the input voltage range.

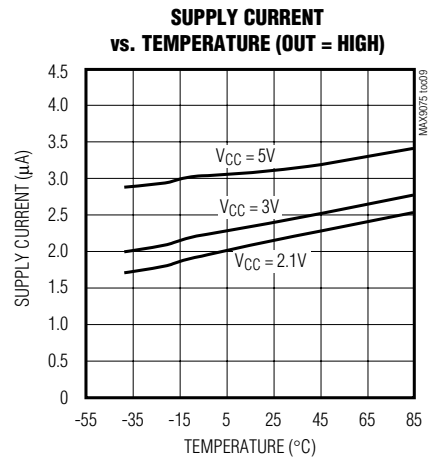
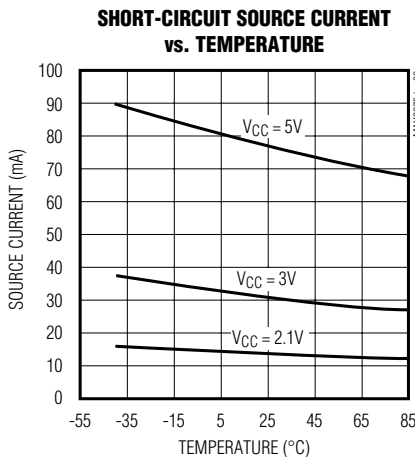
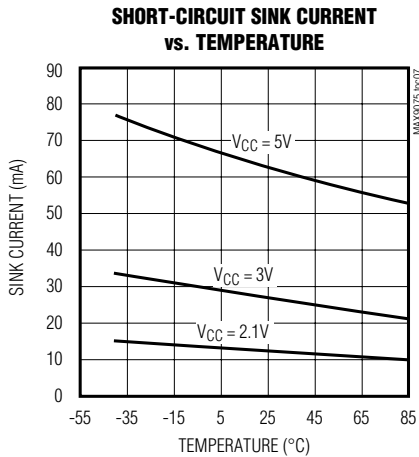
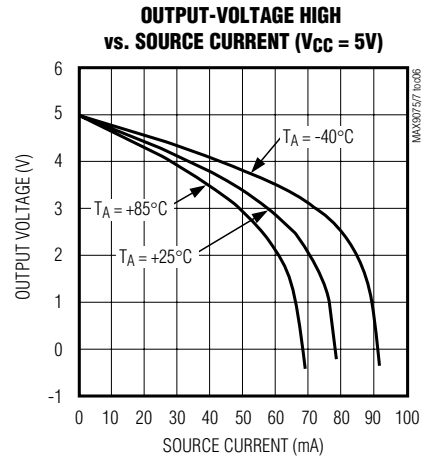
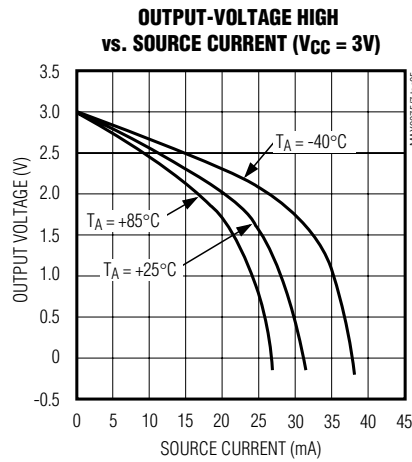
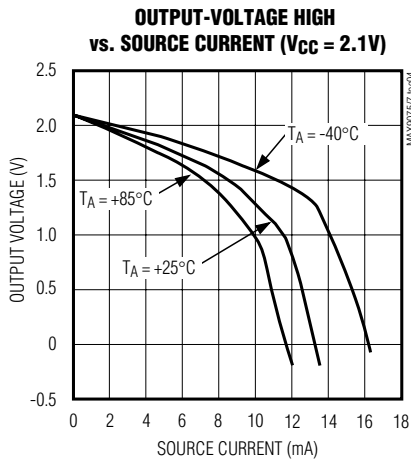
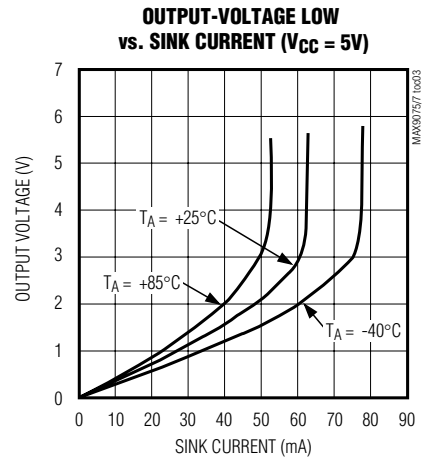
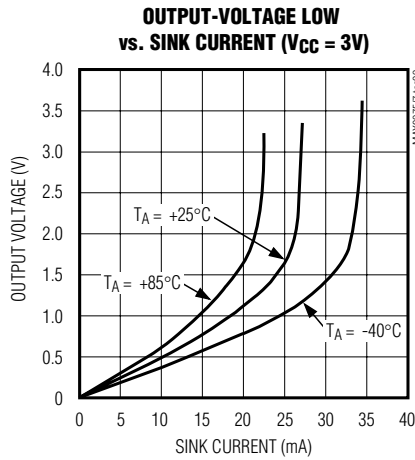
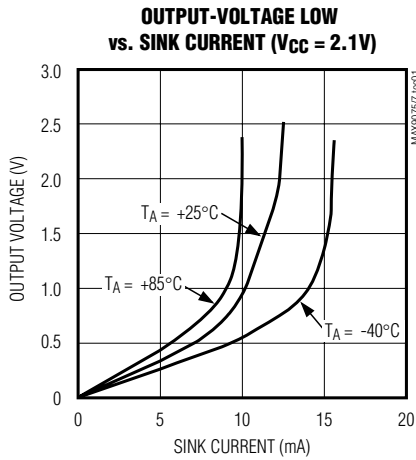
Note 3: Guaranteed by design.

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Typical Operating Characteristics

($V_{CC} = 5V$, $V_{CM} = 0V$, 100mV overdrive, $T_A = +25^\circ C$, unless otherwise noted.)

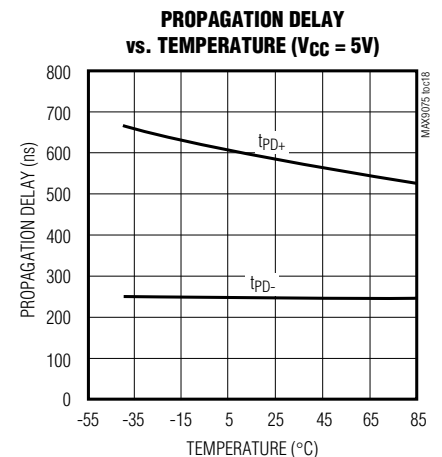
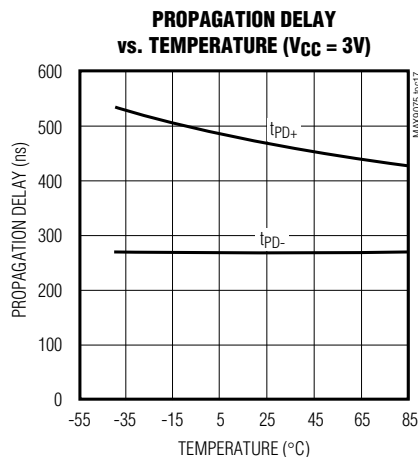
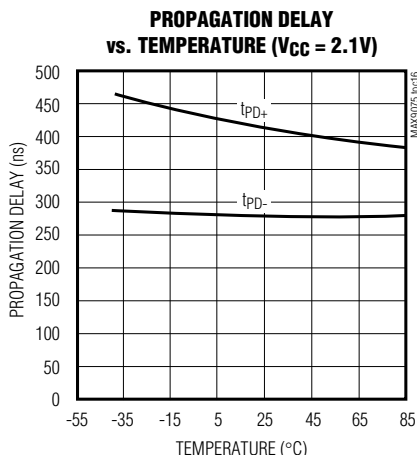
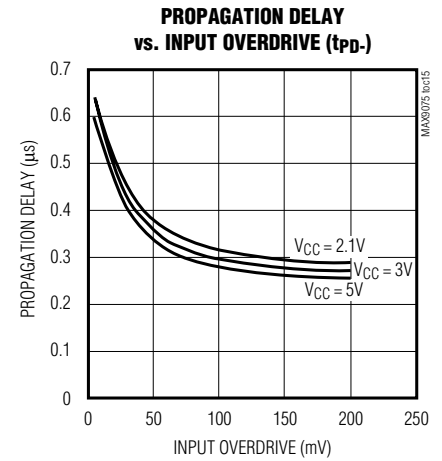
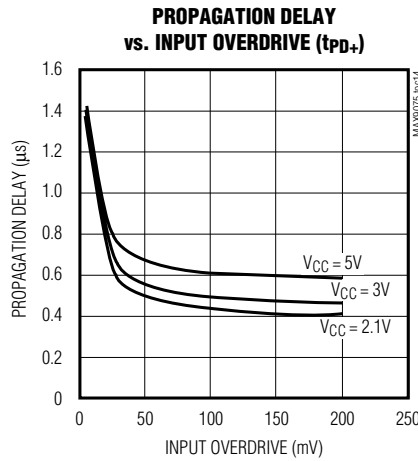
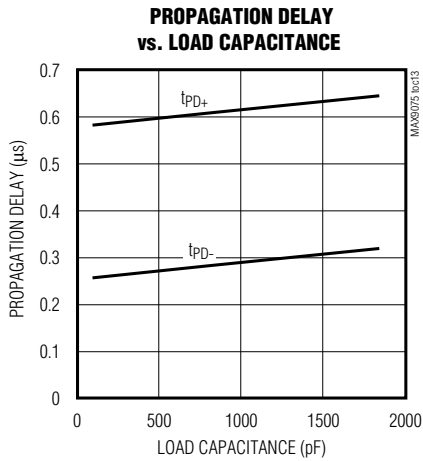
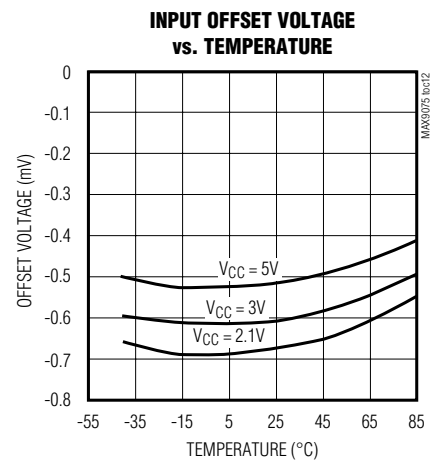
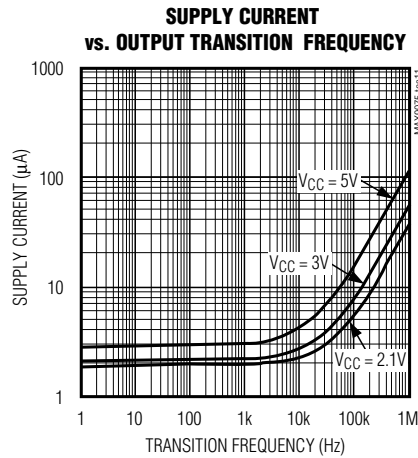
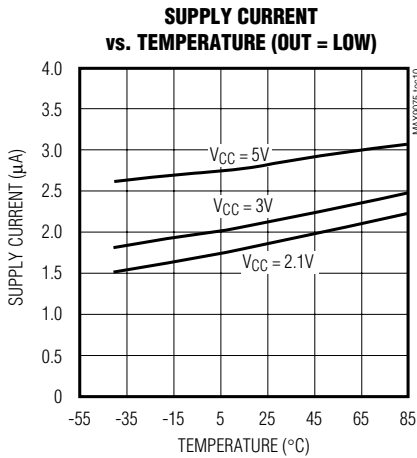


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Typical Operating Characteristics (continued)

($V_{CC} = 5V$, $V_{CM} = 0V$, 100mV overdrive, $T_A = +25^\circ C$, unless otherwise noted.)

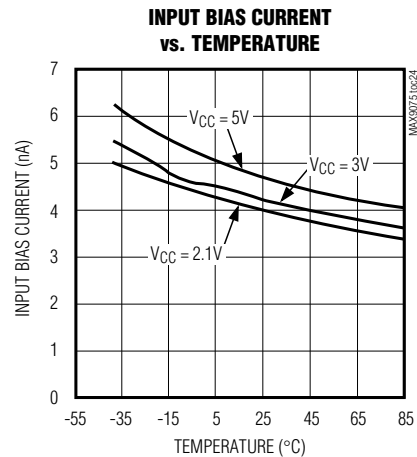
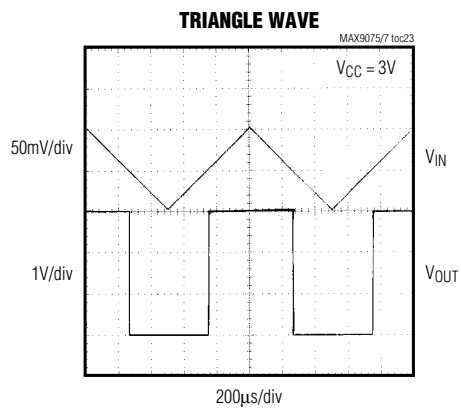
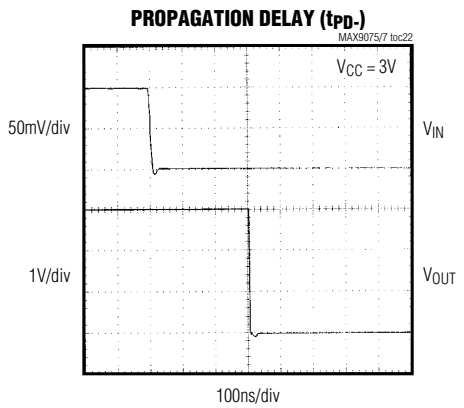
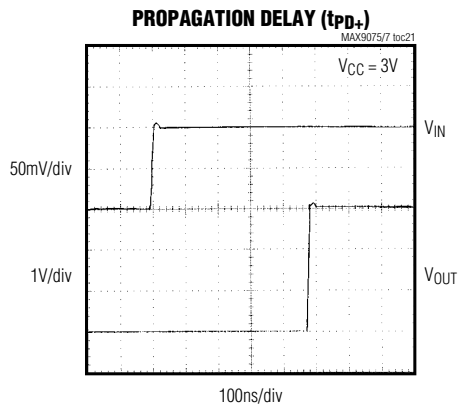
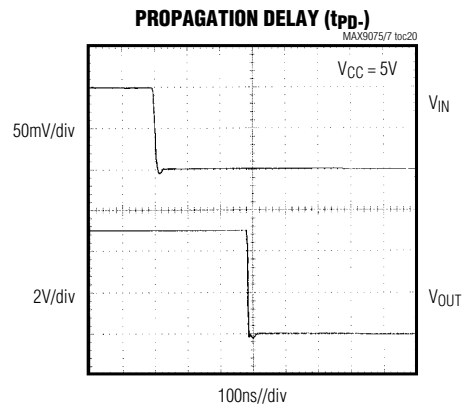
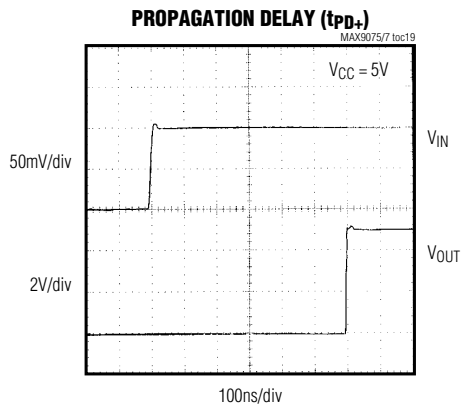


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Typical Operating Characteristics (continued)

($V_{CC} = 5V$, $V_{CM} = 0V$, 100mV overdrive, $T_A = +25^\circ C$, unless otherwise noted.)



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Pin Description

| PIN | | | | NAME | FUNCTION |
|---------|------|--------------|-------|------|------------------------------------|
| MAX9075 | | MAX9077 | | | |
| SOT23 | SC70 | μ MAX/SO | SOT23 | | |
| 1 | 1 | — | — | OUT | Comparator Output |
| — | — | 1 | 1 | OUTA | Output of Comparator A |
| 2 | 2 | 4 | 2 | GND | Ground |
| 3 | 3 | — | — | IN+ | Noninverting Comparator Input |
| — | — | 3 | 4 | INA+ | Noninverting Input of Comparator A |
| 4 | 4 | — | — | IN- | Inverting Comparator Input |
| — | — | 2 | 3 | INA- | Inverting Input of Comparator A |
| 5 | 5 | 8 | 8 | VCC | Positive Supply Voltage |
| — | — | 5 | 5 | INB+ | Noninverting Input of Comparator B |
| — | — | 6 | 6 | INB- | Inverting Input of Comparator B |
| — | — | 7 | 7 | OUTB | Output of Comparator B |

Detailed Description

The MAX9075/MAX9077 feature a 580ns propagation delay from an ultra-low supply current of only 3 μ A per comparator. These devices are capable of single-supply operation in the 2.1V to 5.5V range. Large internal output drivers allow rail-to-rail output swing with up to 2mA loads. Both comparators offer a push-pull output that sinks and sources current.

Comparator Output

The MAX9075/MAX9077 are designed to maintain a low-supply current during repeated transitions by limiting the shoot-through current.

Noise Considerations, Comparator Input

The input common-mode voltage range for these devices extends from 0V to $V_{CC} - 1.2V$. Unlike many other comparators, the MAX9075/MAX9077 can operate at any differential input voltage within these limits. Input bias current is typically -5nA if the input voltage is between the supply rails.

Although the comparators have a very high gain, useful gain is limited by noise. The comparator has a wide-band peak-to-peak noise of approximately 70 μ V.

Applications Information

Adding Hysteresis

Hysteresis extends the comparator's noise margin by increasing the upper threshold and decreasing the lower threshold. A voltage divider from the output of the comparator sets the trip voltage. Therefore, the trip voltage is related to the output voltage. Set the hysteresis with three resistors using positive feedback, as shown in Figure 1.

The design procedure is as follows:

- 1) Choose R3. The leakage current of IN+ may cause a small error; however, the current through R3 can be approximately 500nA and still maintain accuracy. The added supply current due to the circuit at the trip point is $V_{CC}/R3$; 10M Ω is a good practical value for R3, as this keeps the current well below the supply current of the chip.
- 2) Choose the hysteresis voltage (V_{HYS}), which is the voltage between the upper and lower thresholds. In this example, choose $V_{HYS} = 50mV$ and assume $V_{REF} = 1.2V$ and $V_{CC} = 5V$.
- 3) Calculate R1 as follows:

$$R1 = R3 \times V_{HYS}/V_{CC} = 10M\Omega \times 0.05/5 = 100k\Omega$$

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- 4) Choose the threshold voltage for V_{IN} rising (V_{THR}). In this example, choose $V_{THR} = 3V$.
- 5) Calculate R_2 as follows:

$$R_2 = 1 / \left\{ \left[\frac{V_{THR}}{V_{REF} \times R_1} \right] - \frac{1}{R_1} - \frac{1}{R_3} \right\} = 1 / \left\{ \left[\frac{3}{1.2 \times 100k\Omega} \right] - \frac{1}{100k\Omega} - \frac{1}{10M\Omega} \right\} = 67.114k\Omega$$

A 1% preferred value is 64.9kΩ.

- 6) Verify the threshold voltages with these formulas:

V_{IN} rising:

$$V_{THR} = V_{REF} \times R_1 \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} \right)$$

V_{IN} falling:

$$V_{THF} = V_{THR} - (R_1 \times V_{CC}) / R_3$$

- 7) Check the error due to input bias current (5nA). If the error is too large, reduce R_3 and recalculate.

$$V_{TH} = I_B (R_1 \times R_2 \times R_3) / (R_1 + R_2 + R_3) = 0.2mV$$

Board Layout and Bypassing

Use 10nF power-supply bypass capacitors. Use 100nF bypass capacitors when supply impedance is high, when supply leads are long, or when excessive noise is expected on the supply lines. Minimize signal trace lengths to reduce stray capacitance. Minimize the capacitive coupling between $IN-$ and OUT . For slow-moving input signals (rise time > 1ms) use a 1nF capacitor between $IN+$ and $IN-$.

Chip Information

PROCESS: BiCMOS

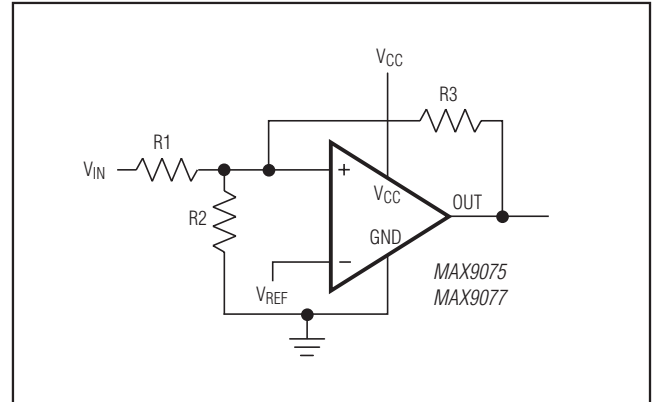
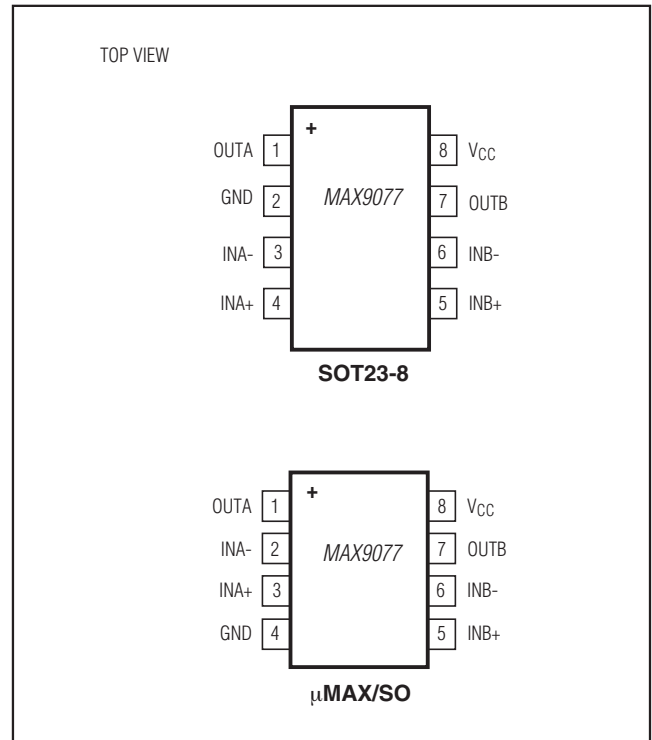


Figure 1. Adding Hysteresis

Pin Configurations (continued)



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Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|--------------|--------------|-------------------------|-------------------------|
| 5 SC70 | X5+1 | 21-0076 | 90-0188 |
| 5 SOT23 | U5+1 | 21-0057 | 90-0174 |
| 8 SOT23 | K8+2 | 21-0078 | 90-0176 |
| 8 μ MAX | U8+1 | 21-0036 | 90-0092 |
| 8 S0 | S8+4 | 21-0041 | 90-0096 |

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Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|-----------------|---------------|--|---------------|
| 0 | 0/99 | Initial release | — |
| 3 | 1/07 | Revised <i>Absolute Maximum Ratings</i> | 2 |
| 4 | 12/12 | Added MAX9077MSA/PR2 to <i>Ordering Information</i> and updated for lead-free notation. Revised <i>Absolute Maximum Ratings</i> , <i>Electrical Characteristics</i> , and the <i>Noise Considerations</i> , <i>Comparator Input</i> section. | 1, 2, 6 |



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Maxim Integrated 160 Rio Robles, San Jose, CA 95134 USA 1-408-601-1000

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