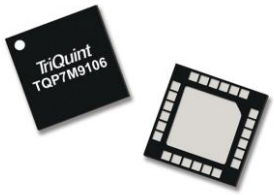
TQP7M9106

2 Watt High Linearity Amplifier

Applications

- Repeaters
- BTS Transceivers
- BTS High Power Amplifiers
- CDMA / WCDMA / LTE
- General Purpose Wireless

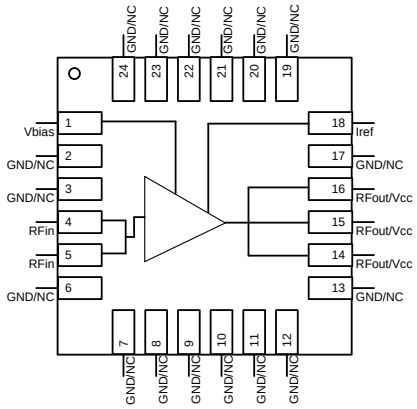


24 Pin 4x4 mm QFN Package

Product Features

- 50−1500 MHz
- +33 dBm P1dB at 940 MHz
- +50 dBm Output IP3 at 940 MHz
- 20.8 dB Gain at 940 MHz
- +5V Single Supply, 455 mA Current
- Patented internal RF overdrive protection
- Patented internal DC overvoltage protection
- On chip ESD protection
- Shut-down capability
- Capable of handling 10:1 VSWR at Vcc=+5 V, 0.9 GHz, 33 dBm CW Pout or 23.5 dBm WCDMA Pout

Functional Block Diagram



General Description

The TQP7M9106 is a high linearity, high gain 2W driver amplifier in industry standard, RoHS compliant, QFN surface mount package. This InGaP/GaAs HBT delivers high performance across 0.05 to 1.5 GHz range of frequencies while achieving 20.8 dB gain, +50 dBm OIP3 and +33 dBm P1dB at 940MHz while only consuming 455 mA quiescent current. All devices are 100% RF and DC tested.

The TQP7M9106 incorporates patented on-chip circuit techniques that differentiate it from other products in the market. The amplifier integrates an on-chip DC over-voltage and RF over-drive protection. This protects the amplifier from electrical DC voltage surges and high input RF input power levels that may occur in a system.

The TQP7M9106 is targeted for use as a driver amplifier in wireless infrastructure where high linearity, medium power, and high efficiency are required. The device is an excellent candidate for transceiver line cards and high power amplifiers in current and next generation multi-carrier 3G / 4G base stations.

Pin Configuration

Pin No.	Symbol
1	Vbias
4, 5	RFin
14, 15, 16	RFout/Vcc
18	Iref
2, 3, 6-13, 17, 19-24	GND/NC

Ordering Information

Part No.	Description
TQP7M9106	2 W High Linearity Amplifier
TQP7M9106-PCB900	920−960 MHz Evaluation Board

Standard T/R size = 2500 pieces on a 13” reel.

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to 150°C
RF Input Power, CW, 50Ω, T=25°C	+30 dBm
Device Voltage (V_{CC})	+8 V

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Device Voltage (V_{CC})	4.75	5.0	5.25	V
Case Temperature	-40		+85	°C
Tj for >10^6 hours MTTF			+170	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

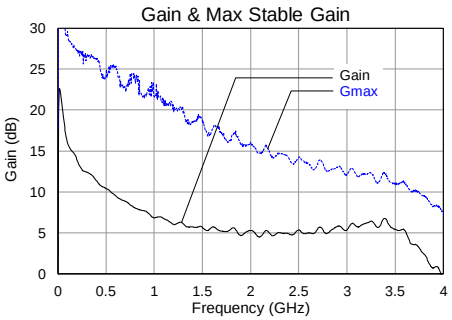
Test conditions unless otherwise noted: V_{CC}=+5 V, Temp= +25°C, tuned application circuit

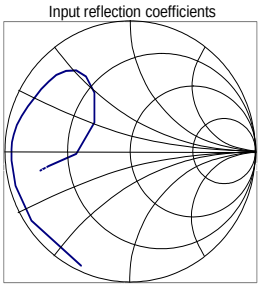
Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		50		1500	MHz
Test Frequency			940		MHz
Gain		19	20.8	22	dB
Input Return Loss			9.2		dB
Output Return Loss			12.7		dB
Output P1dB		32	+33.1		dBm
Output IP3	Pout = +17 dBm/tone, Δf = 1 MHz	+46	+50.3		dBm
WCDMA Channel Power	ACLR=-50 dBc (1)		+23.5		dBm
Noise Figure			4.8		dB
Quiescent Current (I_{CQ})		360	455	510	mA
Reference Current (I_{ref})			8.9		mA
Thermal Resistance, θ_{jc}	Junction to case		17.2		°C/W

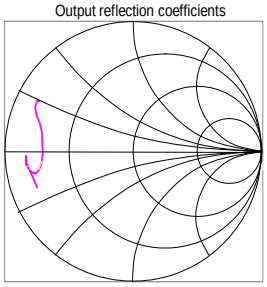
Notes:

1. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 9.7 dB at 0.01% Prob.

Device Characterization Data







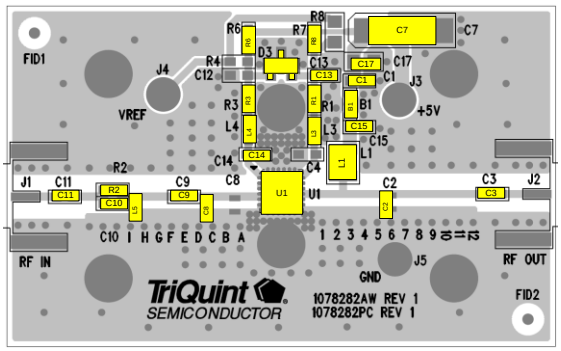
Note: The gain for the unmatched device in 50 ohm system is shown as the trace in black color, [gain (S(21)]. For a tuned circuit for a particular frequency, it is expected that actual gain will be higher, up to the maximum stable gain. The maximum stable gain is shown as the blue trace [Gmax]. The impedance plots are shown from 0.05 – 4 GHz.

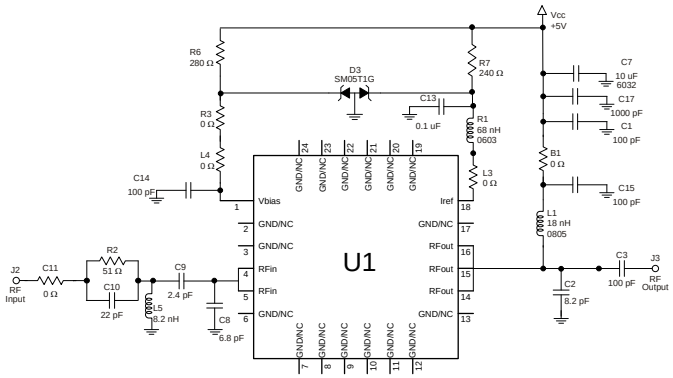
S-Parameters

Test Conditions: V_{CC}=+5 V, I_{CQ}=450 mA, T=+25°C, unmatched 50 ohm system, calibrated to device leads

Freq (GHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
0.05	-0.44	-114.25	19.78	144.69	-42.10	39.11	-1.98	-159.88
0.1	-0.52	-146.09	16.00	138.73	-43.22	20.45	-1.71	-170.16
0.2	-0.50	-164.26	13.87	132.03	-40.75	6.76	-1.50	-175.13
0.4	-0.54	-176.18	11.35	121.63	-40.83	3.60	-1.55	-177.80
0.6	-0.53	178.67	9.50	112.30	-41.24	0.84	-1.56	-176.22
0.8	-0.56	175.24	8.04	104.69	-40.31	1.88	-1.53	-175.02
1.0	-0.62	171.69	6.85	98.63	-39.99	3.20	-1.53	-173.42
1.2	-0.72	167.05	6.03	91.72	-39.96	4.12	-1.56	-172.13
1.4	-0.89	162.02	5.70	85.91	-39.07	0.13	-1.69	-171.07
1.6	-1.08	156.59	5.69	79.97	-37.92	-5.54	-1.79	-169.68
1.8	-1.27	150.93	5.48	72.26	-37.57	-7.78	-1.95	-168.21
2.0	-1.38	145.46	5.28	63.03	-36.04	-20.25	-2.21	-167.59
2.2	-1.48	139.99	4.89	53.16	-36.36	-23.44	-2.57	-169.42
2.4	-1.62	134.72	4.85	45.77	-35.84	-33.51	-2.83	-173.07
2.6	-1.90	129.34	5.02	36.67	-34.86	-43.30	-3.01	-178.95
2.8	-2.39	124.31	4.93	26.06	-34.10	-48.61	-2.94	174.59
3.0	-3.38	121.03	5.32	14.17	-33.25	-62.68	-2.76	167.99
3.2	-5.41	121.85	6.17	-3.37	-32.23	-83.93	-2.38	163.09
3.4	-8.79	141.69	6.71	-26.85	-31.82	-110.34	-1.88	159.52
3.6	-7.36	-178.09	5.31	-52.42	-32.46	-138.25	-1.53	155.58
3.8	-3.69	-170.72	0.70	-76.13	-36.73	-172.04	-1.47	151.81
4.0	-2.78	-168.72	-0.74	-86.65	-37.56	176.73	-1.65	152.04

TQP7M9106-PCB900 Evaluation Board (920-960 MHz)





Notes:

1. Components shown on the silkscreen but not on the schematic are not used.
2. 0 Ω resistor can be replaced with copper trace in the target application layout.
3. To power down the device, voltage can be applied to V_{ref} to control I_{ref} by placing resistor R8 and removing R7.
4. The recommended component values are dependent upon the frequency of operation.
5. All components are of 0603 size unless stated on the schematic.
6. R1 is critical for device linearity performance.
7. Critical component placement locations:
   - Distance between center of C8 and TQP7M9106 (U1) device package is 243 mil (11.7º at 940MHz)
   - Distance between center of L5 and TQP7M9106 (U1) device package is 452 mil (21.8º at 940MHz)
   - Distance between center of C9 and TQP7M9106 (U1) device package is 275 mil (13.3º at 940MHz)
   - Distance between center of C2 and TQP7M9106 (U1) device package is 355 mil (17.2º at 940MHz)

Bill of Material – TQP7M9106-PCB900

Reference Des.	Value	Description	Manuf.	Part Number
U1	n/a	2W High Linearity Amplifier	TriQuint	TQP7M9106
n/a	n/a	Printed Circuit Board	TriQuint	
D3	n/a	Zener, dual, SOT-23	various	
B1, L3, L4, R3, C11	0 Ω	Resistor, Chip, 0603, 5%, 1/16W	various	
R2	51 Ω	Resistor, Chip, 0603, 5%, 1/16W	various	
R6	280 Ω	Resistor, Chip, 0603, 1%, 1/16W	various	
R7	240 Ω	Resistor, Chip, 0603, 1%, 1/16W	various	
C2	8.2 pF	Capacitor, Chip, 0603, ±0.05pF, 50 V, Accu-P	AVX	06035J8R2ABSTR
C7	10 uF	Capacitor , Tantalum, 6032, 35V, 10%	various	
C8	6.8pF	Capacitor, Chip, 0603, ±0.05pF, 50 V, Accu-P	AVX	06035J6R8ABSTR
C9	2.4 pF	Capacitor, Chip, 0603, ±0.05pF, 50 V, Accu-P	AVX	06035J2R4ABSTR
C10	22 pF	Capacitor, Chip, 0603, 5%, 50 V, NPO/COG	various	
C1, C3, C14, C15	100 pF	Capacitor, Chip, 0603, 5%, 50V, NPO/COG	various	
C13	0.1 uF	Capacitor, Chip, 0603, 50V, X5R, 10%	various	
C17	1000 pF	Capacitor, Chip, 0603, 10%, 50V, NPO/COG	various	
L1	18 nH	Inductor, 0805, 5%, Coilcraft CS Series	Coilcraft	0805CS-180XJLB
L5	8.2 nH	Inductor, 0603, 5%	Toko	LL1608-FSL8N2
R1	68 nH	Inductor, 0603, 5%	Toko	LL1608-FSL68N
R4, C12, C4	n/a	Do Not Place		

Typical Performance – TQP7M9106-PCB900

Test conditions unless otherwise noted: V_{CC}=+5 V, Temp=+25°C

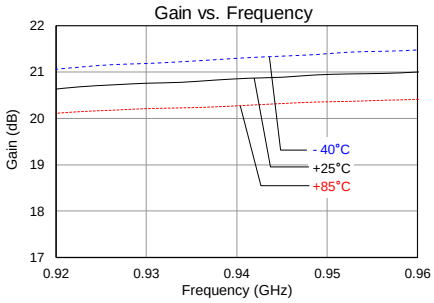
Parameter	Conditions	Typical Value			Units
Frequency		920	940	960	MHz
Gain		20.6	20.8	21	dB
Input Return Loss		8.5	9.2	9.4	dB
Output Return Loss		11.3	12.7	14.9	dB
Output P1dB		+32.9	+33.1	+33.2	dBm
Output IP3	Pout= +17 dBm/tone, Δf=1 MHz	+49.8	+50.3	+50.5	dBm
WCDMA Channel Power	ACLR=-50 dBc (1)	+23.3	+23.5	+23.5	dBm
Noise Figure		4.8	4.8	4.8	dB
Quiescent Collector Current, I_{CQ}			455		mA

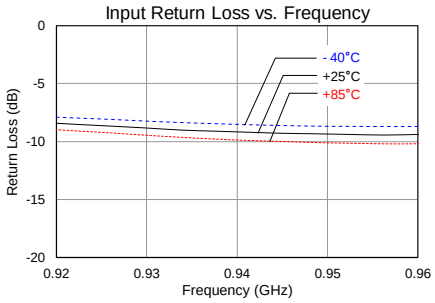
Notes:

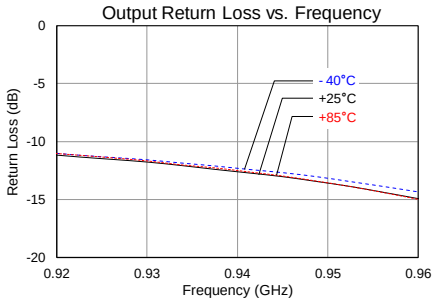
1. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 9.7 dB at 0.01% Prob.

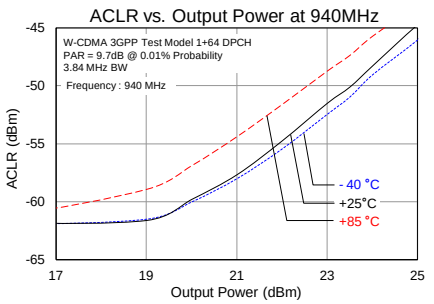
Performance Plots – TQP7M9106-PCB900

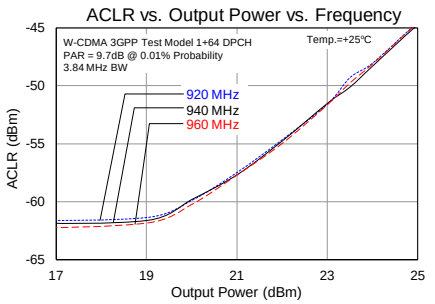
Test conditions unless otherwise noted: V_{CC}=+5 V, Temp=+25°C

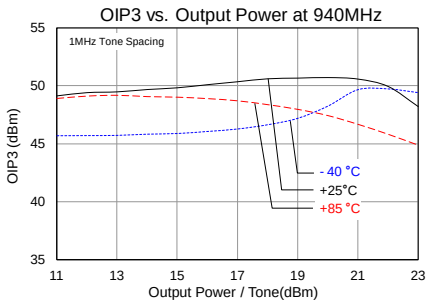


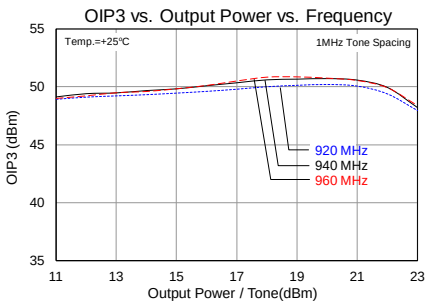


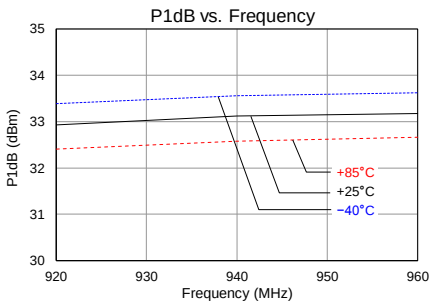


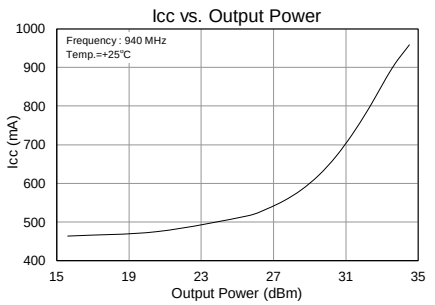




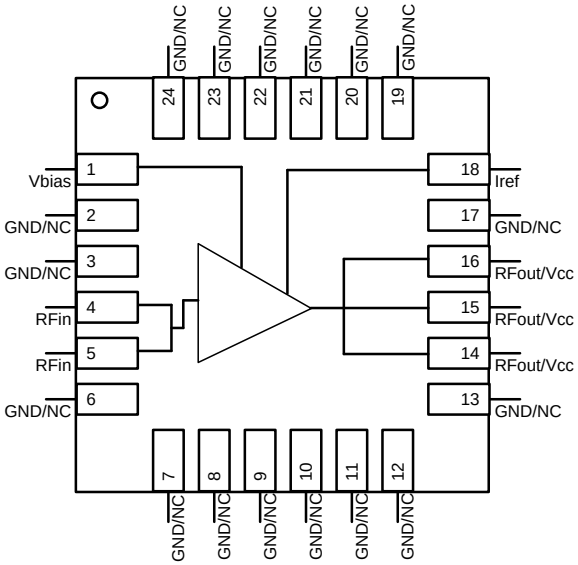








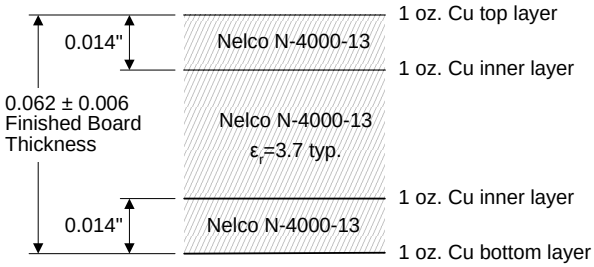
Pin Configuration and Description



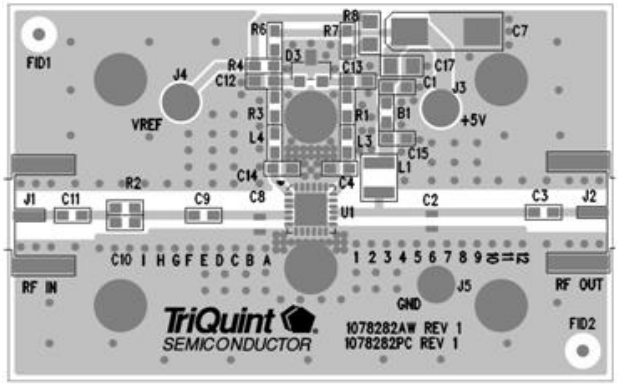
Pin No.	Symbol	Description
1	Vbias	Voltage supply for active bias for the amp. Connect to same supply voltage as Vcc.
4, 5	RF IN	RF Input. Requires external match for optimal performance. External DC Block required.
14, 15, 16	RFout / V_{cc}	RF Output. Requires external match for optimal performance. External DC Block and supply voltage is required.
18	I_{ref}	Reference current into internal active bias current mirror. Current into I_{ref} sets device quiescent current. Also, can be used as on/off control.
2, 3, 6-13, 17, 19-24	GND	RF/DC Ground Connection
Backside Paddle	RF/DC GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance. See PCB Mounting Pattern for suggested footprint.

Evaluation Board PCB Information

TriQuint PCB 1078282 Material and Stack-up

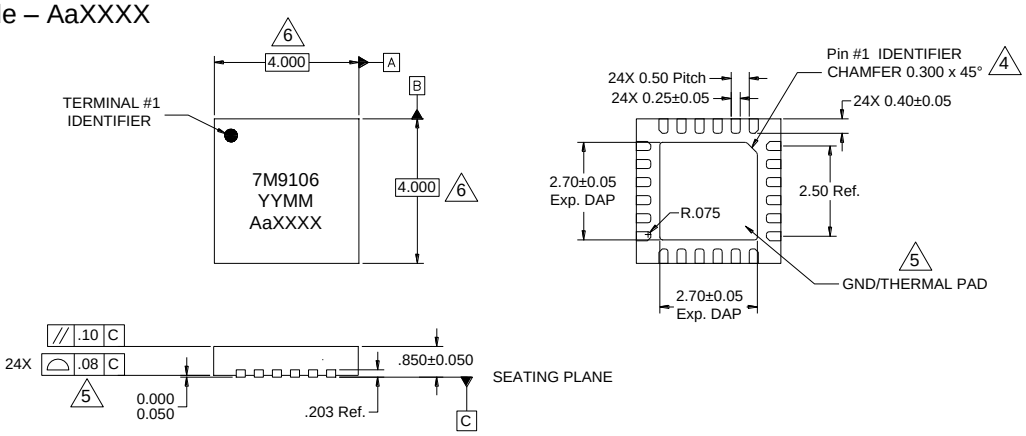


50 ohm line dimensions: width = .031”
spacing = .035"



Package Marking and Dimensions

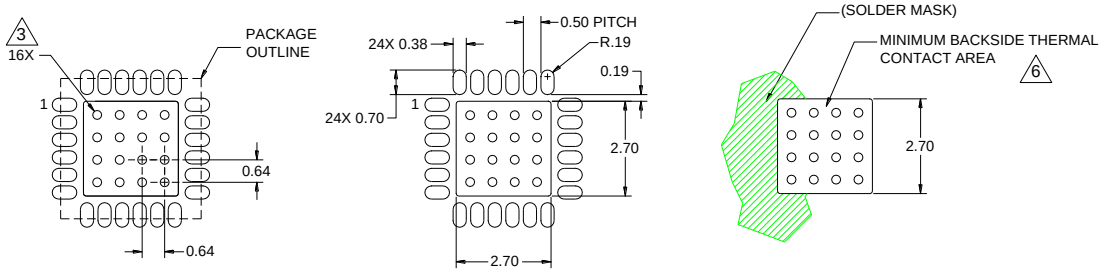
Marking: Part Number – 7M9106
Date Code – YYMM
Lot code – AaXXXX



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Except where noted, this part outline conforms to JEDEC standard MO-220, Issue E (Variation VGGC) for thermally enhanced plastic very thin fine pitch quad flat no lead package (QFN).
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
5. Co-planarity applies to the exposed ground/thermal pad as well as the contact pins.
6. Package body length/width does not include plastic flash protrusion across mold parting line.

PCB Mounting Pattern



COMPONENT SIDE

BACK SIDE

Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25mm (0.10”).
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.
5. Place mounting screws near the part to fasten a back side heat sink.
6. Do not apply solder mask to the back side of the PC board in the heat sink contact region.
7. Ensure that the backside via region makes good physical contact with the heat sink.

Product Compliance Information

ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating:	Class 1C
Value:	≥ 1000 V and < 2000 V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114

ESD Rating:	Class IV
Value:	Passes ≥ 1000 V
Test:	Charged Device Model (CDM)
Standard:	JEDEC Standard JESD22-C101

MSL Rating

MSL Rating:	Level 1
Test:	260°C convection reflow
Standard:	JEDEC Standard IPC/JEDEC J-STD-020

Solderability

Compatible with both lead-free (260°C maximum reflow temperature) and tin/lead (245°C maximum reflow temperature) soldering processes.

Contact plating: Annealed matte tin over copper.

RoHs Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

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Email: info-sales@tqs.com **Fax:** +1.503.615.8902

For technical questions and application information: **Email:** sjcapplications.engineering@tqs.com

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