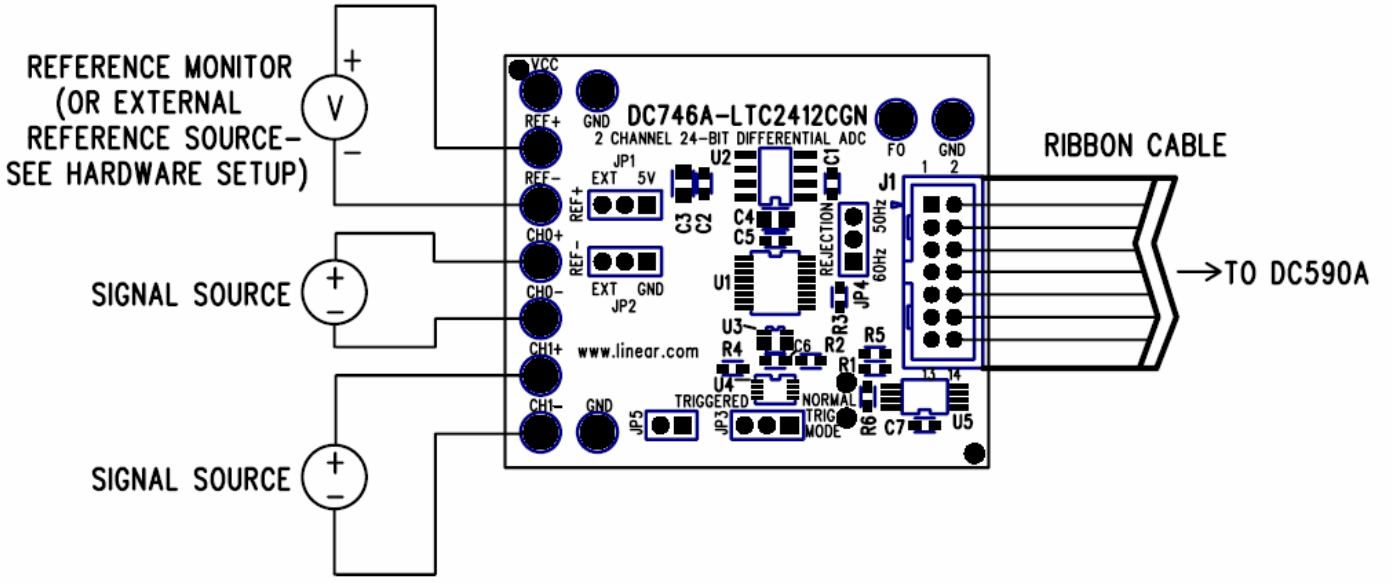
DESCRIPTION

Demonstration circuit 746 features the LTC2412, a 2 channel, 24-bit high performance ΔΣ analog-to-digital converter (ADC). The LTC2412 features 2ppm linearity, 2.5ppm full-scale accuracy, 0.1ppm offset, and 0.16ppm noise. The inputs and reference are fully differential, with input common mode rejection of 140 dB. The LTC2412 is available in a 16 pin GN package and has an easy to use SPI interface.

DC746 is a member of Linear Technology's QuickEval™ family of demonstration boards. It is designed to allow easy evaluation of the LTC2412 and may be connected directly to the target application's analog signals while using the DC590 USB Serial Controller board and supplied software to measure performance. The exposed ground planes allow proper grounding to prototype circuitry. After evaluating with Linear Technology's software, the digital signals can be connected to the end application's processor / controller for development of the serial interface.

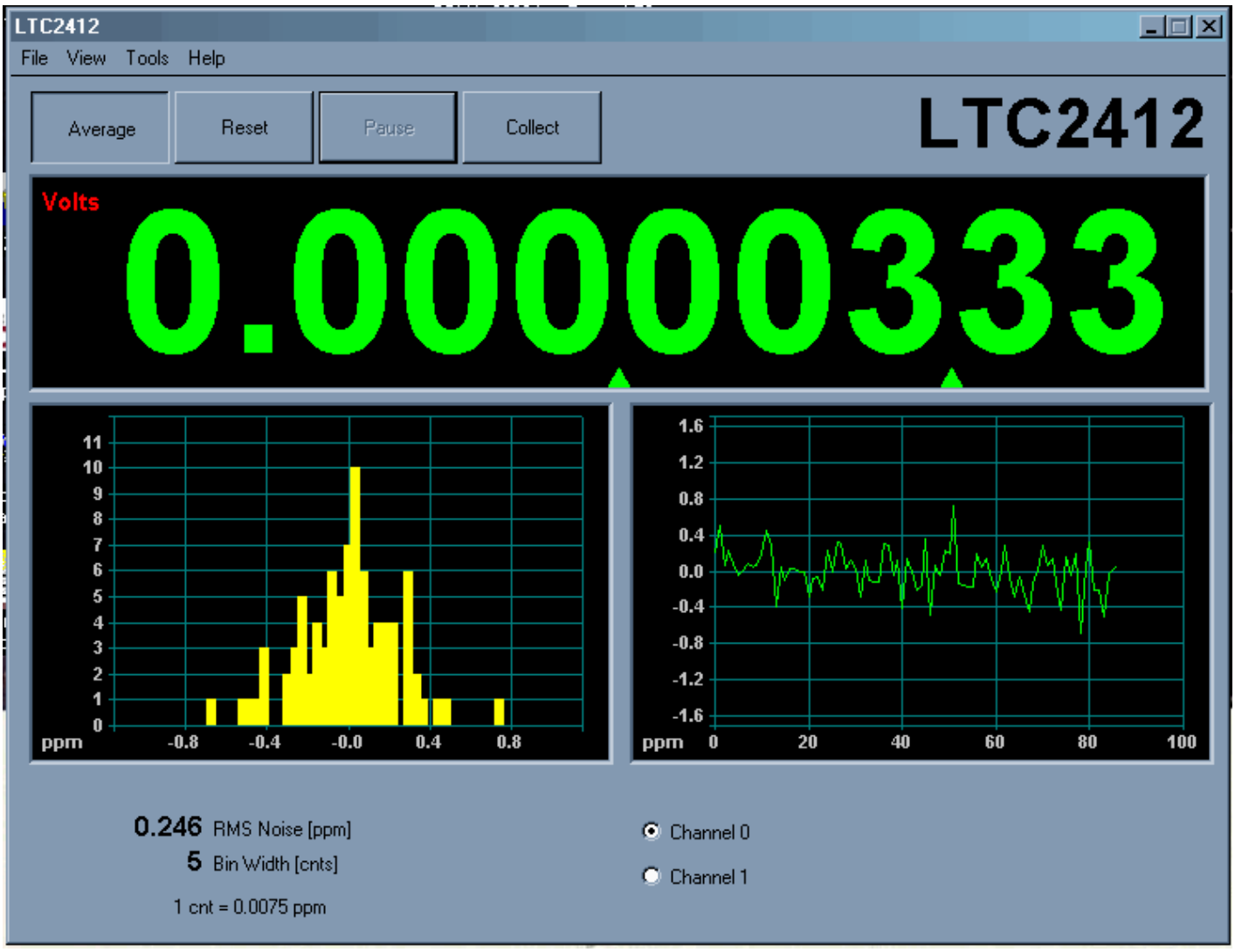
Design files for this circuit board are available. Call the LTC factory.



QUICK START PROCEDURE

Connect DC746 to a DC590 USB Serial Controller using the supplied 14 conductor ribbon cable. Connect DC590 to a host PC with a standard USB A/B cable. Run the evaluation software supplied with DC590 or downloaded from www.linear.com. The correct program will be loaded automatically. Click the COLLECT button to start reading the input voltage. Details on software features are documented in the control panel's help menu.

Tools are available for logging data, changing reference voltage, changing the number of points in the strip chart and histogram, and changing the number of points averaged for the DVM display.



HARDWARE SET-UP

JUMPERS

JP1 – Select the source for REF+, either external or 5.00 volts from the onboard LT1236 reference (default.)

JP2 – Select the source for REF-, either external or Ground (0 volts, default.)

JP3 – Trigger mode, either normal (default) or externally triggered.

JP4 – Notch frequency. This selects either 50Hz or 60Hz rejection mode. Remove this jumper when supplying an external clock to the Fo turret.

JP5 – Trigger input signal. Pin 1 is a 5 volt logic signal, pin 2 is ground. When triggered mode is selected on JP3, a rising edge starts a new conversion.

CONNECTION TO DC590 SERIAL CONTROLLER

J2 is the power and digital interface connector. Connect to DC590 serial controller with supplied 14 conductor ribbon cable.

An external conversion clock may be applied to the Fo turret to modify the frequency rejection characteristics or data output rate of the LTC2412. Be sure to remove JP4 before applying an external clock. This should be a square wave with a low level equal to ground and a high level equal to Vcc. While up to a 2MHz clock can be used, performance may be compromised. Refer to the LTC2412 data sheet.

ANALOG CONNECTIONS

Analog signal connections are made via the row of turret posts along the edge of the board. Also, when connecting the board to an existing circuit, the exposed ground planes along the edges of the board may be used to form a solid connection between grounds.

GND – Ground turrets are connected directly to the internal ground planes.

VCC – This is the supply for the ADC. Do not draw any power from this point.

REF+, REF- – These are connected to the LTC2412 REF+ and REF- pins. If the onboard reference is being used, the reference voltage may be monitored from this point. An external reference may be connected to these terminals if JP1 and JP2 are configured for external reference.

CH0+, CH0-, CH1+, CH1- – These are the differential inputs to the LTC2412.

EXPERIMENTS

INPUT NOISE

Solder a short wire from the IN- turret post to the IN+ turret post. Noise should be approximately 0.16ppm (800nV.)

COMMON MODE REJECTION

Tie the two inputs (still connected together) to ground through a short wire and note the indicated voltage. Tie the inputs to REF+; the difference should be less than 1.6uV due to the 130 dB CMRR of the LTC2412.

RESOLVING MILLIAMPS WITH MILLIOHM SHUNTS

One application that can benefit greatly from the LTC2412's input resolution is current measurement. It is advantageous to use a very low resistance shunt to minimize the voltage drop. To demonstrate this, make a simple current shunt by soldering a 1 inch length of 24 gauge copper wire from the CH0+ turret to the CH0- turret. This is a resistance of ap-

proximately 2.4 milliohms. Connect the CH0- turret to the GND turret through a short wire. Start the demonstration software and note the initial voltage, which should be close to zero. Next, connect IN+ to REF+ through a 1k resistor, which will allow approximately 5mA to flow through the shunt. The indicated voltage should increase by approximately 12uV (The actual increase will depend on the tolerance of the wire material, diameter, and length.)

Since the common mode range of the inputs extends from ground to VCC, the current shunt can also be used at the "high side." To do this, tie the IN+ turret to VCC and connect the resistor from IN- to ground. Thus the current of a circuit can be monitored with minimal impact on supply voltage and without breaking any ground connections.

BIPOLAR SYMMETRY

To demonstrate the symmetry of the ADCs transfer function, connect a stable, low noise, floating voltage source (with a voltage less than Vref/2) from CH0+ to CH0- and note the indicated voltage. Reverse the polarity; the indicated voltage will typically be within 15uV of the first reading multiplied by –1.

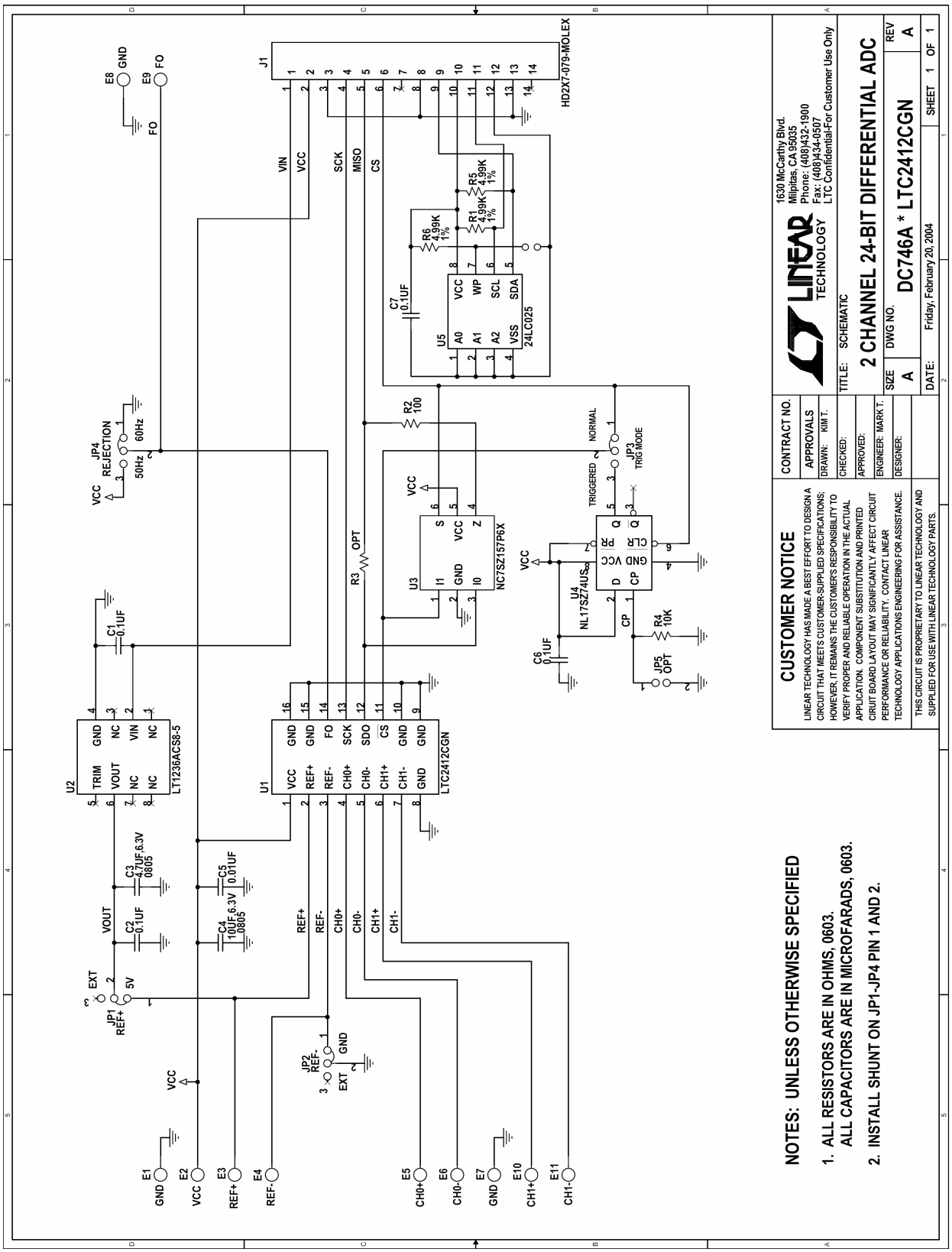
One convenient voltage source for this experiment is a single alkaline battery. While a battery has fairly low noise, it is sensitive to temperature drift. It is best to use a large (D-size) battery that is insulated from air currents. A better source is a battery powered series reference such as the LT1790. This part is available with output voltages of 1.25V, 2.048V, 2.5V, 3V, 3.3V, 4.096V and 5V.

INPUT NORMAL MODE REJECTION

The LTC2412's SINC4 digital filter is trimmed to strongly reject 50 or 60Hz line noise when operated with the internal conversion clock. To measure input normal mode rejection, connect CH0- to a 2.5 volt source such as an LT1790-2.5 reference or a power supply. Apply a 10Hz, 2V peak-to-peak sine wave to CH0+ through a 1uF capacitor. No DC bias is required because the 2-3MΩ input impedance of the LTC2412 tends to self-bias the input to mid-reference (see datasheet applications information for details.)

Start taking data. The input noise will be quite large, and the graph of output vs. time should show large variations.

Next, slowly increase the frequency to 60Hz. The noise should be almost undetectable in the graph. Note that the indicated noise in ppm may still be above that of the datasheet specification because the inputs are not connected to a DC source.


NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS, 0603.
ALL CAPACITORS ARE IN MICROFARADS, 0603.
2. INSTALL SHUNT ON JP1-JP4 PIN 1 AND 2.
CUSTOMER NOTICE
LINEAR TECHNOLOGY HAS MADE A BEST EFFORT TO DESIGN A CIRCUIT THAT MEETS CUSTOMER-SUPPLIED SPECIFICATIONS; HOWEVER, IT REMAINS THE CUSTOMER'S RESPONSIBILITY TO VERIFY PROPER AND RELIABLE OPERATION IN THE ACTUAL APPLICATION. COMPONENT SUBSTITUTION AND PRINTED CIRUIT BOARD LAYOUT MAY SIGNIFICANTLY AFFECT CIRCUIT PERFORMANCE OR RELIABILITY. CONTACT LINEAR TECHNOLOGY APPLICATIONS ENGINEERING FOR ASSISTANCE.
THIS CIRCUIT IS PROPRIETARY TO LINEAR TECHNOLOGY AND SUPPLIED FOR USE WITH LINEAR TECHNOLOGY PARTS.
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LTC Confidential-For Customer Use Only
TITLE: SCHEMATIC
2 CHANNEL 24-BIT DIFFERENTIAL ADC
SIZE A
DWG NO. DC746A * LTC2412CGN
REV A
DATE: Friday, February 20, 2004
SHEET 1 OF 1
U1 LTC2412CGN
U2 LT1236ACS8-5
U3 NC7SZ157P6X
U4 NL17SZ74USG
U5 24LC025
J1 HD2X7-079-MOLEX
JP1 REF+ EXT 5V VOUT
JP2 REF- EXT GND
JP3 TRIG MODE TRIGGERED NORMAL
JP4 REJECTION 50Hz 60Hz
JP5 OPT
R1 4.99K 1%
R2 100
R3 OPT
R4 10K
R5 4.99K 1%
R6 4.99K 1%
C1 0.1UF
C2 0.1UF
C3 4.7UF,6.3V 0805
C4 10UF,6.3V 0805
C5 0.01UF
C6 0.1UF
C7 0.1UF
E1 GND
E2 VCC
E3 REF+
E4 REF-
E5 CH0+
E6 CH0-
E7 GND
E10 CH1+
E11 CH1-
E8 GND
E9 FO