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# MB9A140NB Series

# 32-bit ARM® Cortex®-M3 FM3 Microcontroller

The MB9A140NB Series are highly integrated 32-bit microcontrollers dedicated for embedded controllers with low-power consumption mode and competitive cost.

These series are based on the ARM Cortex-M3 Processor with on-chip Flash memory and SRAM, and have peripheral functions such as various timers, ADCs, and Communication Interfaces (UART, CSIO, $I^2C$).

The products which are described in this datasheet are placed into TYPE6 product categories in FM3 Family Peripheral Manual.

## Features

### 32-bit ARM® Cortex®-M3 Core

- Processor version: r2p1
- Up to 40 MHz Frequency Operation
- Integrated Nested Vectored Interrupt Controller (NVIC): 1 NMI (non-maskable interrupt) and 48 peripheral interrupts and 16 priority levels
- 24-bit System timer (Sys Tick): System timer for OS task management

### On-chip Memories

#### [Flash memory]

- Dual operation Flash memory
  - Dual Operation Flash memory has the upper bank and the lower bank.
    So, this series could implement erase, write and read operations
    for each bank simultaneously.
  - Main area: Up to 256 Kbytes (Up to 240 Kbytes upper bank + 16 Kbytes lower bank)
  - Work area: 32 Kbytes (lower bank)
- Read cycle: 0 wait-cycle
- Security function for code protection

#### [SRAM]

This Series on-chip SRAM is composed of two independent SRAM (SRAM0, SRAM1). SRAM0 is connected to I-code bus and D-code bus of Cortex-M3 core. SRAM1 is connected to System bus.

- SRAM0: Up to 16 KB
- SRAM1: Up to 16 KB

### External Bus Interface*

- Supports SRAM, NOR Flash memory device
- Up to 8 chip selects
- 8-/16-bit Data width
- Up to 25-bit Address bit
- Maximum area size: Up to 256 MB
- Supports Address/Data multiplex
- Supports external RDY function

*: MB9AF141LB, F142LB and F144LB do not support External Bus Interface.

### Multi-function Serial Interface (Max 8 channels)

- 4 channels with 16 steps×9-bit FIFO (ch.4 to ch.7), 4 channels without FIFO (ch.0 to ch.3)
- Operation mode is selectable from the followings for each channel.
  - UART
  - CSIO
  - I2C

#### [UART]

- Full-duplex double buffer
- Selection with or without parity supported
- Built-in dedicated baud rate generator
- External clock available as a serial clock
- Hardware Flow control*: Automatically control the transmission by CTS/RTS (only ch.4)
- Various error detection functions available (parity errors, framing errors, and overrun errors)

*: MB9AF141LB, F142LB and F144LB do not support Hardware Flow control.

### [CSIO]

- Full-duplex double buffer
- Built-in dedicated baud rate generator
- Overrun error detection function available

### [I²C]

Standard-mode (Max 100 kbps) / Fast-mode (Max 400 kbps) supported

### DMA Controller (8 channels)

The DMA Controller has an independent bus from the CPU, so CPU and DMA Controller can process simultaneously.

- 8 independently configured and operated channels
- Transfer can be started by software or request from the built-in peripherals
- Transfer address area: 32-bit (4 GB)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: byte/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

### A/D Converter (Max 24 channels)

### [12-bit A/D Converter]

- Successive Approximation type
- Built-in 2 units
- Conversion time: 2.0 µs @ 2.7 V to 3.6 V
- Priority conversion available (priority at 2 levels)
- Scanning conversion mode
- Built-in FIFO for conversion data storage (for SCAN conversion: 16 steps, for Priority conversion: 4 steps)

### Base Timer (Max 8 channels)

Operation mode is selectable from the followings for each channel.

- 16-bit PWM timer
- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer

### General-Purpose I/O Port

This series can use its pins as general-purpose I/O ports when they are not used for external bus or peripherals. Moreover, the port relocate function is built in. It can set which I/O port the peripheral function can be allocated to.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in the port relocate function
- Up to 83 fast general-purpose I/O Ports@100 pin Package
- Some ports are 5 V tolerant I/O.
  See Pin Description to confirm the corresponding pins.

### Dual Timer (32-/16-bit Down Counter)

The Dual Timer consists of two programmable 32-/16-bit down counters.
Operation mode is selectable from the followings for each channel.

- Free-running
- Periodic (=Reload)
- One-shot

### HDMI-CEC/Remote Control Receiver (Up to 2 channels)

- HDMI-CEC transmitter
  - Header block automatic transmission by judging Signal free
  - Generating status interrupt by detecting Arbitration lost
  - Generating START, EOM, ACK automatically to output CEC transmission by setting 1 byte data
  - Generating transmission status interrupt when transmitting 1 block (1 byte data and EOM/ACK)
- HDMI-CEC receiver
  - Automatic ACK reply function available
  - Line error detection function available
- Remote control receiver
  - 4 bytes reception buffer
  - Repeat code detection function available

### Real-time clock (RTC)

The Real-time clock can count Year/Month/Day/Hour/Minute/Second/A day of the week from 00 to 99.

- The interrupt function with specifying date and time (Year/Month/Day/Hour/Minute) is available. This function is also available by specifying only Year, Month, Day, Hour or Minute.
- Timer interrupt function after set time or each set time.
- Capable of rewriting the time with continuing the time count.
- Leap year automatic count is available.

### Watch Counter

The Watch counter is used for wake up from sleep and timer mode.

Interval timer: up to 64 s (Max) @ Sub Clock: 32.768 kHz

### External Interrupt Controller Unit

- Up to 16 external interrupt input pins
- Include one non-maskable interrupt (NMI) input pin

### Watchdog Timer (2 channels)

A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs, a Hardware watchdog and a Software watchdog.

The Hardware watchdog timer is clocked by the built-in low-speed CR oscillator. Therefore, the Hardware watchdog is active in any low-power consumption modes except RTC, Stop, Deep Standby RTC and Deep Standby Stop modes.

### CRC (Cyclic Redundancy Check) Accelerator

The CRC accelerator calculates the CRC which has a heavy software processing load, and achieves a reduction of the integrity check processing load for reception data and storage.

CCITT CRC16 and IEEE-802.3 CRC32 are supported.

- CCITT CRC16 Generator Polynomial: 0x1021
- IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

### Clock and Reset

#### [Clocks]

Selectable from five clock sources (2 external oscillators, 2 built-in CR oscillators, and Main PLL).

- Main Clock: 4 MHz to 48 MHz
- Sub Clock: 32.768 kHz
- Built-in high-speed CR Clock: 4 MHz
- Built-in low-speed CR Clock: 100 kHz
- Main PLL Clock

#### [Resets]

- Reset requests from INITX pin
- Power on reset
- Software reset
- Watchdog timers reset
- Low-voltage detection reset
- Clock Super Visor reset

### Clock Super Visor (CSV)

Clocks generated by built-in CR oscillators are used to supervise abnormality of the external clocks.

- External clock failure (clock stop) is detected, reset is asserted.
- External frequency anomaly is detected, interrupt or reset is asserted.

### Low-Voltage Detector (LVD)

This Series includes 2-stage monitoring of voltage on the VCC pins. When the voltage falls below the voltage that has been set, Low-Voltage Detector generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

### Low-Power Consumption Mode
Six low-power consumption modes supported.

- Sleep
- Timer
- RTC
- Stop
- Deep Standby RTC (selectable between keeping the value of RAM and not)
- Deep Standby Stop (selectable between keeping the value of RAM and not)

### Debug
- Serial Wire JTAG Debug Port (SWJ-DP)
- Embedded Trace Macrocells (ETM)*

  *: MB9AF141LB/MB, F142LB/MB and F144LB/MB support only SWJ-DP.

### Unique ID
Unique value of the device (41-bit) is set.

### Power Supply
Wide range voltage: VCC = 1.65 V to 3.6 V

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# 1. Product Lineup

## Memory Size

| Product name | | MB9AF141LB/MB/NB | MB9AF142LB/MB/NB | MB9AF144LB/MB/NB |
|---|---|---|---|---|
| On-chip Flash memory | Main area | 64 KB | 128 KB | 256 KB |
| | Work area | 32 KB | 32 KB | 32 KB |
| On-chip SRAM | SRAM0 | 8 KB | 8 KB | 16 KB |
| | SRAM1 | 8 KB | 8 KB | 16 KB |
| | Total | 16 KB | 16 KB | 32 KB |

## Function

| Product name | | MB9AF141LB<br>MB9AF142LB<br>MB9AF144LB | MB9AF141MB<br>MB9AF142MB<br>MB9AF144MB | MB9AF141NB<br>MB9AF142NB<br>MB9AF144NB |
|---|---|---|---|---|
| Pin count | | 64 | 80/96 | 100/112 |
| CPU | | Cortex-M3 | | |
| | Freq. | 40 MHz | | |
| Power supply voltage range | | 1.65 V to 3.6 V | | |
| DMAC | | 8 ch. | | |
| External Bus Interface | | - | Addr: 21-bit (Max)<br>R/W Data: 8-bit (Max)<br>CS: 4 (Max)<br>Support: SRAM, NOR Flash memory | Addr: 25-bit (Max)<br>R/W Data: 8-/16-bit (Max)<br>CS: 8 (Max)<br>Support: SRAM, NOR Flash memory |
| Multi-function Serial Interface (UART/CSIO/I$^2$C) | | 8 ch. (Max)<br>ch.4 to ch.7: FIFO (16steps × 9-bit)<br>ch.0 to ch.3: No FIFO | | |
| Base Timer (PWC/Reload timer/PWM/PPG) | | 8 ch. (Max) | | |
| Dual Timer | | 1 unit | | |
| HDMI-CEC/ Remote Control Receiver | | 2 ch. (Max) | | |
| Real-Time Clock | | 1 unit | | |
| Watch Counter | | 1 unit | | |
| CRC Accelerator | | Yes | | |
| Watchdog timer | | 1ch. (SW) + 1ch. (HW) | | |
| External Interrupts | | 8 pins (Max) + NMI × 1 | 11 pins (Max) + NMI × 1 | 16 pins (Max) + NMI × 1 |
| I/O ports | | 51 pins (Max) | 66 pins (Max) | 83 pins (Max) |
| 12-bit A/D converter | | 12 ch. (2 units) | 17 ch. (2 units) | 24 ch. (2 units) |
| CSV (Clock Super Visor) | | Yes | | |
| LVD (Low-Voltage Detector) | | 2 ch. | | |
| Built-in CR | High-speed | 4 MHz | | |
| | Low-speed | 100 kHz | | |
| Debug Function | | SWJ-DP | | SWJ-DP/ETM |
| Unique ID | | Yes | | |

***Note:***

- *All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the I/O port according to your function use. See 12. Electrical Characteristics 12.4. AC Characteristics 12.4.3. Built-in CR Oscillation Characteristics for accuracy of built-in CR.*

## 2. Packages

| Package \ Product name | MB9AF141LB<br>MB9AF142LB<br>MB9AF144LB | MB9AF141MB<br>MB9AF142MB<br>MB9AF144MB | MB9AF141NB<br>MB9AF142NB<br>MB9AF144NB |
|---|---|---|---|
| LQFP: LQD064 (0.5 mm pitch) | ❍ | - | - |
| LQFP: LQG064 (0.65 mm pitch) | ❍ | - | - |
| QFN: VNC064 (0.5 mm pitch) | ❍ | - | - |
| LQFP: LQH080 (0.5 mm pitch) | - | ❍ | - |
| LQFP: LQJ080 (0.65 mm pitch) | - | ❍ | - |
| BGA: FDG096 (0.5 mm pitch) | - | ❍ | - |
| LQFP: LQI100 (0.5 mm pitch) | - | - | ❍ |
| QFP: PQH100 (0.65 mm pitch) | - | - | ❍ |
| BGA: LBC112 (0.8 mm pitch) | - | - | ❍ |

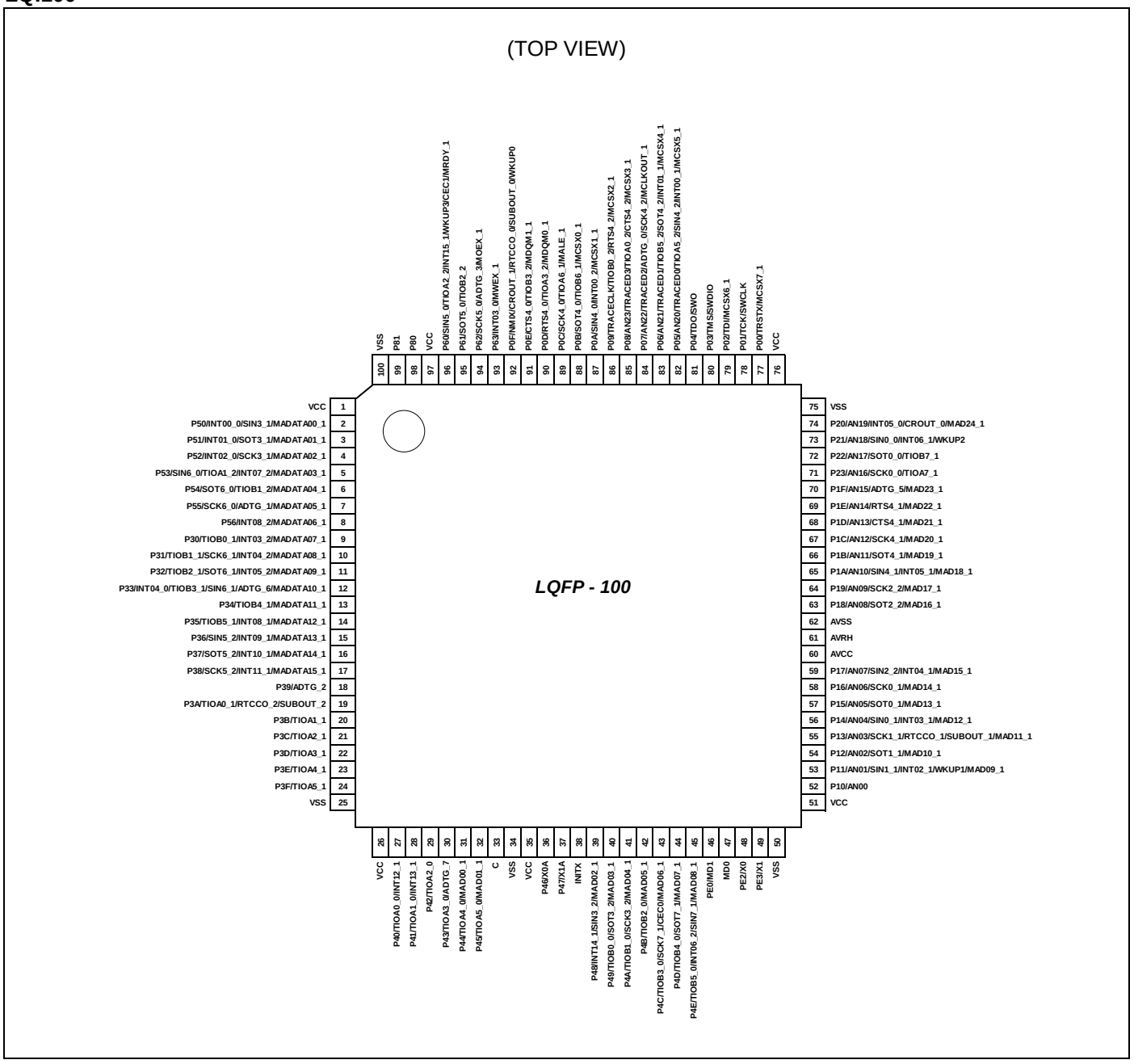
❍: Supported

***Note:***

- *See "14. Package Dimensions" for detailed information on each package.*

# 3. Pin Assignment

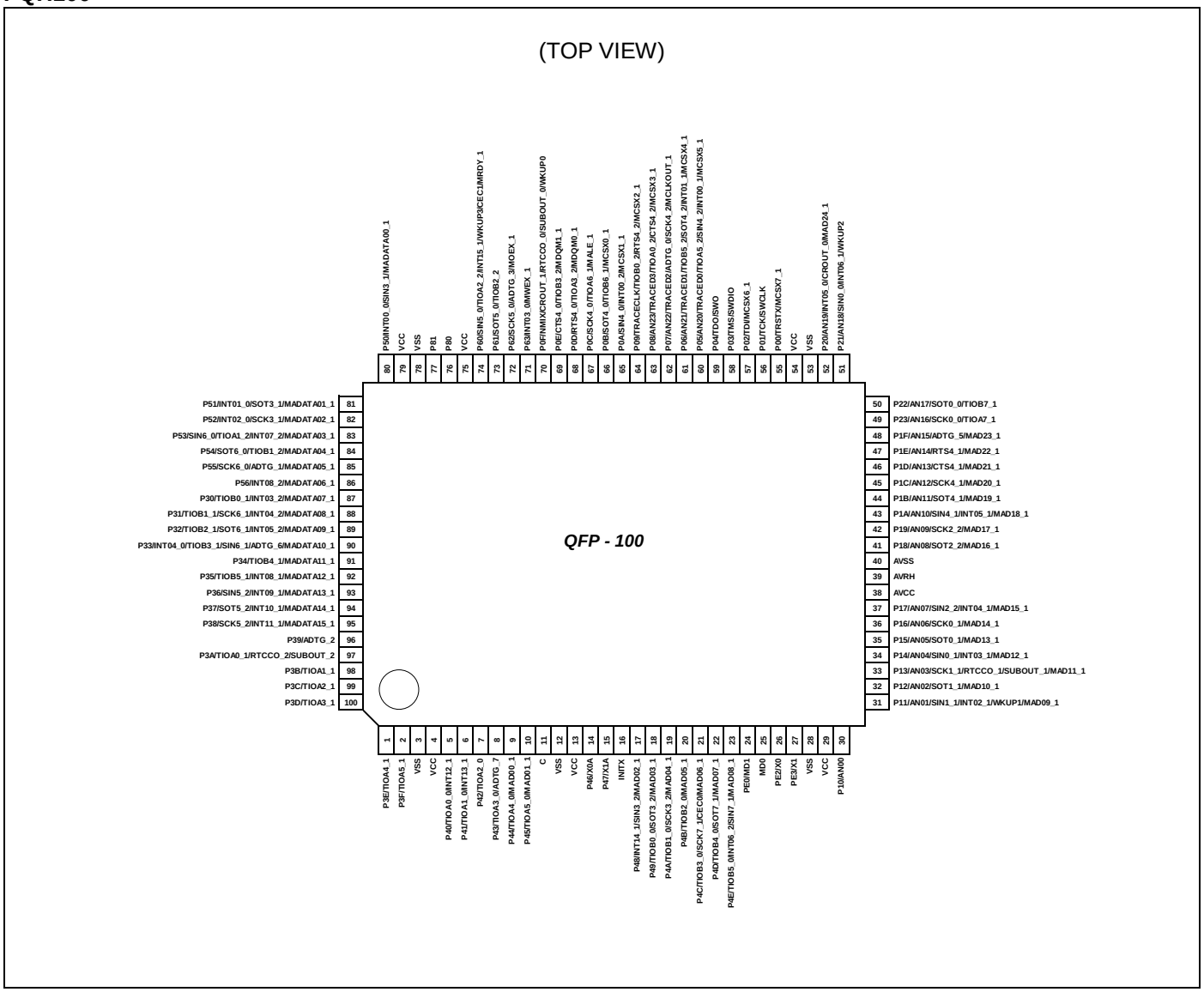
## LQI100




***Note:***

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

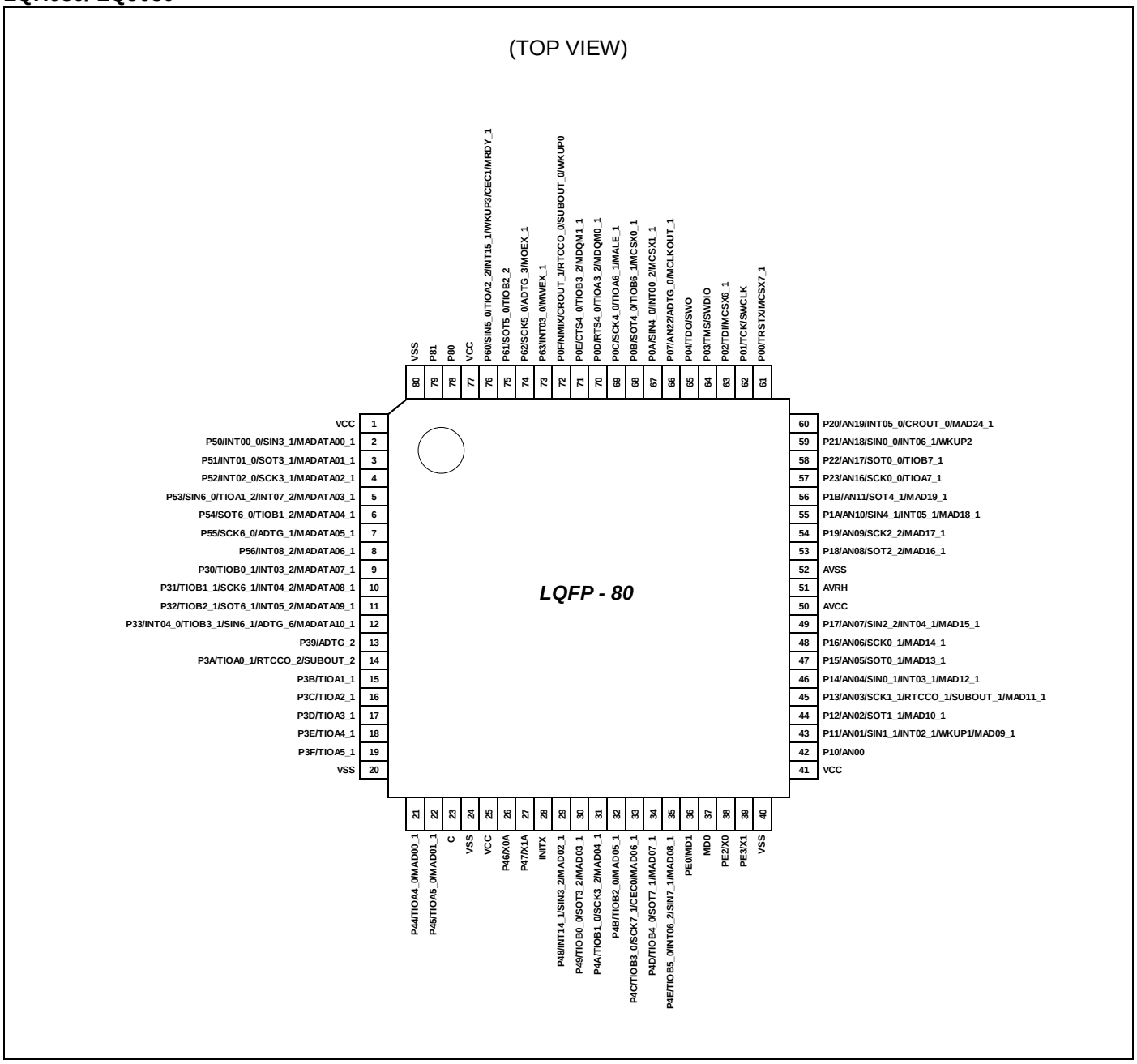
## PQH100




***Note:***

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

## LQH080/ LQJ080

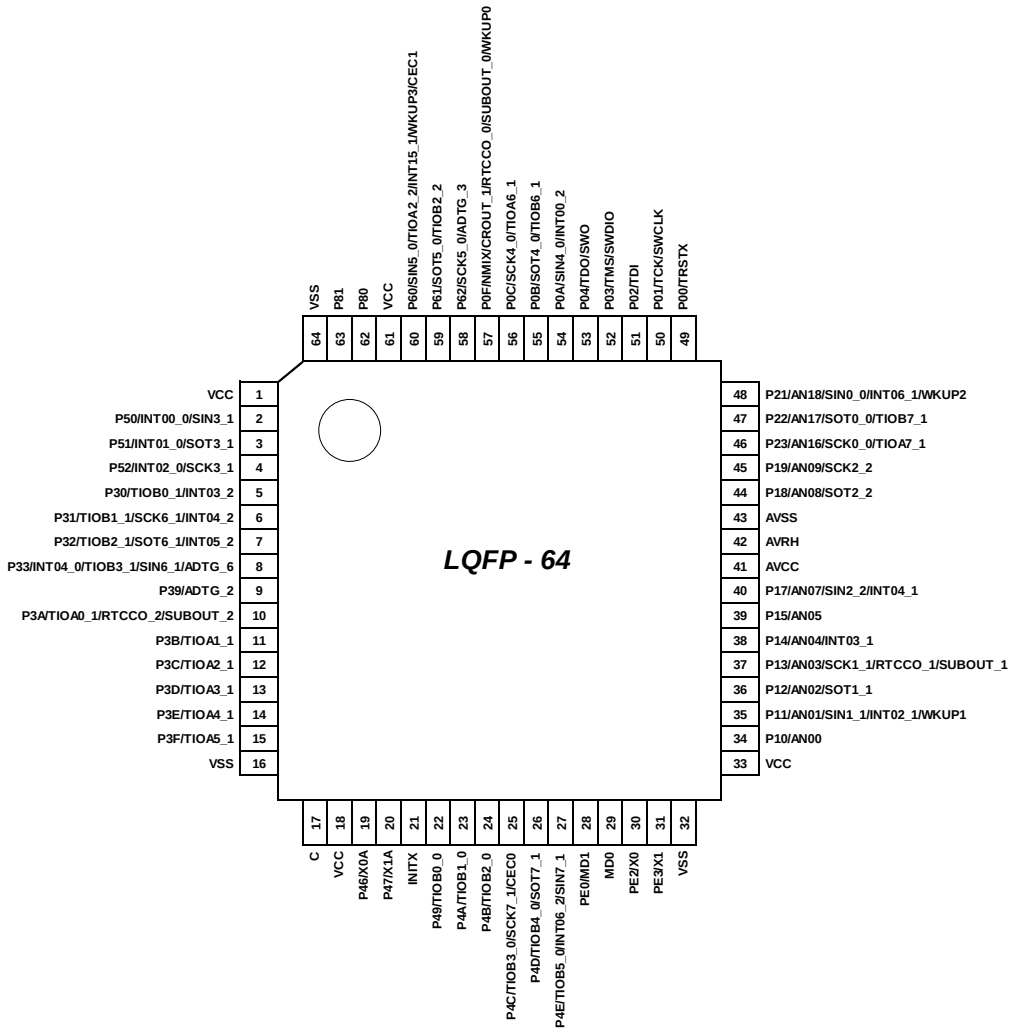



***Note:***

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

## LQD064/ LQG064

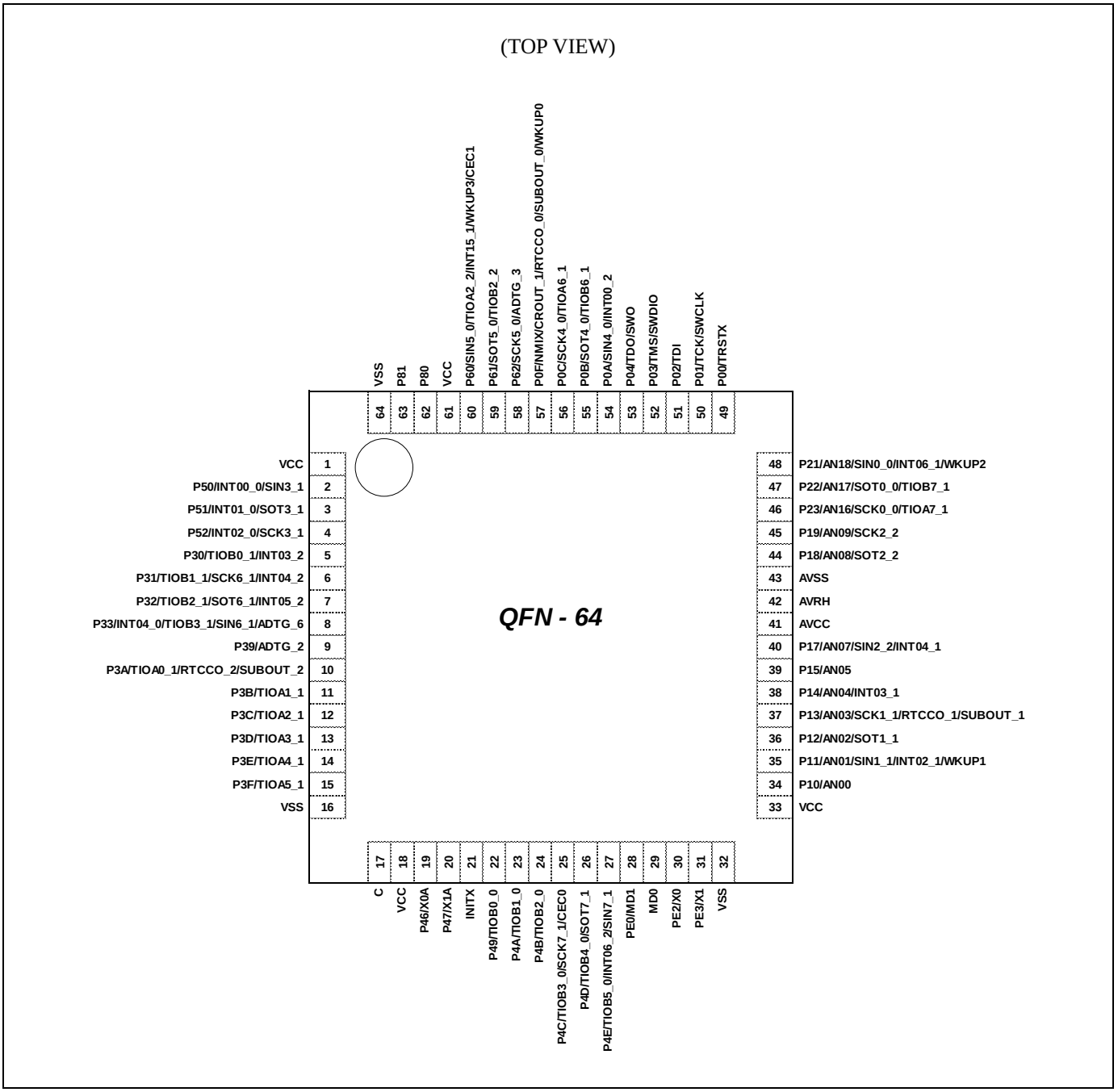
(TOP VIEW)




***Note:***

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

**VNC064**




***Note:***

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

**LBC112**

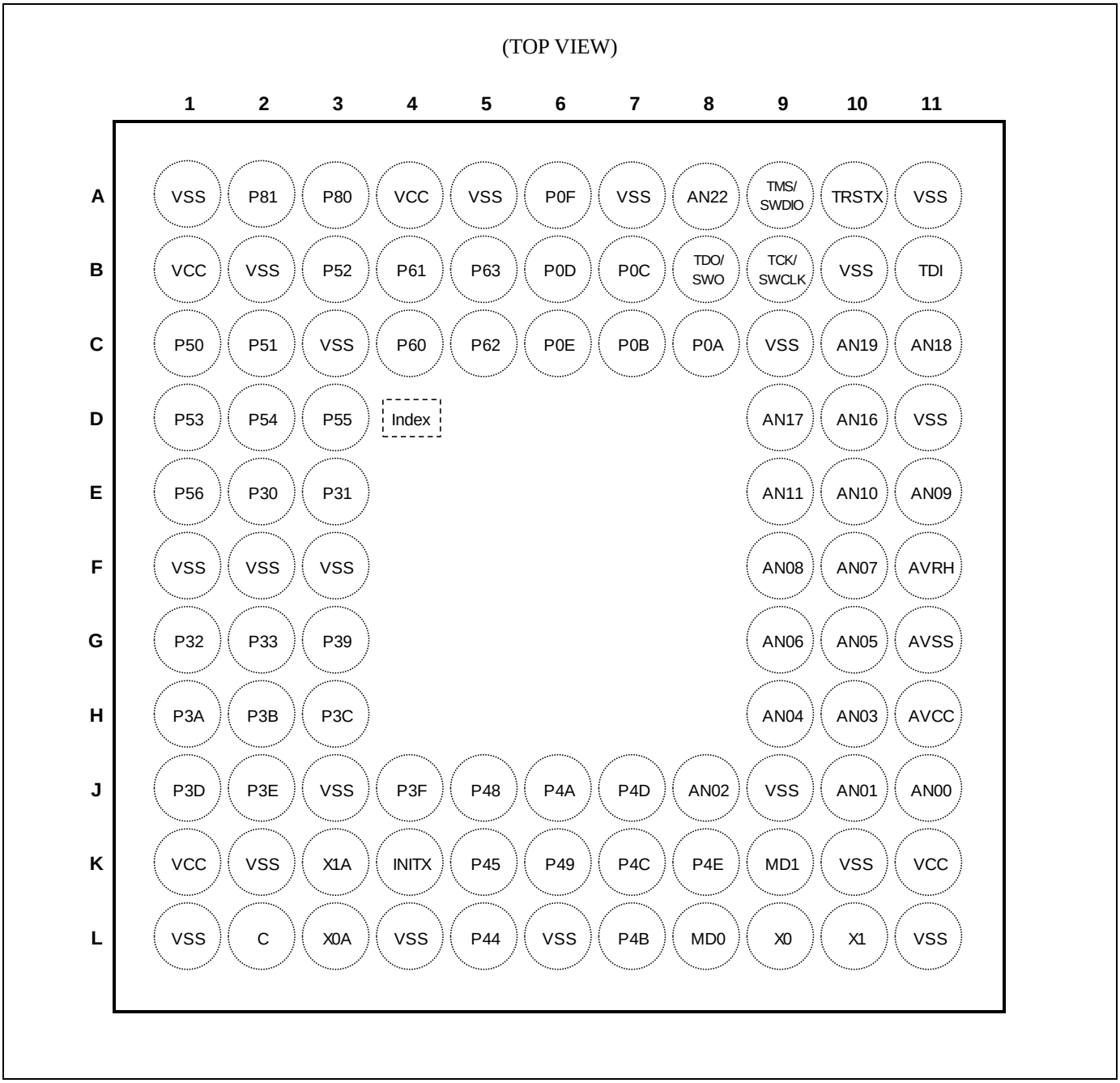
(TOP VIEW)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A | VSS | P81 | P80 | VCC | P0E | P0B | AN22 | TMS/ SWDIO | TRSTX | VCC | VSS |
| B | VCC | VSS | P52 | P61 | P0F | P0C | AN23 | TDO/ SWO | TCK/ SWCLK | VSS | TDI |
| C | P50 | P51 | VSS | P60 | P62 | P0D | P09 | AN20 | VSS | AN19 | AN18 |
| D | P53 | P54 | P55 | VSS | P56 | P63 | P0A | VSS | AN21 | AN16 | AN15 |
| E | P30 | P31 | P32 | P33 | Index | | | AN17 | AN14 | AN12 | AN11 |
| F | P34 | P35 | P36 | P39 | | | | AN13 | AN10 | AN09 | AVRH |
| G | P37 | P38 | P3A | P3D | | | | AN08 | AN07 | AN06 | AVSS |
| H | P3B | P3C | P3E | VSS | P44 | P4C | AN05 | VSS | AN04 | AN03 | AVCC |
| J | VCC | P3F | VSS | P40 | P43 | P49 | P4D | AN02 | VSS | AN01 | AN00 |
| K | VCC | VSS | X1A | INITX | P42 | P48 | P4B | P4E | MD1 | VSS | VCC |
| L | VSS | C | X0A | VSS | P41 | P45 | P4A | MD0 | X0 | X1 | VSS |

***Note:***

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

**FDG096**




***Note:***

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

# 4. List of Pin Functions

### List of pin numbers

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

| Pin No | | | | | | Pin Name | I/O Circuit Type | Pin State Type |
|---|---|---|---|---|---|---|---|---|
| LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | BGA-96 | LQFP-64 QFN-64 | | | |
| 1 | 79 | B1 | 1 | B1 | 1 | VCC | - | |
| 2 | 80 | C1 | 2 | C1 | 2 | P50 | E | L |
| | | | | | | INT00_0 | | |
| | | | | | | SIN3_1 | | |
| | | | | | - | MADATA00_1 | | |
| 3 | 81 | C2 | 3 | C2 | 3 | P51 | E | L |
| | | | | | | INT01_0 | | |
| | | | | | | SOT3_1 (SDA3_1) | | |
| | | | | | - | MADATA01_1 | | |
| 4 | 82 | B3 | 4 | B3 | 4 | P52 | E | L |
| | | | | | | INT02_0 | | |
| | | | | | | SCK3_1 (SCL3_1) | | |
| | | | | | - | MADATA02_1 | | |
| 5 | 83 | D1 | 5 | D1 | - | P53 | E | L |
| | | | | | | SIN6_0 | | |
| | | | | | | TIOA1_2 | | |
| | | | | | | INT07_2 | | |
| | | | | | | MADATA03_1 | | |
| 6 | 84 | D2 | 6 | D2 | - | P54 | E | K |
| | | | | | | SOT6_0 (SDA6_0) | | |
| | | | | | | TIOB1_2 | | |
| | | | | | | MADATA04_1 | | |
| 7 | 85 | D3 | 7 | D3 | - | P55 | E | K |
| | | | | | | SCK6_0 (SCL6_0) | | |
| | | | | | | ADTG_1 | | |
| | | | | | | MADATA05_1 | | |
| 8 | 86 | D5 | 8 | E1 | - | P56 | E | L |
| | | | | | | INT08_2 | | |
| | | | | | | MADATA06_1 | | |
| 9 | 87 | E1 | 9 | E2 | 5 | P30 | E | L |
| | | | | | | TIOB0_1 | | |
| | | | | | | INT03_2 | | |
| | | | | | - | MADATA07_1 | | |

| Pin No | | | | | | Pin Name | I/O Circuit Type | Pin State Type |
|---|---|---|---|---|---|---|---|---|
| LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | BGA-96 | LQFP-64 QFN-64 | | | |
| 10 | 88 | E2 | 10 | E3 | 6 | P31 | E | L |
| | | | | | | TIOB1_1 | | |
| | | | | | | SCK6_1 (SCL6_1) | | |
| | | | | | | INT04_2 | | |
| | | | | | - | MADATA08_1 | | |
| 11 | 89 | E3 | 11 | G1 | 7 | P32 | E | L |
| | | | | | | TIOB2_1 | | |
| | | | | | | SOT6_1 (SDA6_1) | | |
| | | | | | | INT05_2 | | |
| | | | | | - | MADATA09_1 | | |
| 12 | 90 | E4 | 12 | G2 | 8 | P33 | E | L |
| | | | | | | INT04_0 | | |
| | | | | | | TIOB3_1 | | |
| | | | | | | SIN6_1 | | |
| | | | | | | ADTG_6 | | |
| | | | | | - | MADATA10_1 | | |
| 13 | 91 | F1 | - | - | - | P34 | E | K |
| | | | | | | TIOB4_1 | | |
| | | | | | | MADATA11_1 | | |
| 14 | 92 | F2 | - | - | - | P35 | E | L |
| | | | | | | TIOB5_1 | | |
| | | | | | | INT08_1 | | |
| | | | | | | MADATA12_1 | | |
| 15 | 93 | F3 | - | - | - | P36 | E | L |
| | | | | | | SIN5_2 | | |
| | | | | | | INT09_1 | | |
| | | | | | | MADATA13_1 | | |
| - | - | - | - | F1 | - | VSS | - | |
| - | - | - | - | F2 | - | VSS | - | |
| - | - | - | - | F3 | - | VSS | - | |
| 16 | 94 | G1 | - | - | - | P37 | E | L |
| | | | | | | SOT5_2 (SDA5_2) | | |
| | | | | | | INT10_1 | | |
| | | | | | | MADATA14_1 | | |
| 17 | 95 | G2 | - | - | - | P38 | E | L |
| | | | | | | SCK5_2 (SCL5_2) | | |
| | | | | | | INT11_1 | | |
| | | | | | | MADATA15_1 | | |
| 18 | 96 | F4 | 13 | G3 | 9 | P39 | E | K |
| | | | | | | ADTG_2 | | |

| Pin No | | | | | | Pin Name | I/O Circuit Type | Pin State Type |
|---|---|---|---|---|---|---|---|---|
| LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | BGA-96 | LQFP-64 QFN-64 | | | |
| 19 | 97 | G3 | 14 | H1 | 10 | P3A<br>TIOA0_1<br>RTCCO_2<br>SUBOUT_2 | E | K |
| 20 | 98 | H1 | 15 | H2 | 11 | P3B<br>TIOA1_1 | E | K |
| 21 | 99 | H2 | 16 | H3 | 12 | P3C<br>TIOA2_1 | E | K |
| 22 | 100 | G4 | 17 | J1 | 13 | P3D<br>TIOA3_1 | E | K |
| - | - | B2 | - | B2 | - | VSS | - | |
| 23 | 1 | H3 | 18 | J2 | 14 | P3E<br>TIOA4_1 | E | K |
| 24 | 2 | J2 | 19 | J4 | 15 | P3F<br>TIOA5_1 | E | K |
| 25 | 3 | L1 | 20 | L1 | 16 | VSS | - | |
| 26 | 4 | J1 | - | - | - | VCC | - | |
| 27 | 5 | J4 | - | - | - | P40<br>TIOA0_0<br>INT12_1 | E | L |
| 28 | 6 | L5 | - | - | - | P41<br>TIOA1_0<br>INT13_1 | E | L |
| 29 | 7 | K5 | - | - | - | P42<br>TIOA2_0 | E | K |
| 30 | 8 | J5 | - | - | - | P43<br>TIOA3_0<br>ADTG_7 | E | K |
| 31 | 9 | H5 | 21 | L5 | - | P44<br>TIOA4_0<br>MAD00_1 | E | K |
| 32 | 10 | L6 | 22 | K5 | - | P45<br>TIOA5_0<br>MAD01_1 | E | K |
| - | - | K2 | - | K2 | - | VSS | - | |
| - | - | J3 | - | J3 | - | VSS | - | |
| - | - | H4 | - | - | - | VSS | - | |
| - | - | - | - | L6 | - | VSS | - | |
| 33 | 11 | L2 | 23 | L2 | 17 | C | - | |
| 34 | 12 | L4 | 24 | L4 | - | VSS | - | |
| 35 | 13 | K1 | 25 | K1 | 18 | VCC | - | |
| 36 | 14 | L3 | 26 | L3 | 19 | P46<br>X0A | D | F |
| 37 | 15 | K3 | 27 | K3 | 20 | P47<br>X1A | D | G |

| Pin No | | | | | | Pin Name | I/O Circuit Type | Pin State Type |
|---|---|---|---|---|---|---|---|---|
| LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | BGA-96 | LQFP-64 QFN-64 | | | |
| 38 | 16 | K4 | 28 | K4 | 21 | INITX | B | C |
| 39 | 17 | K6 | 29 | J5 | - | P48 | E | L |
| | | | | | | INT14_1 | | |
| | | | | | | SIN3_2 | | |
| | | | | | | MAD02_1 | | |
| 40 | 18 | J6 | 30 | K6 | 22 | P49 | E | K |
| | | | | | | TIOB0_0 | | |
| | | | | | - | SOT3_2 (SDA3_2) | | |
| | | | | | | MAD03_1 | | |
| 41 | 19 | L7 | 31 | J6 | 23 | P4A | E | K |
| | | | | | | TIOB1_0 | | |
| | | | | | - | SCK3_2 (SCL3_2) | | |
| | | | | | | MAD04_1 | | |
| 42 | 20 | K7 | 32 | L7 | 24 | P4B | E | K |
| | | | | | | TIOB2_0 | | |
| | | | | | - | MAD05_1 | | |
| 43 | 21 | H6 | 33 | K7 | 25 | P4C | I | S |
| | | | | | | TIOB3_0 | | |
| | | | | | | SCK7_1 (SCL7_1) | | |
| | | | | | | CEC0 | | |
| | | | | | - | MAD06_1 | | |
| 44 | 22 | J7 | 34 | J7 | 26 | P4D | I | K |
| | | | | | | TIOB4_0 | | |
| | | | | | | SOT7_1 (SDA7_1) | | |
| | | | | | - | MAD07_1 | | |
| 45 | 23 | K8 | 35 | K8 | 27 | P4E | I | L |
| | | | | | | TIOB5_0 | | |
| | | | | | | INT06_2 | | |
| | | | | | | SIN7_1 | | |
| | | | | | - | MAD08_1 | | |
| 46 | 24 | K9 | 36 | K9 | 28 | MD1 | C | E |
| | | | | | | PE0 | | |
| 47 | 25 | L8 | 37 | L8 | 29 | MD0 | G | D |
| 48 | 26 | L9 | 38 | L9 | 30 | X0 | A | A |
| | | | | | | PE2 | | |
| 49 | 27 | L10 | 39 | L10 | 31 | X1 | A | B |
| | | | | | | PE3 | | |
| 50 | 28 | L11 | 40 | L11 | 32 | VSS | - | |
| 51 | 29 | K11 | 41 | K11 | 33 | VCC | - | |
| 52 | 30 | J11 | 42 | J11 | 34 | P10 | F | M |
| | | | | | | AN00 | | |

| Pin No | | | | | | Pin Name | I/O Circuit Type | Pin State Type |
|---|---|---|---|---|---|---|---|---|
| LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | BGA-96 | LQFP-64 QFN-64 | | | |
| 53 | 31 | J10 | 43 | J10 | 35 | P11 | F | R |
| | | | | | | AN01 | | |
| | | | | | | SIN1_1 | | |
| | | | | | | INT02_1 | | |
| | | | | | | WKUP1 | | |
| | | | | | - | MAD09_1 | | |
| 54 | 32 | J8 | 44 | J8 | 36 | P12 | F | M |
| | | | | | | AN02 | | |
| | | | | | | SOT1_1 (SDA1_1) | | |
| | | | | | - | MAD10_1 | | |
| - | - | K10 | - | K10 | - | VSS | - | |
| - | - | J9 | - | J9 | - | VSS | - | |
| 55 | 33 | H10 | 45 | H10 | 37 | P13 | F | M |
| | | | | | | AN03 | | |
| | | | | | | SCK1_1 (SCL1_1) | | |
| | | | | | | RTCCO_1 | | |
| | | | | | | SUBOUT_1 | | |
| | | | | | - | MAD11_1 | | |
| 56 | 34 | H9 | 46 | H9 | 38 | P14 | F | N |
| | | | | | | AN04 | | |
| | | | | | | INT03_1 | | |
| | | | | | - | SIN0_1 | | |
| | | | | | | MAD12_1 | | |
| 57 | 35 | H7 | 47 | G10 | 39 | P15 | F | M |
| | | | | | | AN05 | | |
| | | | | | - | SOT0_1 (SDA0_1) | | |
| | | | | | | MAD13_1 | | |
| 58 | 36 | G10 | 48 | G9 | - | P16 | F | M |
| | | | | | | AN06 | | |
| | | | | | | SCK0_1 (SCL0_1) | | |
| | | | | | | MAD14_1 | | |
| 59 | 37 | G9 | 49 | F10 | 40 | P17 | F | N |
| | | | | | | AN07 | | |
| | | | | | | SIN2_2 | | |
| | | | | | | INT04_1 | | |
| | | | | | - | MAD15_1 | | |
| 60 | 38 | H11 | 50 | H11 | 41 | AVCC | - | |
| 61 | 39 | F11 | 51 | F11 | 42 | AVRH | - | |
| 62 | 40 | G11 | 52 | G11 | 43 | AVSS | - | |

| Pin No | | | | | | Pin Name | I/O Circuit Type | Pin State Type |
|---|---|---|---|---|---|---|---|---|
| LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | BGA-96 | LQFP-64 QFN-64 | | | |
| 63 | 41 | G8 | 53 | F9 | 44 | P18<br>AN08<br>SOT2_2 (SDA2_2) | F | M |
| | | | | | - | MAD16_1 | | |
| 64 | 42 | F10 | 54 | E11 | 45 | P19<br>AN09<br>SCK2_2 (SCL2_2) | F | M |
| | | | | | - | MAD17_1 | | |
| - | - | H8 | - | - | - | VSS | - | |
| 65 | 43 | F9 | 55 | E10 | - | P1A<br>AN10<br>SIN4_1<br>INT05_1<br>MAD18_1 | F | N |
| 66 | 44 | E11 | 56 | E9 | - | P1B<br>AN11<br>SOT4_1 (SDA4_1)<br>MAD19_1 | F | M |
| 67 | 45 | E10 | - | - | - | P1C<br>AN12<br>SCK4_1 (SCL4_1)<br>MAD20_1 | F | M |
| 68 | 46 | F8 | - | - | - | P1D<br>AN13<br>CTS4_1<br>MAD21_1 | F | M |
| 69 | 47 | E9 | - | - | - | P1E<br>AN14<br>RTS4_1<br>MAD22_1 | F | M |
| 70 | 48 | D11 | - | - | - | P1F<br>AN15<br>ADTG_5<br>MAD23_1 | F | M |
| - | - | B10 | - | B10 | - | VSS | - | |
| - | - | C9 | - | C9 | - | VSS | - | |
| - | - | - | - | D11 | - | VSS | - | |

| Pin No | | | | | | Pin Name | I/O Circuit Type | Pin State Type |
|---|---|---|---|---|---|---|---|---|
| LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | BGA-96 | LQFP-64 QFN-64 | | | |
| 71 | 49 | D10 | 57 | D10 | 46 | P23<br>AN16<br>SCK0_0 (SCL0_0)<br>TIOA7_1 | F | M |
| 72 | 50 | E8 | 58 | D9 | 47 | P22<br>AN17<br>SOT0_0 (SDA0_0)<br>TIOB7_1 | F | M |
| 73 | 51 | C11 | 59 | C11 | 48 | P21<br>AN18<br>SIN0_0<br>INT06_1<br>WKUP2 | F | R |
| 74 | 52 | C10 | 60 | C10 | - | P20<br>AN19<br>INT05_0<br>CROUT_0<br>MAD24_1 | F | N |
| 75 | 53 | A11 | - | A11 | - | VSS | - | |
| 76 | 54 | A10 | - | - | - | VCC | - | |
| 77 | 55 | A9 | 61 | A10 | 49<br>- | P00<br>TRSTX<br>MCSX7_1 | E | J |
| 78 | 56 | B9 | 62 | B9 | 50 | P01<br>TCK<br>SWCLK | E | J |
| 79 | 57 | B11 | 63 | B11 | 51<br>- | P02<br>TDI<br>MCSX6_1 | E | J |
| 80 | 58 | A8 | 64 | A9 | 52 | P03<br>TMS<br>SWDIO | E | J |
| 81 | 59 | B8 | 65 | B8 | 53 | P04<br>TDO<br>SWO | E | J |
| 82 | 60 | C8 | - | - | - | P05<br>AN20<br>TRACED0<br>TIOA5_2<br>SIN4_2<br>INT00_1<br>MCSX5_1 | F | Q |

| Pin No | | | | | | Pin Name | I/O Circuit Type | Pin State Type |
|---|---|---|---|---|---|---|---|---|
| LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | BGA-96 | LQFP-64 QFN-64 | | | |
| - | - | D8 | - | - | - | VSS | - | |
| 83 | 61 | D9 | - | - | - | P06<br>AN21<br>TRACED1<br>TIOB5_2<br>SOT4_2 (SDA4_2)<br>INT01_1<br>MCSX4_1 | F | Q |
| 84 | 62 | A7 | 66 | A8 | - | P07<br>AN22<br>ADTG_0<br>MCLKOUT_1 | F | P |
| | | | - | - | | TRACED2<br>SCK4_2 (SCL4_2) | | |
| - | - | - | - | A7 | - | VSS | - | |
| 85 | 63 | B7 | - | - | - | P08<br>AN23<br>TRACED3<br>TIOA0_2<br>CTS4_2<br>MCSX3_1 | F | P |
| 86 | 64 | C7 | - | - | - | P09<br>TRACECLK<br>TIOB0_2<br>RTS4_2<br>MCSX2_1 | E | O |
| 87 | 65 | D7 | 67 | C8 | 54 | P0A<br>SIN4_0<br>INT00_2 | I | L |
| | | | | | - | MCSX1_1 | | |
| 88 | 66 | A6 | 68 | C7 | 55 | P0B<br>SOT4_0 (SDA4_0)<br>TIOB6_1 | I | K |
| | | | | | - | MCSX0_1 | | |
| 89 | 67 | B6 | 69 | B7 | 56 | P0C<br>SCK4_0 (SCL4_0)<br>TIOA6_1 | I | K |
| | | | | | - | MALE_1 | | |
| - | - | D4 | - | - | - | VSS | - | |

| Pin No | | | | | | Pin Name | I/O Circuit Type | Pin State Type |
|---|---|---|---|---|---|---|---|---|
| LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | BGA-96 | LQFP-64 QFN-64 | | | |
| - | - | C3 | - | C3 | - | VSS | - | |
| 90 | 68 | C6 | 70 | B6 | - | P0D<br>RTS4_0<br>TIOA3_2<br>MDQM0_1 | E | K |
| 91 | 69 | A5 | 71 | C6 | - | P0E<br>CTS4_0<br>TIOB3_2<br>MDQM1_1 | E | K |
| - | - | - | - | A5 | - | VSS | - | |
| 92 | 70 | B5 | 72 | A6 | 57 | P0F<br>NMIX<br>CROUT_1<br>RTCCO_0<br>SUBOUT_0<br>WKUP0 | E | I |
| 93 | 71 | D6 | 73 | B5 | - | P63<br>INT03_0<br>MWEX_1 | E | L |
| 94 | 72 | C5 | 74 | C5 | 58<br><br><br>- | P62<br>SCK5_0 (SCL5_0)<br>ADTG_3<br>MOEX_1 | E | K |
| 95 | 73 | B4 | 75 | B4 | 59 | P61<br>SOT5_0 (SDA5_0)<br>TIOB2_2 | E | K |
| 96 | 74 | C4 | 76 | C4 | 60<br><br><br><br><br>- | P60<br>SIN5_0<br>TIOA2_2<br>INT15_1<br>WKUP3<br>CEC1<br>MRDY_1 | I | T |
| 97 | 75 | A4 | 77 | A4 | 61 | VCC | - | |
| 98 | 76 | A3 | 78 | A3 | 62 | P80 | H | H |
| 99 | 77 | A2 | 79 | A2 | 63 | P81 | H | H |
| 100 | 78 | A1 | 80 | A1 | 64 | VSS | - | |

## List of pin functions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

| Pin Function | Pin Name | Function Description | Pin No | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | BGA-96 | LQFP/ QFN-64 |
| ADC | ADTG_0 | A/D converter external trigger input pin | 84 | 62 | A7 | 66 | A8 | - |
| | ADTG_1 | | 7 | 85 | D3 | 7 | D3 | - |
| | ADTG_2 | | 18 | 96 | F4 | 13 | G3 | 9 |
| | ADTG_3 | | 94 | 72 | C5 | 74 | C5 | 58 |
| | ADTG_4 | | - | - | - | - | - | - |
| | ADTG_5 | | 70 | 48 | D11 | - | - | - |
| | ADTG_6 | | 12 | 90 | E4 | 12 | G2 | 8 |
| | ADTG_7 | | 30 | 8 | J5 | - | - | - |
| | ADTG_8 | | - | - | - | - | - | - |
| | AN00 | A/D converter analog input pin. ANxx describes ADC ch.xx. | 52 | 30 | J11 | 42 | J11 | 34 |
| | AN01 | | 53 | 31 | J10 | 43 | J10 | 35 |
| | AN02 | | 54 | 32 | J8 | 44 | J8 | 36 |
| | AN03 | | 55 | 33 | H10 | 45 | H10 | 37 |
| | AN04 | | 56 | 34 | H9 | 46 | H9 | 38 |
| | AN05 | | 57 | 35 | H7 | 47 | G10 | 39 |
| | AN06 | | 58 | 36 | G10 | 48 | G9 | - |
| | AN07 | | 59 | 37 | G9 | 49 | F10 | 40 |
| | AN08 | | 63 | 41 | G8 | 53 | F9 | 44 |
| | AN09 | | 64 | 42 | F10 | 54 | E11 | 45 |
| | AN10 | | 65 | 43 | F9 | 55 | E10 | - |
| | AN11 | | 66 | 44 | E11 | 56 | E9 | - |
| | AN12 | | 67 | 45 | E10 | - | - | - |
| | AN13 | | 68 | 46 | F8 | - | - | - |
| | AN14 | | 69 | 47 | E9 | - | - | - |
| | AN15 | | 70 | 48 | D11 | - | - | - |
| | AN16 | | 71 | 49 | D10 | 57 | D10 | 46 |
| | AN17 | | 72 | 50 | E8 | 58 | D9 | 47 |
| | AN18 | | 73 | 51 | C11 | 59 | C11 | 48 |
| | AN19 | | 74 | 52 | C10 | 60 | C10 | - |
| | AN20 | | 82 | 60 | C8 | - | - | - |
| | AN21 | | 83 | 61 | D9 | - | - | - |
| | AN22 | | 84 | 62 | A7 | 66 | A8 | - |
| | AN23 | | 85 | 63 | B7 | - | - | - |

| Pin Function | Pin Name | Function Description | Pin No | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | BGA-96 | LQFP/ QFN-64 |
| Base Timer 0 | TIOA0_0 | Base timer ch.0 TIOA pin | 27 | 5 | J4 | - | - | - |
| | TIOA0_1 | | 19 | 97 | G3 | 14 | H1 | 10 |
| | TIOA0_2 | | 85 | 63 | B7 | - | - | - |
| | TIOB0_0 | Base timer ch.0 TIOB pin | 40 | 18 | J6 | 30 | K6 | 22 |
| | TIOB0_1 | | 9 | 87 | E1 | 9 | E2 | 5 |
| | TIOB0_2 | | 86 | 64 | C7 | - | - | - |
| Base Timer 1 | TIOA1_0 | Base timer ch.1 TIOA pin | 28 | 6 | L5 | - | - | - |
| | TIOA1_1 | | 20 | 98 | H1 | 15 | H2 | 11 |
| | TIOA1_2 | | 5 | 83 | D1 | 5 | D1 | - |
| | TIOB1_0 | Base timer ch.1 TIOB pin | 41 | 19 | L7 | 31 | J6 | 23 |
| | TIOB1_1 | | 10 | 88 | E2 | 10 | E3 | 6 |
| | TIOB1_2 | | 6 | 84 | D2 | 6 | D2 | - |
| Base Timer 2 | TIOA2_0 | Base timer ch.2 TIOA pin | 29 | 7 | K5 | - | - | - |
| | TIOA2_1 | | 21 | 99 | H2 | 16 | H3 | 12 |
| | TIOA2_2 | | 96 | 74 | C4 | 76 | C4 | 60 |
| | TIOB2_0 | Base timer ch.2 TIOB pin | 42 | 20 | K7 | 32 | L7 | 24 |
| | TIOB2_1 | | 11 | 89 | E3 | 11 | G1 | 7 |
| | TIOB2_2 | | 95 | 73 | B4 | 75 | B4 | 59 |
| Base Timer 3 | TIOA3_0 | Base timer ch.3 TIOA pin | 30 | 8 | J5 | - | - | - |
| | TIOA3_1 | | 22 | 100 | G4 | 17 | J1 | 13 |
| | TIOA3_2 | | 90 | 68 | C6 | 70 | B6 | - |
| | TIOB3_0 | Base timer ch.3 TIOB pin | 43 | 21 | H6 | 33 | K7 | 25 |
| | TIOB3_1 | | 12 | 90 | E4 | 12 | G2 | 8 |
| | TIOB3_2 | | 91 | 69 | A5 | 71 | C6 | - |
| Base Timer 4 | TIOA4_0 | Base timer ch.4 TIOA pin | 31 | 9 | H5 | 21 | L5 | - |
| | TIOA4_1 | | 23 | 1 | H3 | 18 | J2 | 14 |
| | TIOA4_2 | | - | - | - | - | - | - |
| | TIOB4_0 | Base timer ch.4 TIOB pin | 44 | 22 | J7 | 34 | J7 | 26 |
| | TIOB4_1 | | 13 | 91 | F1 | - | - | - |
| | TIOB4_2 | | - | - | - | - | - | - |
| Base Timer 5 | TIOA5_0 | Base timer ch.5 TIOA pin | 32 | 10 | L6 | 22 | K5 | - |
| | TIOA5_1 | | 24 | 2 | J2 | 19 | J4 | 15 |
| | TIOA5_2 | | 82 | 60 | C8 | - | - | - |
| | TIOB5_0 | Base timer ch.5 TIOB pin | 45 | 23 | K8 | 35 | K8 | 27 |
| | TIOB5_1 | | 14 | 92 | F2 | - | - | - |
| | TIOB5_2 | | 83 | 61 | D9 | - | - | - |
| Base Timer 6 | TIOA6_1 | Base timer ch.6 TIOA pin | 89 | 67 | B6 | 69 | B7 | 56 |
| | TIOB6_1 | Base timer ch.6 TIOB pin | 88 | 66 | A6 | 68 | C7 | 55 |
| Base Timer 7 | TIOA7_0 | Base timer ch.7 TIOA pin | - | - | - | - | - | - |
| | TIOA7_1 | | 71 | 49 | D10 | 57 | D10 | 46 |
| | TIOA7_2 | | - | - | - | - | - | - |
| | TIOB7_0 | Base timer ch.7 TIOB pin | - | - | - | - | - | - |
| | TIOB7_1 | | 72 | 50 | E8 | 58 | D9 | 47 |
| | TIOB7_2 | | - | - | - | - | - | - |

| Pin Function | Pin Name | Function Description | Pin No | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | BGA-96 | LQFP/ QFN-64 |
| Debugger | SWCLK | Serial wire debug interface clock input pin | 78 | 56 | B9 | 62 | B9 | 50 |
| | SWDIO | Serial wire debug interface data input / output pin | 80 | 58 | A8 | 64 | A9 | 52 |
| | SWO | Serial wire viewer output pin | 81 | 59 | B8 | 65 | B8 | 53 |
| | TCK | JTAG test clock input pin | 78 | 56 | B9 | 62 | B9 | 50 |
| | TDI | JTAG test data input pin | 79 | 57 | B11 | 63 | B11 | 51 |
| | TDO | JTAG debug data output pin | 81 | 59 | B8 | 65 | B8 | 53 |
| | TMS | JTAG test mode state input/output pin | 80 | 58 | A8 | 64 | A9 | 52 |
| | TRACECLK | Trace CLK output pin of ETM | 86 | 64 | C7 | - | - | - |
| | TRACED0 | Trace data output pins of ETM | 82 | 60 | C8 | - | - | - |
| | TRACED1 | | 83 | 61 | D9 | - | - | - |
| | TRACED2 | | 84 | 62 | A7 | - | - | - |
| | TRACED3 | | 85 | 63 | B7 | - | - | - |
| | TRSTX | JTAG test reset input pin | 77 | 55 | A9 | 61 | A10 | 49 |
| External Bus | MAD00_1 | External bus interface address bus | 31 | 9 | H5 | 21 | L5 | - |
| | MAD01_1 | | 32 | 10 | L6 | 22 | K5 | - |
| | MAD02_1 | | 39 | 17 | K6 | 29 | J5 | - |
| | MAD03_1 | | 40 | 18 | J6 | 30 | K6 | - |
| | MAD04_1 | | 41 | 19 | L7 | 31 | J6 | - |
| | MAD05_1 | | 42 | 20 | K7 | 32 | L7 | - |
| | MAD06_1 | | 43 | 21 | H6 | 33 | K7 | - |
| | MAD07_1 | | 44 | 22 | J7 | 34 | J7 | - |
| | MAD08_1 | | 45 | 23 | K8 | 35 | K8 | - |
| | MAD09_1 | | 53 | 31 | J10 | 43 | J10 | - |
| | MAD10_1 | | 54 | 32 | J8 | 44 | J8 | - |
| | MAD11_1 | | 55 | 33 | H10 | 45 | H10 | - |
| | MAD12_1 | | 56 | 34 | H9 | 46 | H9 | - |
| | MAD13_1 | | 57 | 35 | H7 | 47 | G10 | - |
| | MAD14_1 | | 58 | 36 | G10 | 48 | G9 | - |
| | MAD15_1 | | 59 | 37 | G9 | 49 | F10 | - |
| | MAD16_1 | | 63 | 41 | G8 | 53 | F9 | - |
| | MAD17_1 | | 64 | 42 | F10 | 54 | E11 | - |
| | MAD18_1 | | 65 | 43 | F9 | 55 | E10 | - |
| | MAD19_1 | | 66 | 44 | E11 | 56 | E9 | - |
| | MAD20_1 | | 67 | 45 | E10 | - | - | - |
| | MAD21_1 | | 68 | 46 | F8 | - | - | - |
| | MAD22_1 | | 69 | 47 | E9 | - | - | - |
| | MAD23_1 | | 70 | 48 | D11 | - | - | - |
| | MAD24_1 | | 74 | 52 | C10 | 60 | C10 | - |

| Pin Function | Pin Name | Function Description | Pin No | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | BGA-96 | LQFP/ QFN-64 |
| External Bus | MCSX0_1 | External bus interface chip select output pin | 88 | 66 | A6 | 68 | C7 | - |
| | MCSX1_1 | | 87 | 65 | D7 | 67 | C8 | - |
| | MCSX2_1 | | 86 | 64 | C7 | - | - | - |
| | MCSX3_1 | | 85 | 63 | B7 | - | - | - |
| | MCSX4_1 | | 83 | 61 | D9 | - | - | - |
| | MCSX5_1 | | 82 | 60 | C8 | - | - | - |
| | MCSX6_1 | | 79 | 57 | B11 | 63 | B11 | - |
| | MCSX7_1 | | 77 | 55 | A9 | 61 | A10 | - |
| | MDQM0_1 | External bus interface byte mask signal output pin | 90 | 68 | C6 | 70 | B6 | - |
| | MDQM1_1 | | 91 | 69 | A5 | 71 | C6 | - |
| | MOEX_1 | External bus interface read enable signal for SRAM | 94 | 72 | C5 | 74 | C5 | - |
| | MWEX_1 | External bus interface write enable signal for SRAM | 93 | 71 | D6 | 73 | B5 | - |
| | MADATA00_1 | External bus interface data bus | 2 | 80 | C1 | 2 | C1 | - |
| | MADATA01_1 | | 3 | 81 | C2 | 3 | C2 | - |
| | MADATA02_1 | | 4 | 82 | B3 | 4 | B3 | - |
| | MADATA03_1 | | 5 | 83 | D1 | 5 | D1 | - |
| | MADATA04_1 | | 6 | 84 | D2 | 6 | D2 | - |
| | MADATA05_1 | | 7 | 85 | D3 | 7 | D3 | - |
| | MADATA06_1 | | 8 | 86 | D5 | 8 | E1 | - |
| | MADATA07_1 | | 9 | 87 | E1 | 9 | E2 | - |
| | MADATA08_1 | | 10 | 88 | E2 | 10 | E3 | - |
| | MADATA09_1 | | 11 | 89 | E3 | 11 | G1 | - |
| | MADATA10_1 | | 12 | 90 | E4 | 12 | G2 | - |
| | MADATA11_1 | | 13 | 91 | F1 | - | - | - |
| | MADATA12_1 | | 14 | 92 | F2 | - | - | - |
| | MADATA13_1 | | 15 | 93 | F3 | - | - | - |
| | MADATA14_1 | | 16 | 94 | G1 | - | - | - |
| | MADATA15_1 | | 17 | 95 | G2 | - | - | - |
| | MALE_1 | Address Latch enable signal for multiplex | 89 | 67 | B6 | 69 | B7 | - |
| | MRDY_1 | External RDY input signal | 96 | 74 | C4 | 76 | C4 | - |
| | MCLKOUT_1 | External bus clock output pin | 84 | 62 | A7 | 66 | A8 | - |

| Pin Function | Pin Name | Function Description | Pin No | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | BGA-96 | LQFP/ QFN-64 |
| External Interrupt | INT00_0 | External interrupt request 00 input pin | 2 | 80 | C1 | 2 | C1 | 2 |
| | INT00_1 | | 82 | 60 | C8 | - | - | - |
| | INT00_2 | | 87 | 65 | D7 | 67 | C8 | 54 |
| | INT01_0 | External interrupt request 01 input pin | 3 | 81 | C2 | 3 | C2 | 3 |
| | INT01_1 | | 83 | 61 | D9 | - | - | - |
| | INT02_0 | External interrupt request 02 input pin | 4 | 82 | B3 | 4 | B3 | 4 |
| | INT02_1 | | 53 | 31 | J10 | 43 | J10 | 35 |
| | INT03_0 | External interrupt request 03 input pin | 93 | 71 | D6 | 73 | B5 | - |
| | INT03_1 | | 56 | 34 | H9 | 46 | H9 | 38 |
| | INT03_2 | | 9 | 87 | E1 | 9 | E2 | 5 |
| | INT04_0 | External interrupt request 04 input pin | 12 | 90 | E4 | 12 | G2 | 8 |
| | INT04_1 | | 59 | 37 | G9 | 49 | F10 | 40 |
| | INT04_2 | | 10 | 88 | E2 | 10 | E3 | 6 |
| | INT05_0 | External interrupt request 05 input pin | 74 | 52 | C10 | 60 | C10 | - |
| | INT05_1 | | 65 | 43 | F9 | 55 | E10 | - |
| | INT05_2 | | 11 | 89 | E3 | 11 | G1 | 7 |
| | INT06_1 | External interrupt request 06 input pin | 73 | 51 | C11 | 59 | C11 | 48 |
| | INT06_2 | | 45 | 23 | K8 | 35 | K8 | 27 |
| | INT07_2 | External interrupt request 07 input pin | 5 | 83 | D1 | 5 | D1 | - |
| | INT08_1 | External interrupt request 08 input pin | 14 | 92 | F2 | - | - | - |
| | INT08_2 | | 8 | 86 | D5 | 8 | E1 | - |
| | INT09_1 | External interrupt request 09 input pin | 15 | 93 | F3 | - | - | - |
| | INT10_1 | External interrupt request 10 input pin | 16 | 94 | G1 | - | - | - |
| | INT11_1 | External interrupt request 11 input pin | 17 | 95 | G2 | - | - | - |
| | INT12_1 | External interrupt request 12 input pin | 27 | 5 | J4 | - | - | - |
| | INT13_1 | External interrupt request 13 input pin | 28 | 6 | L5 | - | - | - |
| | INT14_1 | External interrupt request 14 input pin | 39 | 17 | K6 | 29 | J5 | - |
| | INT15_1 | External interrupt request 15 input pin | 96 | 74 | C4 | 76 | C4 | 60 |
| | NMIX | Non-Maskable Interrupt input pin | 92 | 70 | B5 | 72 | A6 | 57 |

| Pin Function | Pin Name | Function Description | Pin No | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | BGA-96 | LQFP/ QFN-64 |
| GPIO | P00 | General-purpose I/O port 0 | 77 | 55 | A9 | 61 | A10 | 49 |
| | P01 | | 78 | 56 | B9 | 62 | B9 | 50 |
| | P02 | | 79 | 57 | B11 | 63 | B11 | 51 |
| | P03 | | 80 | 58 | A8 | 64 | A9 | 52 |
| | P04 | | 81 | 59 | B8 | 65 | B8 | 53 |
| | P05 | | 82 | 60 | C8 | - | - | - |
| | P06 | | 83 | 61 | D9 | - | - | - |
| | P07 | | 84 | 62 | A7 | 66 | A8 | - |
| | P08 | | 85 | 63 | B7 | - | - | - |
| | P09 | | 86 | 64 | C7 | - | - | - |
| | P0A | | 87 | 65 | D7 | 67 | C8 | 54 |
| | P0B | | 88 | 66 | A6 | 68 | C7 | 55 |
| | P0C | | 89 | 67 | B6 | 69 | B7 | 56 |
| | P0D | | 90 | 68 | C6 | 70 | B6 | - |
| | P0E | | 91 | 69 | A5 | 71 | C6 | - |
| | P0F | | 92 | 70 | B5 | 72 | A6 | 57 |
| | P10 | General-purpose I/O port 1 | 52 | 30 | J11 | 42 | J11 | 34 |
| | P11 | | 53 | 31 | J10 | 43 | J10 | 35 |
| | P12 | | 54 | 32 | J8 | 44 | J8 | 36 |
| | P13 | | 55 | 33 | H10 | 45 | H10 | 37 |
| | P14 | | 56 | 34 | H9 | 46 | H9 | 38 |
| | P15 | | 57 | 35 | H7 | 47 | G10 | 39 |
| | P16 | | 58 | 36 | G10 | 48 | G9 | - |
| | P17 | | 59 | 37 | G9 | 49 | F10 | 40 |
| | P18 | | 63 | 41 | G8 | 53 | F9 | 44 |
| | P19 | | 64 | 42 | F10 | 54 | E11 | 45 |
| | P1A | | 65 | 43 | F9 | 55 | E10 | - |
| | P1B | | 66 | 44 | E11 | 56 | E9 | - |
| | P1C | | 67 | 45 | E10 | - | - | - |
| | P1D | | 68 | 46 | F8 | - | - | - |
| | P1E | | 69 | 47 | E9 | - | - | - |
| | P1F | | 70 | 48 | D11 | - | - | - |
| | P20 | General-purpose I/O port 2 | 74 | 52 | C10 | 60 | C10 | - |
| | P21 | | 73 | 51 | C11 | 59 | C11 | 48 |
| | P22 | | 72 | 50 | E8 | 58 | D9 | 47 |
| | P23 | | 71 | 49 | D10 | 57 | D10 | 46 |

| Pin Function | Pin Name | Function Description | Pin No | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | BGA-96 | LQFP/ QFN-64 |
| GPIO | P30 | General-purpose I/O port 3 | 9 | 87 | E1 | 9 | E2 | 5 |
| | P31 | | 10 | 88 | E2 | 10 | E3 | 6 |
| | P32 | | 11 | 89 | E3 | 11 | G1 | 7 |
| | P33 | | 12 | 90 | E4 | 12 | G2 | 8 |
| | P34 | | 13 | 91 | F1 | - | - | - |
| | P35 | | 14 | 92 | F2 | - | - | - |
| | P36 | | 15 | 93 | F3 | - | - | - |
| | P37 | | 16 | 94 | G1 | - | - | - |
| | P38 | | 17 | 95 | G2 | - | - | - |
| | P39 | | 18 | 96 | F4 | 13 | G3 | 9 |
| | P3A | | 19 | 97 | G3 | 14 | H1 | 10 |
| | P3B | | 20 | 98 | H1 | 15 | H2 | 11 |
| | P3C | | 21 | 99 | H2 | 16 | H3 | 12 |
| | P3D | | 22 | 100 | G4 | 17 | J1 | 13 |
| | P3E | | 23 | 1 | H3 | 18 | J2 | 14 |
| | P3F | | 24 | 2 | J2 | 19 | J4 | 15 |
| | P40 | General-purpose I/O port 4 | 27 | 5 | J4 | - | - | - |
| | P41 | | 28 | 6 | L5 | - | - | - |
| | P42 | | 29 | 7 | K5 | - | - | - |
| | P43 | | 30 | 8 | J5 | - | - | - |
| | P44 | | 31 | 9 | H5 | 21 | L5 | - |
| | P45 | | 32 | 10 | L6 | 22 | K5 | - |
| | P46 | | 36 | 14 | L3 | 26 | L3 | 19 |
| | P47 | | 37 | 15 | K3 | 27 | K3 | 20 |
| | P48 | | 39 | 17 | K6 | 29 | J5 | - |
| | P49 | | 40 | 18 | J6 | 30 | K6 | 22 |
| | P4A | | 41 | 19 | L7 | 31 | J6 | 23 |
| | P4B | | 42 | 20 | K7 | 32 | L7 | 24 |
| | P4C | | 43 | 21 | H6 | 33 | K7 | 25 |
| | P4D | | 44 | 22 | J7 | 34 | J7 | 26 |
| | P4E | | 45 | 23 | K8 | 35 | K8 | 27 |
| | P50 | General-purpose I/O port 5 | 2 | 80 | C1 | 2 | C1 | 2 |
| | P51 | | 3 | 81 | C2 | 3 | C2 | 3 |
| | P52 | | 4 | 82 | B3 | 4 | B3 | 4 |
| | P53 | | 5 | 83 | D1 | 5 | D1 | - |
| | P54 | | 6 | 84 | D2 | 6 | D2 | - |
| | P55 | | 7 | 85 | D3 | 7 | D3 | - |
| | P56 | | 8 | 86 | D5 | 8 | E1 | - |
| | P60 | General-purpose I/O port 6 | 96 | 74 | C4 | 76 | C4 | 60 |
| | P61 | | 95 | 73 | B4 | 75 | B4 | 59 |
| | P62 | | 94 | 72 | C5 | 74 | C5 | 58 |
| | P63 | | 93 | 71 | D6 | 73 | B5 | - |
| | P80 | General-purpose I/O port 8 | 98 | 76 | A3 | 78 | A3 | 62 |
| | P81 | | 99 | 77 | A2 | 79 | A2 | 63 |
| | PE0 | General-purpose I/O port E | 46 | 24 | K9 | 36 | K9 | 28 |
| | PE2 | | 48 | 26 | L9 | 38 | L9 | 30 |
| | PE3 | | 49 | 27 | L10 | 39 | L10 | 31 |

| Pin Function | Pin Name | Function Description | Pin No | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | BGA-96 | LQFP/ QFN-64 |
| Multi-function Serial 0 | SIN0_0 | Multi-function serial interface ch.0 input pin | 73 | 51 | C11 | 59 | C11 | 48 |
| | SIN0_1 | | 56 | 34 | H9 | 46 | H9 | - |
| | SOT0_0 (SDA0_0) | Multi-function serial interface ch.0 output pin. This pin operates as SOT0 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA0 when it is used in an $I^2C$ (operation mode 4). | 72 | 50 | E8 | 58 | D9 | 47 |
| | SOT0_1 (SDA0_1) | | 57 | 35 | H7 | 47 | G10 | - |
| | SCK0_0 (SCL0_0) | Multi-function serial interface ch.0 clock I/O pin. This pin operates as SCK0 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL0 when it is used in an $I^2C$ (operation mode 4). | 71 | 49 | D10 | 57 | D10 | 46 |
| | SCK0_1 (SCL0_1) | | 58 | 36 | G10 | 48 | G9 | - |
| Multi-function Serial 1 | SIN1_1 | Multi-function serial interface ch.1 input pin | 53 | 31 | J10 | 43 | J10 | 35 |
| | SOT1_1 (SDA1_1) | Multi-function serial interface ch.1 output pin. This pin operates as SOT1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA1 when it is used in an $I^2C$ (operation mode 4). | 54 | 32 | J8 | 44 | J8 | 36 |
| | SCK1_1 (SCL1_1) | Multi-function serial interface ch.1 clock I/O pin. This pin operates as SCK1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL1 when it is used in an $I^2C$ (operation mode 4). | 55 | 33 | H10 | 45 | H10 | 37 |

| Pin Function | Pin Name | Function Description | Pin No | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | BGA-96 | LQFP/ QFN-64 |
| Multi-function Serial 2 | SIN2_2 | Multi-function serial interface ch.2 input pin | 59 | 37 | G9 | 49 | F10 | 40 |
| | SOT2_2 (SDA2_2) | Multi-function serial interface ch.2 output pin. This pin operates as SOT2 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA2 when it is used in an $I^2C$ (operation mode 4). | 63 | 41 | G8 | 53 | F9 | 44 |
| | SCK2_2 (SCL2_2) | Multi-function serial interface ch.2 clock I/O pin. This pin operates as SCK2 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL2 when it is used in an $I^2C$ (operation mode 4). | 64 | 42 | F10 | 54 | E11 | 45 |
| Multi-function Serial 3 | SIN3_1 | Multi-function serial interface ch.3 input pin | 2 | 80 | C1 | 2 | C1 | 2 |
| | SIN3_2 | | 39 | 17 | K6 | 29 | J5 | - |
| | SOT3_1 (SDA3_1) | Multi-function serial interface ch.3 output pin. This pin operates as SOT3 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA3 when it is used in an $I^2C$ (operation mode 4). | 3 | 81 | C2 | 3 | C2 | 3 |
| | SOT3_2 (SDA3_2) | | 40 | 18 | J6 | 30 | K6 | - |
| | SCK3_1 (SCL3_1) | Multi-function serial interface ch.3 clock I/O pin. This pin operates as SCK3 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL3 when it is used in an $I^2C$ (operation mode 4). | 4 | 82 | B3 | 4 | B3 | 4 |
| | SCK3_2 (SCL3_2) | | 41 | 19 | L7 | 31 | J6 | - |

| Pin Function | Pin Name | Function Description | Pin No | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | BGA-96 | LQFP/ QFN-64 |
| Multi-function Serial 4 | SIN4_0 | Multi-function serial interface ch.4 input pin | 87 | 65 | D7 | 67 | C8 | 54 |
| | SIN4_1 | | 65 | 43 | F9 | 55 | E10 | - |
| | SIN4_2 | | 82 | 60 | C8 | - | - | - |
| | SOT4_0 (SDA4_0) | Multi-function serial interface ch.4 output pin. This pin operates as SOT4 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA4 when it is used in an I²C (operation mode 4). | 88 | 66 | A6 | 68 | C7 | 55 |
| | SOT4_1 (SDA4_1) | | 66 | 44 | E11 | 56 | E9 | - |
| | SOT4_2 (SDA4_2) | | 83 | 61 | D9 | - | - | - |
| | SCK4_0 (SCL4_0) | Multi-function serial interface ch.4 clock I/O pin. This pin operates as SCK4 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL4 when it is used in an I²C (operation mode 4). | 89 | 67 | B6 | 69 | B7 | 56 |
| | SCK4_1 (SCL4_1) | | 67 | 45 | E10 | - | - | - |
| | SCK4_2 (SCL4_2) | | 84 | 62 | A7 | - | - | - |
| | RTS4_0 | Multi-function serial interface ch.4 RTS output pin | 90 | 68 | C6 | 70 | B6 | - |
| | RTS4_1 | | 69 | 47 | E9 | - | - | - |
| | RTS4_2 | | 86 | 64 | C7 | - | - | - |
| | CTS4_0 | Multi-function serial interface ch.4 CTS input pin | 91 | 69 | A5 | 71 | C6 | - |
| | CTS4_1 | | 68 | 46 | F8 | - | - | - |
| | CTS4_2 | | 85 | 63 | B7 | - | - | - |
| Multi-function Serial 5 | SIN5_0 | Multi-function serial interface ch.5 input pin | 96 | 74 | C4 | 76 | C4 | 60 |
| | SIN5_2 | | 15 | 93 | F3 | - | - | - |
| | SOT5_0 (SDA5_0) | Multi-function serial interface ch.5 output pin. This pin operates as SOT5 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA5 when it is used in an I²C (operation mode 4). | 95 | 73 | B4 | 75 | B4 | 59 |
| | SOT5_2 (SDA5_2) | | 16 | 94 | G1 | - | - | - |
| | SCK5_0 (SCL5_0) | Multi-function serial interface ch.5 clock I/O pin. This pin operates as SCK5 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL5 when it is used in an I²C (operation mode 4). | 94 | 72 | C5 | 74 | C5 | 58 |
| | SCK5_2 (SCL5_2) | | 17 | 95 | G2 | - | - | - |

| Pin Function | Pin Name | Function Description | Pin No | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | BGA-96 | LQFP/ QFN-64 |
| Multi-function Serial 6 | SIN6_0 | Multi-function serial interface ch.6 input pin | 5 | 83 | D1 | 5 | D1 | - |
| | SIN6_1 | | 12 | 90 | E4 | 12 | G2 | 8 |
| | SOT6_0 (SDA6_0) | Multi-function serial interface ch.6 output pin. This pin operates as SOT6 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA6 when it is used in an I²C (operation mode 4). | 6 | 84 | D2 | 6 | D2 | - |
| | SOT6_1 (SDA6_1) | | 11 | 89 | E3 | 11 | G1 | 7 |
| | SCK6_0 (SCL6_0) | Multi-function serial interface ch.6 clock I/O pin. This pin operates as SCK6 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL6 when it is used in an I²C (operation mode 4). | 7 | 85 | D3 | 7 | D3 | - |
| | SCK6_1 (SCL6_1) | | 10 | 88 | E2 | 10 | E3 | 6 |
| Multi-function Serial 7 | SIN7_1 | Multi-function serial interface ch.7 input pin | 45 | 23 | K8 | 35 | K8 | 27 |
| | SOT7_1 (SDA7_1) | Multi-function serial interface ch.7 output pin. This pin operates as SOT7 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA7 when it is used in an I²C (operation mode 4). | 44 | 22 | J7 | 34 | J7 | 26 |
| | SCK7_1 (SCL7_1) | Multi-function serial interface ch.7 clock I/O pin. This pin operates as SCK7 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL7 when it is used in an I²C (operation mode 4). | 43 | 21 | H6 | 33 | K7 | 25 |

| Pin Function | Pin Name | Function Description | Pin No | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | BGA-96 | LQFP/ QFN-64 |
| Real-time clock | RTCCO_0 | 0.5 seconds pulse output pin of Real-time clock | 92 | 70 | B5 | 72 | A6 | 57 |
| | RTCCO_1 | | 55 | 33 | H10 | 45 | H10 | 37 |
| | RTCCO_2 | | 19 | 97 | G3 | 14 | H1 | 10 |
| | SUBOUT_0 | Sub clock output pin | 92 | 70 | B5 | 72 | A6 | 57 |
| | SUBOUT_1 | | 55 | 33 | H10 | 45 | H10 | 37 |
| | SUBOUT_2 | | 19 | 97 | G3 | 14 | H1 | 10 |
| Low-Power Consumption Mode | WKUP0 | Deep standby mode return signal input pin 0 | 92 | 70 | B5 | 72 | A6 | 57 |
| | WKUP1 | Deep standby mode return signal input pin 1 | 53 | 31 | J10 | 43 | J10 | 35 |
| | WKUP2 | Deep standby mode return signal input pin 2 | 73 | 51 | C11 | 59 | C11 | 48 |
| | WKUP3 | Deep standby mode return signal input pin 3 | 96 | 74 | C4 | 76 | C4 | 60 |
| HDMI-CEC/ Remote Control | CEC0 | HDMI-CEC/Remote Control Reception ch.0 input/output pin | 43 | 21 | H6 | 33 | K7 | 25 |
| | CEC1 | HDMI-CEC/Remote Control Reception ch.1 input/output pin | 96 | 74 | C4 | 76 | C4 | 60 |

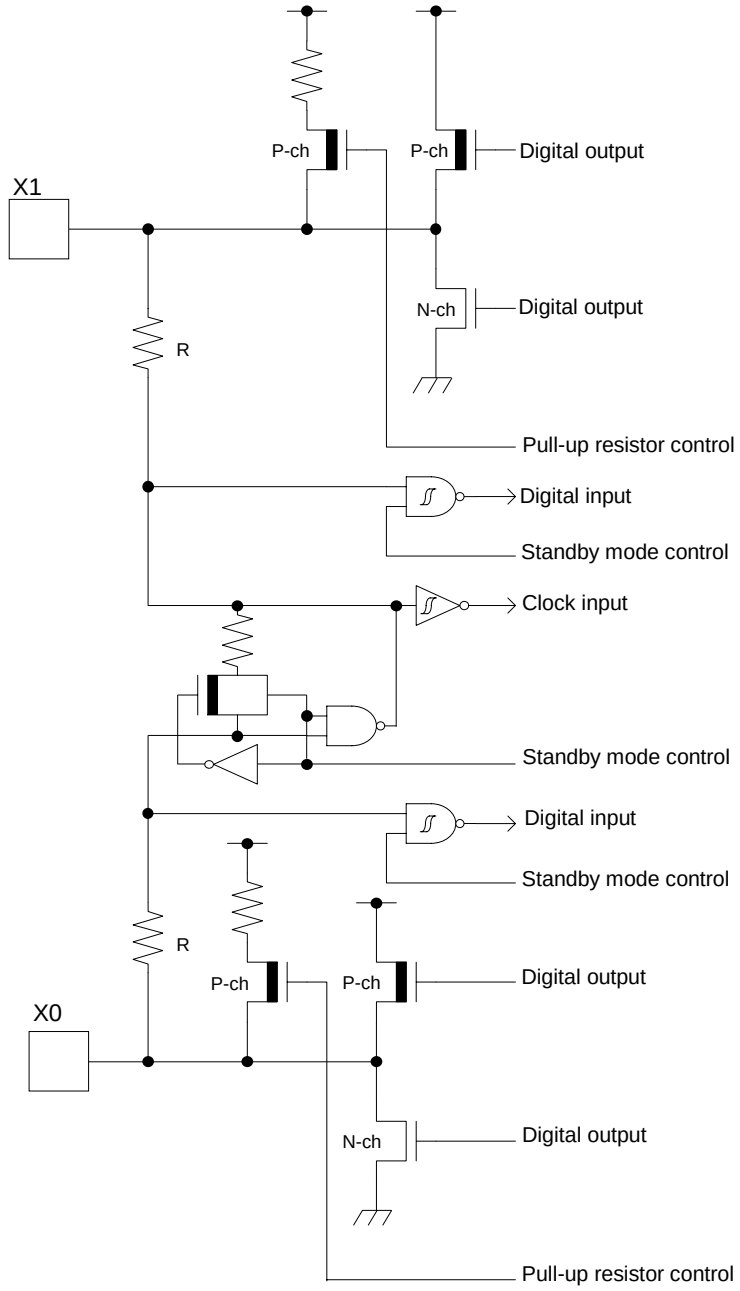
| Pin Function | Pin Name | Function Description | Pin No | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | BGA-96 | LQFP/ QFN-64 |
| Reset | INITX | External Reset Input pin. A reset is valid when INITX=L. | 38 | 16 | K4 | 28 | K4 | 21 |
| Mode | MD0 | Mode 0 pin. During normal operation, MD0=L must be input. During serial programming to Flash memory, MD0=H must be input. | 47 | 25 | L8 | 37 | L8 | 29 |
| | MD1 | Mode 1 pin. During serial programming to Flash memory, MD1=L must be input. | 46 | 24 | K9 | 36 | K9 | 28 |
| Power | VCC | Power supply Pin | 1 | 79 | B1 | 1 | B1 | 1 |
| | VCC | Power supply Pin | 26 | 4 | J1 | - | - | - |
| | VCC | Power supply Pin | 35 | 13 | K1 | 25 | K1 | 18 |
| | VCC | Power supply Pin | 51 | 29 | K11 | 41 | K11 | 33 |
| | VCC | Power supply Pin | 76 | 54 | A10 | - | - | - |
| | VCC | Power supply Pin | 97 | 75 | A4 | 77 | A4 | 61 |
| GND | VSS | GND Pin | - | - | - | - | F1 | - |
| | VSS | GND Pin | - | - | - | - | F2 | - |
| | VSS | GND Pin | - | - | - | - | F3 | - |
| | VSS | GND Pin | - | - | B2 | - | B2 | - |
| | VSS | GND Pin | 25 | 3 | L1 | 20 | L1 | 16 |
| | VSS | GND Pin | - | - | K2 | - | K2 | - |
| | VSS | GND Pin | - | - | J3 | - | J3 | - |
| | VSS | GND Pin | - | - | H4 | - | - | - |
| | VSS | GND Pin | - | - | - | - | L6 | - |
| | VSS | GND Pin | 34 | 12 | L4 | 24 | L4 | - |
| | VSS | GND Pin | 50 | 28 | L11 | 40 | L11 | 32 |
| | VSS | GND Pin | - | - | K10 | - | K10 | - |
| | VSS | GND Pin | - | - | J9 | - | J9 | - |
| | VSS | GND Pin | - | - | H8 | - | - | - |
| | VSS | GND Pin | - | - | B10 | - | B10 | - |
| | VSS | GND Pin | - | - | C9 | - | C9 | - |
| | VSS | GND Pin | - | - | - | - | D11 | - |
| | VSS | GND Pin | 75 | 53 | A11 | - | A11 | - |
| | VSS | GND Pin | - | - | D8 | - | - | - |
| | VSS | GND Pin | - | - | - | - | A7 | - |
| | VSS | GND Pin | - | - | D4 | - | - | - |
| | VSS | GND Pin | - | - | C3 | - | C3 | - |
| | VSS | GND Pin | - | - | - | - | A5 | - |
| | VSS | GND Pin | 100 | 78 | A1 | 80 | A1 | 64 |

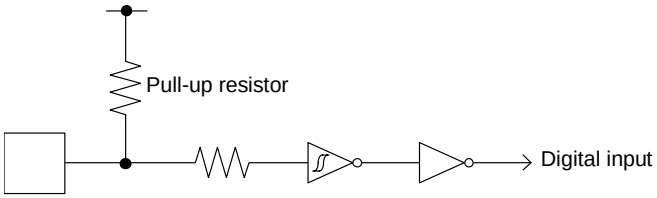
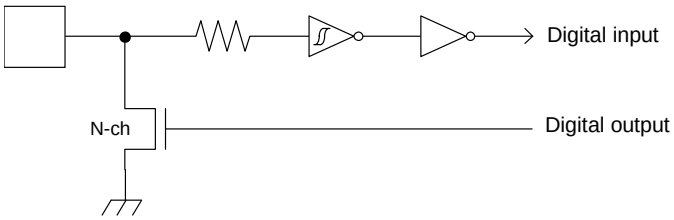
| Pin Function | Pin Name | Function Description | Pin No | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | BGA-96 | LQFP/ QFN-64 |
| Clock | X0 | Main clock (oscillation) input pin | 48 | 26 | L9 | 38 | L9 | 30 |
| | X0A | Sub clock (oscillation) input pin | 36 | 14 | L3 | 26 | L3 | 19 |
| | X1 | Main clock (oscillation) I/O pin | 49 | 27 | L10 | 39 | L10 | 31 |
| | X1A | Sub clock (oscillation) I/O pin | 37 | 15 | K3 | 27 | K3 | 20 |
| | CROUT_0 | Built-in high-speed CR-osc clock output port | 74 | 52 | C10 | 60 | C10 | - |
| | CROUT_1 | | 92 | 70 | B5 | 72 | A6 | 57 |
| ADC power | AVCC | A/D converter analog power supply pin | 60 | 38 | H11 | 50 | H11 | 41 |
| | AVRH | A/D converter analog reference voltage input pin | 61 | 39 | F11 | 51 | F11 | 42 |
| ADC GND | AVSS | A/D converter GND pin | 62 | 40 | G11 | 52 | G11 | 43 |
| C pin | C | Power stabilization capacity pin | 33 | 11 | L2 | 23 | L2 | 17 |

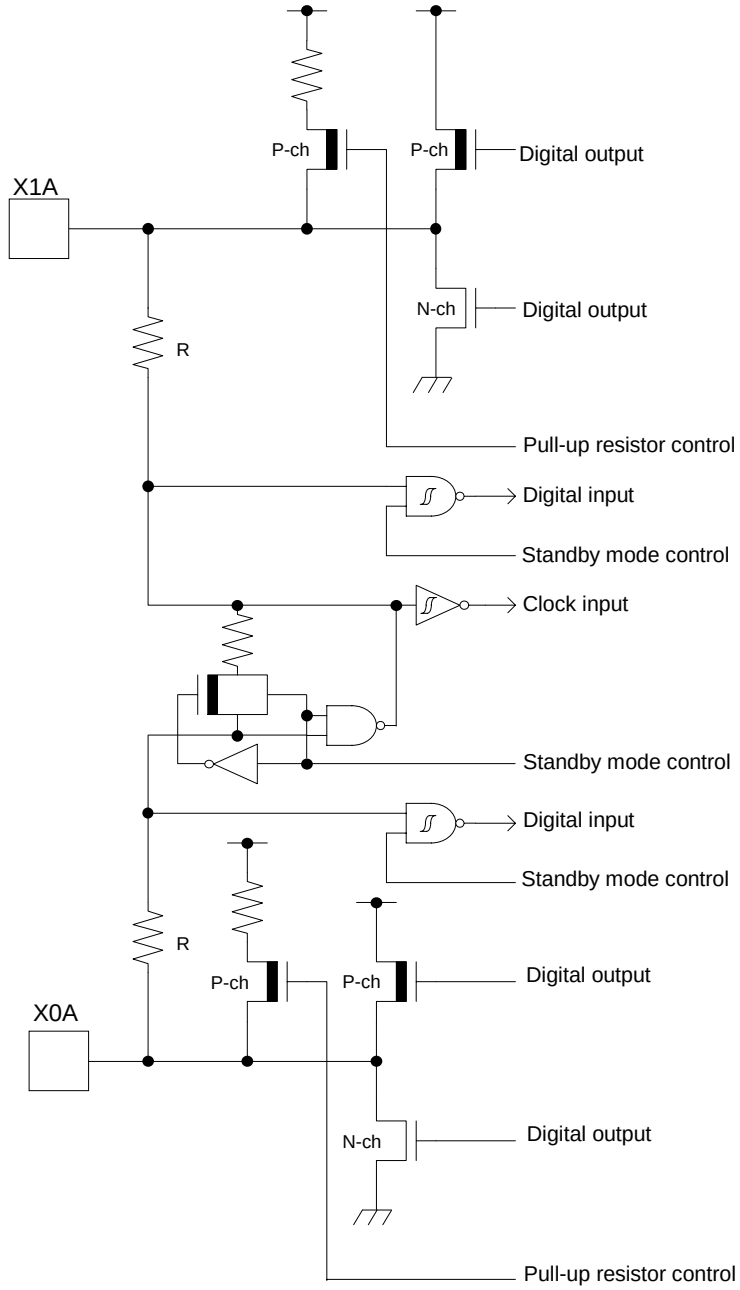
***Note:***

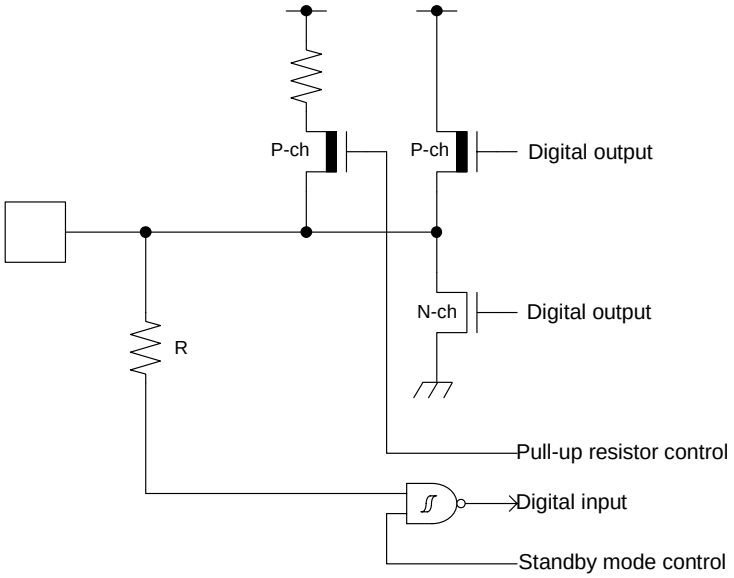
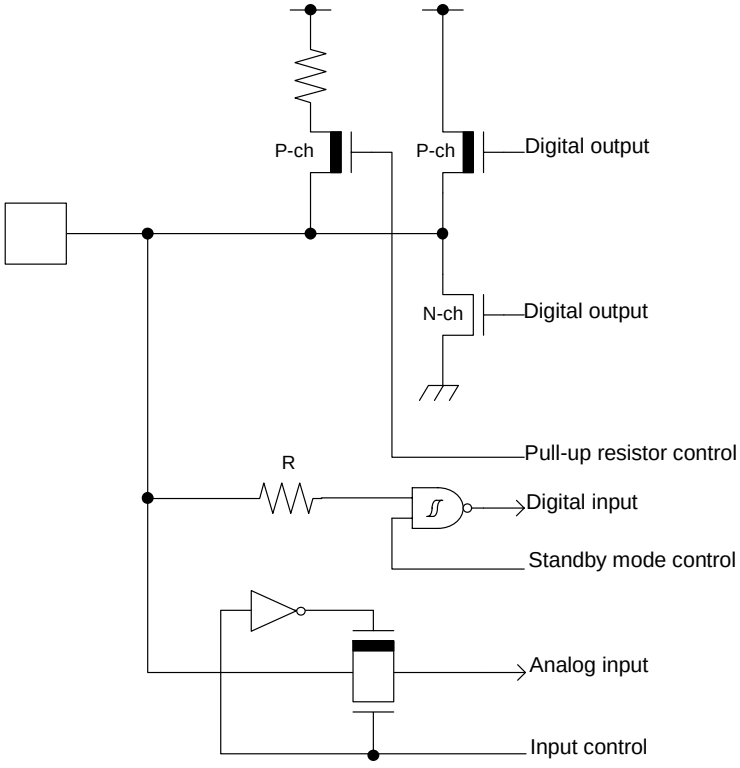
- *While this device contains a Test Access Port (TAP) based on the IEEE 1149.1-2001 JTAG standard, it is not fully compliant to all requirements of that standard. This device may contain a 32-bit device ID that is the same as the 32-bit device ID in other devices with different functionality. The TAP pins may also be configurable for purposes other than access to the TAP controller.*

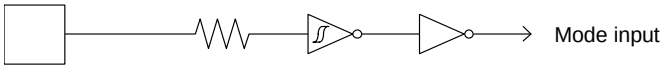
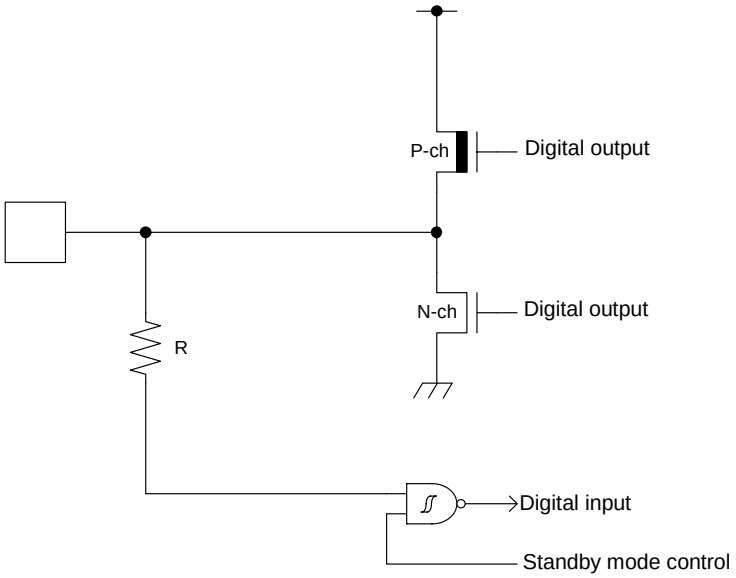
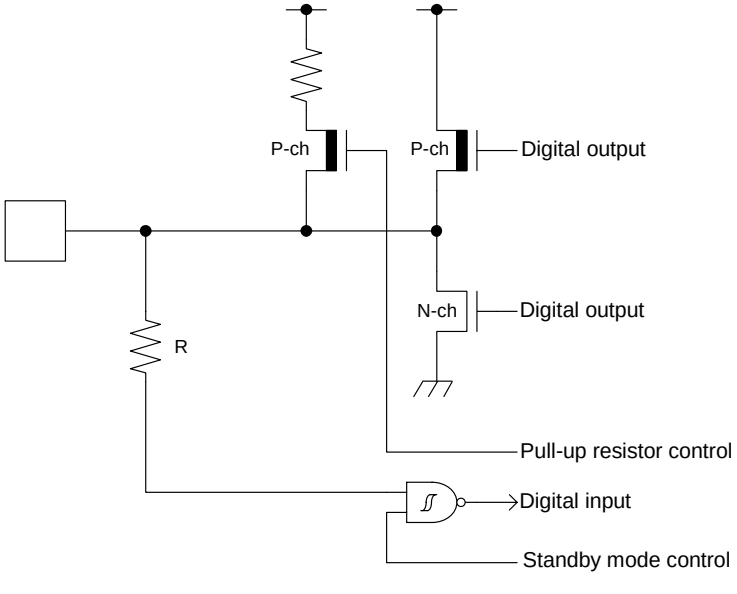
## 5. I/O Circuit Type

| Type | Circuit | Remarks |
|---|---|---|
| A |  | It is possible to select the main oscillation / GPIO function<br><br>When the main oscillation is selected.<br>– Oscillation feedback resistor : Approximately 1 MΩ<br>– With Standby mode control<br><br>When the GPIO is selected.<br>– CMOS level output.<br>– CMOS level hysteresis input<br>– With pull-up resistor control<br>– With standby mode control<br>– Pull-up resistor : Approximately 33 kΩ<br>– $I_{OH}$ = -4 mA, $I_{OL}$ = 4 mA |

| Type | Circuit | Remarks |
|---|---|---|
| B |  | – CMOS level hysteresis input<br>– Pull-up resistor<br>: Approximately 33 kΩ |
| C |  | – Open drain output<br>– CMOS level hysteresis input |

| Type | Circuit | Remarks |
|---|---|---|
| D |  | It is possible to select the sub oscillation / GPIO function<br><br>When the sub oscillation is selected.<br>– Oscillation feedback resistor : Approximately 5 MΩ<br>– With Standby mode control<br><br>When the GPIO is selected.<br>– CMOS level output.<br>– CMOS level hysteresis input<br>– With pull-up resistor control<br>– With standby mode control<br>– Pull-up resistor : Approximately 33 kΩ<br>– $I_{OH}$ = -4 mA, $I_{OL}$ = 4 mA |

| Type | Circuit | Remarks |
|---|---|---|
| E |  | – CMOS level output<br>– CMOS level hysteresis input<br>– With pull-up resistor control<br>– With standby mode control<br>– Pull-up resistor<br>: Approximately 33 kΩ<br>– $I_{OH}$ = -4 mA, $I_{OL}$ = 4 mA<br>– When this pin is used as an $I^2C$ pin, the digital output P-ch transistor is always off |
| F |  | – CMOS level output<br>– CMOS level hysteresis input<br>– With input control<br>– Analog input<br>– With pull-up resistor control<br>– With standby mode control<br>– Pull-up resistor<br>: Approximately 33 kΩ<br>– $I_{OH}$ = -4 mA, $I_{OL}$ = 4 mA<br>– When this pin is used as an $I^2C$ pin, the digital output P-ch transistor is always off |

| Type | Circuit | Remarks |
|---|---|---|
| G |  | – CMOS level hysteresis input |
| H |  | – CMOS level output<br>– CMOS level hysteresis input<br>– With standby mode control<br>$I_{OH}$ = -12.0 mA, $I_{OL}$ = 10.5 mA |
| I |  | – CMOS level output<br>– CMOS level hysteresis input<br>– 5 V tolerant<br>– With pull-up resistor control<br>– With standby mode control<br>– Pull-up resistor<br>: Approximately 33 kΩ<br>– $I_{OH}$ = -4 mA, $I_{OL}$ = 4 mA<br>– Available to control PZR registers.<br>– When this pin is used as an $I^2C$ pin, the digital output P-ch transistor is always off |

# 6. Handling Precaution

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

## 6.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

### Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

### Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the datasheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

### Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

1. Preventing Over-Voltage and Over-Current Conditions
   Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.
2. Protection of Output Pins
   Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
   Therefore, avoid this type of connection.
3. Handling of Unused Input Pins
   Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

#### Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

### Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

### Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

.

### Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

## 6.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress' recommended conditions. For detailed information about mount conditions, contact your sales representative.

### Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

### Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress Inc. recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

### Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

### Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
   When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress Inc. packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

#### Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

**Static Electricity**

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
   Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

## 6.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

   Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.
2. Discharge of Static Electricity

   When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.
3. Corrosive Gases, Dust, or Oil

   Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.
4. Radiation, Including Cosmic Radiation

   Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.
5. Smoke, Flame

   CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

# 7. Handling Devices

### Power supply pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with each Power supply pin and GND pin of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1 µF be connected as a bypass capacitor between each Power supply pin and GND pin, between AVCC pin and AVSS pin near this device.

### Stabilizing supply voltage

A malfunction may occur when the power supply voltage fluctuates rapidly even though the fluctuation is within the recommended operating conditions of the VCC power supply voltage. As a rule, with voltage stabilization, suppress the voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the VCC value in the recommended operating conditions, and the transient fluctuation rate does not exceed 0.1 V/µs when there is a momentary fluctuation on switching the power supply..

### Crystal oscillator circuit

Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator, and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

Evaluate oscillation of your using crystal oscillator by your mount board.

### Sub crystal oscillator

This series sub oscillator circuit is low gain to keep the low current consumption.
The crystal oscillator to fill the following conditions is recommended for sub crystal oscillator to stabilize the oscillation.

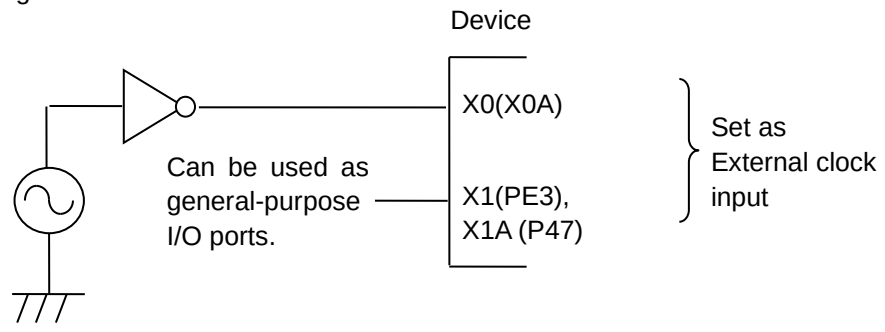
■ Surface mount type
Size: More than 3.2 mm × 1.5 mm
Load capacitance: Approximately 6 pF to 7 pF

■ Lead type
Load capacitance: Approximately 6 pF to 7 pF

### Using an external clock

When using an external clock as an input of the main clock, set X0/X1 to the external clock input, and input the clock to X0. X1(PE3) can be used as a general-purpose I/O port.
Similarly, when using an external clock as an input of the sub clock, set X0A/X1A to the external clock input, and input the clock to X0A. X1A (P47) can be used as a general-purpose I/O port.

Example of Using an External Clock

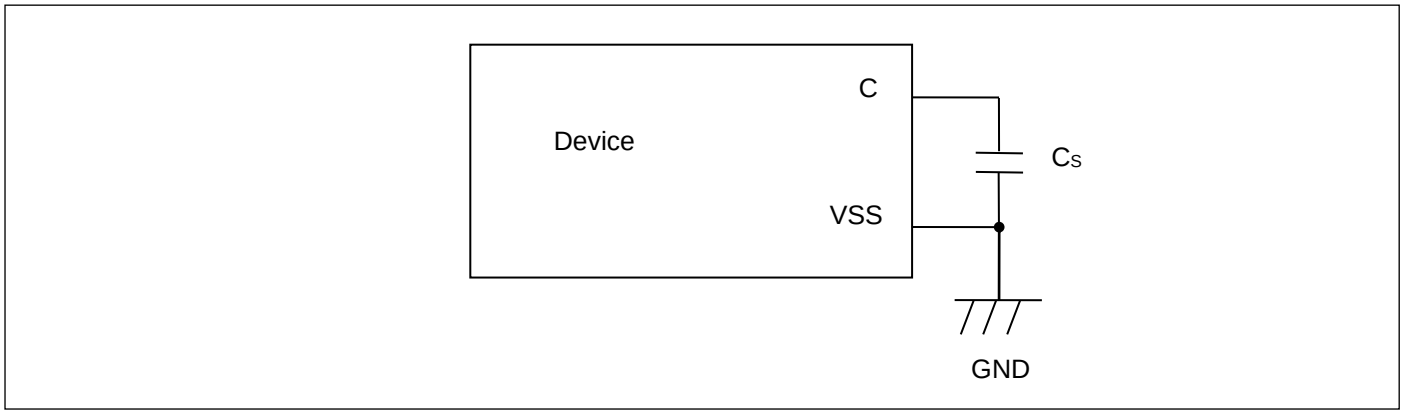


### Handling when using Multi-function serial pin as I²C pin

If it is using the multi-function serial pin as I²C pins, P-ch transistor of digital output is always disabled. However, I²C pins need to keep the electrical characteristic like other pins and not to connect to the external I²C bus system with power OFF.

### C Pin

This series contains the regulator. Be sure to connect a smoothing capacitor ($C_S$) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor.
However, some laminated ceramic capacitors have the characteristics of capacitance variation due to thermal fluctuation (F characteristics and Y5V characteristics). Please select the capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of a capacitor. A smoothing capacitor of about 4.7 µF would be recommended for this series.




### Mode pins (MD0)

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistor stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

### Notes on power-on

Turn power on/off in the following order or at the same time.
If not using the A/D converter, connect AVCC = VCC and AVSS = VSS.

Turning on: VCC →AVCC → AVRH

Turning off: AVRH → AVCC → VCC

### Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.
Consider the case of receiving wrong data due to noise, perform error detection such as by applying a checksum of data at the end.
If an error is detected, retransmit the data.

### Differences in features among the products with different memory sizes and between Flash memory products and MASK products

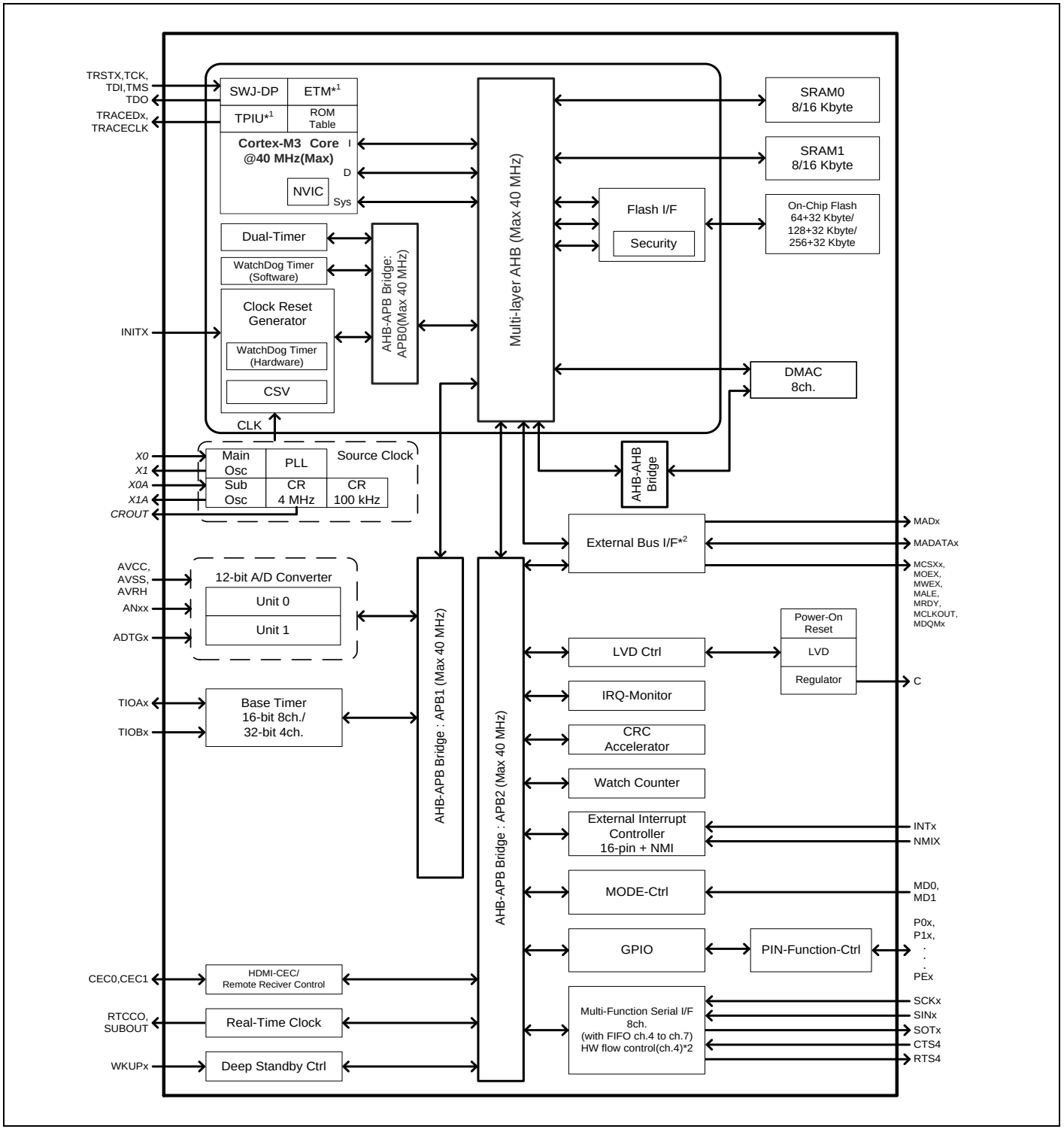
The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash memory products and MASK products are different because chip layout and memory structures are different.

If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

### Pull-Up function of 5 V tolerant I/O

Please do not input the signal more than VCC voltage at the time of Pull-Up function use of 5 V tolerant I/O.

## 8. Block Diagram




*1: For the MB9AF141LB/MB, MB9AF142LB/MB, and MB9AF144LB/MB, ETM is not available.

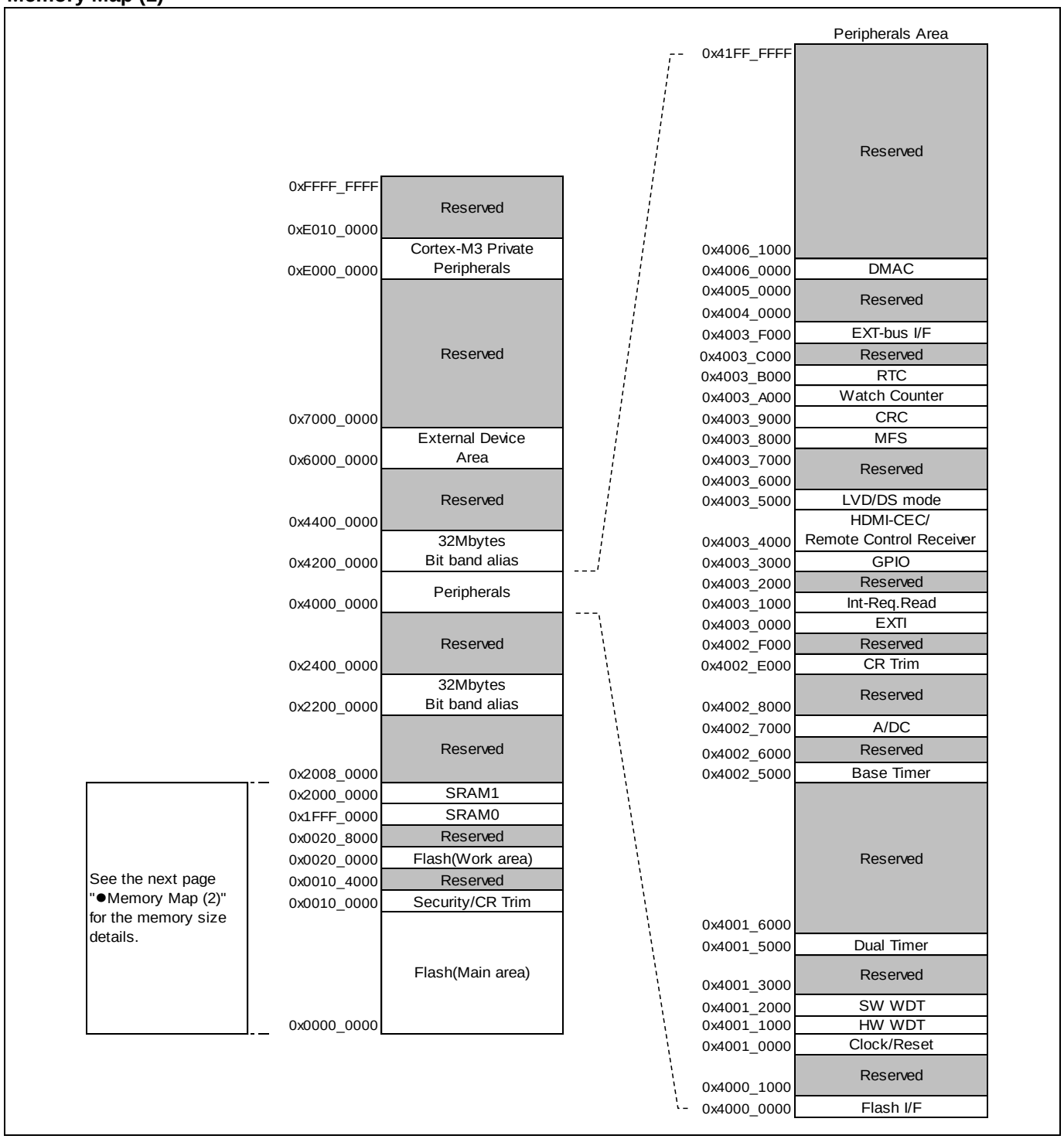
*2: For the MB9AF141LB, MB9AF142LB and MB9AF144LB, the External Bus Interface is not available. And the Multi-function Serial Interface does not support hardware flow control in these products.

## 9. Memory Size

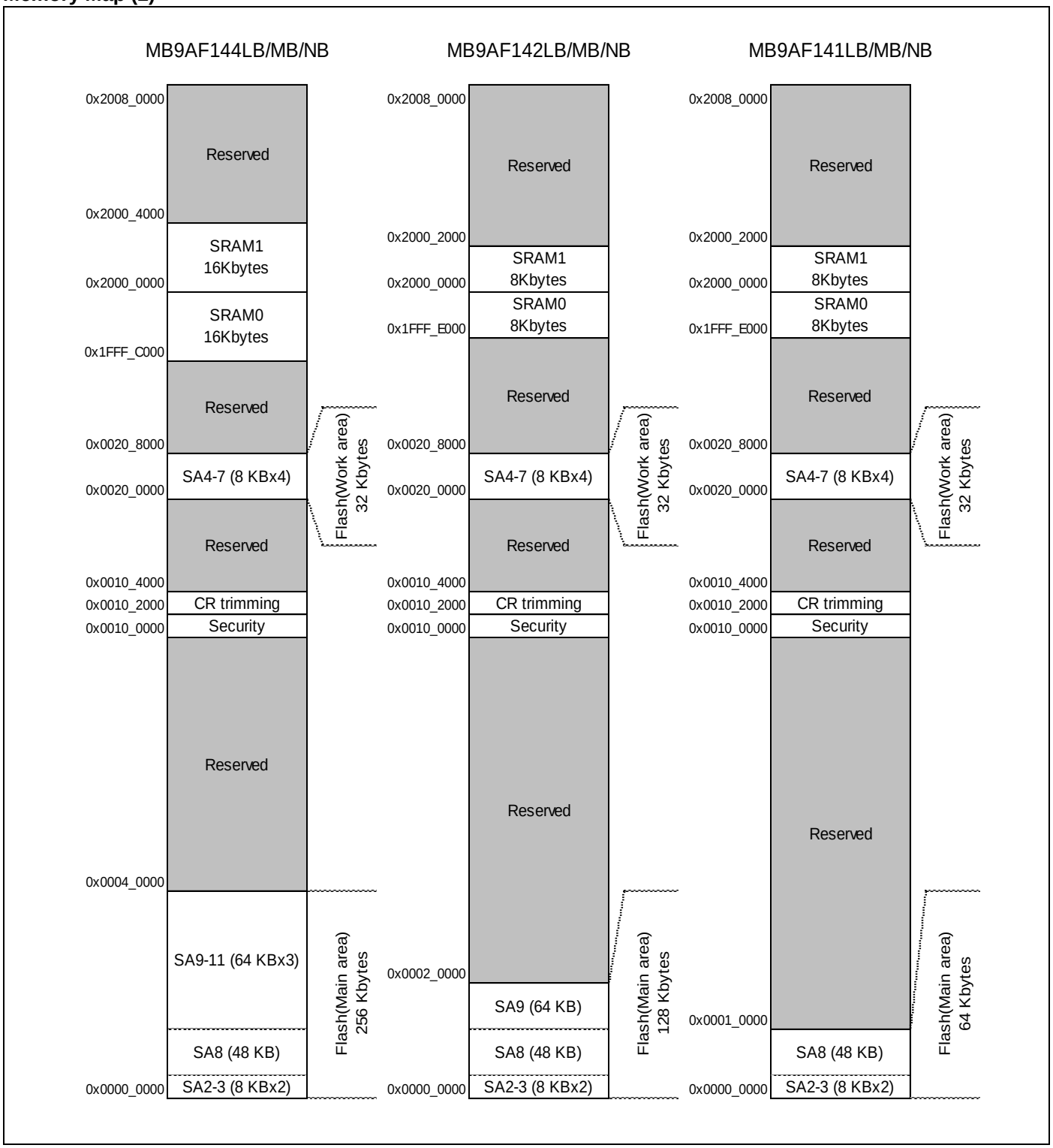
See “Memory size” in “1. Product Lineup” to confirm the memory size.

## 10. Memory Map

### Memory Map (1)



**Memory Map (2)**




Refer to the programming manual for the detail of Flash main area.
MB9AB40N/A40N/340N/140N/150R,MB9B520M/320M/120M Series Flash Programming Manual

## Peripheral Address Map

| Start address | End address | Bus | Peripherals |
|---|---|---|---|
| 0x4000_0000 | 0x4000_0FFF | AHB | Flash memory I/F register |
| 0x4000_1000 | 0x4000_FFFF | | Reserved |
| 0x4001_0000 | 0x4001_0FFF | APB0 | Clock/Reset Control |
| 0x4001_1000 | 0x4001_1FFF | | Hardware Watchdog timer |
| 0x4001_2000 | 0x4001_2FFF | | Software Watchdog timer |
| 0x4001_3000 | 0x4001_4FFF | | Reserved |
| 0x4001_5000 | 0x4001_5FFF | | Dual Timer |
| 0x4001_6000 | 0x4001_FFFF | | Reserved |
| 0x4002_0000 | 0x4002_4FFF | APB1 | Reserved |
| 0x4002_5000 | 0x4002_5FFF | | Base Timer |
| 0x4002_6000 | 0x4002_6FFF | | Reserved |
| 0x4002_7000 | 0x4002_7FFF | | A/D Converter |
| 0x4002_8000 | 0x4002_DFFF | | Reserved |
| 0x4002_E000 | 0x4002_EFFF | | Built-in CR trimming |
| 0x4002_F000 | 0x4002_FFFF | | Reserved |
| 0x4003_0000 | 0x4003_0FFF | APB2 | External Interrupt |
| 0x4003_1000 | 0x4003_1FFF | | Interrupt Source Check Register |
| 0x4003_2000 | 0x4003_2FFF | | Reserved |
| 0x4003_3000 | 0x4003_3FFF | | GPIO |
| 0x4003_4000 | 0x4003_4FFF | | HDMI-CEC/Remote control Receiver |
| 0x4003_5000 | 0x4003_57FF | | Low-Voltage Detector |
| 0x4003_5800 | 0x4003_5FFF | | Deep standby mode Controller |
| 0x4003_6000 | 0x4003_7FFF | | Reserved |
| 0x4003_8000 | 0x4003_8FFF | | Multi-function serial |
| 0x4003_9000 | 0x4003_9FFF | | CRC |
| 0x4003_A000 | 0x4003_AFFF | | Watch Counter |
| 0x4003_B000 | 0x4003_BFFF | | Real-time clock |
| 0x4003_C000 | 0x4003_EFFF | | Reserved |
| 0x4003_F000 | 0x4003_FFFF | | External bus interface |
| 0x4004_0000 | 0x4005_FFFF | AHB | Reserved |
| 0x4006_0000 | 0x4006_0FFF | | DMAC register |
| 0x4006_1000 | 0x41FF_FFFF | | Reserved |

## 11. Pin Status in Each CPU State

The terms used for pin status have the following meanings.

- INITX=0

  This is the period when the INITX pin is the L level.

- INITX=1

  This is the period when the INITX pin is the H level.

- SPL=0

  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 0.

- SPL=1

  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 1.

- Input enabled

  Indicates that the input function can be used.

- Internal input fixed at 0

  This is the status that the input function cannot be used. Internal input is fixed at L.

- Hi-Z

  Indicates that the pin drive transistor is disabled and the pin is put in the Hi-Z state.

- Setting disabled

  Indicates that the setting is disabled.

- Maintain previous state

  Maintains the state that was immediately prior to entering the current mode.
  If a built-in peripheral function is operating, the output follows the peripheral function.
  If the pin is being used as a port, that output is maintained.

- Analog input is enabled

  Indicates that the analog input is enabled.

- Trace output

  Indicates that the trace function can be used.

- GPIO selected

  In Deep standby mode, pins switch to the general-purpose I/O port.

## List of Pin Status

| Pin status type | Function group | Power-on reset or low-voltage detection state | INITX input state | Device internal reset state | Run mode or Sleep mode state | Timer mode, RTC mode, or Stop mode state | | Deep standby RTC mode or Deep standby Stop mode state | | Return from Deep standby mode state |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Power supply unstable | Power supply stable | | Power supply stable | Power supply stable | | Power supply stable | | Power supply stable |
| | | - | INITX = 0 | INITX = 1 | INITX = 1 | INITX = 1 | | INITX = 1 | | INITX = 1 |
| | | - | - | - | - | SPL = 0 | SPL = 1 | SPL = 0 | SPL = 1 | - |
| A | GPIO selected | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Hi-Z / Internal input fixed at 0 | GPIO selected Internal input fixed at 0 | Hi-Z / Internal input fixed at 0 | GPIO selected |
| | Main crystal oscillator input pin/ External main clock input selected | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled |
| B | GPIO selected | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Hi-Z / Internal input fixed at "0" | GPIO selected Internal input fixed at 0 | Hi-Z / Internal input fixed at 0 | GPIO selected |
| | External main clock input selected | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Hi-Z / Internal input fixed at 0 | Maintain previous state | Hi-Z / Internal input fixed at 0 | Maintain previous state |
| | Main crystal oscillator output pin | Hi-Z / Internal input fixed at 0/ or Input enabled | Hi-Z / Internal input fixed at 0 | Hi-Z / Internal input fixed at 0 | Maintain previous state/ When oscillation stops *1, Hi-Z / Internal input fixed at 0 | Maintain previous state/ When oscillation stops *1, Hi-Z / Internal input fixed at 0 | Maintain previous state/ When oscillation stops *1, Hi-Z / Internal input fixed at 0 | Maintain previous state/ When oscillation stops *1, Hi-Z / Internal input fixed at 0 | Maintain previous state/ When oscillation stops *1, Hi-Z / Internal input fixed at 0 | Maintain previous state/ When oscillation stops *1, Hi-Z / Internal input fixed at 0 |
| C | INITX input pin | Pull-up / Input enabled | Pull-up / Input enabled | Pull-up / Input enabled | Pull-up / Input enabled | Pull-up / Input enabled | Pull-up / Input enabled | Pull-up / Input enabled | Pull-up / Input enabled | Pull-up / Input enabled |
| D | Mode input pin | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled |

| Pin status type | Function group | Power-on reset or low-voltage detection state | INITX input state | Device internal reset state | Run mode or Sleep mode state | Timer mode, RTC mode, or Stop mode state | | Deep standby RTC mode or Deep standby Stop mode state | | Return from Deep standby mode state |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Power supply unstable | Power supply stable | | Power supply stable | Power supply stable | | Power supply stable | | Power supply stable |
| | | - | INITX = 0 | INITX = 1 | INITX = 1 | INITX = 1 | | INITX = 1 | | INITX = 1 |
| | | - | - | - | - | SPL = 0 | SPL = 1 | SPL = 0 | SPL = 1 | - |
| E | Mode input pin | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled |
| | GPIO selected | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Hi-Z / Input enabled | GPIO selected | Hi-Z / Input enabled | GPIO selected |
| F | GPIO selected | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Hi-Z / Internal input fixed at 0 | GPIO selected Internal input fixed at 0 | Hi-Z / Internal input fixed at 0 | GPIO selected |
| | Sub crystal oscillator input pin / External sub clock input selected | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled |
| G | GPIO selected | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Hi-Z / Internal input fixed at 0 | GPIO selected Internal input fixed at 0 | Hi-Z / Internal input fixed at 0 | GPIO selected |
| | External sub clock input selected | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Hi-Z / Internal input fixed at 0 | Maintain previous state | Hi-Z/ Internal input fixed at 0 | Maintain previous state |
| | Sub crystal oscillator output pin | Hi-Z / Internal input fixed at 0 / or Input enable | Hi-Z / Internal input fixed at 0 | Hi-Z / Internal input fixed at 0 | Maintain previous state | Maintain previous state/ When oscillation stops [*2], Hi-Z / Internal input fixed at 0 | Maintain previous state/ When oscillation stops [*2], Hi-Z / Internal input fixed at 0 | Maintain previous state/ When oscillation stops [*2], Hi-Z/ Internal input fixed at 0 | Maintain previous state/ When oscillation stops [*2], Hi-Z/ Internal input fixed at 0 | Maintain previous state/ When oscillation stops [*2], Hi-Z/ Internal input fixed at 0 |

| Pin status type | Function group | Power-on reset or low-voltage detection state | INITX input state | Device internal reset state | Run mode or Sleep mode state | Timer mode, RTC mode, or Stop mode state | | Deep standby RTC mode or Deep standby Stop mode state | | Return from Deep standby mode state |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Power supply unstable | Power supply stable | | Power supply stable | Power supply stable | | Power supply stable | | Power supply stable |
| | | - | INITX = 0 | INITX = 1 | INITX = 1 | INITX = 1 | | INITX = 1 | | INITX = 1 |
| | | - | - | - | - | SPL = 0 | SPL = 1 | SPL = 0 | SPL = 1 | - |
| H | GPIO selected | Hi-Z | Hi-Z / Input enabled | Hi-Z / Input enabled | Maintain previous state | Maintain previous state | Hi-Z / Internal input fixed at 0 | GPIO selected Internal input fixed at 0 | Hi-Z / Internal input fixed at 0 | GPIO selected |
| I | NMIX selected | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Maintain previous state | WKUP input enabled | Hi-Z / WKUP input enabled | GPIO selected |
| | Resource other than above selected | Hi-Z | Hi-Z / Input enabled | Hi-Z / Input enabled | | | Hi-Z / Internal input fixed at 0 | | | |
| | GPIO selected | | | | | | | | | |
| J | JTAG selected | Hi-Z | Pull-up / Input enabled | Pull-up / Input enabled | Maintain previous state | Maintain previous state | Maintain previous state | Maintain previous state | Maintain previous state | Maintain previous state |
| | GPIO selected | Setting disabled | Setting disabled | Setting disabled | | | Hi-Z / Internal input fixed at 0 | GPIO selected Internal input fixed at 0 | Hi-Z / Internal input fixed at 0 | GPIO selected |
| K | Resource selected | Hi-Z | Hi-Z / Input enabled | Hi-Z / Input enabled | Maintain previous state | Maintain previous state | Hi-Z / Internal input fixed at 0 | GPIO selected Internal input fixed at 0 | Hi-Z / Internal input fixed at 0 | GPIO selected |
| | GPIO selected | | | | | | | | | |
| L | External interrupt enabled selected | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Maintain previous state | GPIO selected Internal input fixed at 0 | Hi-Z / Internal input fixed at 0 | GPIO selected |
| | Resource other than above selected | Hi-Z | Hi-Z / Input enabled | Hi-Z / Input enabled | | | Hi-Z / Internal input fixed at 0 | | | |
| | GPIO selected | | | | | | | | | |

| Pin status type | Function group | Power-on reset or low-voltage detection state | INITX input state | Device internal reset state | Run mode or Sleep mode state | Timer mode, RTC mode, or Stop mode state | | Deep standby RTC mode or Deep standby Stop mode state | | Return from Deep standby mode state |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Power supply unstable | Power supply stable | | Power supply stable | Power supply stable | | Power supply stable | | Power supply stable |
| | | - | INITX = 0 | INITX = 1 | INITX = 1 | INITX = 1 | | INITX = 1 | | INITX = 1 |
| | | - | - | - | - | SPL = 0 | SPL = 1 | SPL = 0 | SPL = 1 | - |
| M | Analog input selected | Hi-Z | Hi-Z / Internal input fixed at 0 / Analog input enabled | Hi-Z / Internal input fixed at 0 / Analog input enabled | Hi-Z / Internal input fixed at 0 / Analog input enabled | Hi-Z / Internal input fixed at 0 / Analog input enabled | Hi-Z / Internal input fixed at 0 / Analog input enabled | Hi-Z / Internal input fixed at 0 / Analog input enabled | Hi-Z / Internal input fixed at 0 / Analog input enabled | Hi-Z / Internal input fixed at 0 / Analog input enabled |
| | Resource other than above selected | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Hi-Z / Internal input fixed at 0 | GPIO selected Internal input fixed at 0 | Hi-Z / Internal input fixed at 0 | GPIO selected |
| | GPIO selected | | | | | | | | | |
| N | Analog input selected | Hi-Z | Hi-Z / Internal input fixed at 0 / Analog input enabled | Hi-Z / Internal input fixed at 0 / Analog input enabled | Hi-Z / Internal input fixed at 0 / Analog input enabled | Hi-Z / Internal input fixed at 0 / Analog input enabled | Hi-Z / Internal input fixed at 0 / Analog input enabled | Hi-Z / Internal input fixed at 0 / Analog input enabled | Hi-Z / Internal input fixed at 0 / Analog input enabled | Hi-Z / Internal input fixed at 0 / Analog input enabled |
| | External interrupt enabled selected | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Maintain previous state | GPIO selected Internal input fixed at 0 | Hi-Z / Internal input fixed at 0 | GPIO selected |
| | Resource other than above selected | | | | | | Hi-Z / Internal input fixed at 0 | | | |
| | GPIO selected | | | | | | | | | |
| O | Trace selected | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Trace output | GPIO selected Internal input fixed at 0 | Hi-Z / Internal input fixed at 0 | GPIO selected |
| | Resource other than above selected | Hi-Z | Hi-Z / Input enabled | Hi-Z / Input enabled | | | Hi-Z / Internal input fixed at 0 | | | |
| | GPIO selected | | | | | | | | | |

| Pin status type | Function group | Power-on reset or low-voltage detection state | INITX input state | Device internal reset state | Run mode or Sleep mode state | Timer mode, RTC mode, or Stop mode state | | Deep standby RTC mode or Deep standby Stop mode state | | Return from Deep standby mode state |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Power supply unstable | Power supply stable | | Power supply stable | Power supply stable | | Power supply stable | | Power supply stable |
| | | - | INITX = 0 | INITX = 1 | INITX = 1 | INITX = 1 | | INITX = 1 | | INITX = 1 |
| | | - | - | - | - | SPL = 0 | SPL = 1 | SPL = 0 | SPL = 1 | - |
| P | Analog input selected | Hi-Z | Hi-Z / Internal input fixed at 0 / Analog input enabled | Hi-Z / Internal input fixed at 0 / Analog input enabled | Hi-Z / Internal input fixed at 0 / Analog input enabled | Hi-Z / Internal input fixed at 0 / Analog input enabled | Hi-Z / Internal input fixed at 0 / Analog input enabled | Hi-Z / Internal input fixed at 0 / Analog input enabled | Hi-Z / Internal input fixed at 0 / Analog input enabled | Hi-Z / Internal input fixed at 0 / Analog input enabled |
| | Trace selected | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Trace output | GPIO selected Internal input fixed at 0 | Hi-Z / Internal input fixed at 0 | GPIO selected |
| | Resource other than above selected | | | | | | Hi-Z / Internal input fixed at 0 | | | |
| | GPIO selected | | | | | | | | | |
| Q | Analog input selected | Hi-Z | Hi-Z / Internal input fixed at 0 / Analog input enabled | Hi-Z / Internal input fixed at 0 / Analog input enabled | Hi-Z / Internal input fixed at 0 / Analog input enabled | Hi-Z / Internal input fixed at 0 / Analog input enabled | Hi-Z / Internal input fixed at 0 / Analog input enabled | Hi-Z / Internal input fixed at 0 / Analog input enabled | Hi-Z / Internal input fixed at 0 / Analog input enabled | Hi-Z / Internal input fixed at 0 / Analog input enabled |
| | Trace selected | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Trace output | GPIO selected Internal input fixed at 0 | Hi-Z / Internal input fixed at 0 | GPIO selected |
| | External interrupt enabled selected | | | | | | Maintain previous state | | | |
| | Resource other than above selected | | | | | | Hi-Z / Internal input fixed at 0 | | | |
| | GPIO selected | | | | | | | | | |

| Pin status type | Function group | Power-on reset or low-voltage detection state | INITX input state | Device internal reset state | Run mode or Sleep mode state | Timer mode, RTC mode, or Stop mode state | | Deep standby RTC mode or Deep standby Stop mode state | | Return from Deep standby mode state |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Power supply unstable | Power supply stable | | Power supply stable | Power supply stable | | Power supply stable | | Power supply stable |
| | | - | INITX = 0 | INITX = 1 | INITX = 1 | INITX = 1 | | INITX = 1 | | INITX = 1 |
| | | - | - | - | - | SPL = 0 | SPL = 1 | SPL = 0 | SPL = 1 | - |
| R | Analog input selected | Hi-Z | Hi-Z / Internal input fixed at 0 / Analog input enabled | Hi-Z / Internal input fixed at 0 / Analog input enabled | Hi-Z / Internal input fixed at 0 / Analog input enabled | Hi-Z / Internal input fixed at 0 / Analog input enabled | Hi-Z / Internal input fixed at 0 / Analog input enabled | Hi-Z / Internal input fixed at 0 / Analog input enabled | Hi-Z / Internal input fixed at 0 / Analog input enabled | Hi-Z / Internal input fixed at 0 / Analog input enabled |
| | WKUP enabled | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Maintain previous state | WKUP input enabled | Hi-Z / WKUP input enabled | GPIO selected |
| | External interrupt enabled selected | | | | | | | GPIO selected Internal input fixed at 0 | Hi-Z / Internal input fixed at 0 | |
| | Resource other than above selected | | | | | | Hi-Z / Internal input fixed at 0 | | | |
| | GPIO selected | | | | | | | | | |
| S | CEC enabled | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Maintain previous state | Maintain previous state | Maintain previous state | Maintain previous state |
| | Resource other than above selected | Hi-Z | Hi-Z / Input enabled | Hi-Z / Input enabled | Maintain previous state | Maintain previous state | Hi-Z / Internal input fixed at 0 | GPIO selected Internal input fixed at 0 | Hi-Z / Internal input fixed at 0 | GPIO selected |
| | GPIO selected | | | | | | | | | |
| T | CEC enabled | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Maintain previous state | Maintain previous state | Maintain previous state | Maintain previous state |
| | WKUP enabled | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Maintain previous state | WKUP input enabled | Hi-Z / WKUP input enabled | GPIO selected |
| | External interrupt enabled selected | | | | | | | GPIO selected Internal input fixed at 0 | Hi-Z / Internal input fixed at 0 | |
| | Resource other than above selected | Hi-Z | Hi-Z / Input enabled | Hi-Z / Input enabled | | | Hi-Z / Internal input fixed at 0 | | | |
| | GPIO selected | | | | | | | | | |

*1: Oscillation is stopped at Sub Timer mode, Low-speed CR Timer mode, RTC mode, Stop mode, Deep Standby RTC mode, and Deep Standby Stop mode.

*2: Oscillation is stopped at Stop mode and Deep Standby Stop mode.

# 12. Electrical Characteristics

## 12.1 Absolute Maximum Ratings

| Parameter | Symbol | Rating | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Power supply voltage *1, *2 | $V_{CC}$ | $V_{SS}$ - 0.5 | $V_{SS}$ + 4.6 | V | |
| Analog power supply voltage *1, *3 | $AV_{CC}$ | $V_{SS}$ - 0.5 | $V_{SS}$ + 4.6 | V | |
| Analog reference voltage *1, *3 | AVRH | $V_{SS}$ - 0.5 | $V_{SS}$ + 4.6 | V | |
| Input voltage *1 | $V_I$ | $V_{SS}$ - 0.5 | $V_{CC}$ + 0.5 (≤ 4.6 V) | V | |
| | | $V_{SS}$ - 0.5 | $V_{SS}$ + 6.5 | V | 5 V tolerant |
| Analog pin input voltage *1 | $V_{IA}$ | $V_{SS}$ - 0.5 | $AV_{CC}$ + 0.5 (≤ 4.6 V) | V | |
| Output voltage *1 | $V_O$ | $V_{SS}$ - 0.5 | $V_{CC}$ + 0.5 (≤ 4.6 V) | V | |
| L level maximum output current *4 | $I_{OL}$ | - | 10 | mA | |
| | | | 39 | mA | P80/P81 pins |
| L level average output current *5 | $I_{OLAV}$ | - | 4 | mA | |
| | | | 10.5 | mA | P80/P81 pins |
| L level total maximum output current | $\sum I_{OL}$ | - | 100 | mA | |
| L level total average output current *6 | $\sum I_{OLAV}$ | - | 50 | mA | |
| H level maximum output current *4 | $I_{OH}$ | - | - 10 | mA | |
| | | | 39 | mA | P80/P81 pins |
| H level average output current *5 | $I_{OHAV}$ | - | - 4 | mA | |
| | | | 12 | mA | P80/P81 pins |
| H level total maximum output current | $\sum I_{OH}$ | - | - 100 | mA | |
| H level total average output current *6 | $\sum I_{OHAV}$ | - | - 50 | mA | |
| Power consumption | $P_D$ | - | 300 | mW | |
| Storage temperature | $T_{STG}$ | - 55 | + 150 | °C | |

*1: These parameters are based on the condition that $V_{SS} = AV_{SS} = 0$ V.

*2: $V_{CC}$ must not drop below $V_{SS}$ - 0.5 V.

*3: Ensure that the voltage does not to exceed $V_{CC}$ + 0.5 V, for example, when the power is turned on.

*4: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*5: The average output current is defined as the average current value flowing through any one of the corresponding pins for a 100 ms period.

*6: The total average output current is defined as the average current value flowing through all of corresponding pins for a 100 ms.

***WARNING:***

- *Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings.*
  *Do not exceed any of these ratings.*

## 12.2 Recommended Operating Conditions

($V_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| Power supply voltage | $V_{CC}$ | - | 1.65 *2 | 3.6 | V | |
| Analog power supply voltage | $AV_{CC}$ | - | 1.65 | 3.6 | V | $AV_{CC}$ = $V_{CC}$ |
| Analog reference voltage | AVRH | - | 2.7 | $AV_{CC}$ | V | $AV_{CC}$ ≥ 2.7 V |
| | | | $AV_{CC}$ | $AV_{CC}$ | V | $AV_{CC}$< 2.7 V |
| | AVRL | - | $AV_{SS}$ | $AV_{SS}$ | V | |
| Smoothing capacitor | $C_S$ | -- | 1 | 10 | µF | For Regulator *1 |
| Operating temperature | $T_A$ | - | - 40 | + 85 | °C | |

*1: See "C Pin" in "7. Handling Devices" for the connection of the smoothing capacitor.

*2: In between less than the minimum power supply voltage and low voltage reset/interrupt detection voltage or more, instruction execution and low voltage detection function by built-in High-speed CR (including Main PLL is used) or built-in Low-speed CR is possible to operate only.

***WARNING:***

- *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.*
  *Any use of semiconductor devices will be under their recommended operating condition.*
  *Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.*
  *No warranty is made with respect to any use, operating conditions or combinations not represented on this datasheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.*

## 12.3 DC Characteristics

### *12.3.1 Current Rating*

($V_{CC}$ = $AV_{CC}$ = 1.65 V to 3.6 V, $V_{SS}$ = $AV_{SS}$ = 0 V, $T_A$ = - 40°C to + 85°C)

| Parameter | Symbol | Pin name | Conditions | | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | | Typ *3 | Max *4 | | |
| Power supply current | $I_{CC}$ | VCC | PLL Rrun mode | CPU: 40 MHz, Peripheral: 40 MHz | 15.5 | 21 | mA | *1, *5 |
| | | | | CPU: 40 MHz, Peripheral: the clock stops NOP operation | 8.7 | 12 | mA | *1, *5 |
| | | | High-speed CR Rrun mode | CPU/ Peripheral: 4 MHz *2 | 1.8 | 2.9 | mA | *1 |
| | | | Sub Rrun mode | CPU/ Peripheral: 32 kHz | 110 | 680 | µA | *1, *6 |
| | | | Low-speed CR Run mode | CPU/ Peripheral: 100 kHz | 125 | 700 | µA | *1 |
| | $I_{CCS}$ | | PLL Sleep mode | Peripheral: 40 MHz | 9 | 12.5 | mA | *1, *5 |
| | | | High-speed CR Sleep mode | Peripheral: 4 MHz *2 | 0.8 | 1.6 | mA | *1 |
| | | | Sub Sleep mode | Peripheral: 32 kHz | 96 | 670 | µA | *1, *6 |
| | | | Low-speed CR Sleep mode | Peripheral: 100 kHz | 110 | 680 | µA | *1 |

*1: When all ports are fixed.

*2: When setting it to 4 MHz by trimming.

*3: $T_A$=+25°C, $V_{CC}$=3.6 V

*4: $T_A$=+85°C, $V_{CC}$=3.6 V

*5: When using the crystal oscillator of 4 MHz (Including the current consumption of the oscillation circuit)

*6: When using the crystal oscillator of 32 kHz (Including the current consumption of the oscillation circuit)

| Parameter | Symbol | Pin name | Conditions | | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | | Typ *2 | Max *2 | | |
| Power supply current | $I_{CCT}$ | VCC | Main Timer mode | $T_A$ = + 25°C, When LVD is off | 2.1 | 2.5 | mA | *1, *3 |
| | | | | $T_A$ = + 85°C, When LVD is off | - | 3.4 | mA | *1, *3 |
| | | | Sub Timer mode | $T_A$ = + 25°C, When LVD is off | 12 | 35 | µA | *1, *4 |
| | | | | $T_A$ = + 85°C, When LVD is off | - | 330 | µA | *1, *4 |
| | $I_{CCR}$ | | RTC mode | $T_A$ = + 25°C, When LVD is off | 9.8 | 29 | µA | *1, *4 |
| | | | | $T_A$ = + 85°C, When LVD is off | - | 280 | µA | *1, *4 |
| | $I_{CCH}$ | | Stop mode | $T_A$ = + 25°C, When LVD is off | 9 | 28 | µA | *1 |
| | | | | $T_A$ = + 85°C, When LVD is off | - | 270 | µA | *1 |
| | $I_{CCHD}$ | | Deep Standby Stop mode | $T_A$ = + 25°C, When LVD is off, When RAM is off | 1.25 | 7 | µA | *1, *4, *5 |
| | | | | $T_A$ = + 25°C, When LVD is off, When RAM is on | 5.3 | 18 | µA | *1, *4, *5 |
| | | | | $T_A$ = + 85°C, When LVD is off, When RAM is off | - | 70 | µA | *1, *4, *5 |
| | | | | $T_A$ = + 85°C, When LVD is off, When RAM is on | | 100 | µA | *1, *4, *5 |
| | $I_{CCRD}$ | | Deep Standby RTC mode | $T_A$ = + 25°C, When LVD is off, When RAM is off | 1.9 | 9 | µA | *1, *5 |
| | | | | $T_A$ = + 25°C, When LVD is off, When RAM is on | 5.9 | 20 | µA | *1, *5 |
| | | | | $T_A$ = + 85°C, When LVD is off, When RAM is off | - | 75 | µA | *1, *5 |
| | | | | $T_A$ = + 85°C, When LVD is off, When RAM is on | | 105 | µA | *1, *5 |

*1: When all ports are fixed.

*2: $V_{CC}$=3.6 V

*3: When using the crystal oscillator of 4 MHz (Including the current consumption of the oscillation circuit)

*4: When using the crystal oscillator of 32 kHz (Including the current consumption of the oscillation circuit)

*5: RAM on/off setting is on-chip SRAM only.

### Low-Voltage Detection Current

($V_{CC}$ = 1.65 V to 3.6 V, $V_{DDI}$ = 1.1 V to 1.3 V, $V_{SS}$ = 0V, $T_A$ = - 40°C to + 85°C)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Typ | Max | | |
| Low-voltage detection circuit (LVD) power supply current | $I_{CCLVD}$ | VCC | At operation for reset $V_{CC}$ = 3.6 V | 0.13 | 0.3 | µA | At not detect |
| | | | At operation for interrupt $V_{CC}$ = 3.6 V | 0.13 | 0.3 | µA | At not detect |

### Flash Memory Current

($V_{CC}$ = 1.65 V to 3.6 V, $V_{DDI}$ = 1.1 V to 1.3 V, $V_{SS}$ = 0 V, $T_A$ = - 40°C to + 85°C)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Typ | Max | | |
| Flash memory write/erase current | $I_{CCFLASH}$ | VCC | At Write/Erase | 9.5 | 11.2 | mA | *1 |

*1: The current at which to write or erase Flash memory, $I_{CCFLASH}$ is added to $I_{CC}$.

### A/D Converter Current

($V_{CC}$ = $V_{CC28}$ = $AV_{CC}$ = 1.65 V to 3.6 V, $V_{DDI}$ = 1.1 V to 1.3 V, $V_{SS}$ = $AV_{SS}$ = 0 V, $T_A$ = - 40°C to +85°C)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Typ | Max | | |
| Power supply current | $I_{CCAD}$ | AVCC | At 1unit operation | 0.27 | 0.42 | mA | |
| | | | At stop | 0.03 | 10 | µA | |
| Reference power supply current | $I_{CCAVRH}$ | AVRH | At 1unit operation AVRH=3.6 V | 0.72 | 1.29 | mA | |
| | | | At stop | 0.02 | 2.6 | µA | |

### 12.3.2 Pin Characteristics

($V_{CC}$ = $AV_{CC}$ = 1.65 V to 3.6 V, $V_{SS}$ = $AV_{SS}$ = 0 V, $T_A$ = - 40°C to + 85°C)

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| H level input voltage (hysteresis input) | $V_{IHS}$ | CMOS hysteresis input pin, MD0, MD1 | $V_{CC} \geq 2.7$ V | $V_{CC} \times 0.8$ | - | $V_{CC} + 0.3$ | V | |
| | | | $V_{CC} < 2.7$ V | $V_{CC} \times 0.7$ | | | | |
| | | 5V tolerant input pin | $V_{CC} \geq 2.7$ V | $V_{CC} \times 0.8$ | - | $V_{SS} + 5.5$ | V | |
| | | | $V_{CC} < 2.7$ V | $V_{CC} \times 0.7$ | | | | |
| L level input voltage (hysteresis input) | $V_{ILS}$ | CMOS hysteresis input pin, MD0, MD1 | $V_{CC} \geq 2.7$ V | $V_{SS} - 0.3$ | - | $V_{CC} \times 0.2$ | V | |
| | | | $V_{CC} < 2.7$ V | | | $V_{CC} \times 0.3$ | | |
| | | 5V tolerant input pin | $V_{CC} \geq 2.7$ V | $V_{SS} - 0.3$ | - | $V_{CC} \times 0.2$ | V | |
| | | | $V_{CC} < 2.7$ V | | | $V_{CC} \times 0.3$ | | |
| H level output voltage | $V_{OH}$ | 4 mA type | $V_{CC} \geq 2.7$ V, $I_{OH}$ = - 4 mA | $V_{CC} - 0.5$ | - | $V_{CC}$ | V | |
| | | | $V_{CC} < 2.7$ V, $I_{OH}$ = - 2 mA | $V_{CC} - 0.45$ | | | | |
| | | P80/P81 | $V_{CC} \geq 2.7$ V, $I_{OH}$ = - 12 mA | $V_{CC} - 0.4$ | - | $V_{CC}$ | V | |
| | | | $V_{CC} < 2.7$ V, $I_{OH}$ = - 6.5 mA | | | | | |
| L level output voltage | $V_{OL}$ | 4 mA type | $V_{CC} \geq 2.7$ V, $I_{OL}$ = 4 mA | $V_{SS}$ | - | 0.4 | V | |
| | | | $V_{CC} < 2.7$ V, $I_{OL}$ = 2 mA | | | | | |
| | | P80/P81 | $V_{CC} \geq 2.7$ V, $I_{OL}$ = 10.5 mA | $V_{SS}$ | - | 0.4 | V | |
| | | | $V_{CC} < 2.7$ V, $I_{OL}$ = 5 mA | | | | | |
| Input leak current | $I_{IL}$ | - | - | - 5 | - | + 5 | µA | |
| | | CEC0, CEC1 | $V_{CC}$ = $AV_{CC}$ = AVRH = $V_{SS}$ = $AV_{SS}$ = 0.0 V | - | - | +1.8 | µA | |
| Pull-up resistor value | $R_{PU}$ | Pull-up pin | $V_{CC} \geq 2.7$ V | 21 | 33 | 66 | kΩ | |
| | | | $V_{CC} < 2.7$ V | - | - | 134 | | |
| Input capacitance | $C_{IN}$ | Other than VCC, VSS, AVCC, AVSS, AVRH | - | - | 5 | 15 | pF | |

## 12.4 AC Characteristics

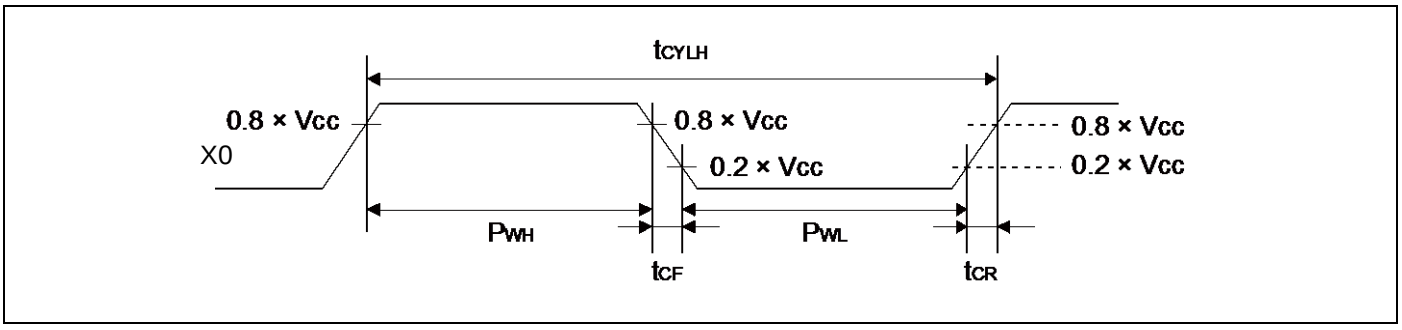
### *12.4.1 Main Clock Input Characteristics*

($V_{CC}$ = 1.65 V to 3.6 V, $V_{SS}$ = 0 V, $T_A$ = - 40°C to + 85°C)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Input frequency | $f_{CH}$ | X0, X1 | $V_{CC} \geq 2.7$ V | 4 | 48 | MHz | When crystal oscillator is connected |
| | | | $V_{CC} < 2.7$ V | 4 | 20 | | |
| | | | - | 4 | 48 | MHz | When using external clock |
| Input clock cycle | $t_{CYLH}$ | | - | 20.83 | 250 | ns | When using external clock |
| Input clock pulse width | - | | $P_{WH}/t_{CYLH}$, $P_{WL}/t_{CYLH}$ | 45 | 55 | % | When using external clock |
| Input clock rising time and falling time | $t_{CF}$, $t_{CR}$ | | - | - | 5 | ns | When using external clock |
| Internal operating clock *1 frequency | $f_{CM}$ | - | - | - | 40 | MHz | Master clock |
| | $f_{CC}$ | - | - | - | 40 | MHz | Base clock (HCLK/FCLK) |
| | $f_{CP0}$ | - | - | - | 40 | MHz | APB0 bus clock *2 |
| | $f_{CP1}$ | - | - | - | 40 | MHz | APB1 bus clock *2 |
| | $f_{CP2}$ | - | - | - | 40 | MHz | APB2 bus clock *2 |
| Internal operating clock[1] cycle time | $t_{CYCC}$ | - | - | 25 | - | ns | Base clock (HCLK/FCLK) |
| | $t_{CYCP0}$ | - | - | 25 | - | ns | APB0 bus clock *2 |
| | $t_{CYCP1}$ | - | - | 25 | - | ns | APB1 bus clock *2 |
| | $t_{CYCP2}$ | - | - | 25 | - | ns | APB2 bus clock *2 |

*1: For more information about each internal operating clock, see Chapter 2-1: Clock in FM3 Family Peripheral Manual.

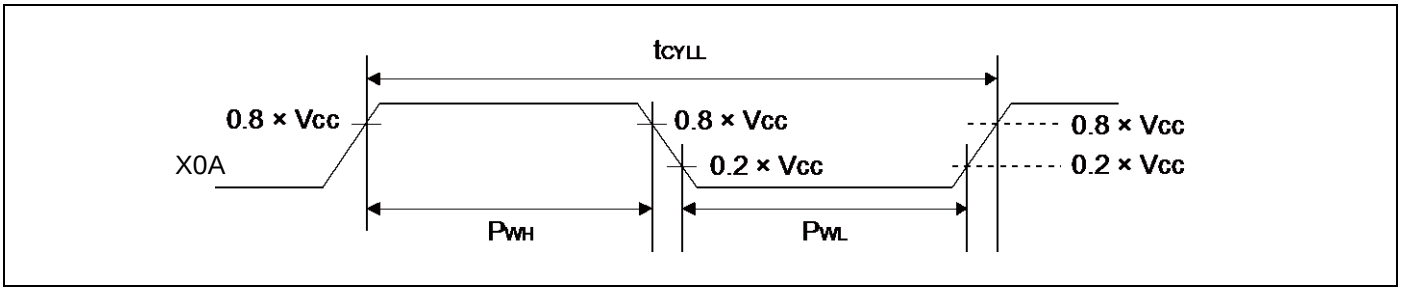
*2: For about each APB bus which each peripheral is connected to, see 8. Block Diagram in this datasheet.



### 12.4.2 Sub Clock Input Characteristics

($V_{CC}$ = 1.65 V to 3.6 V, $V_{SS}$ = 0 V, $T_A$ = - 40°C to + 85°C)

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Input frequency | $f_{CL}$ | X0A, X1A | - | - | 32.768 | - | kHz | When crystal oscillator is connected |
| | | | - | 32 | - | 100 | kHz | When using external clock |
| Input clock cycle | $t_{CYLL}$ | | - | 10 | - | 31.25 | µs | When using external clock |
| Input clock pulse width | - | | PWH/tCYLL, PWL/tCYLL | 45 | - | 55 | % | When using external clock |




### 12.4.3 Built-in CR Oscillation Characteristics

**Built-in high-speed CR**

($V_{CC}$ = 1.65 V to 3.6 V, $V_{SS}$ = 0 V, $T_A$ = - 40°C to + 85°C)

| Parameter | Symbol | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Clock frequency | $f_{CRH}$ | $T_A$ = + 25°C<br>$V_{CC}$ ≥ 2.7 V | 3.96 | 4 | 4.04 | MHz | When trimming *1 |
| | | $T_A$ = + 25°C<br>$V_{CC}$ < 2.7 V | 3.9 | 4 | 4.1 | | |
| | | $T_A$ =<br>- 40°C to + 85°C | 3.84 | 4 | 4.16 | | |
| | | $T_A$ =<br>- 40°C to + 85°C | 2.8 | - | 5.2 | | When not trimming |
| Frequency stabilization time | $t_{CRWT}$ | - | - | - | 30 | µs | *2 |

*1: In the case of using the values in CR trimming area of Flash memory at shipment for frequency/temperature trimming.

*2: This is the time to stabilize the frequency of High-speed CR clock after setting trimming value.
This period is able to use High-speed CR clock as source clock.

**Built-in low-speed CR**

($V_{CC}$ = 1.65 V to 3.6 V, $V_{SS}$ = 0 V, $T_A$ = - 40°C to + 85°C)

| Parameter | Symbol | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Clock frequency | $f_{CRL}$ | - | 50 | 100 | 150 | kHz | |

### 12.4.4 Operating Conditions of Main PLL (In the case of using main clock for input of PLL)

($V_{CC}$ = 1.65 V to 3.6 V, $V_{SS}$ = 0 V, $T_A$ = - 40°C to + 85°C)

| Parameter | Symbol | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| PLL oscillation stabilization wait time *1 (LOCK UP time) | $t_{LOCK}$ | 100 | - | - | µs | |
| PLL input clock frequency | $f_{PLLI}$ | 4 | - | 16 | MHz | |
| PLL multiple rate | - | 5 | - | 37 | multiple | |
| PLL macro oscillation clock frequency | $f_{PLLO}$ | 75 | - | 150 | MHz | |
| Main PLL clock frequency *2 | $f_{CLKPLL}$ | - | - | 40 | MHz | |

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see Chapter 2-1: Clock in FM3 Family Peripheral Manual.

### 12.4.5 Operating Conditions of Main PLL (In the case of using the built-in High-speed CR for the input clock of the Main PLL)

($V_{CC}$ = 1.65 V to 3.6 V, $V_{SS}$ = 0 V, $T_A$ = - 40°C to + 85°C)

| Parameter | Symbol | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| PLL oscillation stabilization wait time *1 (LOCK UP time) | $t_{LOCK}$ | 100 | - | - | µs | |
| PLL input clock frequency | $f_{PLLI}$ | 3.8 | 4 | 4.2 | MHz | |
| PLL multiple rate | - | 19 | - | 35 | multiple | |
| PLL macro oscillation clock frequency | $f_{PLLO}$ | 72 | - | 150 | MHz | |
| Main PLL clock frequency *2 | $f_{CLKPLL}$ | - | - | 40 | MHz | |

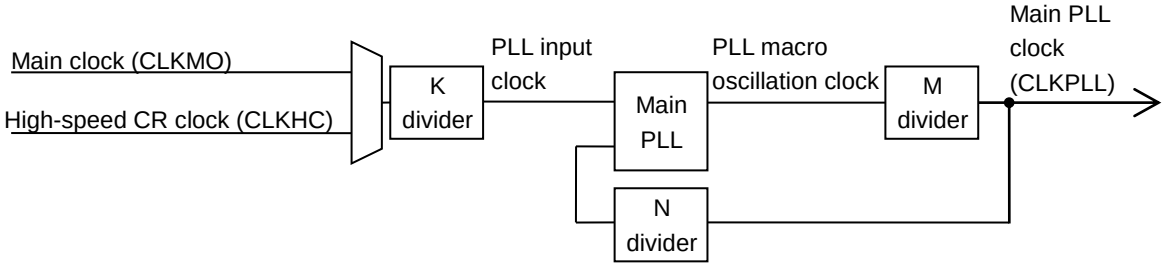
*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see Chapter 2-1: Clock in FM3 Family Peripheral Manual.

***Note:***

- *Make sure to input to the Main PLL source clock, the High-speed CR clock (CLKHC) that the frequency/temperature has been trimmed.*
  *When setting PLL multiple rate, please take the accuracy of the built-in High-speed CR clock into account and prevent the master clock from exceeding the maximum frequency.*

**Main PLL connection**



### 12.4.6 Reset Input Characteristics

($V_{CC}$ = 1.65 V to 3.6 V, $V_{SS}$ = 0 V, $T_A$ = - 40°C to + 85°C)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Reset input time | $t_{INITX}$ | INITX | - | 500 | - | ns | |

### 12.4.7 Power-on Reset Timing

($V_{SS}$ = 0V, $T_A$ = - 40°C to + 85°C)

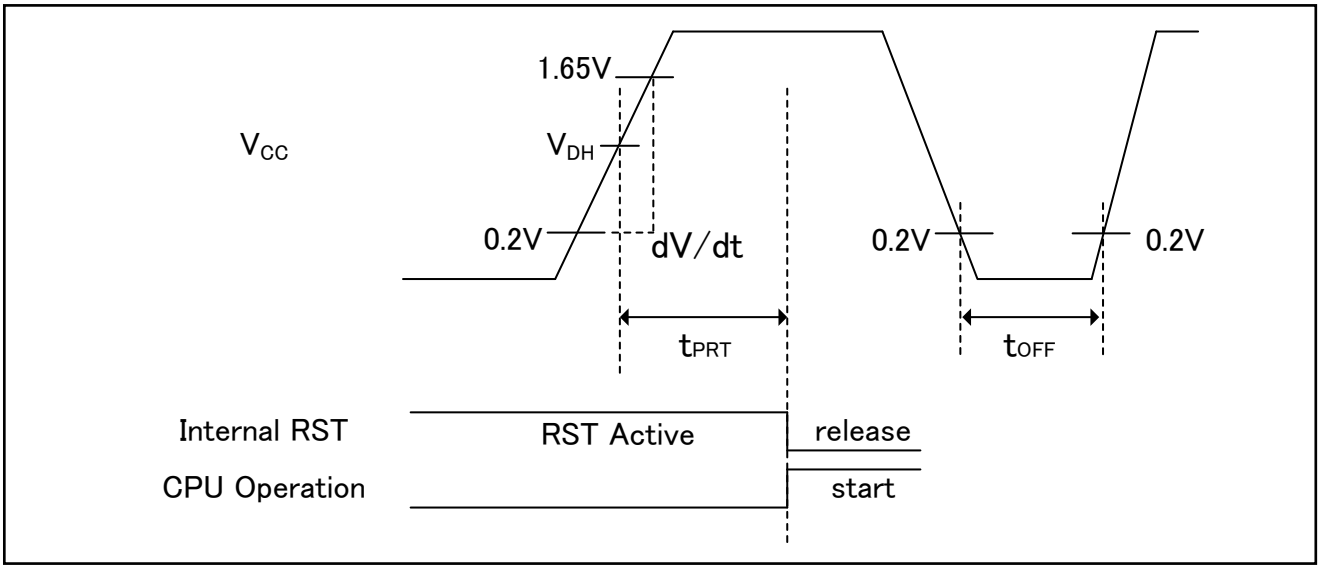
| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Power supply shut down time | $t_{OFF}$ | VCC | - | 1 | - | - | ms | *1 |
| Power ramp rate | dV/dt | | Vcc:0.2 V to 1.65 V | 0.2 | - | 1000 | mV/µs | *2 |
| Time until releasing Power-on reset | $t_{PRT}$ | | - | 1.34 | - | 16.09 | ms | |

*1: $V_{CC}$ must be held below 0.2 V for minimum period of $t_{OFF}$. Improper initialization may occur if this condition is not met.

*2: This dV/dt characteristic is applied at the power-on of cold start ($t_{OFF}$>1 ms).

***Note:***

- *If $t_{OFF}$ cannot be satisfied designs must assert external reset(INITX) at power-up and at any brownout event per "12. 4. 6.Reset Input Characteristics".*




***Glossary:***

VDH: detection voltage of Low Voltage detection reset. See "12.6 Low-Voltage Detection Characteristics"

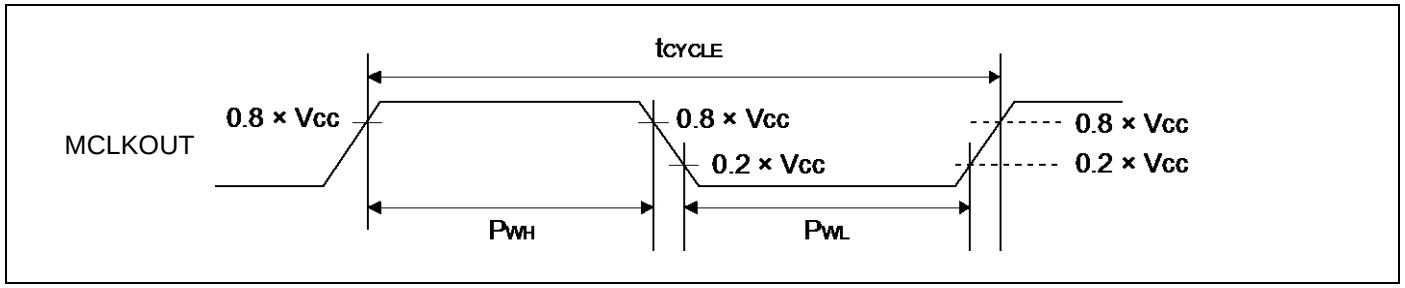
### 12.4.8 External Bus Timing

**External bus clock output characteristics**

($V_{CC}$ = 1.65 V to 3.6 V, $V_{SS}$ = 0 V, $T_A$ = - 40°C to + 85°C)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Output frequency | $t_{CYCLE}$ | MCLKOUT *1 | $V_{CC} \geq 2.7$ V | - | 40 | MHz |
| | | | $V_{CC} < 2.7$ V | - | 20 | MHz |

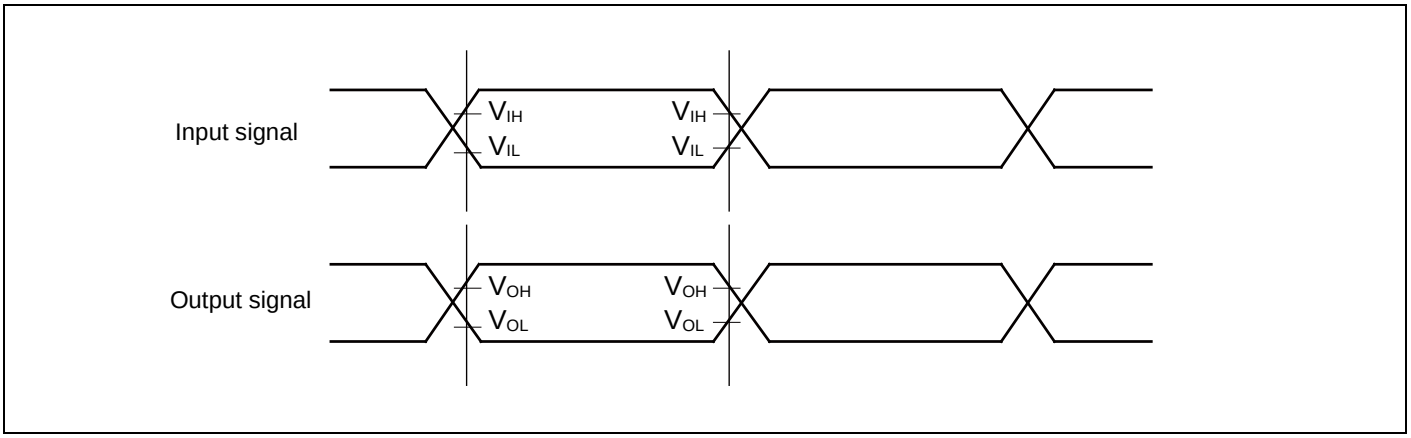
*1: The external bus clock output (MCLKOUT) is a divided clock of HCLK.
For more information about setting of clock divider, see Chapter 12: External Bus Interface in FM3 Family Peripheral Manual.
When external bus clock is not output, this characteristic does not give any effect on external bus operation.




**External bus signal input/output characteristics**

($V_{CC}$ = 1.65 V to 3.6 V, $V_{SS}$ = 0 V, $T_A$ = - 40°C to + 85°C)

| Parameter | Symbol | Conditions | Value | Unit | Remarks |
|---|---|---|---|---|---|
| Signal input characteristics | $V_{IH}$ | - | 0.8 × $V_{CC}$ | V | |
| | $V_{IL}$ | | 0.2 × $V_{CC}$ | V | |
| Signal output characteristics | $V_{OH}$ | | 0.8 × $V_{CC}$ | V | |
| | $V_{OL}$ | | 0.2 × $V_{CC}$ | V | |



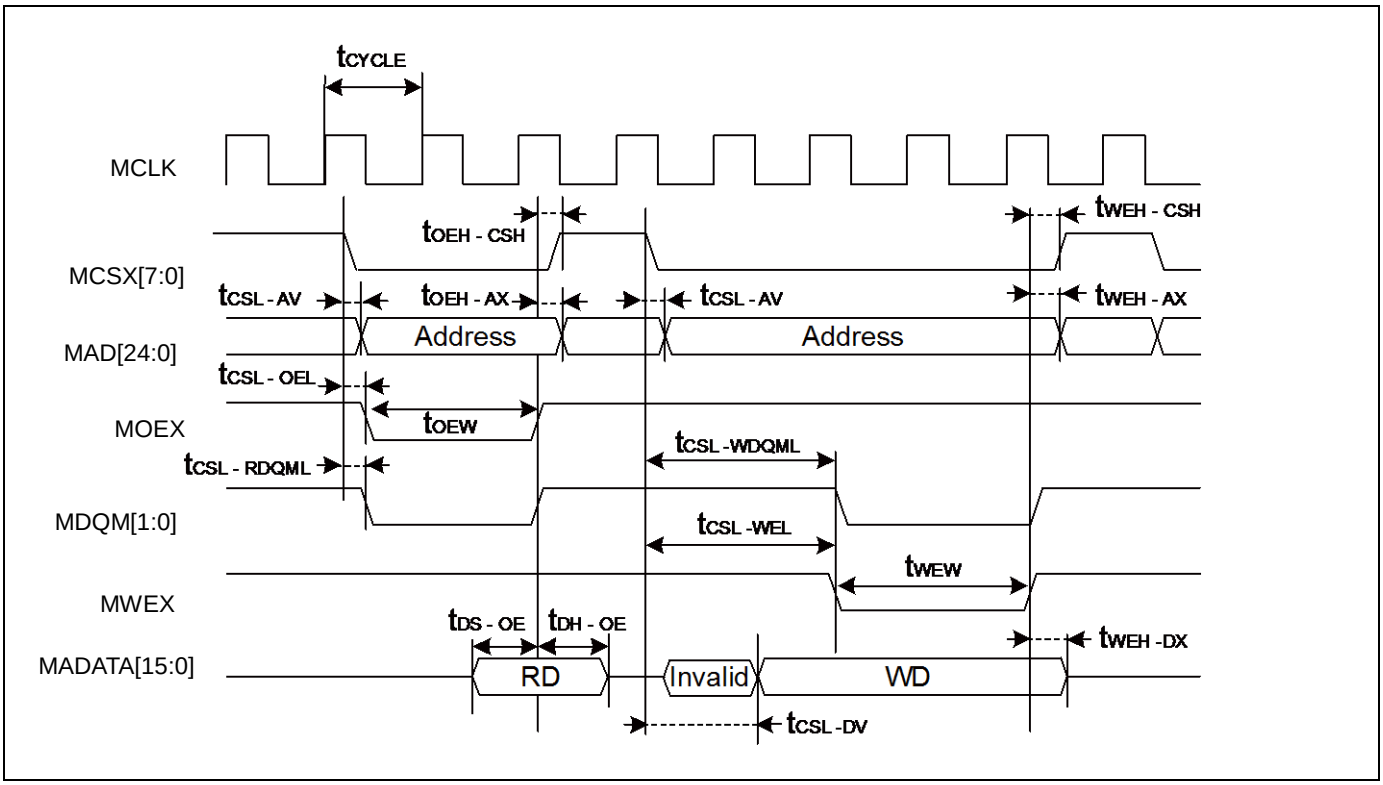
### Separate Bus Access Asynchronous SRAM Mode

($V_{CC}$ = 1.65 V to 3.6 V, $V_{SS}$ = 0 V, $T_A$ = - 40°C to + 85°C)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| MOEX<br>Min pulse width | $t_{OEW}$ | MOEX | $V_{CC} \geq 2.7$ V | MCLK×n-3 | - | ns |
| | | | $V_{CC} < 2.7$ V | | | |
| MCSX ↓ → Address output delay time | $t_{CSL-AV}$ | MCSX[7:0], MAD[24:0] | $V_{CC} \geq 2.7$ V | -9 | +9 | ns |
| | | | $V_{CC} < 2.7$ V | -12 | +12 | |
| MOEX ↑ →<br>Address hold time | $t_{OEH-AX}$ | MOEX, MAD[24:0] | $V_{CC} \geq 2.7$ V | 0 | MCLK×m+9 | ns |
| | | | $V_{CC} < 2.7$ V | | MCLK×m+12 | |
| MCSX ↓ →<br>MOEX ↓ delay time | $t_{CSL-OEL}$ | MOEX, MCSX[7:0] | $V_{CC} \geq 2.7$ V | MCLK×m-9 | MCLK×m+9 | ns |
| | | | $V_{CC} < 2.7$ V | MCLK×m-12 | MCLK×m+12 | |
| MOEX ↑ →<br>MCSX ↑ time | $t_{OEH-CSH}$ | | $V_{CC} \geq 2.7$ V | 0 | MCLK×m+9 | ns |
| | | | $V_{CC} < 2.7$ V | | MCLK×m+12 | |
| MCSX ↓ →<br>MDQM ↓ delay time | $t_{CSL-RDQML}$ | MCSX, MDQM[1:0] | $V_{CC} \geq 2.7$ V | MCLK×m-9 | MCLK×m+9 | ns |
| | | | $V_{CC} < 2.7$ V | MCLK×m-12 | MCLK×m+12 | |
| Data set up →<br>MOEX ↑ time | $t_{DS-OE}$ | MOEX, MADATA[15:0] | $V_{CC} \geq 2.7$ V | 30 | - | ns |
| | | | $V_{CC} < 2.7$ V | 38 | - | |
| MOEX ↑ →<br>Data hold time | $t_{DH-OE}$ | MOEX, MADATA[15:0] | $V_{CC} \geq 2.7$ V | 0 | - | ns |
| | | | $V_{CC} < 2.7$ V | | | |
| MWEX<br>Min pulse width | $t_{WEW}$ | MWEX | $V_{CC} \geq 2.7$ V | MCLK×n-3 | - | ns |
| | | | $V_{CC} < 2.7$ V | | | |
| MWEX ↑ → Address output delay time | $t_{WEH-AX}$ | MWEX, MAD[24:0] | $V_{CC} \geq 2.7$ V | 0 | MCLK×m+9 | ns |
| | | | $V_{CC} < 2.7$ V | | MCLK×m+12 | |
| MCSX ↓ →<br>MWEX ↓ delay time | $t_{CSL-WEL}$ | MWEX, MCSX[7:0] | $V_{CC} \geq 2.7$ V | MCLK×n-9 | MCLK×n+9 | ns |
| | | | $V_{CC} < 2.7$ V | MCLK×n-12 | MCLK×n+12 | |
| MWEX ↑ →<br>MCSX ↑ delay time | $t_{WEH-CSH}$ | | $V_{CC} \geq 2.7$ V | 0 | MCLK×m+9 | ns |
| | | | $V_{CC} < 2.7$ V | | MCLK×m+12 | |
| MCSX ↓→<br>MDQM ↓ delay time | $t_{CSL-WDQML}$ | MCSX, MDQM[1:0] | $V_{CC} \geq 2.7$ V | MCLK×n-9 | MCLK×n+9 | ns |
| | | | $V_{CC} < 2.7$ V | MCLK×n-12 | MCLK×n+12 | |
| MWEX ↓→<br>Data output time | $t_{CSL-DV}$ | MCSX, MADATA[15:0] | $V_{CC} \geq 2.7$ V | MCLK-9 | MCLK+9 | ns |
| | | | $V_{CC} < 2.7$ V | MCLK-12 | MCLK+12 | |
| MWEX ↑ →<br>Data hold time | $t_{WEH-DX}$ | MWEX, MADATA[15:0] | $V_{CC} \geq 2.7$ V | 0 | MCLK×m+9 | ns |
| | | | $V_{CC} < 2.7$ V | | MCLK×m+12 | |

***Note:***

- *When the external load capacitance $C_L$ = 30 pF (m = 0 to 15, n = 1 to 16).*


tCYCLE
MCLK
tOEH - CSH
tWEH - CSH
MCSX[7:0]
tCSL - AV
tOEH - AX
tCSL - AV
tWEH - AX
MAD[24:0]
Address
Address
tCSL - OEL
tOEW
MOEX
tCSL - RDQML
tCSL -WDQML
MDQM[1:0]
tCSL -WEL
tWEW
MWEX
tDS - OE
tDH - OE
tWEH -DX
MADATA[15:0]
RD
Invalid
WD
tCSL -DV

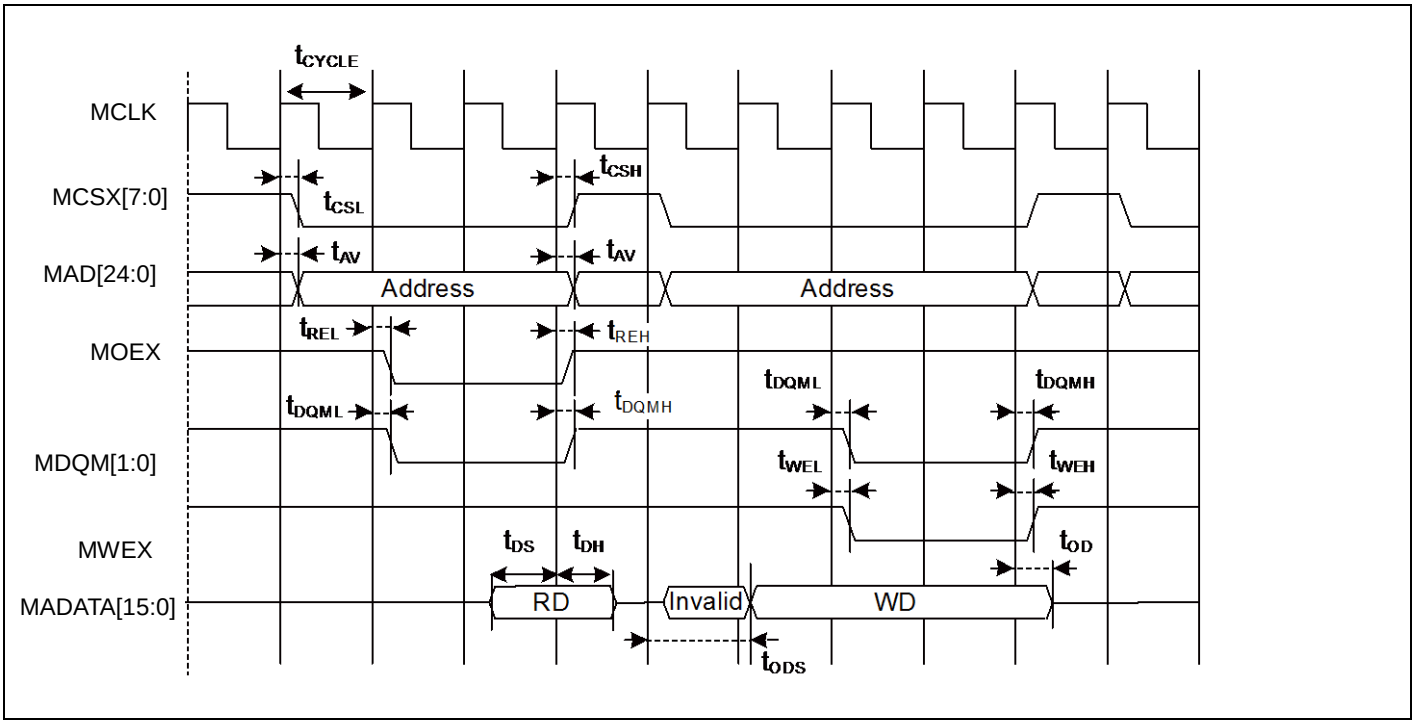
### Separate Bus Access Synchronous SRAM Mode

($V_{CC}$ = 1.65 V to 3.6 V, $V_{SS}$ = 0 V, $T_A$ = - 40°C to + 85°C)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Address delay time | $t_{AV}$ | MCLK, MAD[24:0] | $V_{CC} \geq 2.7$ V | 1 | 12 | ns |
| | | | $V_{CC} < 2.7$ V | | 13 | |
| MCSX delay time | $t_{CSL}$ | MCLK, MCSX[7:0] | $V_{CC} \geq 2.7$ V | 1 | 12 | ns |
| | | | $V_{CC} < 2.7$ V | | | |
| | $t_{CSH}$ | | $V_{CC} \geq 2.7$ V | 1 | 12 | ns |
| | | | $V_{CC} < 2.7$ V | | | |
| MOEX delay time | $t_{REL}$ | MCLK, MOEX | $V_{CC} \geq 2.7$ V | 1 | 9 | ns |
| | | | $V_{CC} < 2.7$ V | | 12 | |
| | $t_{REH}$ | | $V_{CC} \geq 2.7$ V | 1 | 9 | ns |
| | | | $V_{CC} < 2.7$ V | | 12 | |
| Data set up → MCLK ↑ time | $t_{DS}$ | MCLK, MADATA[15:0] | $V_{CC} \geq 2.7$ V | 24 | - | ns |
| | | | $V_{CC} < 2.7$ V | 37 | | |
| MCLK ↑ → Data hold time | $t_{DH}$ | MCLK, MADATA[15:0] | $V_{CC} \geq 2.7$ V | 0 | - | ns |
| | | | $V_{CC} < 2.7$ V | | | |
| MWEX delay time | $t_{WEL}$ | MCLK, MWEX | $V_{CC} \geq 2.7$ V | 1 | 9 | ns |
| | | | $V_{CC} < 2.7$ V | | 12 | |
| | $t_{WEH}$ | | $V_{CC} \geq 2.7$ V | 1 | 9 | ns |
| | | | $V_{CC} < 2.7$ V | | 12 | |
| MDQM[1:0] delay time | $t_{DQML}$ | MCLK, MDQM[1:0] | $V_{CC} \geq 2.7$ V | 1 | 9 | ns |
| | | | $V_{CC} < 2.7$ V | | 12 | |
| | $t_{DQMH}$ | | $V_{CC} \geq 2.7$ V | 1 | 9 | ns |
| | | | $V_{CC} < 2.7$ V | | 12 | |
| MCLK ↑ → Data output time | $t_{ODS}$ | MCLK, MADATA[15:0] | $V_{CC} \geq 2.7$ V | MCLK + 1 | MCLK + 18 | ns |
| | | | $V_{CC}$ <2.7 V | | MCLK + 24 | |
| MCLK ↑ → Data hold time | $t_{OD}$ | MCLK, MADATA[15:0] | $V_{CC} \geq 2.7$ V | 1 | 18 | ns |
| | | | $V_{CC}$ <2.7 V | | 24 | |

***Note:***

- *When the external load capacitance $C_L$ = 30 pF.*



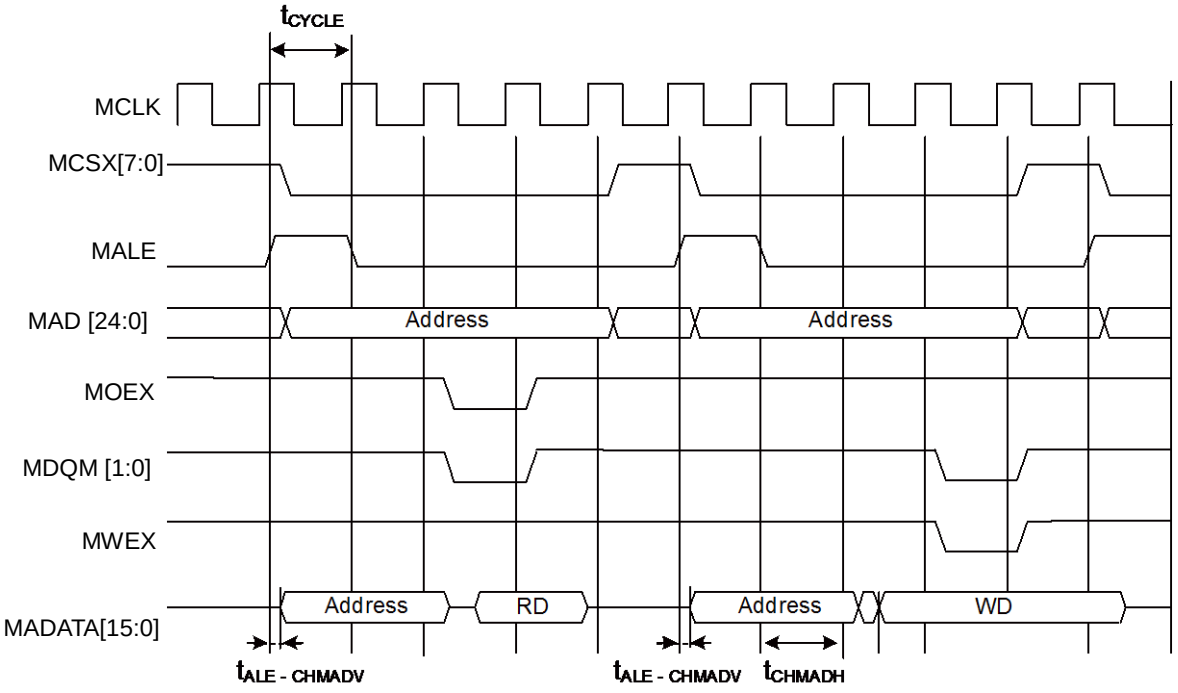
### Multiplexed Bus Access Asynchronous SRAM Mode

($V_{CC}$ = 1.65 V to 3.6 V, $V_{SS}$ = 0 V, $T_A$ = - 40°C to + 85°C)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Multiplexed address delay time | $t_{ALE-CHMADV}$ | MALE, MADATA[15:0] | $V_{CC} \geq 2.7$ V | -2 | +10 | ns |
| | | | $V_{CC} < 2.7$ V | | +20 | |
| Multiplexed address hold time | $t_{CHMADH}$ | | $V_{CC} \geq 2.7$ V | MCLK×n+0 | MCLK×n+10 | ns |
| | | | $V_{CC} < 2.7$ V | MCLK×n+0 | MCLK×n+20 | |

***Note:***

- *When the external load capacitance $C_L$ = 30 pF (m = 0 to 15, n = 1 to 16).*



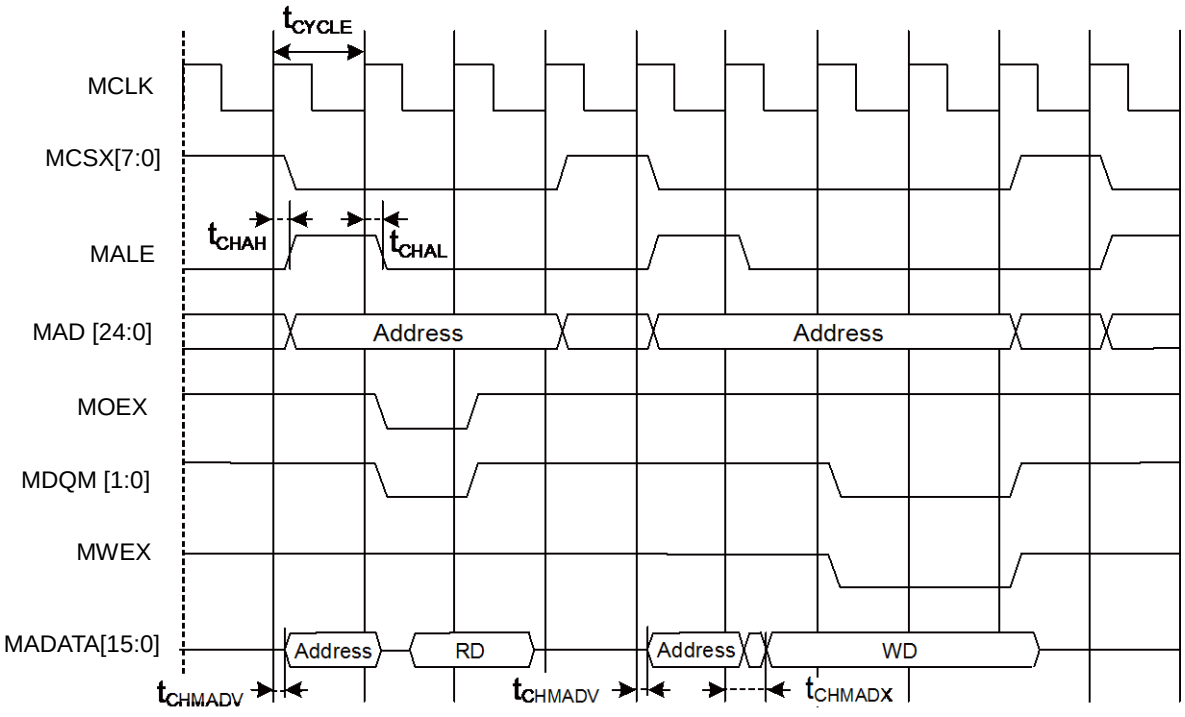
### Multiplexed Bus Access Synchronous SRAM Mode

($V_{CC}$ = 1.65 V to 3.6 V, $V_{SS}$ = 0 V, $T_A$ = - 40°C to + 85°C)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| MALE delay time | $t_{CHAL}$ | MCLK, ALE | $V_{CC} \geq 2.7$ V | 1 | 9 | ns | |
| | | | $V_{CC} < 2.7$ V | | 12 | ns | |
| | $t_{CHAH}$ | | $V_{CC} \geq 2.7$ V | 1 | 9 | ns | |
| | | | $V_{CC} < 2.7$ V | | 12 | ns | |
| MCLK ↑ → Multiplexed Address delay time | $t_{CHMADV}$ | MCLK, MADATA[15:0] | $V_{CC} \geq 2.7$ V | 1 | $t_{OD}$ | ns | |
| | | | $V_{CC} < 2.7$ V | | | | |
| MCLK ↑ → Multiplexed Data output time | $t_{CHMADX}$ | | $V_{CC} \geq 2.7$ V | 1 | $t_{OD}$ | ns | |
| | | | $V_{CC} < 2.7$ V | | | | |

***Note:***

- *When the external load capacitance $C_L$ = 30 pF.*

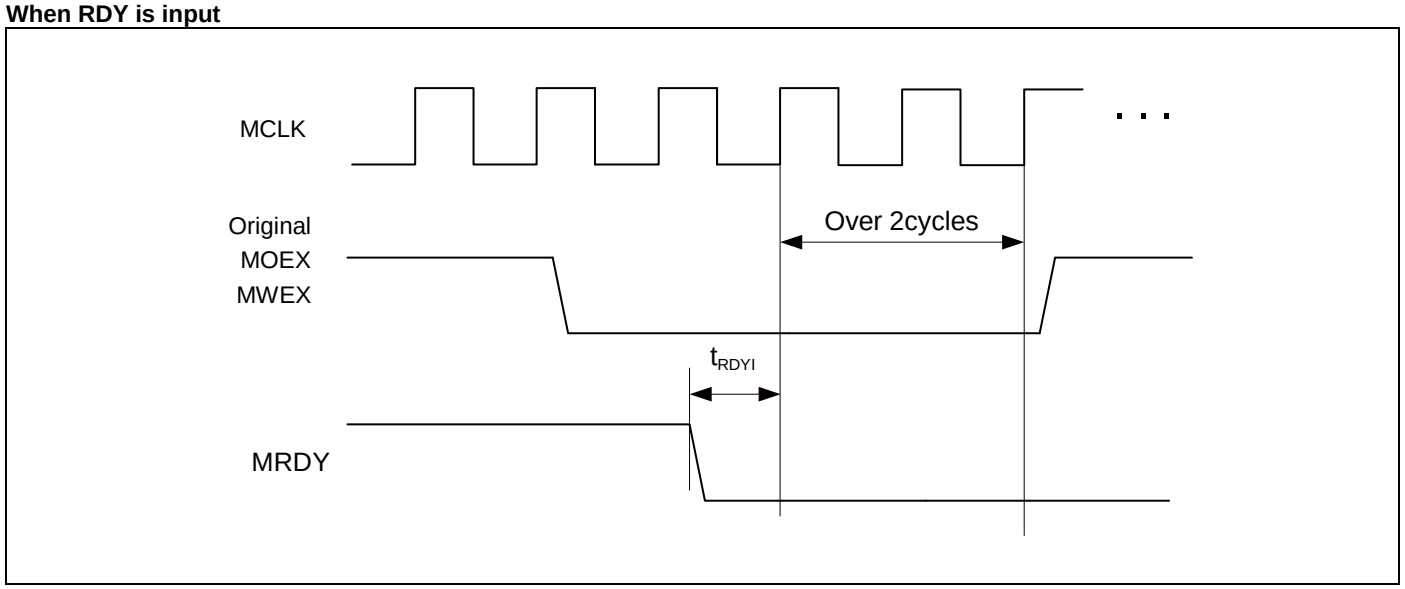


### External Ready Input Timing

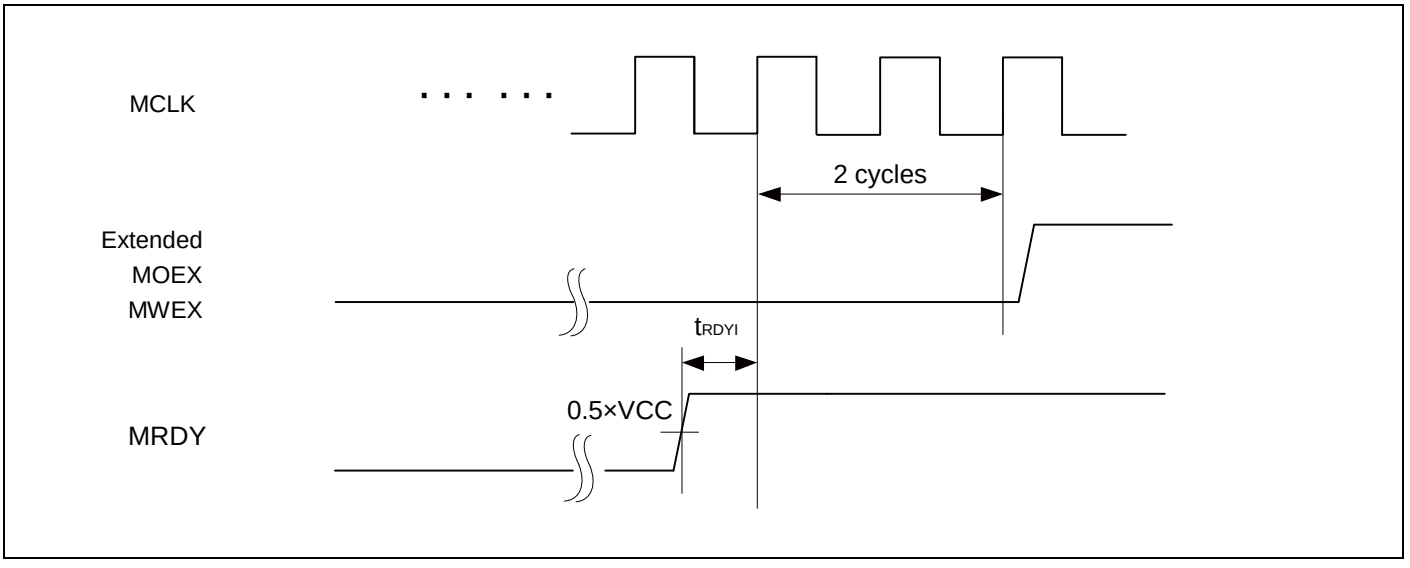
($V_{CC}$ = 1.65 V to 3.6 V, $V_{SS}$ = 0 V, $T_A$ = - 40°C to + 85°C)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| MCLK ↑ MRDY input setup time | $t_{RDYI}$ | MCLK, MRDY | $V_{CC}$ ≥ 2.7 V | 23 | - | ns | |
| | | | $V_{CC}$ < 2.7 V | 37 | | | |

**When RDY is input**




**When RDY is released**

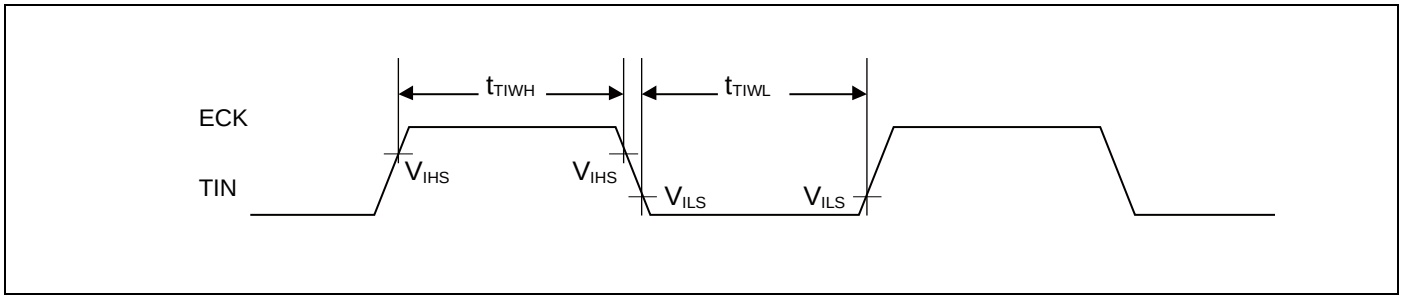


### 12.4.9 Base Timer Input Timing

**Timer input timing**

($V_{CC}$ = 1.65 V to 3.6 V, $V_{SS}$ = 0 V, $T_A$ = - 40°C to + 85°C)

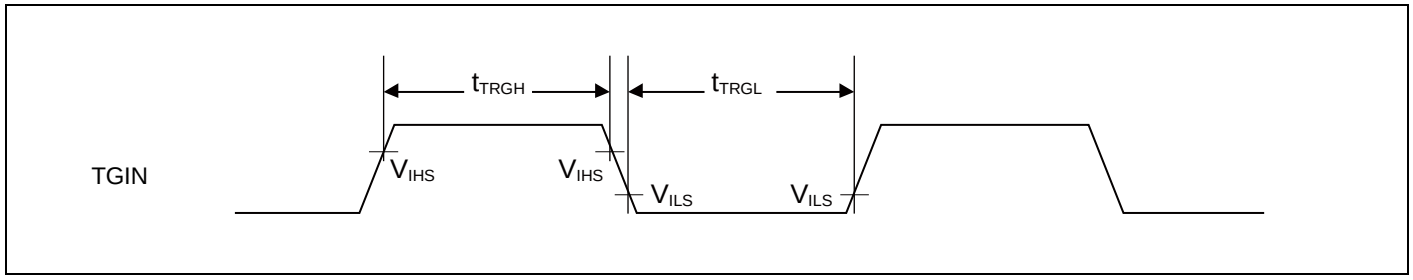
| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Input pulse width | $t_{TIWH}$, $t_{TIWL}$ | TIOAn/TIOBn (when using as ECK, TIN) | - | $2t_{CYCP}$ | - | ns | |




**Trigger input timing**

($V_{CC}$ = 1.65 V to 3.6 V, $V_{SS}$ = 0 V, $T_A$ = - 40°C to + 85°C)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Input pulse width | $t_{TRGH}$, $t_{TRGL}$ | TIOAn/TIOBn (when using as TGIN) | - | $2t_{CYCP}$ | - | ns | |




***Note:***

- *$t_{CYCP}$ indicates the APB bus clock cycle time.*
  *About the APB bus number which the Base Timer is connected to, see "8. Block Diagram" in this datasheet.*

### *12.4.10 CSIO/UART Timing*

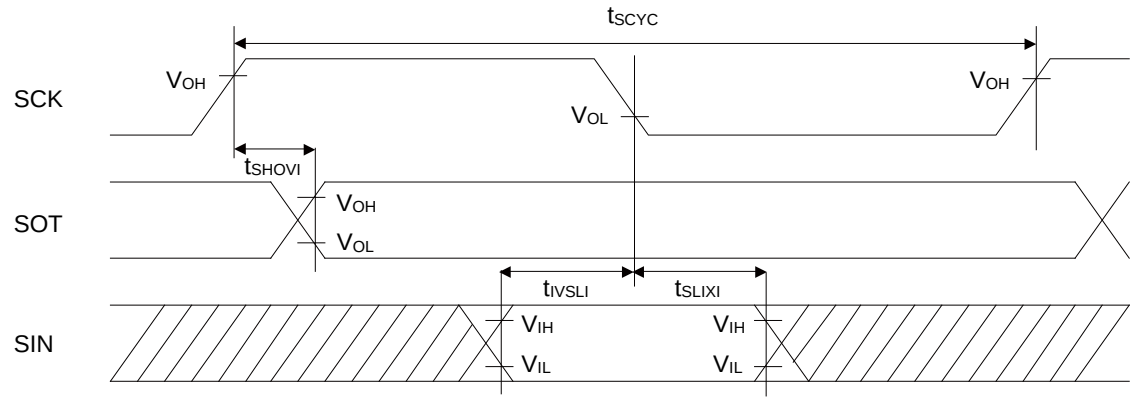
**CSIO (SPI = 0, SCINV = 0)**

($V_{CC}$ = 1.65 V to 3.6 V, $V_{SS}$ = 0 V, $T_A$ = - 40°C to + 85°C)

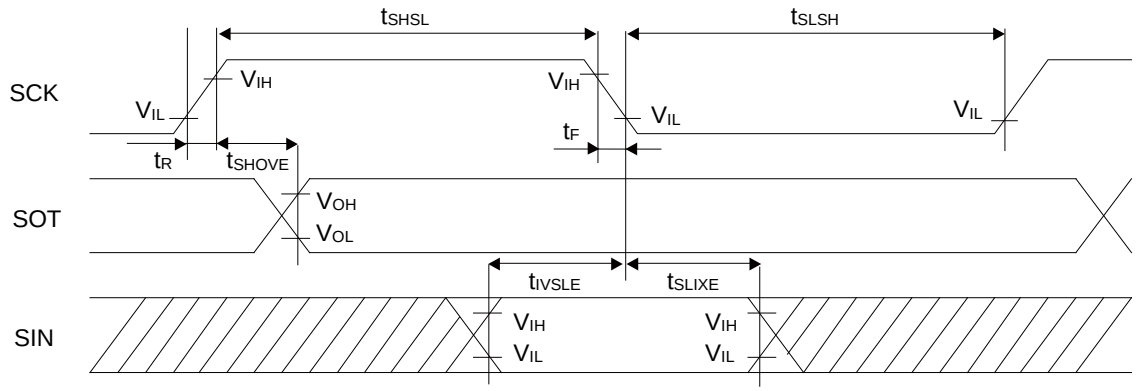
| Parameter | Symbol | Pin name | Conditions | $V_{CC}$ < 2.7 V | | $V_{CC}$ ≥ 2.7 V | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| Baud rate | - | - | - | - | 8 | - | 8 | Mbps |
| Serial clock cycle time | $t_{SCYC}$ | SCKx | Master mode | $4t_{CYCP}$ | - | $4t_{CYCP}$ | - | ns |
| SCK ↓ → SOT delay time | $t_{SLOVI}$ | SCKx, SOTx | | - 30 | + 30 | - 20 | + 20 | ns |
| SIN → SCK ↑ setup time | $t_{IVSHI}$ | SCKx, SINx | | 50 | - | 36 | - | ns |
| SCK ↑ → SIN hold time | $t_{SHIXI}$ | SCKx, SINx | | 0 | - | 0 | - | ns |
| Serial clock L pulse width | $t_{SLSH}$ | SCKx | Slave mode | $2t_{CYCP}$ - 10 | - | $2t_{CYCP}$ - 10 | - | ns |
| Serial clock H pulse width | $t_{SHSL}$ | SCKx | | $t_{CYCP}$ + 10 | - | $t_{CYCP}$ + 10 | - | ns |
| SCK ↓ → SOT delay time | $t_{SLOVE}$ | SCKx, SOTx | | - | 50 | - | 33 | ns |
| SIN → SCK ↑ setup time | $t_{IVSHE}$ | SCKx, SINx | | 10 | - | 10 | - | ns |
| SCK ↑ → SIN hold time | $t_{SHIXE}$ | SCKx, SINx | | 20 | - | 20 | - | ns |
| SCK falling time | $t_F$ | SCKx | | - | 5 | - | 5 | ns |
| SCK rising time | $t_R$ | SCKx | | - | 5 | - | 5 | ns |

***Notes:***

- *The above characteristics apply to clock synchronous mode.*
- *$t_{CYCP}$ indicates the APB bus clock cycle time.*
  *About the APB bus number which Multi-function serial is connected to, see "8. Block Diagram" in this datasheet.*
- *These characteristics only guarantee the same relocate port number.*
  *For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.*
- *When the external load capacitance $C_L$= 30 pF.*




Master mode




Slave mode

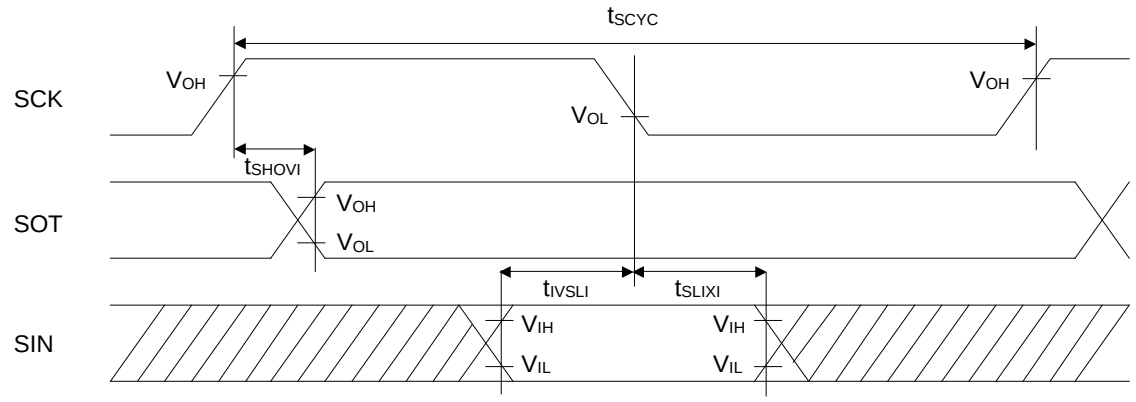
**CSIO (SPI = 0, SCINV = 1)**

($V_{CC}$ = 1.65 V to 3.6 V, $V_{SS}$ = 0 V, $T_A$ = - 40°C to + 85°C)

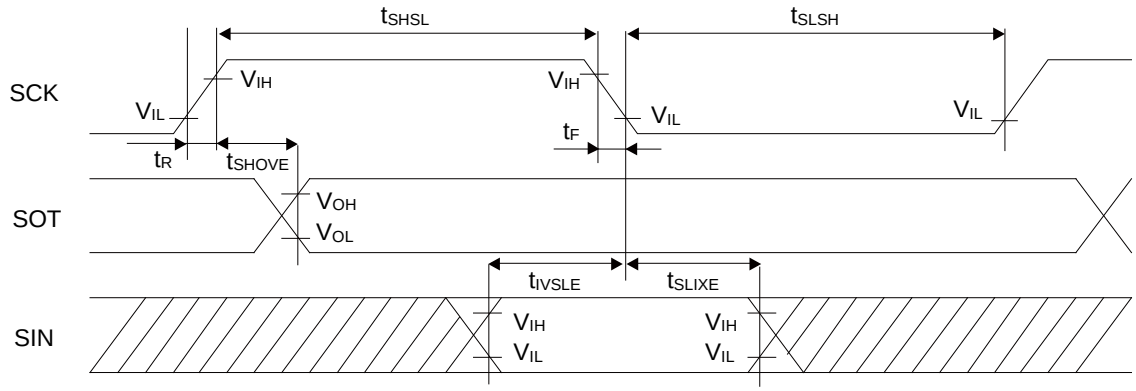
| Parameter | Symbol | Pin name | Conditions | $V_{CC}$ < 2.7 V | | $V_{CC}$ ≥ 2.7 V | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| Baud rate | - | - | - | - | 8 | - | 8 | Mbps |
| Serial clock cycle time | $t_{SCYC}$ | SCKx | Master mode | $4t_{CYCP}$ | - | $4t_{CYCP}$ | - | ns |
| SCK ↑ → SOT delay time | $t_{SHOVI}$ | SCKx, SOTx | | - 30 | + 30 | - 20 | + 20 | ns |
| SIN → SCK ↓ setup time | $t_{IVSLI}$ | SCKx, SINx | | 50 | - | 36 | - | ns |
| SCK ↓ → SIN hold time | $t_{SLIXI}$ | SCKx, SINx | | 0 | - | 0 | - | ns |
| Serial clock L pulse width | $t_{SLSH}$ | SCKx | Slave mode | $2t_{CYCP}$ - 10 | - | $2t_{CYCP}$ - 10 | - | ns |
| Serial clock H pulse width | $t_{SHSL}$ | SCKx | | $t_{CYCP}$ + 10 | - | $t_{CYCP}$ + 10 | - | ns |
| SCK ↑ → SOT delay time | $t_{SHOVE}$ | SCKx, SOTx | | - | 50 | - | 33 | ns |
| SIN → SCK ↓ setup time | $t_{IVSLE}$ | SCKx, SINx | | 10 | - | 10 | - | ns |
| SCK ↓ → SIN hold time | $t_{SLIXE}$ | SCKx, SINx | | 20 | - | 20 | - | ns |
| SCK falling time | $t_F$ | SCKx | | - | 5 | - | 5 | ns |
| SCK rising time | $t_R$ | SCKx | | - | 5 | - | 5 | ns |

***Notes:***

- *The above characteristics apply to clock synchronous mode.*
- *$t_{CYCP}$ indicates the APB bus clock cycle time.*
  *About the APB bus number which Multi-function serial is connected to, see "8. Block Diagram" in this datasheet.*
- *These characteristics only guarantee the same relocate port number.*
  *For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.*
- *When the external load capacitance $C_L$ = 30 pF.*




Master mode




Slave mode

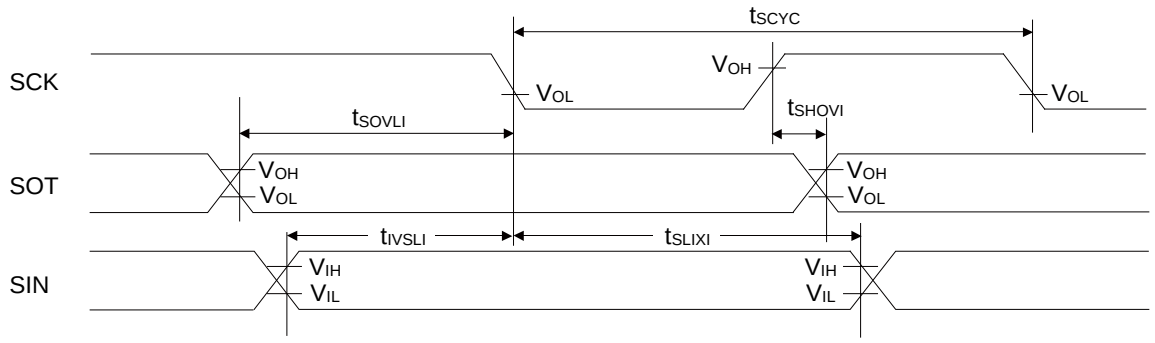
**CSIO (SPI = 1, SCINV = 0)**

($V_{CC}$ = 1.65 V to 3.6 V, $V_{SS}$ = 0 V, $T_A$ = - 40°C to + 85°C)

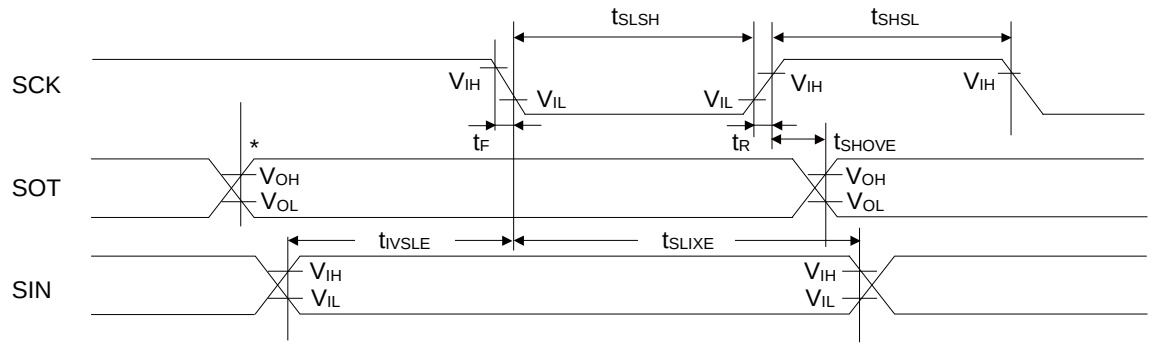
| Parameter | Symbol | Pin name | Conditions | $V_{CC}$ < 2.7 V | | $V_{CC}$ ≥ 2.7 V | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| Baud rate | - | - | - | - | 8 | - | 8 | Mbps |
| Serial clock cycle time | $t_{SCYC}$ | SCKx | Master mode | $4t_{CYCP}$ | - | $4t_{CYCP}$ | - | ns |
| SCK ↑ → SOT delay time | $t_{SHOVI}$ | SCKx, SOTx | | - 30 | + 30 | - 20 | + 20 | ns |
| SIN → SCK ↓ setup time | $t_{IVSLI}$ | SCKx, SINx | | 50 | - | 36 | - | ns |
| SCK ↓→ SIN hold time | $t_{SLIXI}$ | SCKx, SINx | | 0 | - | 0 | - | ns |
| SOT → SCK ↓ delay time | $t_{SOVLI}$ | SCKx, SOTx | | $2t_{CYCP}$ - 34 | - | $2t_{CYCP}$ - 34 | - | ns |
| Serial clock L pulse width | $t_{SLSH}$ | SCKx | Slave mode | $2t_{CYCP}$ - 10 | - | $2t_{CYCP}$ - 10 | - | ns |
| Serial clock H pulse width | $t_{SHSL}$ | SCKx | | $t_{CYCP}$ + 10 | - | $t_{CYCP}$ + 10 | - | ns |
| SCK ↑ → SOT delay time | $t_{SHOVE}$ | SCKx, SOTx | | - | 50 | - | 33 | ns |
| SIN → SCK ↓ setup time | $t_{IVSLE}$ | SCKx, SINx | | 10 | - | 10 | - | ns |
| SCK ↓→ SIN hold time | $t_{SLIXE}$ | SCKx, SINx | | 20 | - | 20 | - | ns |
| SCK falling time | $t_F$ | SCKx | | - | 5 | - | 5 | ns |
| SCK rising time | $t_R$ | SCKx | | - | 5 | - | 5 | ns |

***Notes:***

- *The above characteristics apply to clock synchronous mode.*
- *$t_{CYCP}$ indicates the APB bus clock cycle time.*
  *About the APB bus number which Multi-function serial is connected to, see "8. Block Diagram" in this datasheet.*
- *These characteristics only guarantees the same relocate port number.*
  *For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.*
- *When the external load capacitance $C_L$= 30 pF.*




Master mode




Slave mode

*: Changes when writing to TDR register

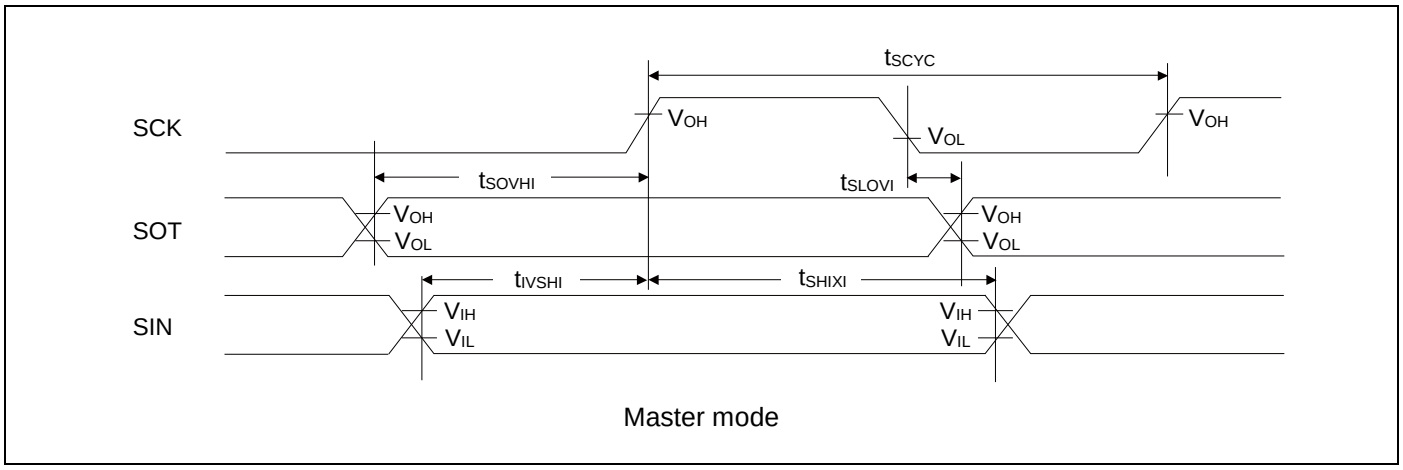
**CSIO (SPI = 1, SCINV = 1)**

($V_{CC}$ = 1.65 V to 3.6 V, $V_{SS}$ = 0 V, $T_A$ = - 40°C to + 85°C)

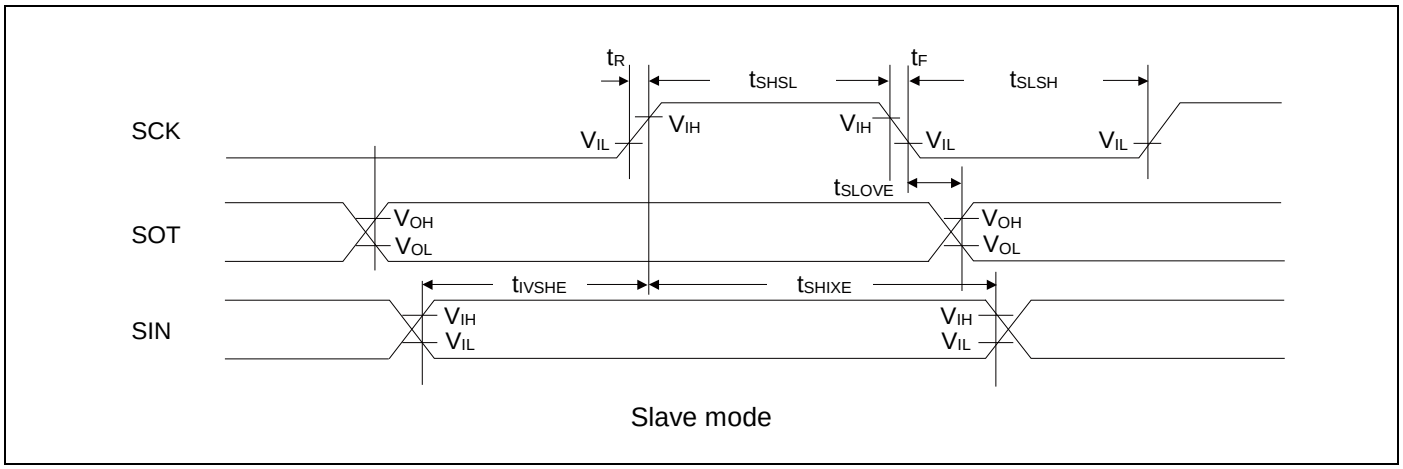
| Parameter | Symbol | Pin name | Conditions | $V_{CC}$ < 2.7 V | | $V_{CC}$ ≥ 2.7 V | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| Baud rate | - | - | - | - | 8 | - | 8 | Mbps |
| Serial clock cycle time | $t_{SCYC}$ | SCKx | Master mode | $4t_{CYCP}$ | - | $4t_{CYCP}$ | - | ns |
| SCK ↓ → SOT delay time | $t_{SLOVI}$ | SCKx, SOTx | | - 30 | + 30 | - 20 | + 20 | ns |
| SIN → SCK ↑ setup time | $t_{IVSHI}$ | SCKx, SINx | | 50 | - | 36 | - | ns |
| SCK ↑ → SIN hold time | $t_{SHIXI}$ | SCKx, SINx | | 0 | - | 0 | - | ns |
| SOT → SCK ↑ delay time | $t_{SOVHI}$ | SCKx, SOTx | | $2t_{CYCP}$ - 34 | - | $2t_{CYCP}$ - 34 | - | ns |
| Serial clock L pulse width | $t_{SLSH}$ | SCKx | Slave mode | $2t_{CYCP}$ - 10 | - | $2t_{CYCP}$ - 10 | - | ns |
| Serial clock H pulse width | $t_{SHSL}$ | SCKx | | $t_{CYCP}$ + 10 | - | $t_{CYCP}$ + 10 | - | ns |
| SCK ↓ → SOT delay time | $t_{SLOVE}$ | SCKx, SOTx | | - | 50 | - | 33 | ns |
| SIN → SCK ↑ setup time | $t_{IVSHE}$ | SCKx, SINx | | 10 | - | 10 | - | ns |
| SCK ↑ → SIN hold time | $t_{SHIXE}$ | SCKx, SINx | | 20 | - | 20 | - | ns |
| SCK falling time | $t_F$ | SCKx | | - | 5 | - | 5 | ns |
| SCK rising time | $t_R$ | SCKx | | - | 5 | - | 5 | ns |

***Notes:***

- *The above characteristics apply to clock synchronous mode.*
- *$t_{CYCP}$ indicates the APB bus clock cycle time.*
  *About the APB bus number which Multi-function serial is connected to, see "8. Block Diagram" in this datasheet.*
- *These characteristics only guarantee the same relocate port number.*
  *For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.*
- *When the external load capacitance $C_L$ = 30 pF.*




Master mode

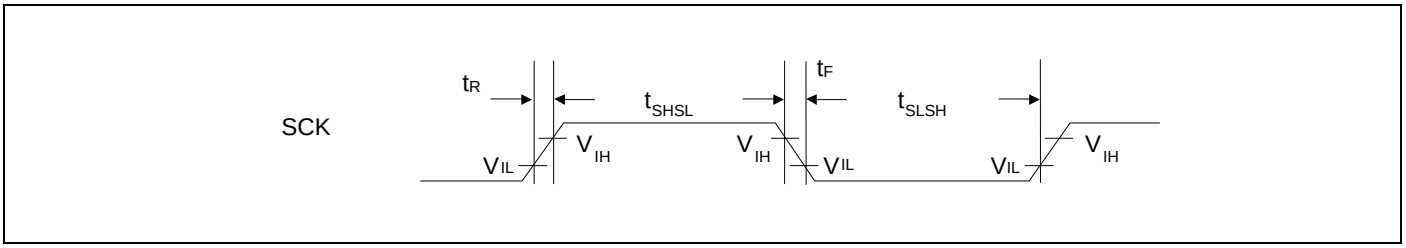



Slave mode

**UART external clock input (EXT = 1)**

($V_{CC}$ = 1.65 V to 3.6 V, $V_{SS}$ = 0 V, $T_A$ = - 40°C to + 85°C)

| Parameter | Symbol | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| Serial clock L pulse width | $t_{SLSH}$ | $C_L$ = 30 pF | $t_{CYCP}$ + 10 | - | ns | |
| Serial clock H pulse width | $t_{SHSL}$ | | $t_{CYCP}$ + 10 | - | ns | |
| SCK falling time | $t_F$ | | - | 5 | ns | |
| SCK rising time | $t_R$ | | - | 5 | ns | |



### 12.4.11 External Input Timing

($V_{CC}$ = 1.65 V to 3.6 V, $V_{SS}$ = 0 V, $T_A$ = - 40°C to + 85°C)

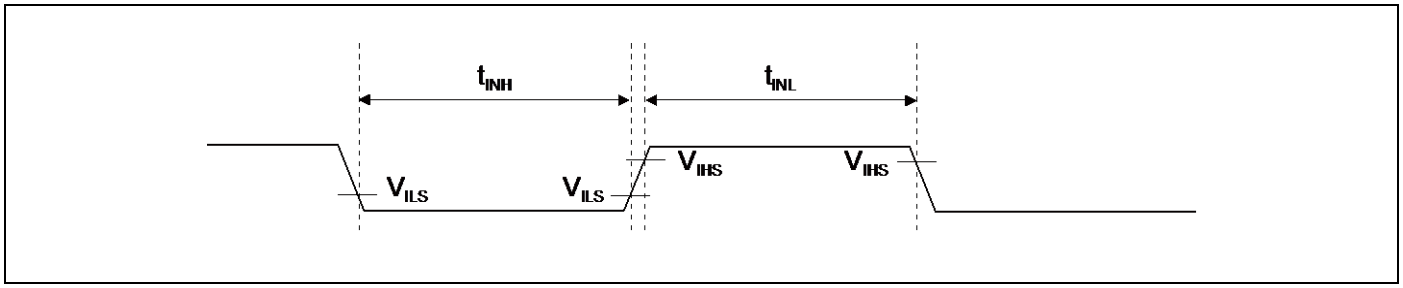
| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Input pulse width | $t_{INH}$, $t_{INL}$ | ADTG | - | $2t_{CYCP}$ *1 | - | ns | A/D converter trigger input |
| | | INTxx, NMIX | *2 | $2t_{CYCP}$ + 100 *1 | - | ns | External interrupt NMI |
| | | | *3 | 500 | - | ns | |
| | | WKUPx | *4 | 600 | - | ns | Deep standby wake up |

*1: $t_{CYCP}$ indicates the APB bus clock cycle time.
About the APB bus number which the Multi-function Timer is connected to, see 8. Block Diagram in this datasheet.

*2: When in Run mode, in Sleep mode.

*3: When in Stop mode, in Timer mode.

*4: When in Deep Standby RTC mode, in Deep Standby Stop mode.



### 12.4.12 I²C Timing

($V_{CC}$ = 1.65 V to 3.6 V, $V_{SS}$ = 0 V, $T_A$ = - 40°C to + 85°C)

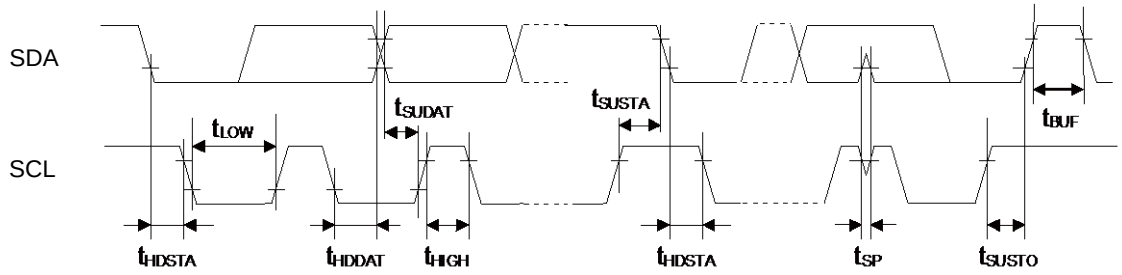
| Parameter | Symbol | Conditions | Standard-mode | | Fast-mode | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | | |
| SCL clock frequency | $F_{SCL}$ | $C_L$ = 30 pF, R = (Vp/$I_{OL}$) *1 | 0 | 100 | 0 | 400 | kHz | |
| (Repeated) START condition hold time SDA ↓ → SCL ↓ | $t_{HDSTA}$ | | 4.0 | - | 0.6 | - | μs | |
| SCL clock L width | $t_{LOW}$ | | 4.7 | - | 1.3 | - | μs | |
| SCL clock H width | $t_{HIGH}$ | | 4.0 | - | 0.6 | - | μs | |
| (Repeated) START condition setup time SCL ↑ → SDA ↓ | $t_{SUSTA}$ | | 4.7 | - | 0.6 | - | μs | |
| Data hold time SCL ↓ → SDA ↓ ↑ | $t_{HDDAT}$ | | 0 | 3.45 *2 | 0 | 0.9 *3 | μs | |
| Data setup time SDA ↓ ↑ → SCL ↑ | $t_{SUDAT}$ | | 250 | - | 100 | - | ns | |
| STOP condition setup time SCL ↑ → SDA ↑ | $t_{SUSTO}$ | | 4.0 | - | 0.6 | - | μs | |
| Bus free time between STOP condition and START condition | $t_{BUF}$ | | 4.7 | - | 1.3 | - | μs | |
| Noise filter | $t_{SP}$ | - | 2 $t_{CYCP}$ *4 | - | 2 $t_{CYCP}$ *4 | - | ns | |

*1: R and C represent the pull-up resistor and load capacitance of the SCL and SDA lines, respectively.
Vp indicates the power supply voltage of the pull-up resistor and $I_{OL}$ indicates $V_{OL}$ guaranteed current.

*2: The maximum $t_{HDDAT}$ must satisfy that it does not extend at least L period ($t_{LOW}$) of device's SCL signal.

*3: A Fast-mode I²C bus device can be used on a Standard-mode I²C bus system as long as the device satisfies the requirement of $t_{SUDAT}$ ≥ 250 ns.

*4: $t_{CYCP}$ is the APB bus clock cycle time.
About the APB bus number that I2C is connected to, see 8. Block Diagram in this datasheet.
To use Standard-mode, set the APB bus clock at 2 MHz or more.
To use Fast-mode, set the APB bus clock at 8 MHz or more.



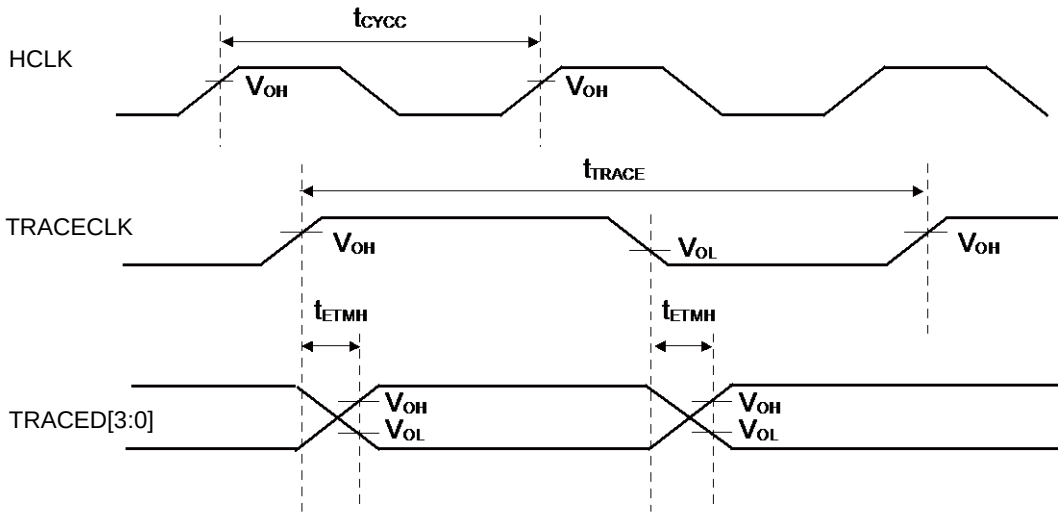
### 12.4.13 ETM Timing

($V_{CC}$ = 1.65 V to 3.6 V, $V_{SS}$ = 0 V, $T_A$ = - 40°C to + 85°C)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Data hold | $t_{ETMH}$ | TRACECLK, TRACED[3:0] | $V_{CC} \geq 2.7$ V | 2 | 11 | ns | |
| | | | $V_{CC} < 2.7$ V | 2 | 15 | | |
| TRACECLK frequency | 1/ $t_{TRACE}$ | TRACECLK | $V_{CC} \geq 2.7$ V | - | 40 | MHz | |
| | | | $V_{CC} < 2.7$ V | - | 20 | MHz | |
| TRACECLK clock cycle | $t_{TRACE}$ | | $V_{CC} \geq 2.7$ V | 25 | - | ns | |
| | | | $V_{CC} < 2.7$ V | 50 | - | ns | |

***Note:***

- *When the external load capacitance $C_L$ = 30 pF.*



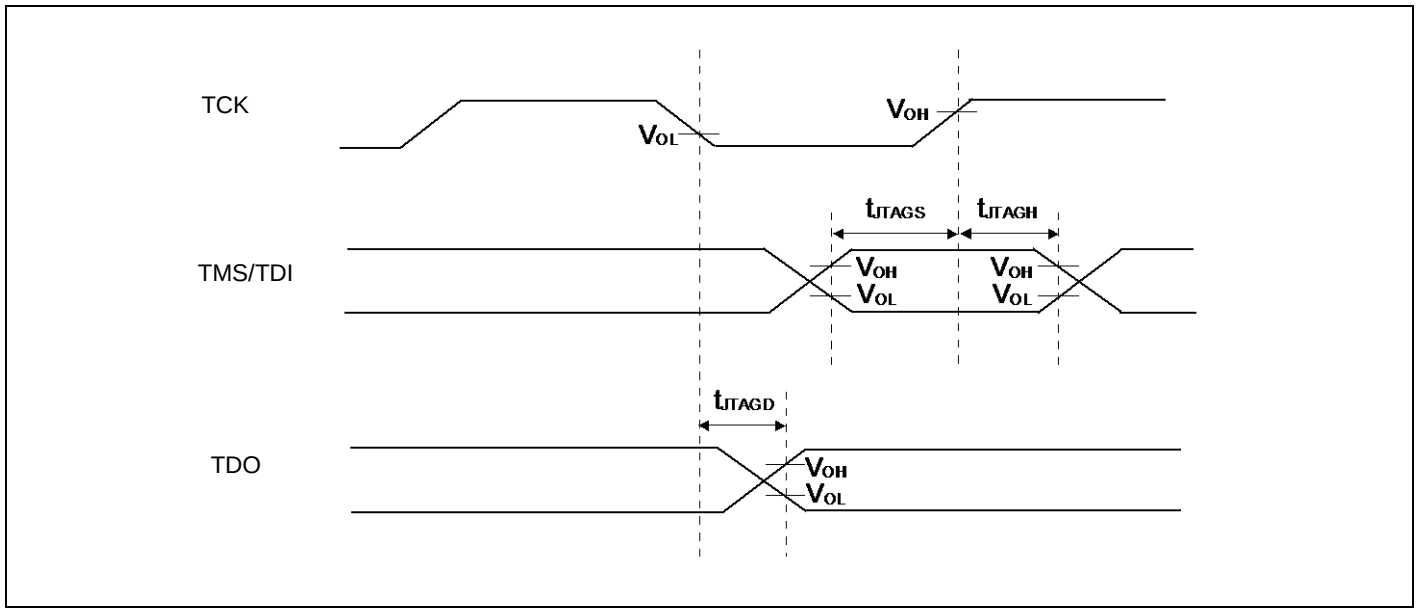
### 12.4.14 JTAG Timing

($V_{CC}$ = 1.65 V to 3.6 V, $V_{SS}$ = 0 V, $T_A$ = - 40°C to + 85°C)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| TMS, TDI setup time | $t_{JTAGS}$ | TCK, TMS, TDI | $V_{CC} \geq 2.7$ V | 15 | - | ns | |
| | | | $V_{CC} < 2.7$ V | | | | |
| TMS, TDI hold time | $t_{JTAGH}$ | TCK, TMS, TDI | $V_{CC} \geq 2.7$ V | 15 | - | ns | |
| | | | $V_{CC} < 2.7$ V | | | | |
| TDO delay time | $t_{JTAGD}$ | TCK, TDO | $V_{CC} \geq 2.7$ V | - | 25 | ns | |
| | | | $V_{CC} < 2.7$ V | - | 45 | | |

***Note:***

- *When the external load capacitance $C_L$ = 30 pF.*



## 12.5 12-bit A/D Converter

### Electrical Characteristics for the A/D Converter

($V_{CC}$ = $AV_{CC}$ = 1.65 V to 3.6 V, $V_{SS}$ = $AV_{SS}$ = 0 V, $T_A$ = - 40°C to + 85°C)

| Parameter | Symbol | Pin name | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Resolution | - | - | - | - | 12 | bit | |
| Integral Nonlinearity | - | - | - | ± 2 | ± 4.5 | LSB | |
| Differential Nonlinearity | - | - | - | ± 2.2 | ± 2.5 | LSB | |
| Zero transition voltage | $V_{ZT}$ | ANxx | - | ± 6 | ± 15 | mV | |
| Full-scale transition voltage | $V_{FST}$ | ANxx | - | AVRH ± 6 | AVRH ± 15 | mV | |
| Conversion time | - | - | 2.0 *1 | - | - | µs | $AV_{CC}$ ≥ 2.7 V |
| | | | 4.0 *1 | - | - | | 1.8 V≤ $AV_{CC}$ < 2.7 V |
| | | | 10 *1 | - | - | | 1.65 V≤ $AV_{CC}$ < 1.8 V |
| Sampling time *2 | $t_S$ | - | 0.6 | - | 10 | us | $AV_{CC}$ ≥ 2.7 V |
| | | | 1.2 | - | | | 1.8 V≤ $AV_{CC}$ < 2.7 V |
| | | | 3.0 | - | | | 1.65 V≤ $AV_{CC}$ < 1.8 V |
| Compare clock cycle *3 | $t_{CCK}$ | - | 100 | - | 1000 | ns | $AV_{CC}$ ≥ 2.7 V |
| | | | 200 | | | | 1.8 V≤ $AV_{CC}$ < 2.7 V |
| | | | 500 | | | | 1.65 V≤ $AV_{CC}$ < 1.8 V |
| State transition time to operation permission | $t_{STT}$ | - | - | - | 1.0 | µs | |
| Power supply current (analog + digital) | - | AVCC | - | 0.27 | 0.42 | mA | A/D 1unit operation |
| | | | - | 0.03 | 10 | µA | When A/D stops |
| Reference power supply current (between AVRH to AVSS) | - | AVRH | - | 0.72 | 1.29 | mA | A/D 1unit operation AVRH=3.6 V |
| | | | - | 0.02 | 2.6 | µA | When A/D stops |
| Analog input capacity | $C_{AIN}$ | - | - | - | 9.4 | pF | |
| Analog input resistor | $R_{AIN}$ | - | - | - | 2.2 | kΩ | $AV_{CC}$ ≥ 2.7 V |
| | | | | | 5.5 | | 1.8 V≤ $AV_{CC}$ < 2.7 V |
| | | | | | 10.5 | | 1.65 V≤ $AV_{CC}$ < 1.8 V |
| Interchannel disparity | - | - | - | - | 4 | LSB | |
| Analog port input leak current | - | ANxx | - | - | 5 | µA | |
| Analog input voltage | - | ANxx | $AV_{SS}$ | - | AVRH | V | |
| Reference voltage | - | AVRH | 2.7 | - | $AV_{CC}$ | V | $AV_{CC}$ ≥ 2.7 V |
| | | | $AV_{CC}$ | | | | $AV_{CC}$ < 2.7 V |
| | - | AVRL | $AV_{SS}$ | - | $AV_{SS}$ | V | |

*1: The conversion time is the value of sampling time ($t_S$) + compare time ($t_C$).

The condition of the minimum conversion time is the following.

$AV_{CC}$ ≥ 2.7 V, HCLK=40 MHz — sampling time: 0.6 µs, compare time: 1.4 µs
1.8 V ≤ $AV_{CC}$ < 2.7 V, HCLK=40 MHz — sampling time: 1.2 µs, compare time: 2.8 µs
1.65 V ≤ $AV_{CC}$ < 1.8 V, HCLK=40 MHz — sampling time: 3 µs, compare time: 7 µs

Ensure that it satisfies the value of the sampling time ($t_S$) and compare clock cycle ($t_{CCK}$).
For setting of the sampling time and the compare clock cycle, see Chapter 1-1: A/D Converter in FM3 Family Peripheral Manual Analog Macro Port.

The register setting of the A/D Converter are reflected in the operation according to the APB bus clock timing.

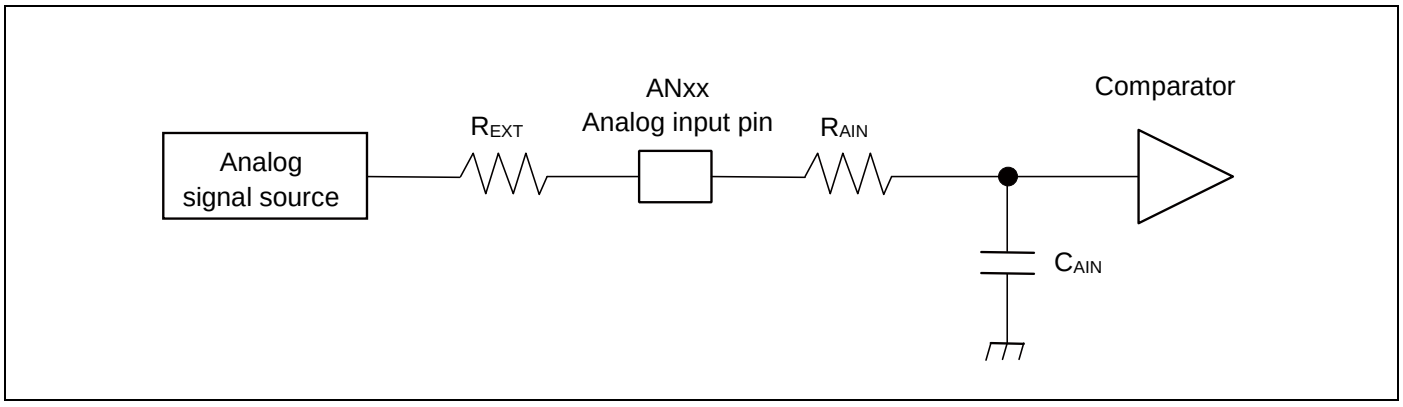
The sampling clock and compare clock is generated from the Base clock (HCLK).

About the APB bus number which the A/D Converter is connected to, see 8. Block Diagram in this datasheet.

*2: A necessary sampling time changes by external impedance.

Ensure that it set the sampling time to satisfy (Equation 1).

*3: The compare time ($t_C$) is the value of (Equation 2).




(Equation 1) $t_S \geq ( R_{AIN} + R_{EXT} ) \times C_{AIN} \times 9$

$t_S$: Sampling time[ns]

$R_{AIN}$: Input resistor of A/D[kΩ] = 2.2 kΩ at 2.7 V ≤ $AV_{CC}$ ≤ 3.6 V
Input resistor of A/D[kΩ] = 5.5 kΩ at 1.8 V ≤ $AV_{CC}$ ≤ 2.7 V
Input resistor of A/D[kΩ] = 10.5 kΩ at 1.65 V ≤ $AV_{CC}$ ≤ 1.8 V

$C_{AIN}$: Input capacity of A/D[pF] = 9.4 pF at 1.65 V ≤ $AV_{CC}$ ≤ 3.6 V

$R_{EXT}$: Output impedance of external circuit [kΩ]

(Equation 2) $t_C = t_{CCK} \times 14$

$t_C$: Compare time

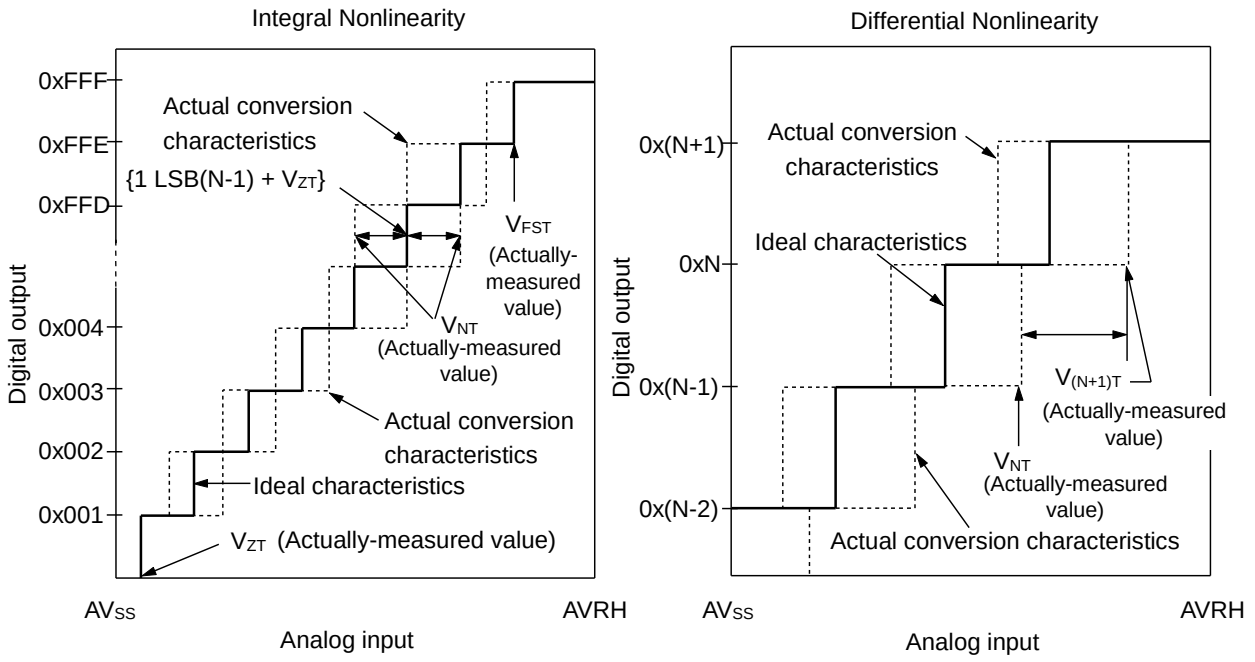
$t_{CCK}$: Compare clock cycle

## Definition of 12-bit A/D Converter Terms

■Resolution: Analog variation that is recognized by an A/D converter.

■Integral Nonlinearity: Deviation of the line between the zero-transition point (0b000000000000 ⟷ 0b000000000001) and the full-scale transition point (0b111111111110 ⟷ 0b111111111111) from the actual conversion characteristics.

■Differential Nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.




$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

N: A/D converter digital output value.
$V_{ZT}$: Voltage at which the digital output changes from 0x000 to 0x001.
$V_{FST}$: Voltage at which the digital output changes from 0xFFE to 0xFFF.
$V_{NT}$: Voltage at which the digital output changes from 0x(N − 1) to 0xN.

## 12.6 Low-Voltage Detection Characteristics

### *12.6.1 Low-Voltage Detection Reset*

($T_A$ = - 40°C to + 85°C)

| Parameter | Symbol | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Detected voltage | VDL | SVHR *1 = 00000 | 1.38 | 1.50 | 1.60 | V | When voltage drops |
| Released voltage | VDH | | 1.43 | 1.55 | 1.65 | V | When voltage rises |
| Detected voltage | VDL | SVHR *1 = 00001 | 1.43 | 1.55 | 1.65 | V | When voltage drops |
| Released voltage | VDH | | Same as SVHR = 00000 value | | | V | When voltage rises |
| Detected voltage | VDL | SVHR *1 = 00010 | 1.47 | 1.60 | 1.73 | V | When voltage drops |
| Released voltage | VDH | | Same as SVHR = 00000 value | | | V | When voltage rises |
| Detected voltage | VDL | SVHR *1 = 00011 | 1.52 | 1.65 | 1.78 | V | When voltage drops |
| Released voltage | VDH | | Same as SVHR = 00000 value | | | V | When voltage rises |
| Detected voltage | VDL | SVHR *1 = 00100 | 1.56 | 1.70 | 1.84 | V | When voltage drops |
| Released voltage | VDH | | Same as SVHR = 00000 value | | | V | When voltage rises |
| Detected voltage | VDL | SVHR *1 = 00101 | 1.61 | 1.75 | 1.89 | V | When voltage drops |
| Released voltage | VDH | | Same as SVHR = 00000 value | | | V | When voltage rises |
| Detected voltage | VDL | SVHR *1 = 00110 | 1.66 | 1.80 | 1.94 | V | When voltage drops |
| Released voltage | VDH | | Same as SVHR = 00000 value | | | V | When voltage rises |
| Detected voltage | VDL | SVHR *1 = 00111 | 1.70 | 1.85 | 2.00 | V | When voltage drops |
| Released voltage | VDH | | Same as SVHR = 00000 value | | | V | When voltage rises |
| Detected voltage | VDL | SVHR *1 = 01000 | 1.75 | 1.90 | 2.05 | V | When voltage drops |
| Released voltage | VDH | | Same as SVHR = 00000 value | | | V | When voltage rises |
| Detected voltage | VDL | SVHR *1 = 01001 | 1.79 | 1.95 | 2.11 | V | When voltage drops |
| Released voltage | VDH | | Same as SVHR = 00000 value | | | V | When voltage rises |
| Detected voltage | VDL | SVHR *1 = 01010 | 1.84 | 2.00 | 2.16 | V | When voltage drops |
| Released voltage | VDH | | Same as SVHR = 00000 value | | | V | When voltage rises |
| Detected voltage | VDL | SVHR *1 = 01011 | 1.89 | 2.05 | 2.21 | V | When voltage drops |
| Released voltage | VDH | | Same as SVHR = 00000 value | | | V | When voltage rises |
| Detected voltage | VDL | SVHR *1 = 01100 | 2.30 | 2.50 | 2.70 | V | When voltage drops |
| Released voltage | VDH | | Same as SVHR = 00000 value | | | V | When voltage rises |
| Detected voltage | VDL | SVHR *1 = 01101 | 2.39 | 2.60 | 2.81 | V | When voltage drops |
| Released voltage | VDH | | Same as SVHR = 00000 value | | | V | When voltage rises |
| Detected voltage | VDL | SVHR *1 = 01110 | 2.48 | 2.70 | 2.92 | V | When voltage drops |
| Released voltage | VDH | | Same as SVHR = 00000 value | | | V | When voltage rises |
| Detected voltage | VDL | SVHR *1 = 01111 | 2.58 | 2.80 | 3.02 | V | When voltage drops |
| Released voltage | VDH | | Same as SVHR = 00000 value | | | V | When voltage rises |
| Detected voltage | VDL | SVHR *1 = 10000 | 2.67 | 2.90 | 3.13 | V | When voltage drops |
| Released voltage | VDH | | Same as SVHR = 00000 value | | | V | When voltage rises |
| Detected voltage | VDL | SVHR *1 = 10001 | 2.76 | 3.00 | 3.24 | V | When voltage drops |
| Released voltage | VDH | | Same as SVHR = 00000 value | | | V | When voltage rises |
| Detected voltage | VDL | SVHR *1 = 10010 | 2.85 | 3.10 | 3.35 | V | When voltage drops |
| Released voltage | VDH | | Same as SVHR = 00000 value | | | V | When voltage rises |
| Detected voltage | VDL | SVHR *1 = 10011 | 2.94 | 3.20 | 3.46 | V | When voltage drops |
| Released voltage | VDH | | Same as SVHR = 00000 value | | | V | When voltage rises |
| LVD stabilization wait time | $t_{LVDW}$ | - | - | - | 5200 × $t_{CYCP}$ *2 | µs | |
| LVD detection delay time | $t_{LVDDL}$ | - | - | - | 200 | µs | |

*1: The SVHR bit of Low-Voltage Detection Voltage Control Register (LVD_CTL) is initialized to 00000 by Low-Voltage Detection Reset.

*2: $t_{CYCP}$ indicates the APB2 bus clock cycle time.

### 12.6.2 Interrupt of Low-Voltage Detection

($T_A$ = - 40°C to + 85°C)

| Parameter | Symbol | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Detected voltage | VDL | SVHI = 00100 | 1.56 | 1.70 | 1.84 | V | When voltage drops |
| Released voltage | VDH | | 1.61 | 1.75 | 1.89 | V | When voltage rises |
| Detected voltage | VDL | SVHI = 00101 | 1.61 | 1.75 | 1.89 | V | When voltage drops |
| Released voltage | VDH | | 1.66 | 1.80 | 1.94 | V | When voltage rises |
| Detected voltage | VDL | SVHI = 00110 | 1.66 | 1.80 | 1.94 | V | When voltage drops |
| Released voltage | VDH | | 1.70 | 1.85 | 2.00 | V | When voltage rises |
| Detected voltage | VDL | SVHI = 00111 | 1.70 | 1.85 | 2.00 | V | When voltage drops |
| Released voltage | VDH | | 1.75 | 1.90 | 2.05 | V | When voltage rises |
| Detected voltage | VDL | SVHI = 01000 | 1.75 | 1.90 | 2.05 | V | When voltage drops |
| Released voltage | VDH | | 1.79 | 1.95 | 2.11 | V | When voltage rises |
| Detected voltage | VDL | SVHI = 01001 | 1.79 | 1.95 | 2.11 | V | When voltage drops |
| Released voltage | VDH | | 1.84 | 2.00 | 2.16 | V | When voltage rises |
| Detected voltage | VDL | SVHI = 01010 | 1.84 | 2.00 | 2.16 | V | When voltage drops |
| Released voltage | VDH | | 1.89 | 2.05 | 2.21 | V | When voltage rises |
| Detected voltage | VDL | SVHI = 01011 | 1.89 | 2.05 | 2.21 | V | When voltage drops |
| Released voltage | VDH | | 1.93 | 2.10 | 2.27 | V | When voltage rises |
| Detected voltage | VDL | SVHI = 01100 | 2.30 | 2.50 | 2.70 | V | When voltage drops |
| Released voltage | VDH | | 2.39 | 2.60 | 2.81 | V | When voltage rises |
| Detected voltage | VDL | SVHI = 01101 | 2.39 | 2.60 | 2.81 | V | When voltage drops |
| Released voltage | VDH | | 2.48 | 2.70 | 2.92 | V | When voltage rises |
| Detected voltage | VDL | SVHI = 01110 | 2.48 | 2.70 | 2.92 | V | When voltage drops |
| Released voltage | VDH | | 2.58 | 2.80 | 3.02 | V | When voltage rises |
| Detected voltage | VDL | SVHI = 01111 | 2.58 | 2.80 | 3.02 | V | When voltage drops |
| Released voltage | VDH | | 2.67 | 2.90 | 3.13 | V | When voltage rises |
| Detected voltage | VDL | SVHI = 10000 | 2.67 | 2.90 | 3.13 | V | When voltage drops |
| Released voltage | VDH | | 2.76 | 3.00 | 3.24 | V | When voltage rises |
| Detected voltage | VDL | SVHI = 10001 | 2.76 | 3.00 | 3.24 | V | When voltage drops |
| Released voltage | VDH | | 2.85 | 3.10 | 3.35 | V | When voltage rises |
| Detected voltage | VDL | SVHI = 10010 | 2.85 | 3.10 | 3.35 | V | When voltage drops |
| Released voltage | VDH | | 2.94 | 3.20 | 3.46 | V | When voltage rises |
| Detected voltage | VDL | SVHI = 10011 | 2.94 | 3.20 | 3.46 | V | When voltage drops |
| Released voltage | VDH | | 3.04 | 3.30 | 3.56 | V | When voltage rises |
| LVD stabilization wait time | $t_{LVDW}$ | - | - | - | 5200 × $t_{CYCP}$ *1 | µs | |
| LVD detection delay time | $t_{LVDDL}$ | - | - | - | 200 | µs | |

*1: $t_{CYCP}$ indicates the APB2 bus clock cycle time.

## 12.7 Flash Memory Write/Erase Characteristics

### *12.7.1 Write / Erase time*

($V_{CC}$ = 1.65 V to 3.6 V, $T_A$ = - 40°C to + 85°C)

| Parameter | | Value | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Typ *1 | Max *1 | | |
| Sector erase time | Large Sector | 1.1 | 2.7 | s | Includes write time prior to internal erase |
| | Small Sector | 0.3 | 0.9 | | |
| Half word (16-bit) write time | | 30 | 528 | µs | Not including system-level overhead time |
| Chip erase time | | 6.8 | 18 | s | Includes write time prior to internal erase |

*1: The typical value is immediately after shipment, the maximum value is guarantee value under 100,000 cycle of erase/write.

### *12.7.2 Erase/write cycles and data hold time*

| Erase/write cycles (cycle) | Data hold time (year) | Remarks |
|---|---|---|
| 1,000 | 20 *1 | |
| 10,000 | 10 *1 | |

*1: At average + 85°C

## 12.8 Return Time from Low-Power Consumption Mode

### *12.8.1 Return Factor: Interrupt/WKUP*

The return time from Low-Power consumption mode is indicated as follows. It is from receiving the return factor to starting the program operation.

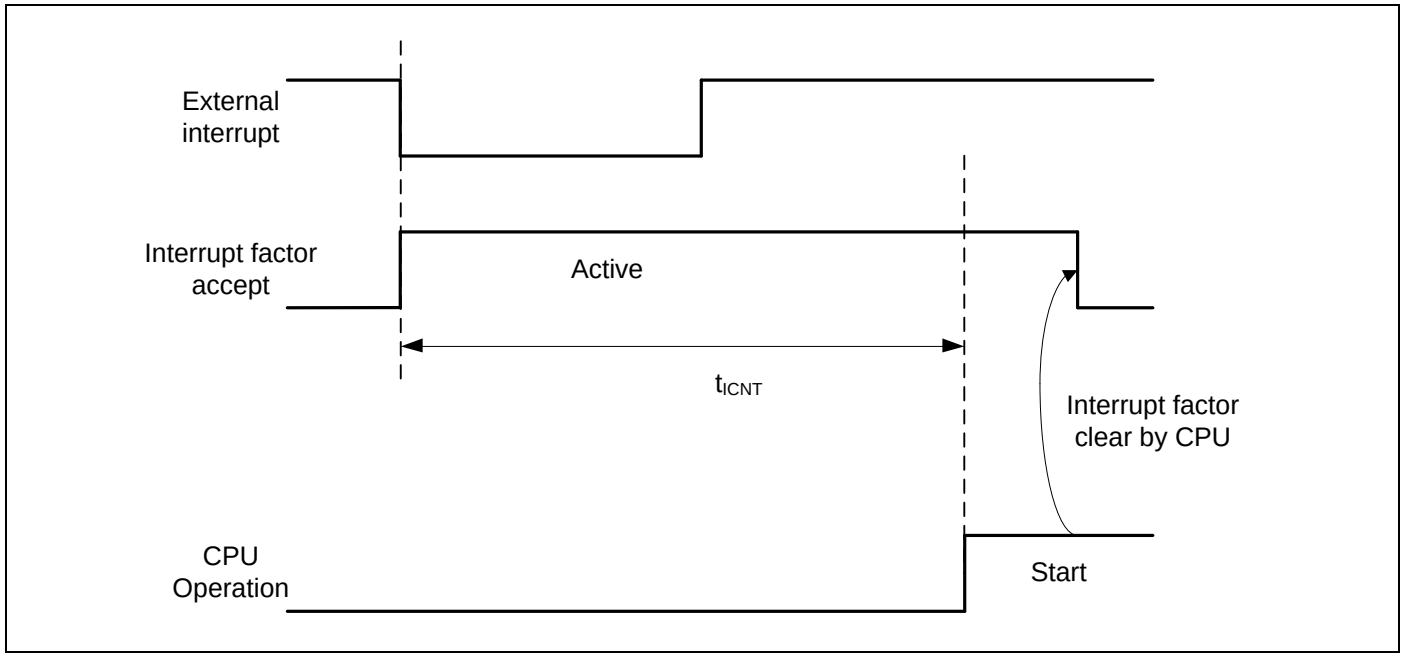
**Return Count Time**

($V_{CC}$ = 1.65 V to 3.6 V, $V_{DDI}$ = 1.1 V to 1.3 V, $V_{SS}$ = 0 V, $T_A$ = - 40°C to + 85°C)

| Parameter | Symbol | Value | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Typ | Max *1 | | |
| Sleep mode | $t_{ICNT}$ | $t_{CYCC}$ | | µs | |
| High-speed CR Timer mode,<br>Main Timer mode,<br>PLL Timer mode | | 40 | 80 | µs | |
| Low-speed CR Timer mode | | 350 | 700 | µs | |
| Sub Timer mode | | 690 | 880 | µs | |
| RTC mode,<br>Stop mode | | 278 | 523 | µs | |
| Deep Standby RTC mode | | 318 | 603 | µs | When RAM is off |
| Deep Standby Stop mode | | 278 | 523 | µs | When RAM is on |

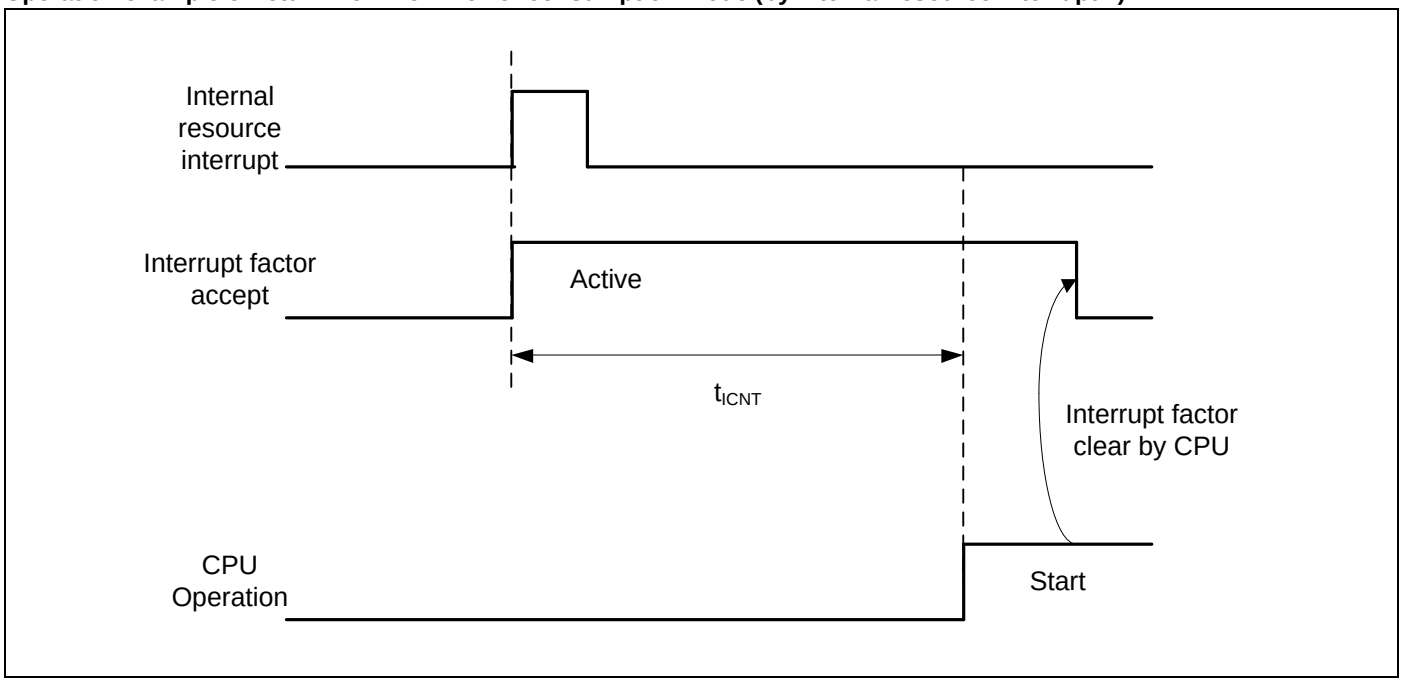
*1: The maximum value depends on the accuracy of built-in CR.

**Operation example of return from Low-Power consumption mode (by external interrupt *1)**




*1: External interrupt is set to detecting fall edge.

**Operation example of return from Low-Power consumption mode (by internal resource interrupt *1)**




*1: Internal resource interrupt is not included in return factor by the kind of Low-Power consumption mode.

***Notes:***

- *The return factor is different in each Low-Power consumption modes.*
  *See Chapter 6: Low Power Consumption Mode and Operations of Standby Modes in FM3 Family Peripheral Manual.*
- *When interrupt recoveries, the operation mode that CPU recoveries depend on the state before the Low-Power consumption mode transition. See Chapter 6: Low Power Consumption Mode in FM3 Family Peripheral Manual.*

### *12.8.2 Return Factor: Reset*

The return time from Low-Power consumption mode is indicated as follows. It is from releasing reset to starting the program operation.

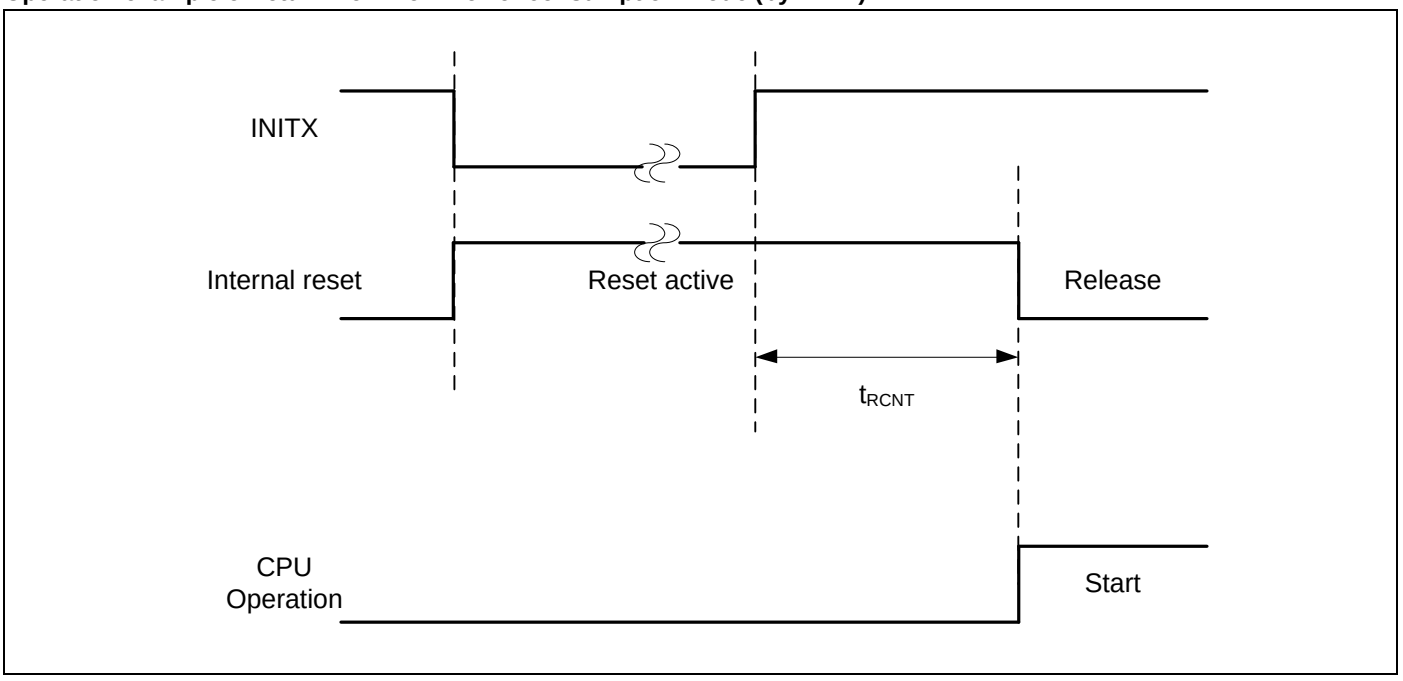
**Return Count Time**

($V_{CC}$ = 1.65 V to 3.6 V, $V_{DDI}$ = 1.1 V to 1.3 V, $V_{SS}$ = 0 V, $T_A$ = - 40°C to + 85°C)

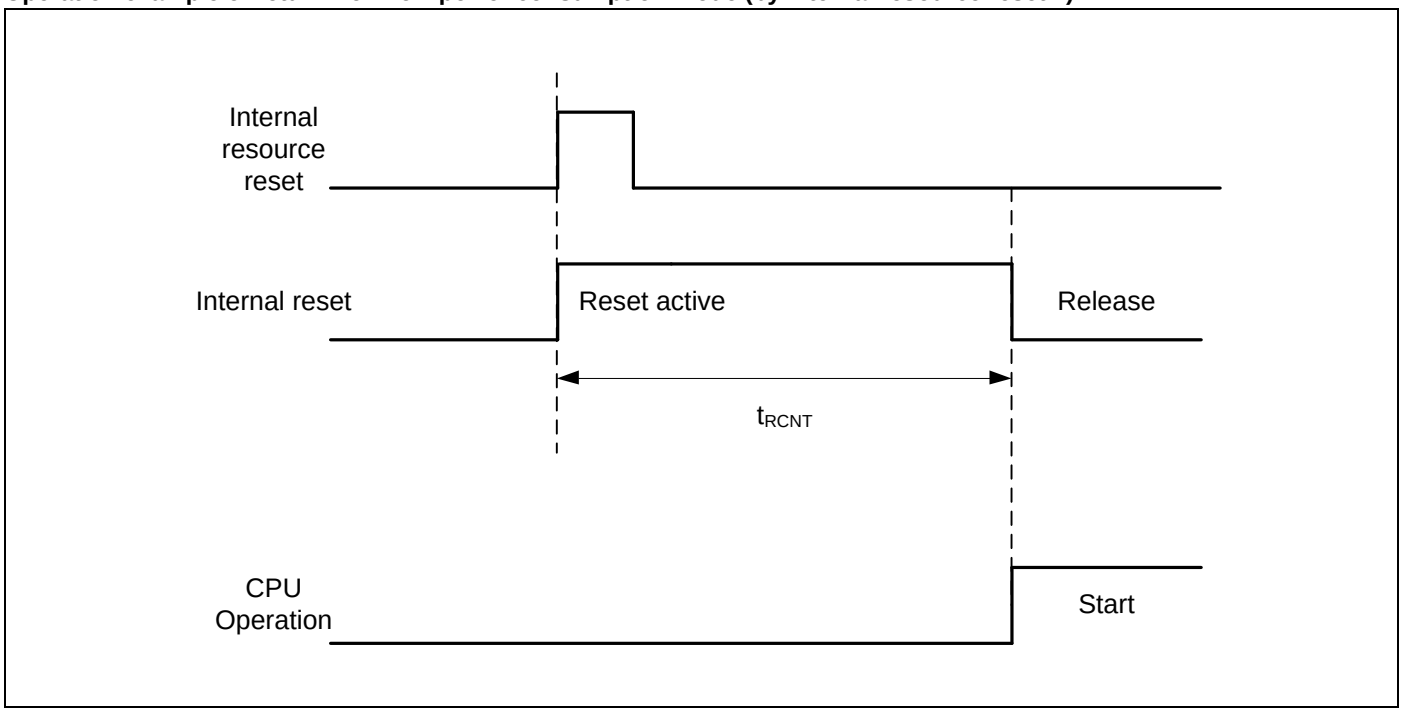
| Parameter | Symbol | Value | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Typ | Max *1 | | |
| Sleep mode | $t_{RCNT}$ | 148 | 263 | µs | |
| High-speed CR Timer mode,<br>Main Timer mode,<br>PLL Timer mode | | 148 | 263 | µs | |
| Low-speed CR Timer mode | | 258 | 483 | µs | |
| Sub Timer mode | | 322 | 516 | µs | |
| RTC/Stop mode | | 278 | 523 | µs | |
| Deep Standby RTC mode | | 318 | 603 | µs | When RAM is off |
| Deep Standby Stop mode | | 278 | 523 | µs | When RAM is on |

*1: The maximum value depends on the accuracy of built-in CR.

**Operation example of return from Low-Power consumption mode (by INITX)**



**Operation example of return from low power consumption mode (by internal resource reset *1)**




*1: Internal resource reset is not included in return factor by the kind of Low-Power consumption mode.

***Notes:***

- *The return factor is different in each Low-Power consumption modes.*
  *See Chapter 6: Low Power Consumption Mode and Operations of Standby Modes in FM3 Family Peripheral Manual.*
- *When interrupt recoveries, the operation mode that CPU recoveries depend on the state before the Low-Power consumption mode transition. See Chapter 6: Low Power Consumption Mode in FM3 Family Peripheral Manual.*
- *The time during the power-on reset/low-voltage detection reset is excluded. See 12.4.7. Power-on Reset Timing 12.4. AC Characteristics in 12. Electrical Characteristics for the detail on the time during the power-on reset/low -voltage detection reset.*
- *When in recovery from reset, CPU changes to the High-speed CR Run mode. When using the main clock or the PLL clock, it is necessary to add the main clock oscillation stabilization wait time or the main PLL clock stabilization wait time.*
- *The internal resource reset means the watchdog reset and the CSV reset.*

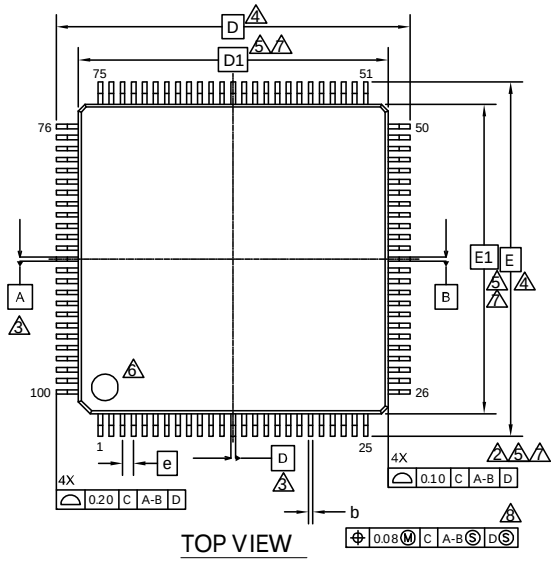
## 13. Ordering Information

| Part number | On-chip Flash memory | On-chip SRAM | Package | Packing |
|---|---|---|---|---|
| MB9AF141LBPMC1-G-JNE2 | Main: 64 KB<br>Work: 32 KB | 16 KB | Plastic • LQFP 64-pin (0.5 mm pitch), (LQD064) | Tray |
| MB9AF142LBPMC1-G-JNE2 | Main: 128 KB<br>Work: 32 KB | 16 KB | | |
| MB9AF144LBPMC1-G-JNE2 | Main: 256 KB<br>Work: 32 KB | 32 KB | | |
| MB9AF141LBPMC-G-JNE2 | Main: 64 KB<br>Work: 32 KB | 16 KB | Plastic • LQFP 64-pin (0.65 mm pitch), (LQG064) | |
| MB9AF142LBPMC-G-JNE2 | Main: 128 KB<br>Work: 32 KB | 16 KB | | |
| MB9AF144LBPMC-G-JNE2 | Main: 256 KB<br>Work: 32 KB | 32 KB | | |
| MB9AF141LBQN-G-AVE2 | Main: 64 KB<br>Work: 32 KB | 16 KB | Plastic • QFN 64-pin (0.5 mm pitch), (VNC064) | |
| MB9AF142LBQN-G-AVE2 | Main: 128 KB<br>Work: 32 KB | 16 KB | | |
| MB9AF144LBQN-G-AVE2 | Main: 256 KB<br>Work: 32 KB | 32 KB | | |
| MB9AF141MBPMC-G-JNE2 | Main: 64 KB<br>Work: 32 KB | 16 KB | Plastic • LQFP 80-pin (0.5 mm pitch), (LQH080) | |
| MB9AF142MBPMC-G-JNE2 | Main: 128 KB<br>Work: 32 KB | 16 KB | | |
| MB9AF144MBPMC-G-JNE2 | Main: 256 KB<br>Work: 32 KB | 32 KB | | |
| MB9AF141MBPMC1-G-JNE2 | Main: 64 KB<br>Work: 32 KB | 16 KB | Plastic • LQFP 80-pin (0.65 mm pitch), (LQJ080) | |
| MB9AF142MBPMC1-G-JNE2 | Main: 128 KB<br>Work: 32 KB | 16 KB | | |
| MB9AF144MBPMC1-G-JNE2 | Main: 256 KB<br>Work: 32 KB | 32 KB | | |
| MB9AF141MBBGL-GE1 | Main: 64 KB<br>Work: 32 KB | 16 KB | Plastic • PFBGA 96-pin (0.5 mm pitch), (FDG096) | |
| MB9AF142MBBGL-GE1 | Main: 128 KB<br>Work: 32 KB | 16 KB | | |
| MB9AF144MBBGL-GE1 | Main: 256 KB<br>Work: 32 KB | 32 KB | | |
| MB9AF141NBPMC-G-JNE2 | Main: 64 KB<br>Work: 32 KB | 16 KB | Plastic • LQFP 100-pin (0.5 mm pitch), (LQI100) | |
| MB9AF142NBPMC-G-JNE2 | Main: 128 KB<br>Work: 32 KB | 16 KB | | |
| MB9AF144NBPMC-G-JNE2 | Main: 256 KB<br>Work: 32 KB | 32 KB | | |

| Part number | On-chip Flash memory | On-chip SRAM | Package | Packing |
|---|---|---|---|---|
| MB9AF141NBPQC-G-JNE2 | Main: 64 KB<br>Work: 32 KB | 16 KB | Plastic • QFP 100-pin<br>(0.65 mm pitch),<br>(PQH100) | Tray |
| MB9AF142NBPQC-G-JNE2 | Main: 128 KB<br>Work: 32 KB | 16 KB | | |
| MB9AF144NBPQC-G-JNE2 | Main: 256 KB<br>Work: 32 KB | 32 KB | | |
| MB9AF141NBBGL-GE1 | Main: 64 KB<br>Work: 32 KB | 16 KB | Plastic • PFBGA 112-pin<br>(0.8 mm pitch),<br>(LBC112) | |
| MB9AF142NBBGL-GE1 | Main: 128 KB<br>Work: 32 KB | 16 KB | | |
| MB9AF144NBBGL-GE1 | Main: 256 KB<br>Work: 32 KB | 32 KB | | |

## 14. Package Dimensions

| Package Type | Package Code |
|---|---|
| LQFP 100 | LQI100 |




| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.70 |
| A1 | 0.05 | — | 0.15 |
| b | 0.15 | — | 0.27 |
| c | 0.09 | — | 0.20 |
| D | 16.00 BSC | | |
| D1 | 14.00 BSC | | |
| e | 0.50 BSC | | |
| E | 16.00 BSC | | |
| E1 | 14.00 BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 0.30 | 0.50 | 0.70 |

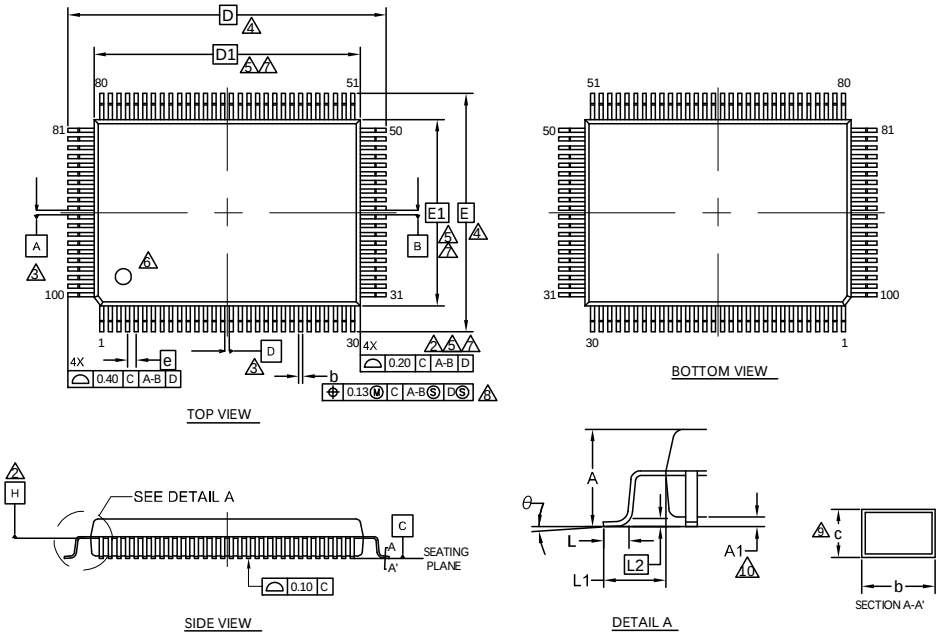
NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

PACKAGE OUTLINE, 100 LEAD LQFP
14.0X14.0X1.7 MM LQI100 REV*A

002-11500 *A

| Package Type | Package Code |
|---|---|
| QFP 100 | PQH100 |




| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | — | — | 3.35 |
| A1 | 0.05 | — | 0.45 |
| b | 0.27 | 0.32 | 0.37 |
| c | 0.11 | — | 0.23 |
| D | 23.90 BSC | | |
| D1 | 20.00 BSC | | |
| e | 0.65 BSC | | |
| E | 17.90 BSC | | |
| E1 | 14.00 BSC | | |
| θ | 0° | — | 8° |
| L | 0.73 | 0.88 | 1.03 |
| L1 | 1.95 REF | | |
| L2 | 0.25 BSC | | |

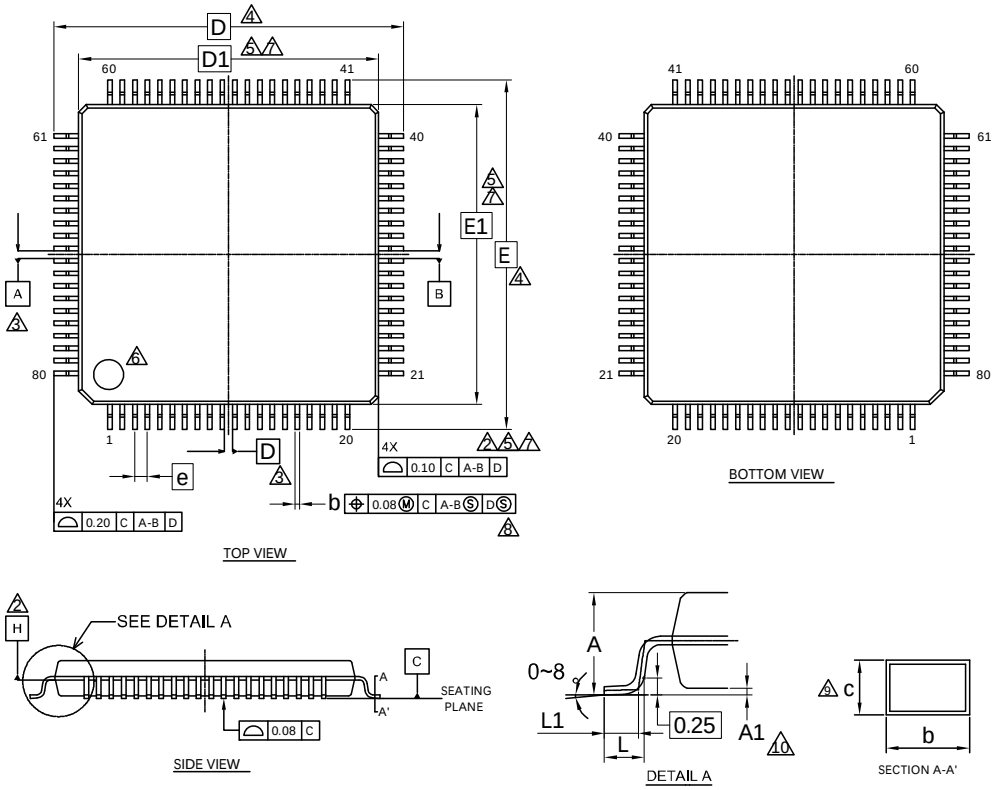
NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

PACKAGE OUTLINE, 100 LEAD QFP
20.00X14.00X3.35 MM PQH100 REV**

002-15156 **

| Package Type | Package Code |
|---|---|
| LQFP 80 | LQH080 |




| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.70 |
| A1 | 0.05 | — | 0.15 |
| b | 0.15 | — | 0.27 |
| c | 0.09 | — | 0.20 |
| D | 14.00 BSC. | | |
| D1 | 12.00 BSC. | | |
| e | 0.50 BSC | | |
| E | 14.00 BSC. | | |
| E1 | 12.00 BSC. | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 0.30 | 0.50 | 0.70 |

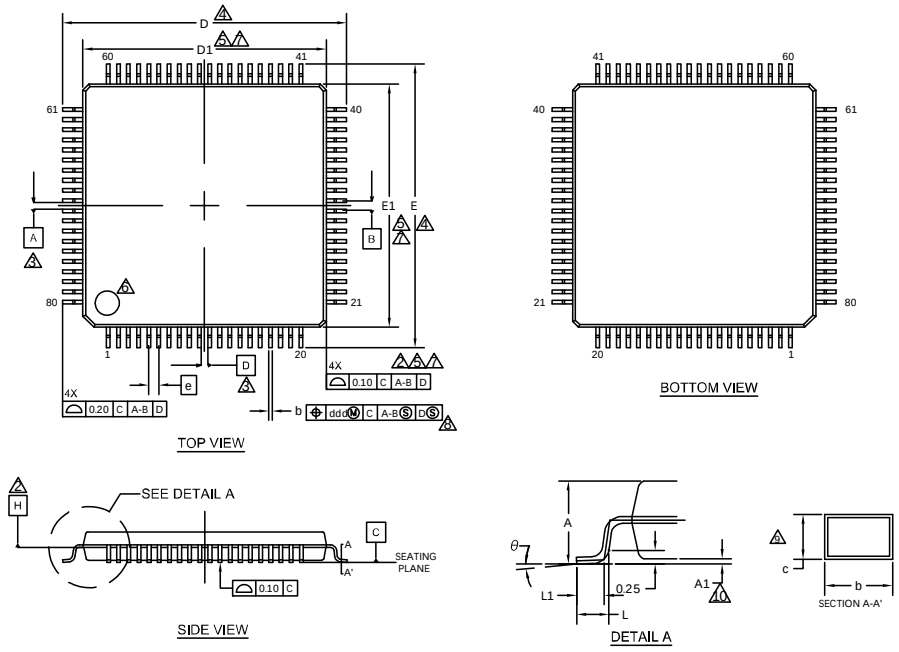
NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

PACKAGE OUTLINE, 80 LEAD LQFP
12.0X12.0X1.7 MM LQH080 Rev **

002-11501 **

| Package Type | Package Code |
|---|---|
| LQFP 80 | LQJ080 |




| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.70 |
| A1 | 0.00 | — | 0.20 |
| b | 0.16 | 0.32 | 0.38 |
| c | 0.09 | — | 0.20 |
| D | 16.00 BSC | | |
| D1 | 14.00 BSC | | |
| e | 0.65 BSC | | |
| E | 16.00 BSC | | |
| E1 | 14.00 BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 0.30 | 0.50 | 0.70 |
| θ | 0° | — | 8° |

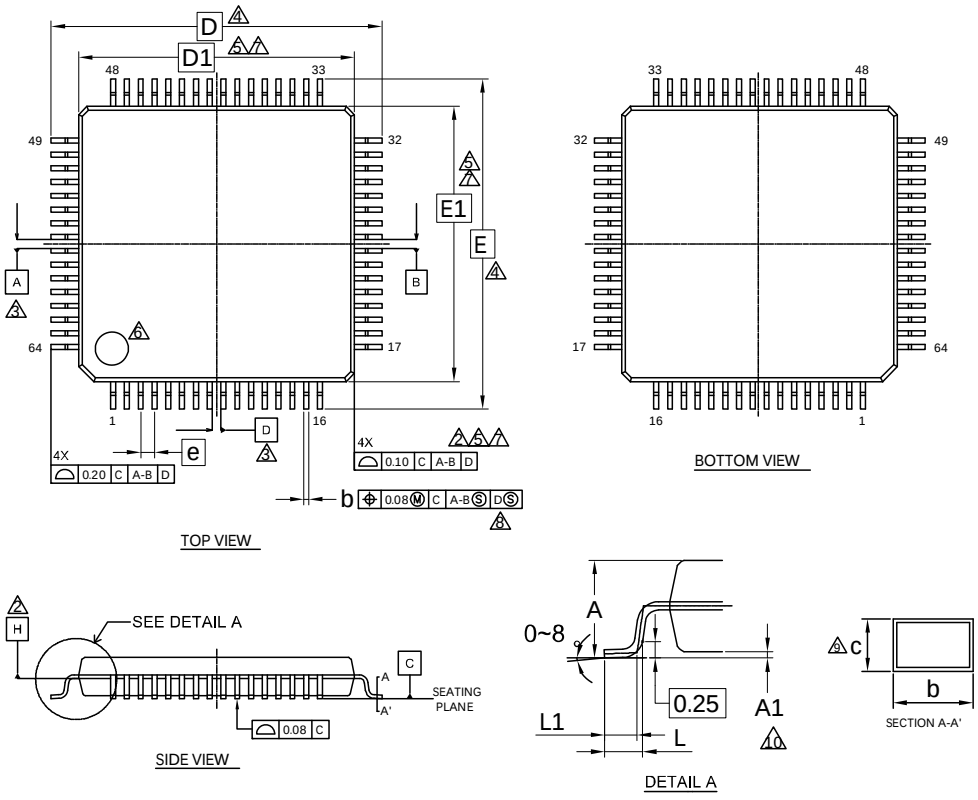
NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

PACKAGE OUTLINE, 80 LEAD LQFP
14.0X14.0X1.7 MM LQJ080 REV**

002-14043 **

| Package Type | Package Code |
|---|---|
| LQFP 64 | LQD064 |




| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.70 |
| A1 | 0.00 | — | 0.20 |
| b | 0.15 | — | 0.27 |
| c | 0.09 | — | 0.20 |
| D | 12.00 BSC. | | |
| D1 | 10.00 BSC. | | |
| e | 0.50 BSC | | |
| E | 12.00 BSC. | | |
| E1 | 10.00 BSC. | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 0.30 | 0.50 | 0.70 |

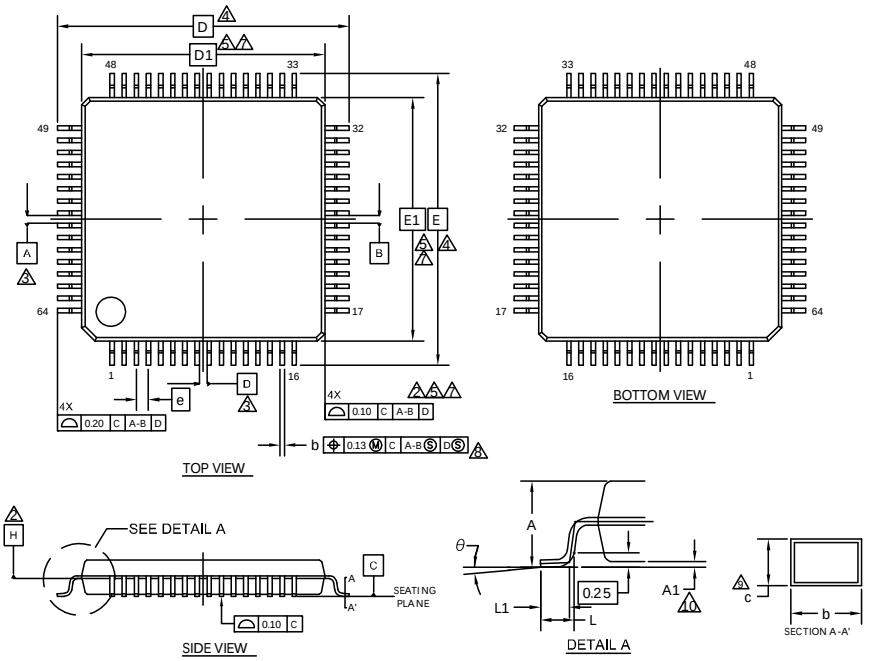
NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

PACKAGE OUTLINE, 64 LEAD LQFP
10.0X10.0X1.7 MM LQD064 Rev**

002-11499 **

| Package Type | Package Code |
|---|---|
| LQFP 64 | LQG064 |




| SYMBOL | DIMENSION | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.70 |
| A1 | 0.00 | — | 0.20 |
| b | 0.27 | 0.32 | 0.37 |
| c | 0.09 | — | 0.20 |
| D | 14.00 BSC | | |
| D1 | 12.00 BSC | | |
| e | 0.65 BSC | | |
| E | 14.00 BSC | | |
| E1 | 12.00 BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 0.30 | 0.50 | 0.70 |
| θ | 0° | — | 8° |

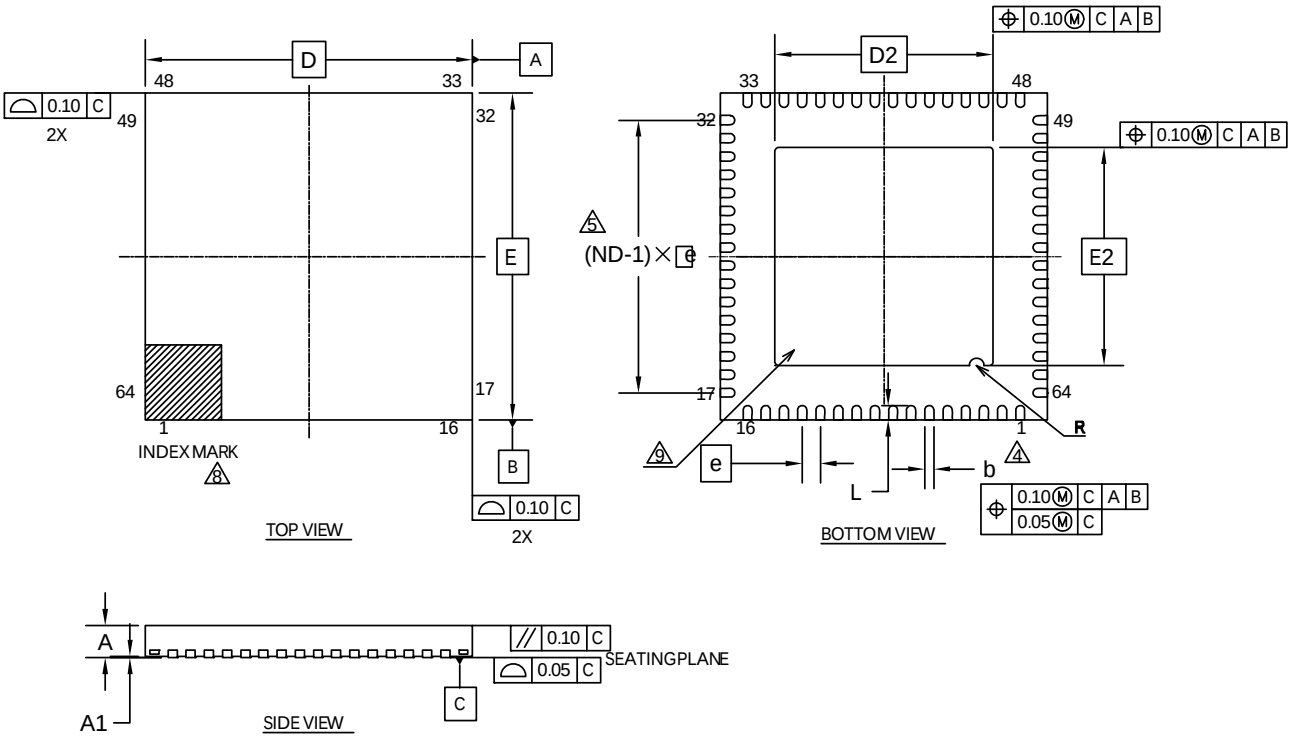
NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS, BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

PACKAGE OUTLINE, 64 LEAD LQFP
12.0X12.0X1.7 MM LQG064 REV**

002-13881 **

| Package Type | Package Code |
|---|---|
| QFN 64 | VNC064 |




| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | — | — | 0.90 |
| A1 | 0.00 | — | 0.05 |
| D | | 9.00 BSC | |
| E | | 9.00 BSC | |
| b | 0.20 | 0.25 | 0.30 |
| D2 | | 6.00 BSC | |
| E2 | | 6.00 BSC | |
| e | | 0.50 BSC | |
| R | | 0.20 REF | |
| L | 0.35 | 0.40 | 0.45 |
| N | | 64 | |
| ND | | 16 | |

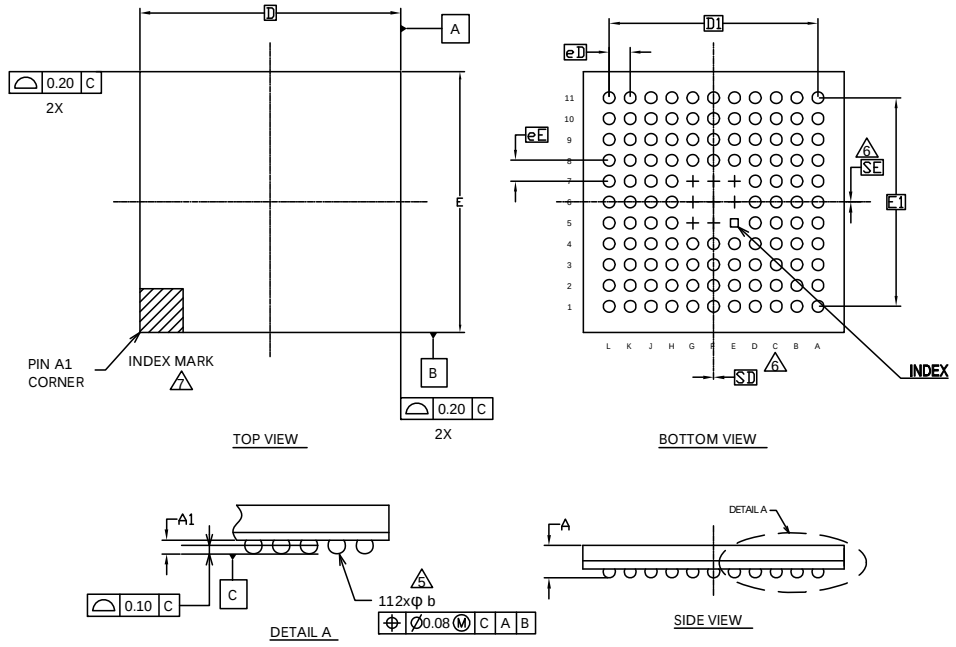
NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING CONFORMS TO ASME Y14.5M-1994.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND REFERS TO THE NUMBER OF TERMINALS ON D SIDE OR E SIDE.
6. MAX. PACKAGE WARPAGE IS 0.05mm.
7. MAXIMUM ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LOCATED WITHIN THE INDICATED ZONE.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

PACKAGE OUTLINE, 64 LEAD QFN
9.0X9.0X0.9 MM VNC064 6.0X6.0 MM EPAD (SAWN) Rev*.*

002-13234 **

| Package Type | Package Code |
|---|---|
| FBGA 112 | LBC112 |




| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | - | - | 1.45 |
| A1 | 0.25 | 0.35 | 0.45 |
| D | 10.00 BSC | | |
| E | 10.00 BSC | | |
| D1 | 8.00 BSC | | |
| E1 | 8.00 BSC | | |
| MD | 11 | | |
| ME | 11 | | |
| N | 112 | | |
| Ø b | 0.35 | 0.45 | 0.55 |
| eD | 0.80 BSC | | |
| eE | 0.80 BSC | | |
| SD | 0.00 | | |
| SE | 0.00 | | |

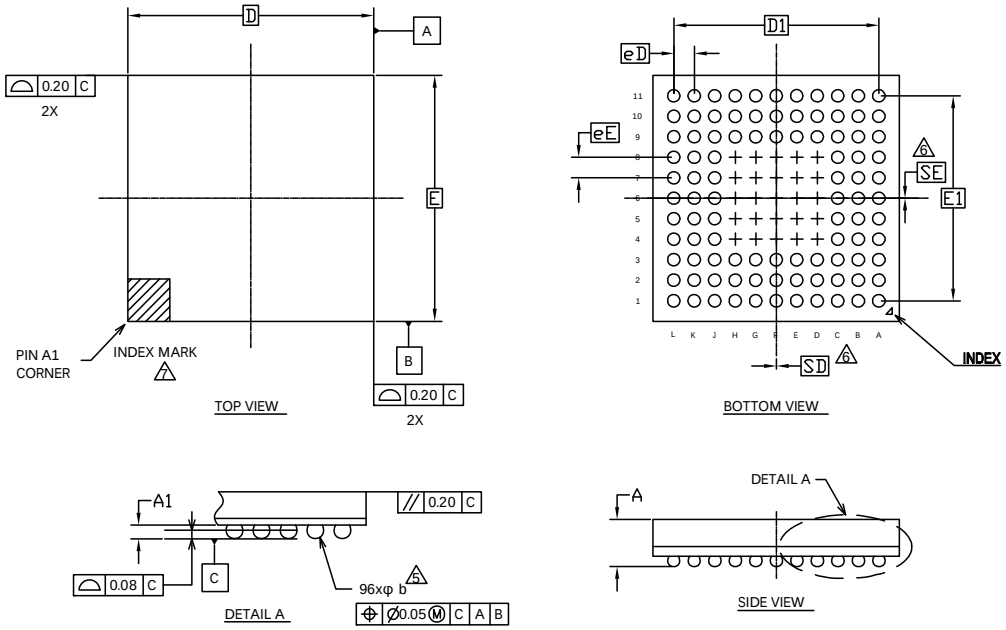
NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATIO N PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.

PACKAGE OUTLINE, 112 BALL FBGA
10.00X10.00X1.45 MM LBC112 REV**

002-13225 **

| Package Type | Package Code |
|---|---|
| FBGA 96 | FDG096 |




| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | - | - | 1.30 |
| A1 | 0.15 | 0.25 | 0.35 |
| D | | 6.00 BSC | |
| E | | 6.00 BSC | |
| D1 | | 5.00 BSC | |
| E1 | | 5.00 BSC | |
| MD | | 11 | |
| ME | | 11 | |
| N | | 96 | |
| Ø b | 0.20 | 0.30 | 0.40 |
| eD | | 0.50 BSC | |
| eE | | 0.50 BSC | |
| SD | | 0.00 | |
| SE | | 0.00 | |

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATIO N PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.

PACKAGE OUTLINE, 96 BALL FBGA
6.0X6.0X1.3 MM FDG096 REV**

002-13224 **

# 15. Errata

This chapter describes the errata for MB9A140N, MB9A140NA and MB9A140MB series. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability.
Contact your local Cypress Sales Representative if you have questions.

## 15.1 Part Numbers Affected

| Part Number |
|---|
| **Initial Revision** |
| MB9AF141NPMC-G-JNE2, MB9AF142NPMC-G-JNE2, MB9AF144NPMC-G-JNE2, MB9AF141NPQC-G-JNE2, MB9AF142NPQC-G-JNE2, MB9AF144NPQC-G-JNE2, MB9AF141NBGL-GE1, MB9AF142NBGL-GE1, MB9AF144NBGL-GE1, MB9AF141MPMC-G-JNE2, MB9AF142MPMC-G-JNE2, MB9AF144MPMC-G-JNE2, MB9AF141MPMC1-G-JNE2, MB9AF142MPMC1-G-JNE2, MB9AF144MPMC1-G-JNE2, MB9AF141MBGL-GE1, MB9AF142MBGL-GE1, MB9AF144MBGL-GE1, MB9AF141LPMC1-G-JNE2, MB9AF142LPMC1-G-JNE2, MB9AF144LPMC1-G-JNE2, MB9AF141LPMC-G-JNE2, MB9AF142LPMC-G-JNE2, MB9AF144LPMC-G-JNE2, MB9AF141LQN-G-AVE2, MB9AF142LQN-G-AVE2, MB9AF144LQN-G-AVE2 |
| Rev. A |
| MB9AF141NAPMC-G-JNE2, MB9AF142NAPMC-G-JNE2, MB9AF144NAPMC-G-JNE2, MB9AF141NAPQC-G-JNE2, MB9AF142NAPQC-G-JNE2, MB9AF144NAPQC-G-JNE2, MB9AF141NABGL-GE1, MB9AF142NABGL-GE1, MB9AF144NABGL-GE1, MB9AF141MAPMC-G-JNE2, MB9AF142MAPMC-G-JNE2, MB9AF144MAPMC-G-JNE2, MB9AF141MAPMC1-G-JNE2, MB9AF142MAPMC1-G-JNE2, MB9AF144MAPMC1-G-JNE2, MB9AF141MABGL-GE1, MB9AF142MABGL-GE1, MB9AF144MABGL-GE1, MB9AF141LAPMC1-G-JNE2, MB9AF142LAPMC1-G-JNE2, MB9AF144LAPMC1-G-JNE2, MB9AF141LAPMC-G-JNE2, MB9AF142LAPMC-G-JNE2, MB9AF144LAPMC-G-JNE2, MB9AF141LAQN-G-AVE2, MB9AF142LAQN-G-AVE2, MB9AF144LAQN-G-AVE2 |
| Rev. B |
| MB9AF141NBPMC-G-JNE2, MB9AF142NBPMC-G-JNE2, MB9AF144NBPMC-G-JNE2, MB9AF141NBPQC-G-JNE2, MB9AF142NBPQC-G-JNE2, MB9AF144NBPQC-G-JNE2, MB9AF141NBBGL-GE1, MB9AF142NBBGL-GE1, MB9AF144NBBGL-GE1, MB9AF141MBPMC-G-JNE2, MB9AF142MBPMC-G-JNE2, MB9AF144MBPMC-G-JNE2, MB9AF141MBPMC1-G-JNE2, MB9AF142MBPMC1-G-JNE2, MB9AF144MBPMC1-G-JNE2, MB9AF141MBBGL-GE1, MB9AF142MBBGL-GE1, MB9AF144MBBGL-GE1, MB9AF141LBPMC1-G-JNE2, MB9AF142LBPMC1-G-JNE2, MB9AF144LBPMC1-G-JNE2, MB9AF141LBPMC-G-JNE2, MB9AF142LBPMC-G-JNE2, MB9AF144LBPMC-G-JNE2, MB9AF141LBQN-G-AVE2, MB9AF142LBQN-G-AVE2, MB9AF144LBQN-G-AVE2 |

## 15.2 Qualification Status

Product Status: In Production − Qual.

## 15.3 Errata Summary

This table defines the errata applicability to available devices.

| Items | Part Number | Silicon Revision | Fix Status |
|---|---|---|---|
| [1] FLASH lower bank read during write | Refer to 15.1 | Initial rev. | Fixed in Rev. A |
| [2] FLASH read during write & erase suspend | Refer to 15.1 | Initial rev. | Fixed in Rev. A |
| [3] Regulator issue | Refer to 15.1 | Initial rev., Rev. A | Fixed in Rev. B |
| [4] HDMI-CEC arbitration lost issue | Refer to 15.1 | Initial rev., Rev. A | Fixed in Rev. B |
| [5] HDMI-CEC polling message issue | Refer to 15.1 | Initial rev., Rev. A , Rev. B | Next silicon is not planned |

**1. FLASH lower bank read during write**

■PROBLEM DEFINITION
During writing (programming) to FLASH memory of an upper bank, FLASH memory of a lower bank could not be read at a specific timing in some operation combinations.

■PARAMETERS AFFECTED
N/A

■TRIGGER CONDITION(S)
This issue may happen when read data or fetch instruction from the FLASH memory lower bank (smaller sector), while a write (program) operation to the FLASH memory upper bank (larger sector) is in progress.

■SCOPE OF IMPACT
Instructions could not be fetched (read) correctly from the lower bank, and then execution of the (corrupted) instructions may cause a hard fault or run-away. If an instruction in RAM reads a data from the lower bank while writing to the upper bank, an incorrect value might be read.

■WORKAROUND
To rewrite the upper bank of FLASH memory, put the write instruction in RAM instead of the lower bank and execute it from the RAM. Do not access the lower bank until the write operation is completed (RDY=1). Especially to avoid a vector fetch from the lower bank of the FLASH memory by an interrupt occurred, the interrupt should be prohibited or the vector address should be set to RAM by the vector table offset register.

■FIX STATUS
This issue was fixed in Rev. A.

**2. FLASH Read during Write & Sector Erase Suspend**

■PROBLEM DEFINITION
When writing is executed during sector erase suspend, FLASH memory could not be read correctly at a specific timing.

■PARAMETERS AFFECTED
N/A

■TRIGGER CONDITION(S)
This issue may happen when read data or fetch instruction from the FLASH memory bank (higher or lower), while a write (program) operation is in progress to the opposite bank which has a sector erase suspended. The following flow could not be executed correctly.

(a) Erase a sector of a bank
(b) Suspend the sector erase operation
(c) Write to a different sector of the bank
(d) Execute an instruction or read data in the opposite bank

■SCOPE OF IMPACT

Instructions could not be fetched (read) correctly, and then execution of the (corrupted) instructions may cause a hard fault or run-away. If an instruction in RAM reads a data from the bank, an incorrect value might be read.

■ WORKAROUND
Do not execute the write operation to a different sector in the same bank at sector erase suspend.

■ FIX STATUS
This issue was fixed in Rev. A.

**3. Regulator issue**

■ PROBLEM DEFINITION
The regulator does not get initialized while internal power-up sequence.

■ PARAMETERS AFFECTED
N/A

■ TRIGGER CONDITION(S)
This issue rarely happens depending on states of internal circuits which the user cannot control.

■ SCOPE OF IMPACT
MCU does not start operation if this issue occurs.

■ WORKAROUND
This error cannot be avoided by any software.

■ FIX STATUS
This issue was fixed in Rev. B.

**4. HDMI-CEC arbitration lost issue**

■ PROBLEM DEFINITION
Large external load on CEC bus may cause arbitration lost.

■ PARAMETERS AFFECTED
N/A

■ TRIGGER CONDITION(S)
The arbitration lost detection mechanism samples outputting signals and determines that arbitration lost occurs if sampled signals do not match the outputting signals. The large external load on the CEC bus increases slew rate of the signals. The increased slew rate makes the mismatch between outputting signals and sampled signals and the mismatch misleads MCU that arbitration lost occurs.

■ SCOPE OF IMPACT
Once the arbitration lost is detected, the CEC aborts the transmission. Any transmission cannot be completed.

■ WORKAROUND

This error cannot be avoided by any software. Reduce the external load.

■ FIX STATUS

This issue was fixed in Rev. B.

**5. HDMI-CEC polling message issue**

■ PROBLEM DEFINITION
Error#1) While MCU sends a Polling Message, it always returns a NACK to a message coming to the MCU from another node.

Error#2) MCU always waits for 7-bit signal free on CEC line before it drives the line even when the last line initiator was another node.

■ PARAMETERS AFFECTED
N/A

■ TRIGGER CONDITION(S)
This error always happens.

■ SCOPE OF IMPACT
MCU does not reply properly to another node.

■WORKAROUND

The software workaround is applied to Error #1.

1. Store 0x0 to SFREE register.
2. Monitor CEC line with GPIO and wait until 1 lasts for the signal free time.
3. Store frame data to TXDATA register and store 0x0F to RCADR1 or RCADR2 register.

It sends a message after 3~4 clocks of 32.768 kHz clock when TXDATA is stored 0x0F.

If the device receives a frame from another node within 2~3 clocks after storing TXDATA, the bus error occurs and if the device receives a frame from another node within 3~4 clocks after storing TXDATA, the arbitration lost occurs. In these cases:

4-A-1. Set RCADR1 or RCADR2 to former value from 0x0F to reply ACK

4-A-2. Return back to step 2 above

If the device receives a frame from another node within 1~2 clocks after storing TXDATA, take these steps.

4-B-1. Monitor CEC line with GPIO after 50us from storing TXDATA

4-B-2. Set TXEN to 1 -> 0 -> 1 immediately when GPIO finds state low on the CEC line

4-B-3. Set RCADR1 or RCADR2 to former value from 0x0F to reply ACK

4-B-4. Return back to step 2 above

For Error #2, there is no software workaround, but signal free time of fixed 7-bit does not violate HDMI-CEC specification. The specification says signal free time must be more than and equals to 5-bit.

■FIX STATUS

The user uses the workaround to avoid the issue. The next silicon fixing the issue is not planned.

## 16. Major Changes

**Spansion Publication Number: DS706-00040**

| Page | Section | Change Results |
|---|---|---|
| Revision 2.0 | | |
| 2 | FEATURE<br>On-chip Memories | Revised the descriptions of [Flash memory]. |
| 5 | Unique ID | Added the descriptions of "Unique ID". |
| 6 | PRODUCT LINEUP<br>Function | |
| 48 | HANDLING DEVICES | Added the descriptions. |
| 53 | MEMORY MAP<br>Memory Map (2) | |
| 58 | PIN STATUS IN EACH CPU STATE<br>List of Pin Status | Revised the Pin status type of "I". |
| 65 | ELECTRICAL CHARACTERISTICS<br>3.DC Characteristics<br>(1) Current rating | Revised the descriptions of Power supply current.<br>Added the "Flash memory write/erase current".<br>Added the footnote. |
| 69 | 4.AC Characteristics<br>(3) Built-in CR Oscillation Characteristics<br>Built-in high-speed CR | Revised the table and the footnote. |
| 73, 74 | (7) External Bus Timing<br>Separate Bus Access Asynchronous<br>SRAM Mode | Revised the table and the figure. |
| 75 | Separate Bus Access Synchronous SRAM Mode | |
| 80, 82,<br>84, 86 | (9) CSIO Timing | Revised the title to "CSIO Timing".<br>Revised the note. |
| 89 | (11) $I^2C$ Timing | Revised the footnote. |
| 92 | 5. 12-bit A/D Converter<br>Electrical Characteristics for the A/D Converter | Revised the parameter.<br>Revised the symbol.<br>Corrected the value. |
| 94 | Definition of 12-bit A/D Converter Terms | Revised the parameter.<br>Revised the symbol. |
| 95 | 6. Low-Voltage Detection Characteristics<br>(1) Low-Voltage Detection Reset | Corrected "Conditions" and "Value" in the table.<br>Added the Item.<br>Added the footnote. |
| 96 | (2) Interrupt of Low-Voltage Detection | Added the Item. |
| Revision 2.1 | | |
| - | - | Company name and layout design change |
| Revision 3.0 | | |
| - | - | Corrected the Series name.<br>MB9A140NA Series → MB9A140NB Series |
| - | - | Corrected the Product name as follows.<br>MB9AF144LB, MB9AF142LB, MB9AF141LB<br>MB9AF144MB, MB9AF142MB, MB9AF141MB<br>MB9AF144NB, MB9AF142NB, MB9AF141NB |
| 2 | FEATURES<br>External Bus Interface | Added the Item.<br>Maximum area size : Up to 256 Mbytes |
| 3 | Multi-function Serial Interface | Corrected the description of "$I^2C$" |
| 6 | PRODUCT LINEUP<br>Function | Added the footnote |
| 51 | BLOCK DIAGRAM | Corrected the figure |
| 52 | MEMORY MAP<br>Memory Map (1) | Corrected the address "External Device Area" |
| 63 | ELECTRICAL CHARACTERISTICS<br>2.Recommended Operating Conditions | Add the footnote |
| 64,65 | 3.DC Characteristics<br>(1)Current rating | Corrected the Condition<br>Delete the minimum value<br>Corrected the remarks<br>Add the footnote |

| Page | Section | Change Results |
|---|---|---|
| 86 | (9)CSIO Timing<br>Synchronous serial (SPI=1, SCINV=1) | Corrected the figure of "MS bit=1" |
| | (9) CSIO Timing<br>External clock(EXT=1):asynchronous only | Corrected the figure |
| 88 | (12)$I^2C$ Timing | Corrected the description as follows.<br>Typical mode → Standard-mode<br>High-speed mode→ Fast-mode |
| 91 | 5.12-bit A/D Converter<br>Electrical Characteristics for<br>the A/D Converter | Corrected the terminal name<br>AN00 ~ AN23 → ANxx<br>Corrected the minimum value of "Sampling time"<br>Corrected the max and min value of "State transition time to operation permission"<br>Corrected the footnote |
| 98 | ORDERING INFORMATON | Corrected the "Part number" |
| Revision 4.0 | | |
| 53 | Memory Map<br>Memory map(2) | Added the summary of Flash memory sector and the note |
| 64 - 66 | Electrical Characteristics<br>3. DC Characteristics<br>(1) Current rating | Changed the table format<br>Added Main Timer mode current<br>Moved A/D Converter Current |
| 67 | Electrical Characteristics<br>3. DC Characteristics<br>(2) Pin Characteristics | Added input leak current of CEC pin at power off. |
| 70 | Electrical Characteristics<br>4. AC Characteristics<br>(4-1) Operating Conditions of Main PLL<br>(4-2) Operating Conditions of Main PLL | Added the figure of Main PLL connection |
| 71 | Electrical Characteristics<br>4. AC Characteristics<br>(6) Power-on Reset Timing | Added Time until releasing Power-on reset<br>Changed the figure of timing |
| 80 - 87 | Electrical Characteristics<br>4. AC Characteristics<br>(9) CSIO/UART Timing | Modified from UART Timing to CSIO/UART Timing<br>Changed from Internal shift clock operation to Master mode<br>Changed from External shift clock operation to Slave mode |
| 92 | Electrical Characteristics<br>5. 12bit A/D Converter | Added the typical value of Integral Nonlinearity, Differential Nonlinearity, Zero transition voltage and Full-scale transition voltage<br>Added Conversion time at AVcc < 2.7V |
| 98 - 101 | Electrical Characteristics<br>8. Return Time from Low-Power Consumption Mode | Added Return Time from Low-Power Consumption Mode |
| 102, 103 | Ordering Information | Changed notation of part number |

**Note: Please see “Document History” about later revised information.**

## Document History

**Document Title: MB9A140NB Series 32-bit ARM® Cortex®-M3 FM3 Microcontroller**

**Document Number: 002-05637**

| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
|---|---|---|---|---|
| ** | – | AKIH | 06/08/2015 | Migrated to Cypress and assigned document number 002-05637.<br>No change to document contents or format. |
| *A | 5206810 | AKIH | 04/07/2016 | Updated to Cypress format. |
| *B | 5534251 | YSKA | 06/01/2017 | Updated “12.4.7 Power-On Reset Timing”. Changed parameter from “Power Supply rise time(Tr)[ms]” to “Power ramp rate(dV/dt)[mV/us]” and added some comments (Page 69)<br>Modified RTC description in “Features, Real-Time Clock(RTC)” as below<br>Changed starting count value from 01 to 00. Deleted “second , or day of the week” in the Interrupt function (Page 3)<br>Added Notes for JTAG (Page 38), Changed “J-TAG” to” JTAG” in “4 List of Pin Functions” (Page 27)<br>Updated Package code and dimensions as follows (Page 8-15, 100-110)<br>FPT-64P-M38 -> LQD064, FPT-64P-M39 -> LQG064,<br>LCC-64P-M24 -> VNC064, FPT-80P-M37 -> LQH080,<br>FPT-80P-M40 -> LQJ080, BGA-96P-M07 -> FDG096,<br>FPT-100P-M23 -> LQI100, FPT-100P-M36 -> PQH100<br>BGA-112P-M04 -> LBC112<br>Added “15. Errata” (Page 111)<br>Add “Analog reference voltage(AVRL)” in “12.2 Recommended Operating Conditions” and “12.6 12-bit A/D Converter”(Page 61, 90)<br>Corrected the following statement<br>Analog port input current → Analog port input leak current<br>in chapter 12.6. 12-bit A/D Converter (Page 90)<br>Added the Baud rate spec in “12.5.10 CSIO/UART Timing”(Page 78, 80, 82, 84) |

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