ISL54225

High-Speed USB 2.0 (480Mbps) Multiplexer with Overvoltage Protection (OVP)

FN7627
Rev 0.00
July 2, 2010

The ISL54225 is a single supply dual 2:1 multiplexer that can operate from a single 2.7V to 5.25V supply. It contains two SPDT (Single Pole/Double Throw) switches configured as a DPDT. The part was designed for switching or routing of USB High-Speed signals and/or USB Full-speed signals in portable battery powered products.

The 6.5Ω switches were specifically designed to pass USB high speed/full speed data signals. They have high bandwidth and low capacitance to pass USB high speed data signals with minimal DISTORTION.

The ISL54225 has OVP circuitry on the D-/D+ COM pins that opens the USB in-line switches when the voltage at these pins exceeds 3.8V (typ) or goes negative by -0.5V (typ). It isolates fault voltages up to +5.25V or down to
-5V from getting passed to the other-side of the switch, thereby protecting the USB transceivers.

The digital logic inputs are 1.8V logic compatible when operated with a 2.7V to 3.6V supply. The ISL54225 has an output enable pin to open all the switches. It can be used to facilitate proper bus disconnect and connection when switching between the USB sources.

The ISL54225 is available in 10 Ld 1.8mmx1.4mm µTQFN and 10 Ld TDFN packages. It operates over a temperature range of -40°C to +85°C.

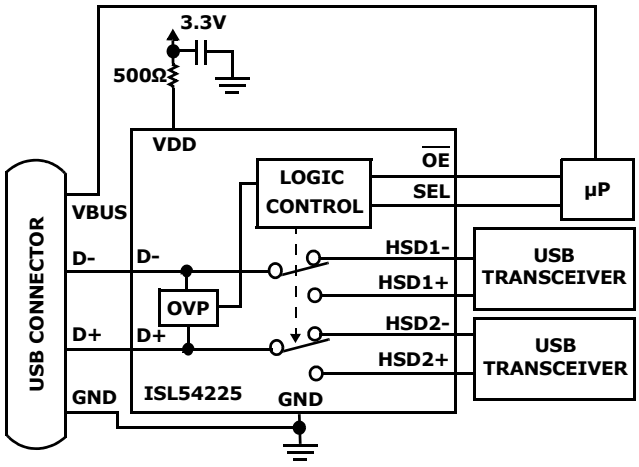
Features

- High-Speed (480Mbps) and Full-Speed (12Mbps) Signaling Capability per USB 2.0
- 1.8V Logic Compatible (2.7V to +3.6V Supply)
- Enable Pin to Open all Switches
- Low Power Mode
- Power OFF Protection
- D-/D+ Pins Overvoltage Protection for +5.25V and -5V Fault Voltages
- -3dB Frequency 780MHz
- Low ON Capacitance @ 240MHz 3.3pF
- Low ON-Resistance 6.5Ω
- Single Supply Operation (V_{DD}) 2.7V to 5.25V
- Available in µTQFN and TDFN Packages
- Pb-Free (RoHS Compliant)
- Compliant with USB 2.0 Short Circuit and Overvoltage Requirements Without Additional External Components

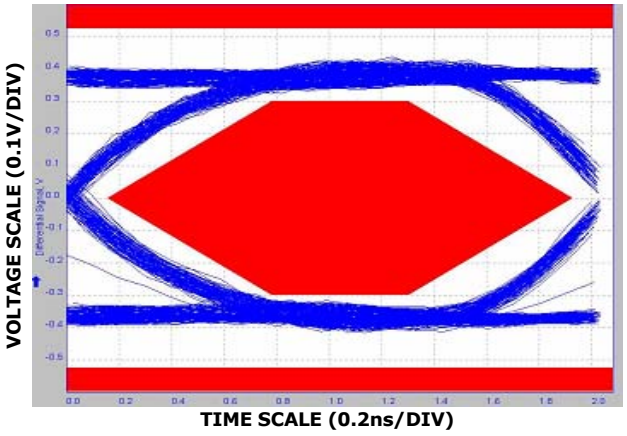
Applications* (see page 16)

- MP3 and other Personal Media Players
- Cellular/Mobile Phones
- PDAs
- Digital Cameras and Camcorders
- USB Switching

Typical Application

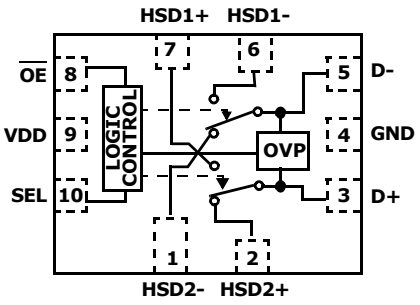


USB 2.0 HS Eye Pattern With Switches in the Signal Path

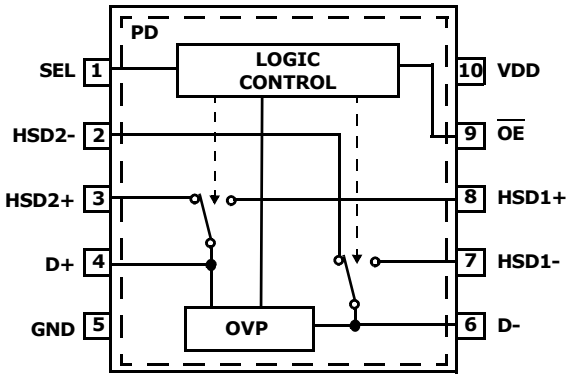


Pin Configuration

ISL54225
(10 LD 1.8X1.4 µTQFN)
TOP VIEW



ISL54225
(10 LD 3X3 TDFN)
TOP VIEW



NOTE:

1. Switches Shown for SEL = Logic "1" and $\overline{OE}$ = Logic "0".

Pin Descriptions

µTQFN	TDFN	PIN NAME	DESCRIPTION
1	2	HSD2-	USB Data Port Channel 2
2	3	HSD2+	USB Data Port Channel 2
3	4	D+	USB Data COM Port
4	5	GND	Ground Connection
5	6	D-	USB Data COM Port
6	7	HSD1-	USB Data Port Channel 1
7	8	HSD1+	USB Data Port Channel 1
8	9	$\overline{OE}$	Bus Switch Enable
9	10	VDD	Power Supply
10	1	SEL	Select Logic Control Input
-	PD	PD	Thermal Pad. Tie to Ground or Float

Truth Table

$\overline{OE}$	SEL	HSD1-, HSD1+	HSD2-, HSD2+	STATE
0	0	ON	OFF	Normal
0	1	OFF	ON	Normal
1	0	OFF	OFF	Low Power
1	1	OFF	OFF	Normal

Logic "0" when ≤ 0.5V, Logic "1" when ≥ 1.4V with a 2.7V to 3.6V Supply.
Note: In Low Power mode there is no persistence checking when in OVP condition.

TABLE 1. USB - OVP POSSIBLE SITUATIONS AND TRIP POINT VOLTAGE

CODEC SUPPLY	SWITCH SUPPLY (V_{DD})	COMs SHORTED TO	PROTECTED	TRIP POINT	
				MIN	MAX
2.7V to 3.3V	2.7V to 5.25V	VBUS	Yes	3.63V	3.95V
2.7V to 3.3V	2.7V to 5.25V	-5V	Yes	-0.76V	-0.29V

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL54225IRUZ-T (Notes 2, 3)	U0	-40 to +85	10 Ld 1.8x1.4mm µTQFN (Tape and Reel)	L10.1.8x1.4A
ISL54225IRUZ-T7A (Notes 2, 3)	U0	-40 to +85	10 Ld 1.8x1.4mm µTQFN (Tape and Reel)	L10.1.8x1.4A
ISL54225IRTZ (Note 4)	4225	-40 to +85	10 Ld 3x3 TDFN	L10.3x3A
ISL54225IRTZ-T (Notes 2, 4)	4225	-40 to +85	10 Ld 3x3 TDFN (Tape and Reel)	L10.3x3A
ISL54225IRTZEVAL1Z	Evaluation Board			

NOTES:

2. Please refer to TB347 for details on reel specifications.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
5. For Moisture Sensitivity Level (MSL), please see device information page for ISL54225. For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings

VDD to GND . . . . . -0.3V to 6.5V
VDD to Dx 10.5V
Dx to HSD1x, HSD2x 8.6V
Input Voltages
HSD2x, HSD1x . . . . . - 0.3V to 6.5V
SEL, $\overline{OE}$ . . . . . -0.3V to 6.5V
Output Voltages
D+, D- . . . . . -5V to 6.5V
Continuous Current (HSD2x, HSD1x) . . . . . ±40mA
Peak Current (HSD2x, HSD1x)
(Pulsed 1ms, 10% Duty Cycle, Max) . . . . . ±100mA
ESD Rating:
Human Body Model (Tested per JESD22-A114-F) . . . >5.5kV
Machine Model (Tested per JESD22-A115-A). . . . . >250V
Charged Device Model (Tested per JESD22-C101-D) . . >2kV
Latch-up Tested per JEDEC; Class II Level A . . . . . at +85°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld µTQFN Package (Note 6, 7)	210	165
10 Ld TDFN Package (Notes 8, 9)	58	22

Maximum Junction Temperature (Plastic Package). . +150°C
Maximum Storage Temperature Range . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Temperature Range . . . . . -40°C to +85°C
V_{DD} Supply Voltage Range . . . . . 2.7V to 5.25V
Logic Control Input Voltage . . . . . 0V to 5.25V
Analog Signal Range
V_{DD} = 2.7V to 5.25V . . . . . 0V to 3.6V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

6. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
7. For θ_{JC}, the "case temp" location is taken at the package top center.
8. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
9. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications - 2.7V to 5.25V Supply

Test Conditions: V_{DD} = +3.3V, GND = 0V, V_{SELH} = 1.4V, V_{SELL} = 0.5V, $V_{\overline{OEH}}$ = 1.4V, $V_{\overline{OEL}}$ = 0.5V, (Note 10), Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 11, 12)	TYP	MAX (Notes 11, 12)	UNITS
ANALOG SWITCH CHARACTERISTICS						
ON-Resistance, r_{ON} (High-Speed)	V_{DD} = 2.7V, SEL = 0.5V or 1.4V, $\overline{OE}$ = 0.5V, I_{Dx} = 17mA, V_{HSD1x} or V_{HSD2x} = 0V to 400mV (see Figure 3, Note 15)	25	-	6.5	8	Ω
		Full	-	-	**10**	Ω
r_{ON} Matching Between Channels, Δr_{ON} (High-Speed)	V_{DD} = 2.7V, SEL = 0.5V or 1.4V, $\overline{OE}$ = 0.5V, I_{Dx} = 17mA, V_{HSD1x} or V_{HSD2x} = Voltage at max r_{ON}, (Notes 14, 15)	25	-	0.2	0.45	Ω
		Full	-	-	**0.5**	Ω
r_{ON} Flatness, $R_{FLAT(ON)}$ (High-Speed)	V_{DD} = 2.7V, SEL = 0.5V or 1.4V, $\overline{OE}$ = 0.5V, I_{Dx} = 17mA, V_{HSD1x} or V_{HSD2x} = 0V to 400mV, (Notes 13, 15)	25	-	0.3	0.5	Ω
		Full	-	-	**1**	Ω
ON-Resistance, r_{ON}	V_{DD} = 3.3V, SEL = 0.5V or 1.4V, $\overline{OE}$ = 0.5V, I_{COMx} = 17mA, V_{D+} or V_{D-}= 3.3V (See Figure 4, Note 15)	25	-	12	20	Ω
		Full	-	-	**25**	Ω
OFF Leakage Current, $I_{HSD1x(OFF)}$	V_{DD} = 5.25V, SEL = V_{DD} and $\overline{OE}$ = V_{DD} or $\overline{OE}$ = 0V, V_{Dx} = 0.3V, 3.3V, V_{HSD1x} = 3.3V, 0.3V, V_{HSD2x} = 0.3V, 3.3V	25	-20	1	20	nA
		Full	**-**	30	**-**	nA
ON Leakage Current, $I_{HSD1x(ON)}$	V_{DD} = 5.25V, SEL = $\overline{OE}$ = 0V, V_{Dx} = 0.3V, 3.3V, V_{HSD1X} = 0.3V, 3.3V, V_{HSD2x} = 3.3V, 0.3V	25	-	2	3	µA
		Full	-	-	**4**	µA
OFF Leakage Current, $I_{HSD2x(OFF)}$	V_{DD} = 5.25V, SEL = $\overline{OE}$ = 0V or $\overline{OE}$ = V_{DD}, V_{Dx} = 3.3V, 0.3V, V_{HSD2x} = 0.3V, 3.3V, V_{HSD1X} = 3.3V, 0.3V	25	-20	1	20	nA
		Full	-	30	-	nA

Electrical Specifications - 2.7V to 5.25V Supply

Test Conditions: V_{DD} = +3.3V, GND = 0V, V_{SELH} = 1.4V, V_{SELL} = 0.5V, $V_{\overline{OE}H}$ = 1.4V, $V_{\overline{OE}L}$ = 0.5V, (Note 10), Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 11, 12)	TYP	MAX (Notes 11, 12)	UNITS
ON Leakage Current, $I_{HSD2x(ON)}$	V_{DD} = 5.25V, SEL = V_{DD}, $\overline{OE}$ = 0V, V_{Dx} = 0.3V, 3.3V, V_{HSD2x} = 0.3V, 3.3V, V_{HSD1x} = 3.3V, 0.3V	25	-	2	3	µA
		Full	-	-	**4**	µA
Power OFF Leakage Current, I_{D+}, I_{D-}	V_{DD} = 0V, V_{D+} = 5.25V, V_{D-}= 5.25V, SEL = $\overline{OE}$ = V_{DD}	25	-	5	13	µA
Power OFF Logic Current, I_{SEL}, $I_{\overline{OE}}$	V_{DD} = 0V, SEL = $\overline{OE}$ = 5.25V	25	-	19	26	µA
Power OFF D+/D- Current, I_{HSDX+}, I_{HSDX-}	V_{DD} = 0V, SEL = $\overline{OE}$ = V_{DD}, V_{HSDX+} = V_{HSDX-} = 5.25V	25	-	0.05	1	µA
OVERVOLTAGE PROTECTION DETECTION						
Positive Fault-Protection Trip Threshold, V_{PFP}	V_{DD} = 2.7V to 5.25V, SEL = 0V or V_{DD}, $\overline{OE}$ = 0V See Table 1 on page 2	25	3.63	3.8	3.95	V
Negative Fault-Protection Trip Threshold, V_{NFP}	V_{DD} = 2.7V to 5.25V, SEL = 0V or V_{DD}, $\overline{OE}$ = 0V See Table 1 on page 2	25	-0.76	-0.5	-0.29	V
OFF Persistence Time Fault Protection Response Time	Negative OVP Response: V_{DD} = 2.7V, SEL = 0V or V_{DD}, $\overline{OE}$ = 0V, V_{Dx} = 0V to -5V, R_L = 15kΩ	25	-	1	-	µs
	Positive OVP Response: V_{DD} = 2.7V, SEL = 0V or V_{DD}, $\overline{OE}$ = 0V, V_{Dx} = 0V to 5.25V, R_L = 15kΩ	25	-	2	-	µs
ON Persistence Time Fault Protection Recovery Time	V_{DD} = 2.7V, SEL = 0V or V_{DD}, $\overline{OE}$ = 0V, V_{Dx} = 0V to 5.25V or 0V to -5V, R_L = 15kΩ	25	-	40	-	µs
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V_{DD} = 3.3V, V_{INPUT} = 3V, R_L = 50Ω, C_L = 50pF (see Figure 1)	25	-	110	-	ns
Turn-OFF Time, t_{OFF}	V_{DD} = 3.3V, V_{INPUT} = 3V, R_L = 50Ω, C_L = 50pF (see Figure 1)	25	-	70	-	ns
Break-Before-Make Time Delay, t_D	V_{DD} = 3.3V, R_L = 50Ω, C_L = 50pF (see Figure 2)	25	-	40	-	ns
Turn-ON Enable Time, t_{ENABLE}	V_{DD} = 3.3V, V_{INPUT} = 3V, R_L = 15kΩ, C_L = 50pF, Time out of All-Off state	25	-	90	-	ns
Turn-OFF Disable Time, $t_{DISABLE}$	V_{DD} = 3.3V, V_{INPUT} = 3V, R_L = 15kΩ, C_L = 50pF, Time into All-Off state, Time is highly dependent on the load (R_L , C_L) time constant.	25	-	120	-	ns
Skew, ($t_{SKEWOUT}$ - t_{SKEWIN})	V_{DD} = 3.3V, SEL = 0V or 3.3V, $\overline{OE}$ = 0V, R_L = 45Ω, C_L = 10pF, t_R = t_F = 500ps at 480Mbps, (Duty Cycle = 50%) (see Figure 6)	25	-	50	-	ps
Rise/Fall Degradation (Propagation Delay), t_{PD}	V_{DD} = 3.3V, SEL = 0V or 3.3V, $\overline{OE}$ = 0V, R_L = 45Ω, C_L = 10pF (see Figure 6)	25	-	250	-	ps
Crosstalk	V_{DD} = 3.3V, R_L = 50Ω, f = 240MHz (see Figure 5)	25	-	-32	-	dB
OFF-Isolation	V_{DD} = 3.3V, $\overline{OE}$ = 3.3V, R_L = 50Ω, f = 240MHz	25	-	-30	-	dB
-3dB Bandwidth	Signal = 0dBm, 0.2VDC offset, R_L = 50Ω	25	-	780	-	MHz
OFF Capacitance, C_{HSxOFF}	f = 1MHz, V_{DD} = 3.3V, SEL = 0V or 3.3V, $\overline{OE}$ = V_{DD} (see Figure 4)	25	-	2.5	-	pF
COM ON Capacitance, $C_{DX(ON)}$	f = 1MHz, V_{DD} = 3.3V, SEL = 0V or 3.3V, $\overline{OE}$ = 0V (see Figure 4)	25	-	5.4	-	pF

Electrical Specifications - 2.7V to 5.25V Supply

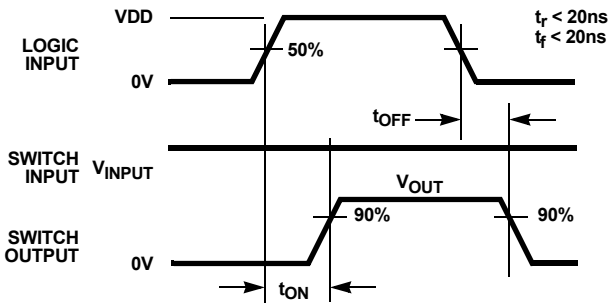
Test Conditions: V_{DD} = +3.3V, GND = 0V, V_{SELH} = 1.4V, V_{SELL} = 0.5V, $V_{\overline{OEH}}$ = 1.4V, $V_{\overline{OEL}}$ = 0.5V, (Note 10), Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 11, 12)	TYP	MAX (Notes 11, 12)	UNITS
COM ON Capacitance, $C_{DX(ON)}$	f = 240MHz, V_{DD} = 3.3V, SEL = 0V or 3.3V, $\overline{OE}$ = 0V (see Figure 4)	25	-	3.3	-	pF
POWER SUPPLY CHARACTERISTICS						
Power Supply Range, V_{DD}		Full	**2.7**		**5.25**	V
Positive Supply Current, I_{DD}	V_{DD} = 5.25V, SEL = 0V or V_{DD}, $\overline{OE}$ = 0V	25	-	45	58	µA
		Full	-	-	**66**	µA
Positive Supply Current, I_{DD}	V_{DD} = 3.6V, SEL = 0V or V_{DD}, $\overline{OE}$ = 0V	25	-	23	30	µA
		Full	-	-	**35**	µA
Positive Supply Current, I_{DD} (Low Power State)	V_{DD} = 3.6V, SEL = 0V, $\overline{OE}$ = V_{DD}	25	-	5	6	µA
		Full	-	-	**10**	µA
Positive Supply Current, I_{DD}	V_{DD} = 4.3V, SEL = 2.6V, $\overline{OE}$ = 0V or 2.6V	25	-	35	45	µA
		Full	-	-	**52**	µA
Positive Supply Current, I_{DD}	V_{DD} = 3.6V, SEL = 1.4V, $\overline{OE}$ = 0V or 1.4V	25	-	25	32	µA
		Full	-	-	**38**	µA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{SELL}, $V_{\overline{OEL}}$	V_{DD} = 2.7V to 3.6V	Full	-	-	**0.5**	V
Input Voltage High, V_{SELH}, $V_{\overline{OEH}}$	V_{DD} = 2.7V to 3.6V	Full	**1.4**	-	**5.25**	V
Input Voltage Low, V_{SELL}, $V_{\overline{OEL}}$	V_{DD} = 3.7V to 4.2V	Full	-	-	**0.7**	V
Input Voltage High, V_{SELH}, $V_{\overline{OEH}}$	V_{DD} = 3.7V to 4.2	Full	**1.7**	-	**5.25**	V
Input Voltage Low, V_{SELL}, $V_{\overline{OEL}}$	V_{DD} = 4.3V to 5.25V	Full	-	-	**0.8**	V
Input Voltage High, V_{SELH}, $V_{\overline{OEH}}$	V_{DD} = 4.3V to 5.25V	Full	**2.0**	-	**5.25**	V
Input Current, I_{SELL}, $I_{\overline{OEH}}$	V_{DD} = 5.25V, SEL = 0V, $\overline{OE}$ = 5.25V	Full	-	3.3	-	nA
Input Current, I_{SELH}	V_{DD} = 5.25V, SEL = 5.25V, 4MΩ pull-down resistor	Full	-	1.4	-	µA
Input Current, $I_{\overline{OEL}}$	V_{DD} = 5.25V, $\overline{OE}$ = 0V, 4MΩ pull-up resistor	Full	-	1.4	-	µA

NOTES:

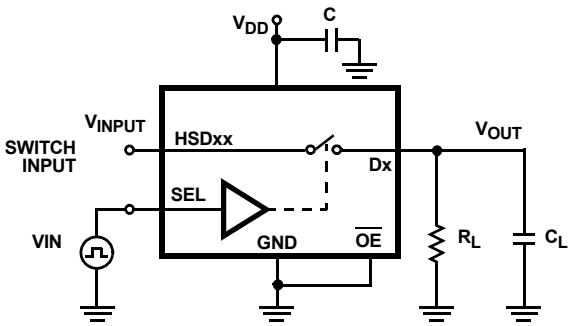
10. V_{LOGIC} = Input voltage to perform proper function.
11. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
12. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
13. Flatness is defined as the difference between maximum and minimum value of ON-resistance over the specified analog signal range.
14. r_{ON} matching between channels is calculated by subtracting the channel with the highest max r_{ON} value from the channel with lowest max r_{ON} value, between HSD2+ and HSD2- or between HSD1+ and HSD1-.
15. Limits established by characterization and are not production tested.

Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. MEASUREMENT POINTS

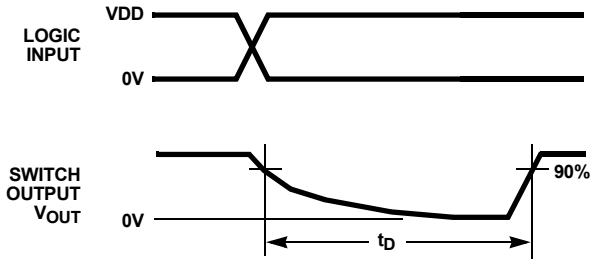


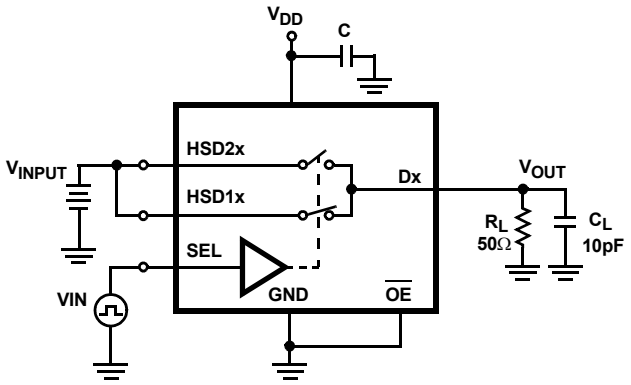
Repeat test for all switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(INPUT)} \frac{R_L}{R_L + r_{ON}}$$

FIGURE 1B. TEST CIRCUIT

FIGURE 1. SWITCHING TIMES



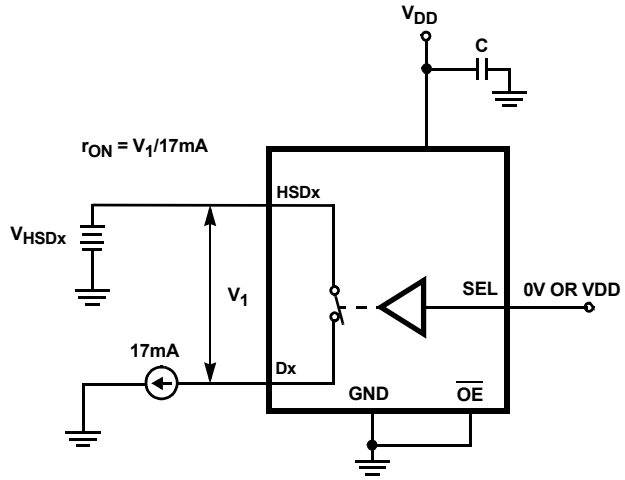


Repeat test for all switches. C_L includes fixture and stray capacitance.

FIGURE 2A. MEASUREMENT POINTS

FIGURE 2B. TEST CIRCUIT

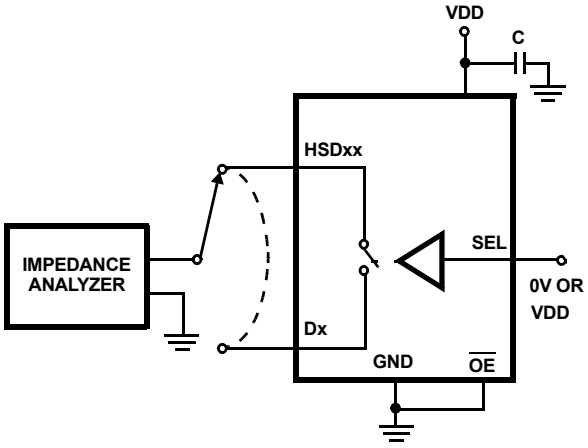
FIGURE 2. BREAK-BEFORE-MAKE TIME



Repeat test for all switches.

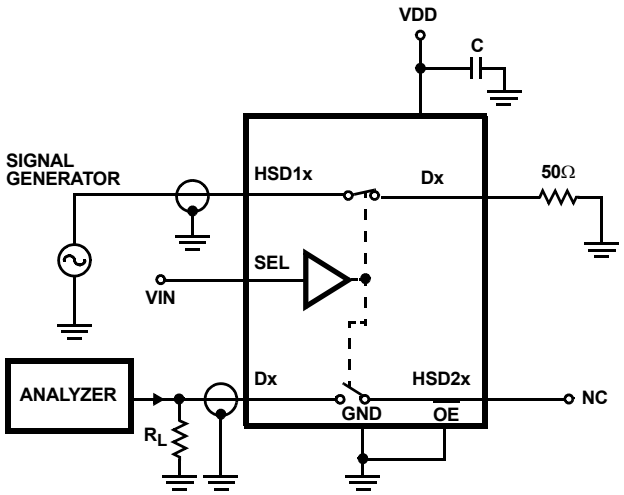
FIGURE 3. r_{ON} TEST CIRCUIT

Test Circuits and Waveforms (Continued)



Repeat test for all switches.

FIGURE 4. CAPACITANCE TEST CIRCUIT



Signal direction through switch is reversed, worst case values are recorded. Repeat test for all switches.

FIGURE 5. CROSSTALK TEST CIRCUIT

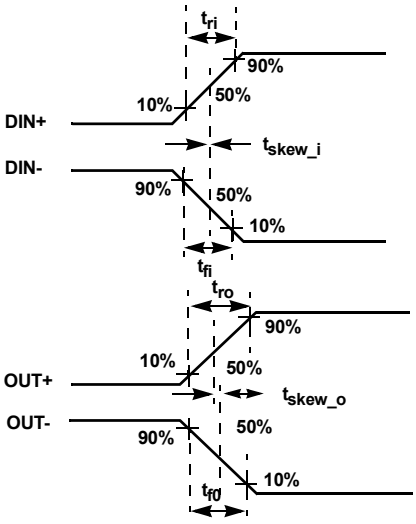
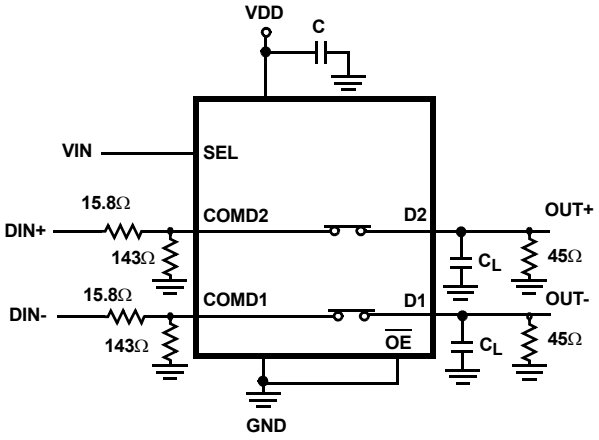


FIGURE 6A. MEASUREMENT POINTS



|tro - tri| Delay Due to Switch for Rising Input and Rising Output Signals.

|tfo - tfi| Delay Due to Switch for Falling Input and Falling Output Signals.

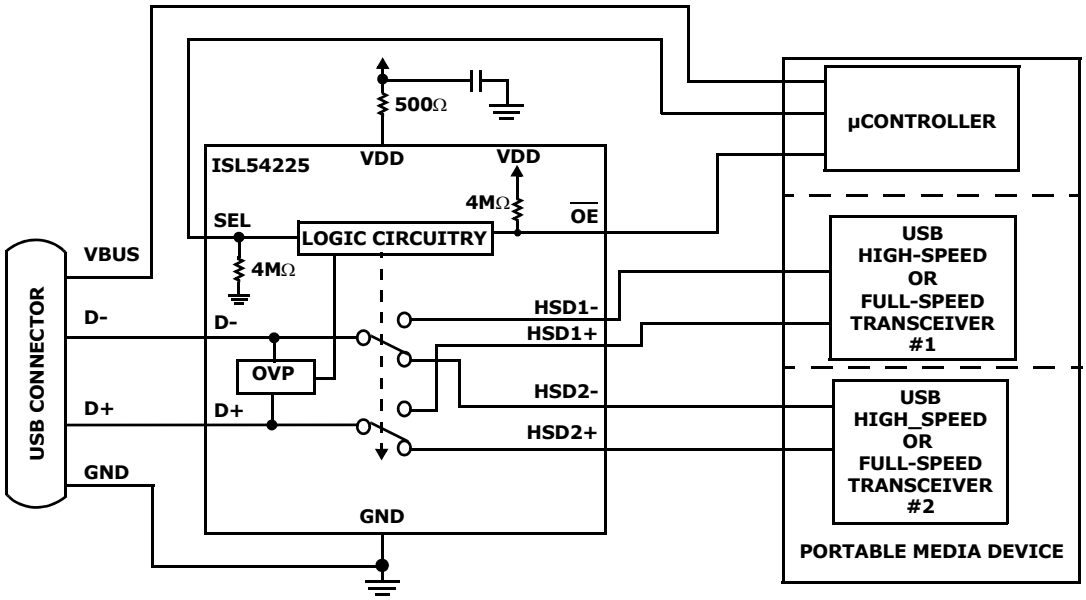
|tskew_0| Change in Skew through the Switch for Output Signals.

|tskew_i| Change in Skew through the Switch for Input Signals.

FIGURE 6B. TEST CIRCUIT

FIGURE 6. SKEW TEST

Application Block Diagram



Detailed Description

The ISL54225 device is a dual single pole/double throw (SPDT) analog switch configured as a DPDT that operates from a single DC power supply in the range of 2.7V to 5.25V.

It was designed to function as a dual 2-to-1 multiplexer to select between two USB high-speed differential data signals in portable battery powered products. It is offered in a TDFN, and a small µTQFN packages for use in MP3 players, cameras, PDAs, cellphones, and other personal media players. The device has an enable pin to open all switches and put the part in a low power state.

The part contains special overvoltage detection and protection (OVP) circuitry on the D-/D+ COM pins. This circuitry acts to open the USB in-line switches when the part senses a voltage on the COM pins that is >3.8V (typ) or < -0.5V (typ). It isolates voltages up to 5.25V and down to -5V from getting through to the other side of the switch to protect the USB transceivers connected at the signal pins (HSD1-, HSD1+, HSD2-, HSD2+).

The part consists of four 6.5Ω high speed (HSx) switches. These switches have high bandwidth and low capacitance to pass USB high-speed (480Mbps) differential data signals with minimal edge and phase distortion. They can also swing from 0V to 3.6V to pass USB full speed (12Mbps) differential data signals with minimal distortion.

The ISL54225 was designed for MP3 players, cameras, cellphones, and other personal media player applications that have multiple high-speed or full-speed transceivers sections and need to multiplex between these USB sources to a single USB host (computer). A typical application block diagram of this functionality is previously shown.

A detailed description of the HS switches is provided in the following section.

High-Speed (HSx) Data Switches

The HSx switches (HSD1-, HSD1+, HSD2-, HSD2+) are bi-directional switches that can pass USB high-speed and USB full-speed signals when V_{DD} is in the range of 2.7V to 5.25V.

When powered with a 2.7V supply, these switches have a nominal r_{ON} of 6.5Ω over the signal range of 0V to 400mV with a r_{ON} flatness of 0.3Ω. The r_{ON} matching between the HSD1x switches and HSD2x switches over this signal range is only 0.2Ω, ensuring minimal impact by the switches to USB high-speed signal transitions. As the signal level increases, the r_{ON} switch resistance increases. At signal level of 3.3V, the switch resistance is nominally 12Ω. See Figures 9, 10, 11, 12, 13, 14, 15 and 16 in the "Typical Performance Curves" beginning on page 12.

The HSx switches were specifically designed to pass USB 2.0 high-speed (480Mbps) differential signals in the range of 0V to 400mV. They have low capacitance and high bandwidth to pass the USB high-speed signals with minimum edge and phase distortion to meet USB 2.0 high speed signal quality specifications. See Figure 21 in the "Typical Performance Curves" on page 14 for USB High-speed Eye Pattern taken with switch in the signal path.

The HSx switches can also pass USB full-speed signals (12Mbps) with minimal distortion and meet all the USB requirements for USB 2.0 full-speed signaling. See Figure 22 in the "Typical Performance Curves" on page 14 for USB Full-speed Eye Pattern taken with switch in the signal path.

The HS1 channel switches are active (turned ON) whenever the SEL voltage is logic "0"(Low) and the $\overline{OE}$ voltage is logic "0"(Low).

The HS2 channel switches are active (turned ON) whenever the SEL voltage is logic "1" (High) and the $\overline{OE}$ voltage is logic "0" (Low).

OVERVOLTAGE PROTECTION (OVP)

The maximum normal operating signal range for the HSx switches is from 0V to 3.6V. For normal operation, the signal voltage should not be allowed to exceed these voltage levels or go below ground by more than -0.3V.

However, in the event that a positive voltage > 3.8V (typ) to 5.25V, such as the USB 5V V_{BUS} voltage, gets shorted to one or both of the COM+ and COM- pins or a negative voltage < -0.5V (typ) to -5V gets shorted to one or both of the COM pins, the ISL54225 has OVP circuitry to detect the overvoltage condition and open the SPDT switches to prevent damage to the USB down-stream transceivers connected at the signal pins (HS1D-, HS1D+, HS2D-, HS2D+).

The OVP and power-off protection circuitry allows the COM pins (D-, D+) to be driven up to 5.25V while the V_{DD} supply voltage is in the range of 0V to 5.25V. In this condition, the part draws < 100µA of I_{COMx} and I_{DD} current and causes no stress to the IC. In addition, the SPDT switches are OFF and the fault voltage is isolated from the other side of the switch.

External V_{DD} Series Resistor to Limit I_{DD} Current during Negative OVP Condition

A 100Ω to 1kΩ resistor in series with the VDD pin (see Figure 7) is required to limit the IDD current draw from the system power supply rail during a negative OVP fault event.

With a negative -5V fault voltage at both COM pins, the graph in Figure 8 shows the IDD current draw for different external resistor values for supply voltages of 2.7V, 3.6V, and 5.25V. With a 500Ω resistor, the current draw is limited to around 5mA. When the negative fault voltage is removed, the I_{DD} current will return to it's normal operation current of 25µA to 45µA.

The series resistor also provides improved ESD and latch-up immunity. During an overvoltage transient event (such as occurs during system level IEC 61000 ESD testing), substrate currents can be generated in the IC that can trigger parasitic SCR structures to turn ON, creating a low impedance path from the VDD power supply to ground. This will result in a significant amount of current flow in the IC, which can potentially create a latch-up state or permanently damage the IC. The external VDD resistor limits the current during this over-stress situation and has been found to prevent latch-up or destructive damage for many overvoltage transient events.

Under normal operation, the low microamp I_{DD} current of the IC produces an insignificant voltage drop across the series resistor resulting in no impact to switch operation or performance.

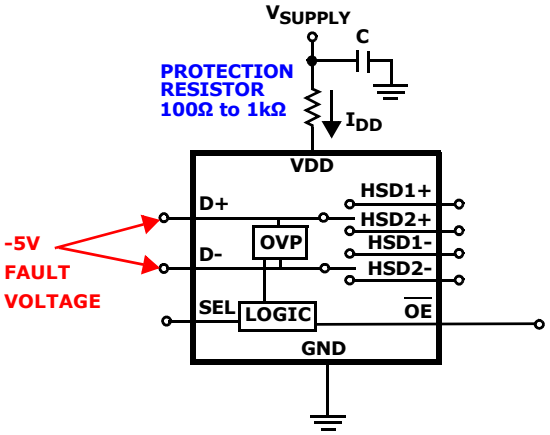


FIGURE 7. VDD SERIES RESISTOR TO LIMIT IDD CURRENT DURING NEGATIVE OVP AND FOR ENHANCED ESD AND LATCH-UP IMMUNITY

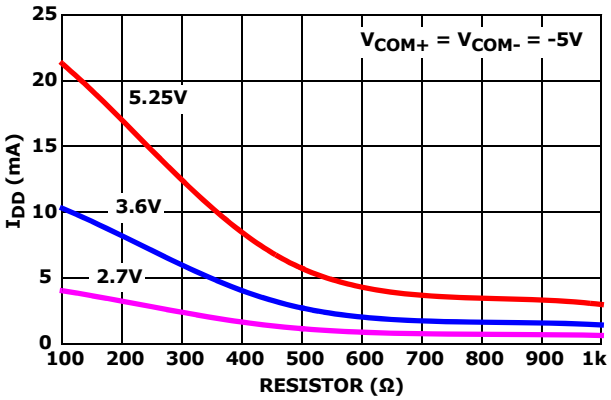


FIGURE 8. NEGATIVE OVP IDD CURRENT vs RESISTOR VALUE vs V_{SUPPLY}

ISL54225 Operation

The following will discuss using the ISL54225 shown in the "Application Block Diagram" on page 9.

POWER

The power supply connected at the VDD pin provides the DC bias voltage required by the ISL54225 part for proper operation. The ISL54225 can be operated with a V_{DD} voltage in the range of 2.7V to 5.25V.

For lowest power consumption you should use the lowest V_{DD} supply.

A 0.01µF or 0.1µF decoupling capacitor should be connected from the VDD pin to ground to filter out any power supply noise from entering the part. The capacitor should be located as close to the VDD pin as possible.

In a typical application, V_{DD} will be in the range of 2.8V to 4.3V and will be connected to the battery or LDO of the portable media device.

LOGIC CONTROL

The state of the ISL54225 device is determined by the voltage at the SEL pin and the $\overline{OE}$ pin. SEL is only active when the $\overline{OE}$ pin is logic "0" (Low). Refer to "Truth Table" on page 2.

The ISL54225 logic pins are designed to minimize current consumption when the logic control voltage is lower than the V_{DD} supply voltage. With V_{DD} = 3.6V and logic pins at 1.4V, the part typically draws only 25µA. With V_{DD} = 4.3V and logic pins at 2.6V, the part typically draws only 35µA. Driving the logic pins to the V_{DD} supply rail minimizes power consumption.

The SEL pin and $\overline{OE}$ pin have special circuitry that allows them to be driven with a voltage higher than the V_{DD} supply voltage. These pins can be driven up to 5.25V with a V_{DD} supply in the range of 2.7V to 5.25V.

The SEL pin is internally pulled low through 4MΩ resistor to ground. The $\overline{OE}$ pin is internally pulled high through a 4MΩ resistor to VDD. These pins can be tri-stated by a µProcessor or left floating.

Logic Control Voltage Levels

TABLE 2. LOGIC CONTROL VOLTAGE LEVELS

V_{DD} SUPPLY RANGE	LOGIC = "0" (LOW)		LOGIC = "1" (HIGH)	
	$\overline{OE}$	SEL	$\overline{OE}$	SEL
2.7V to 3.6V	≤ 0.5V	≤ 0.5V or floating	≥1.4V or floating	≥1.4V
3.7V to 4.2V	≤ 0.7V	≤ 0.7V or floating	≥1.7V or floating	≥1.7V
4.3V to 5.25V	≤ 0.8V	≤ 0.8V or floating	≥2.0V or floating	≥2.0V

HSD1 USB Channel

If the SEL pin = Logic "0" and the $\overline{OE}$ pin = Logic "0", high-speed Channel 1 will be ON. The HSD1- and HSD1+ switches are ON and the HSD2- and HSD2+ switches are OFF (high impedance).

When a computer or USB hub is plugged into the common USB connector and Channel 1 is active, a link will be established between the USB 1 transceiver section of the media player and the computer. The device will be able to transmit and receive data from the computer.

HSD2 USB Channel

If the SEL pin = Logic "1" and the $\overline{OE}$ pin = Logic "0", high-speed Channel 2 will be ON. The HSD2- and HSD2+ switches are ON and the HSD1- and HSD1+ switches are OFF (high impedance).

When a USB cable from a computer or USB hub is connected at the common USB connector and the part has Channel 2 active, a link will be established between the USB 2 driver section of the media player and the computer. The device will be able to transmit and receive data from the computer.

All Switches OFF Mode

If the SEL pin = Logic "0" and the $\overline{OE}$ pin = Logic "1", all of the switches will turn OFF (high impedance) and the part will be put in a low power mode. In this mode, the part draws only 10µA (max) of current across the operating temperature range. In the low power mode, the persistence checking of the OVP circuitry is de-activated.

If the SEL pin = Logic "1" and the $\overline{OE}$ pin = Logic "1", all of the switches will turn OFF (high impedance). In this state the complete OTV circuitry is activated.

The all OFF state can be used to switch between the two USB sections of the media player. When disconnecting from one USB device to the other USB device, you can momentarily put the ISL54225 switch in the "all off" state in order to get the computer to disconnect from the one device so it can properly connect to the other USB device when that channel is turned ON.

Whenever the ISL54225 senses a fault condition on the COM pins, all switches will be turned OFF regardless of the voltage levels at the SEL and $\overline{OE}$ pins.

USB 2.0 V_{BUS} Short Requirements

The USB specification in section 7.1.1 states a USB device must be able to withstand a V_{BUS} short (4.4V to 5.25V) or a -1V short to the D+ or D- signal lines when the device is either powered off or powered on for at least 24 hours.

The ISL54225 part has special power-off protection and OVP detection circuitry to meet these short circuit requirements. This circuitry allows the ISL54225 to provide protection to the USB down-stream transceivers connected at its signal pins (HS1D-, HS1D+, HS2D-, HS2D+) to meet the USB specification short circuit requirements.

The power-off protection and OVP circuitry allows the COM pins (D-, D+) to be driven up to 5.25V or down to -5V while the V_{DD} supply voltage is in the range of 0V to 5.25V. In these overvoltage conditions with a 500Ω external VDD resistor, the part draws < 55µA of current into the COM pins and causes no stress/damage to the IC. In addition, all switches are OFF and the shorted V_{BUS} voltage will be isolated from getting through to the other side of the switch channels, thereby protecting the USB transceivers.

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified

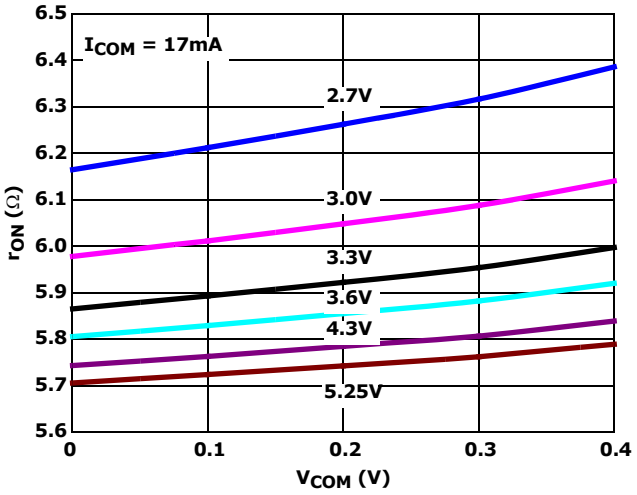


FIGURE 9. ON-RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE

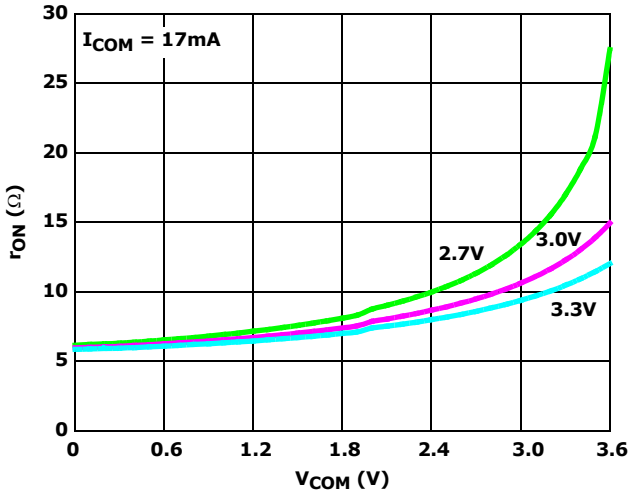


FIGURE 10. ON-RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE

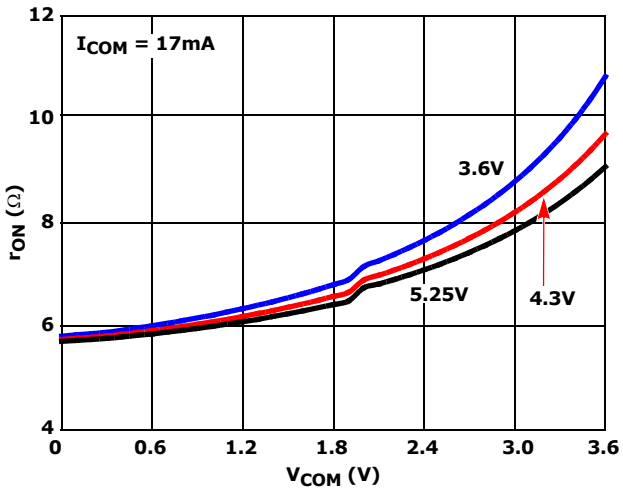


FIGURE 11. ON-RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE

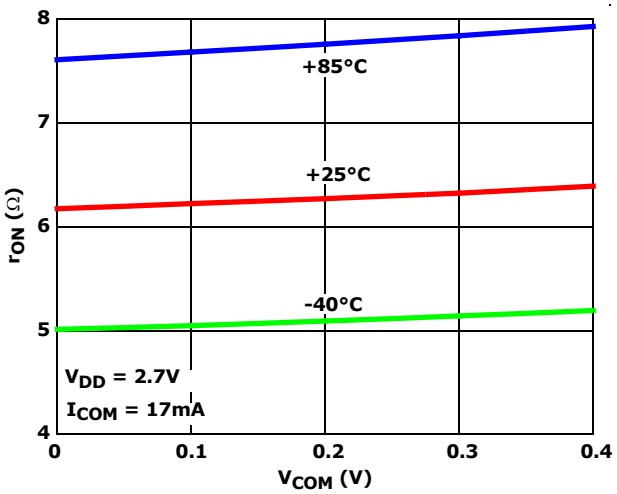


FIGURE 12. ON-RESISTANCE vs SWITCH VOLTAGE

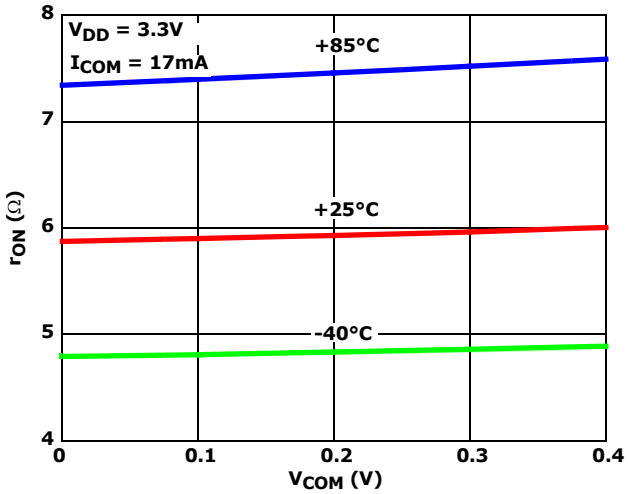


FIGURE 13. ON-RESISTANCE vs SWITCH VOLTAGE

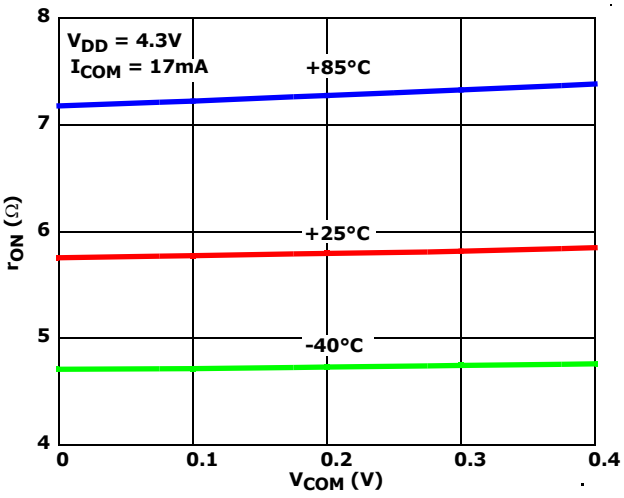


FIGURE 14. ON-RESISTANCE vs SWITCH VOLTAGE

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

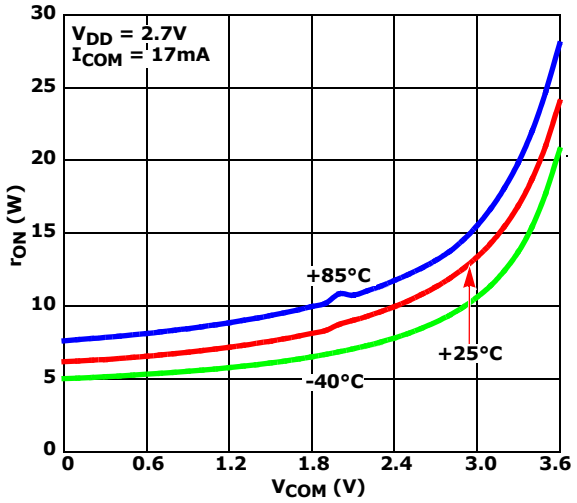


FIGURE 15. ON-RESISTANCE vs SWITCH VOLTAGE

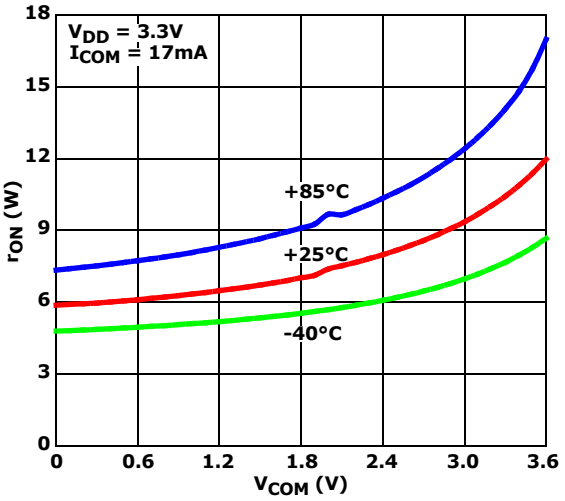


FIGURE 16. ON-RESISTANCE vs SWITCH VOLTAGE

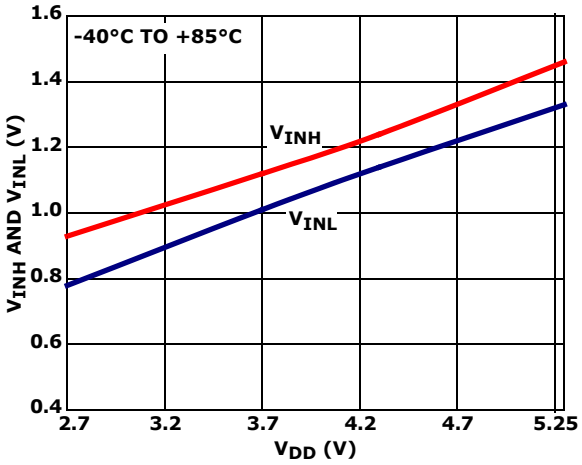


FIGURE 17. DIGITAL SWITCHING POINT vs SUPPLY VOLTAGE

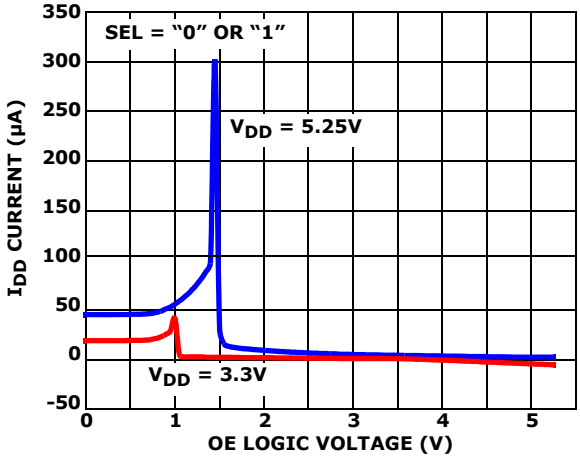


FIGURE 18. I_{DD} vs OE LOGIC VOLTAGE vs V_{DD}

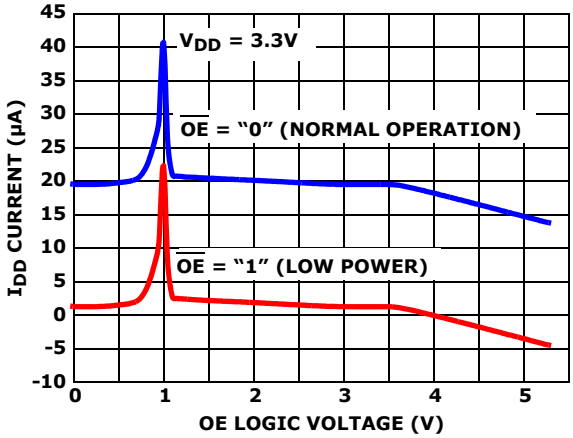


FIGURE 19. IDD vs SEL LOGIC VOLTAGE vs $\overline{OE}$ STATE

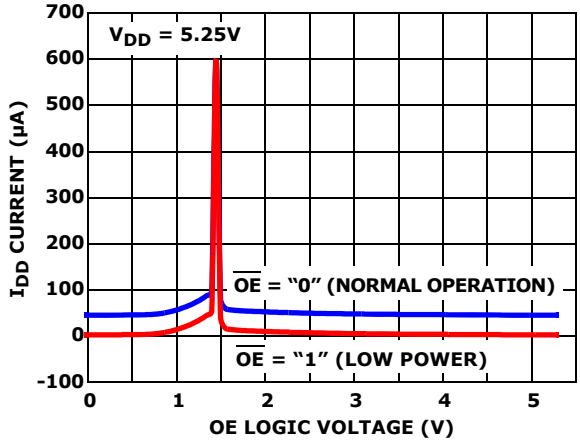


FIGURE 20. IDD vs SEL LOGIC VOLTAGE vs $\overline{OE}$ STATE

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

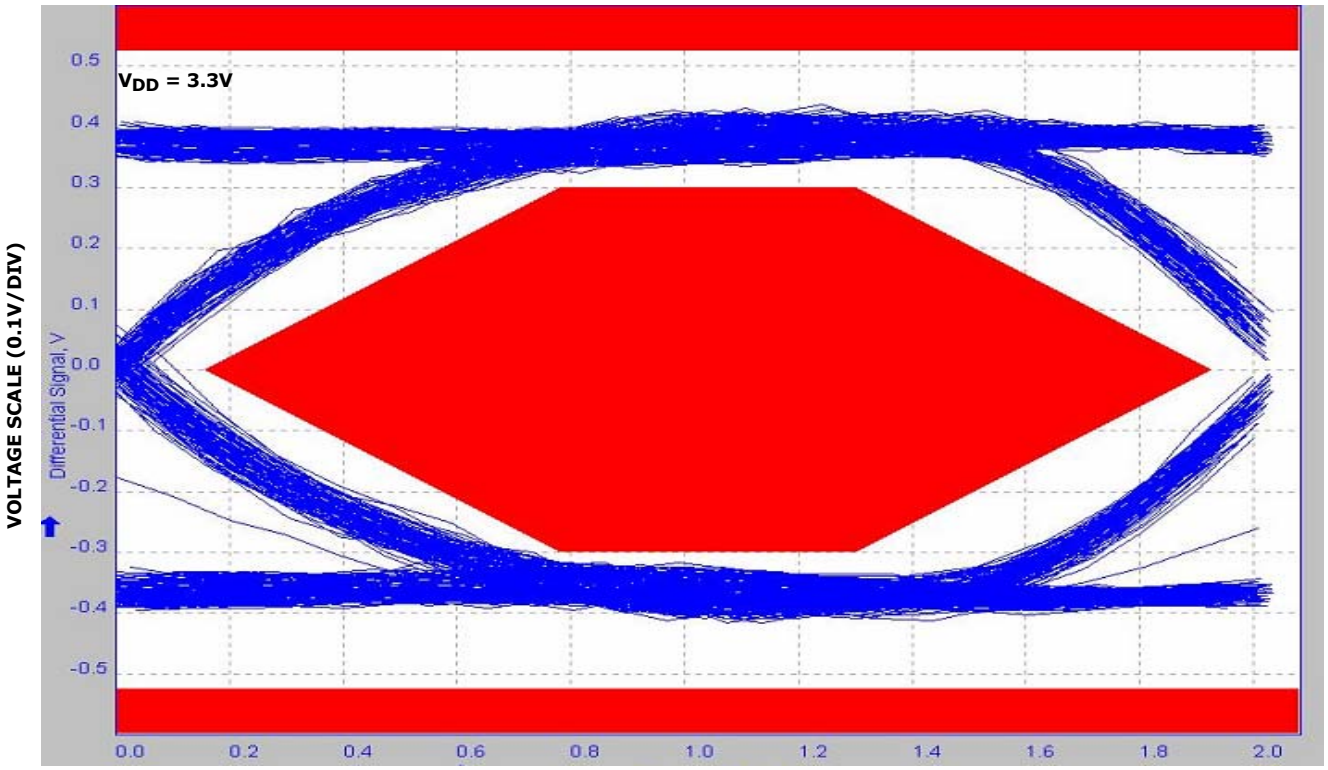


FIGURE 21. EYE PATTERN: 480Mbps WITH USB SWITCHES IN THE SIGNAL PATH

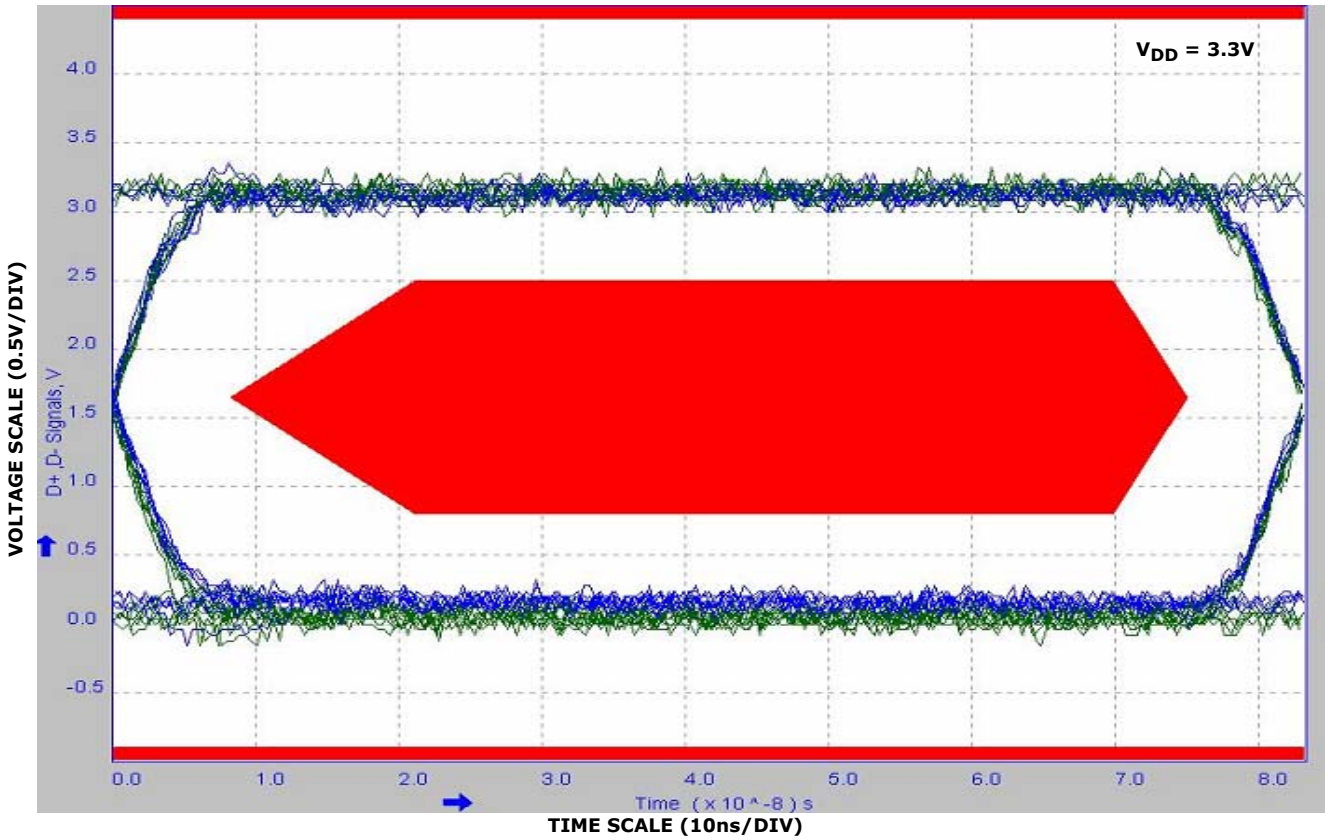


FIGURE 22. EYE PATTERN: 12Mbps WITH USB SWITCHES IN THE SIGNAL PATH

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

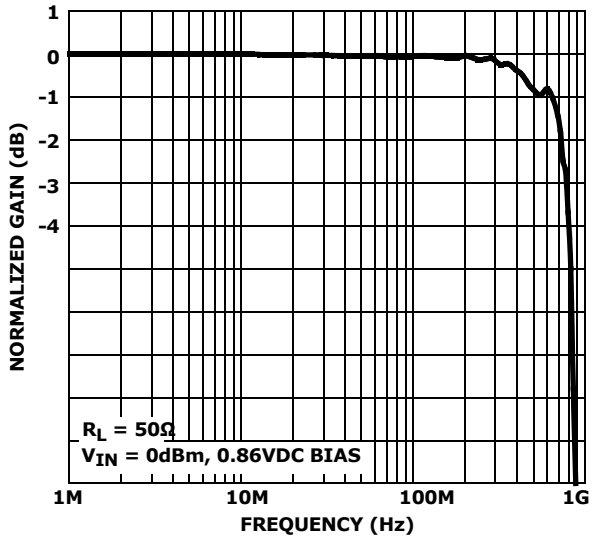


FIGURE 23. FREQUENCY RESPONSE

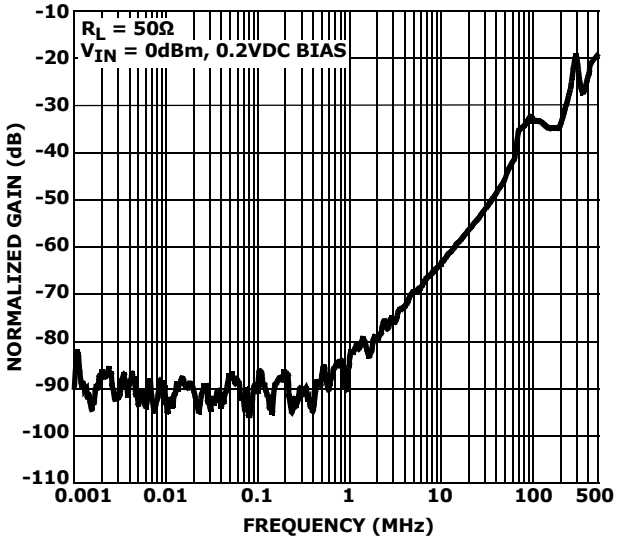


FIGURE 24. OFF-ISOLATION

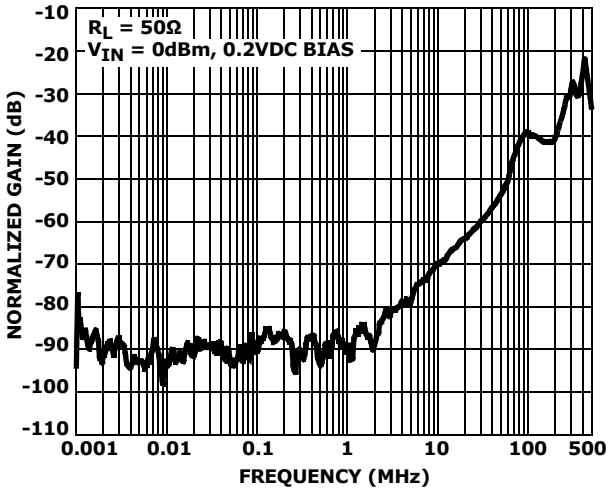


FIGURE 25. CROSSTALK

Die Characteristics

SUBSTRATE AND TDFN THERMAL PAD POTENTIAL (POWERED UP):

GND

TRANSISTOR COUNT:

1297

PROCESS:

Submicron CMOS

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
7/2/10	FN7627.0	Initial Release.

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL54225

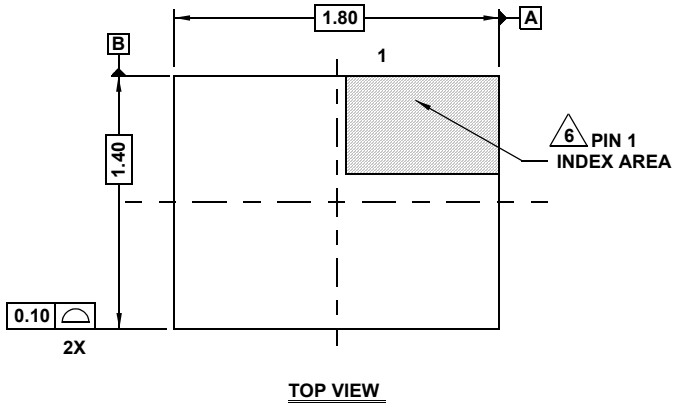
To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

FITs are available from our website at http://rel.intersil.com/reports/search.php

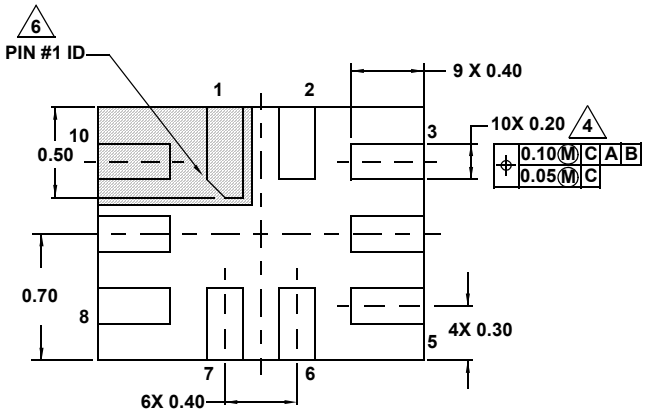
Package Outline Drawing

L10.1.8x1.4A

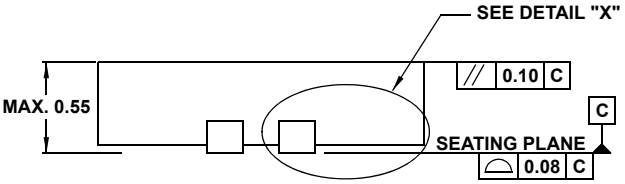
10 LEAD ULTRA THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 5, 3/10



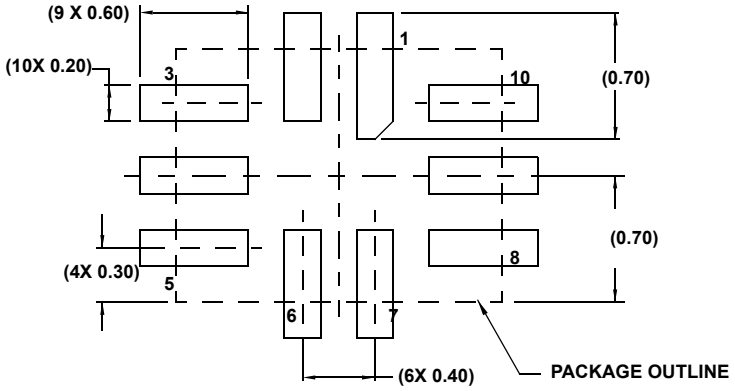
TOP VIEW



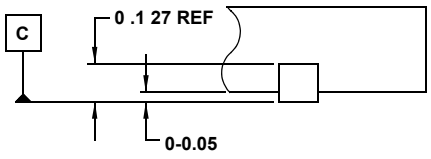
BOTTOM VIEW



SIDE VIEW



TYPICAL RECOMMENDED LAND PATTERN



DETAIL "X"

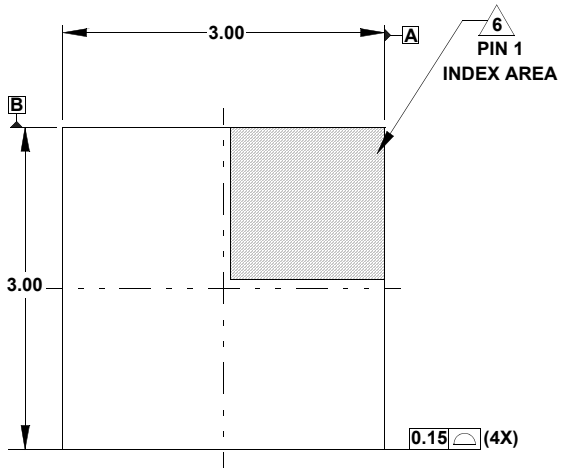
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. JEDEC reference MO-255.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

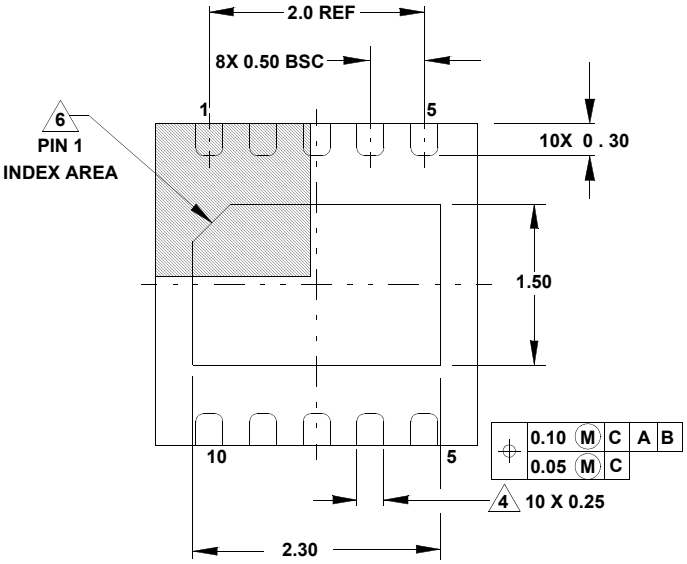
Package Outline Drawing

L10.3x3A

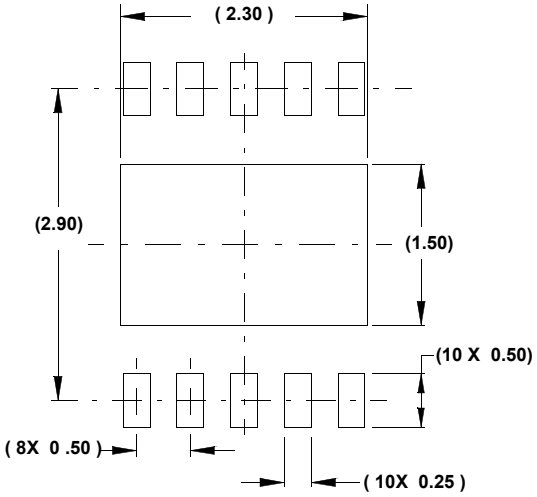
10 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE
Rev 5, 3/10



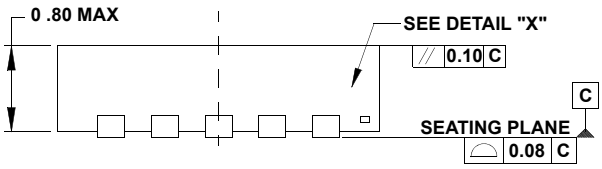
TOP VIEW



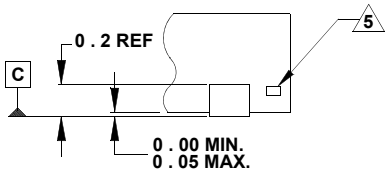
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
   Angular ±2.50°
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Compliant to JEDEC MO-229-WEED-3 except exposed pad length (2.30mm).