LTM2883 SPI/Digital or I²C µModule Isolator with Adjustable ±12.5V and 5V Regulated Power

DESCRIPTION

Demonstration circuit 1748A is a serial peripheral interface bus (SPI) or inter-IC bus (I²C) SPI/digital or I²C µModule isolator with adjustable ±12.5V and 5V regulated power featuring the LTM2883. The demo circuit features an EMI optimized circuit configuration and printed circuit board layout. All components are integrated into the µModule isolator. The demo circuit operates from a single external supply on V_{CC}. The part generates output voltages on V_{CC2}, V^+, and V^-, which may be adjusted by external programming resistors. It communicates all necessary signaling across the isolation barrier through LTC's isolator µModule technology.

Design files for this circuit board are available at http://www.linear.com/demo

PERFORMANCE SUMMARY (T_A = 25°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}	Input Supply Range	LTM2883-5	4.5	5	5.5	V
		LTM2883-3	3.0	3	3.6	V
V_{CC2}	Regulated Output Voltage		4.75	5	5.25	V
	Adjustable Output Voltage Range		3.0		5.5	V
	Maximum Load Current			20		mA
V^+	Regulated Output Voltage		12	12.5	13	V
	Adjustable Output Voltage Range		1.22		14	V
	Maximum Load Current			20		mA
V^-	Regulated Output Voltage		–12	–12.5	–13	V
	Adjustable Output Voltage Range		–1.22		14	V
	Maximum Load Current			15		mA
f_{MAX}	Maximum Data Rate	DI1 → O1, Ix → DOx, C_L = 10pF	10			MHz
		LTM2883-S, Bidirectional Communication LTM2883-S, Unidirectional Communication	4 8			MHz MHz
		LTM2883-I	400			kHz
V_{IORM}	Maximum Working Insulation Voltage	GND to GND2	560 400			V_{DC} V_{RMS}
	Common Mode Transient Immunity		30			kV/µs

OPERATING PRINCIPLES

The LTM2883 contains an isolated DC/DC conversion system, including a boost converter and inverting charge pump, with multiple LDO's to deliver power to the three output voltage rails from V_{CC}. Isolation is maintained by the separation of GND and GND2 where significant operating voltages and transients can exist without affecting the operation of the LTM2883. The logic side ON pin enables or shuts down the LTM2883. All logic side signals are referenced to the logic supply pin V_L. The LTM2883 is available in two data bus configurations, SPI (-S) or I^2C (-I), and with two input voltage ranges, 3.0 to 3.6 volts (-3) or 4.5 to 5.5 volts (-5).

SPI signaling is controlled by the logic inputs $\overline{CS}$, SDI, and SCK. $\overline{SDOE}$ controls the SDO output and is normally connected to $\overline{CS}$. The corresponding Isolated side output signals are $\overline{CS2}$, SDI2, and SCK2. SDO2 is the isolated side SPI data input. All of the SPI communication channels may be used as generic digital I/O.

I^2C signaling is controlled by the logic inputs SDA and SCL, corresponding to SDA2 and SCL2 on the isolated side. The SCL channel is unidirectional supporting master mode only I^2C communication. SCL2 output is standard CMOS push-pull drive. SDA signaling is bidirectional, and includes an internal current source pull-up on SDA2 supporting up to 200pF of load capacitance.

Demo circuit 1748A is available in four configurations supporting all versions of the LTM2883. Table 2 details the demo circuit configurations.

Table 2.

DEMO CIRCUIT	INPUT VOLTAGE	COMMUNICATION
DC1748A-A	3.0V to 3.6V	SPI/Digital
DC1748A-B	4.5V to 5.5V	SPI/Digital
DC1748A-C	3.0V to 3.6V	I^2C
DC1748A-D	4.5V to 5.5V	I^2C

The demo circuit has been designed and optimized for low RF emissions. To this end some features of the LTM2883 are not available for evaluation on the demo circuit. The logic supply voltage V_L is tied to V_{CC} on the demo circuit, and the ON pin is not available on the input pin header, but may be controlled by jumper JP1. EMI mitigation techniques used include the following.

1. Four layer PCB, allowing for isolated side to logic side bridge capacitor. The bridge capacitor is formed between an inner layer of floating copper which overlaps the logic side and isolated side ground planes. This structure creates two series capacitors, each with approximately .008" of insulation, supporting the full dielectric withstand rating of $2500V_{RMS}$. The bridge capacitor provides a low impedance return path for injected currents due to parasitic capacitances of the LTM2883's signal and power isolating elements.
2. Discrete bridge capacitors (C3, C4) mounted between GND2 and GND. The discrete capacitors provide additional attenuation at frequencies below 400MHz. Capacitors are safety rated type Y2, manufactured by Murata, part number GA342QR7GF471KW01L.
3. Board/ground plane size has been minimized. This reduces the dipole antenna formed between the logic side and isolated side ground planes.
4. Top signal routing and ground floods have been optimized to reduce signal loops, minimizing differential mode radiation.
5. Common mode filtering is integrated into the input and output pin headers. Filtering helps to reduce emissions caused by conducted noise and minimizes the effects of cabling to common mode emissions.
6. A combination of low ESL and high ESR decoupling is used. A low ESL ceramic capacitor is located close to the module minimizing high frequency noise conduction. A high ESR tantalum capacitor is included to minimize board resonances and prevent voltage spikes due to hot plugging of the supply voltage.

OPERATING PRINCIPLES

EMI performance is shown in Figure 1, measured using a Gigahertz Transverse Electromagnetic (GTEM) cell and method detailed in IEC 61000-4-20, “Testing and Measurement Techniques – Emission and Immunity Testing in Transverse Electromagnetic Waveguides”.

The demo circuit includes provisions for programming the three output voltage rails. Resistors R5, R6, and R7 allow the V^+, $V^–$, and V_{CC2} power rails, respectively, to be reduced from their nominal operating voltages. The formulas presented in Table 3 allow selection of the appropriate resistor values.

Table 3.

VOLTAGE RAIL	RESISTOR TO REDUCE OUTPUT
V^+	$R5 = 150k \bullet (V^+ – 1.22)/(12.5 – V^+)$
$V^–$	$R6 = 150k \bullet (1.22 + V^–)/(–12.5 – V^–)$
V_{CC2}	$R7 = 110k \bullet (V_{CC2} – 0.6)/(5 – V_{CC2})$

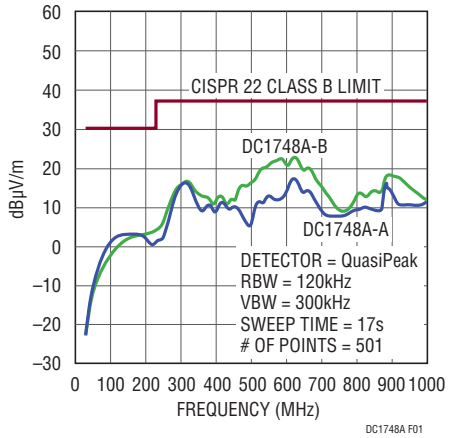


Figure 1. DC1748 Radiated Emissions

QUICK START PROCEDURE

Demonstration circuit 1748A is easy to set up and evaluate the performance of the LTM2883. Refer to Figure 2 for proper measurement equipment setup and follow the procedure below.

NOTE: When measuring the input or output voltage ripple or high speed signals, care must be taken to avoid a long ground lead on the oscilloscope probe.

1. Install JP1 in the ON (default) position.
2. With power off, connect the input power supply to V_{CC} and GND on pin header J1.
3. Turn on the power at the input.

   NOTE: Make sure that the input voltage does not exceed 6V.
4. Check for the proper output voltages. V_{CC2} = 5V, V^+ = 12.5V, and V^- = –12.5V on pin header J2.
5. Once the proper output voltages are established, connect signals to J1 and J2 pin headers as appropriate. The header pin names and locations are detailed on the demo board silkscreen below the pin headers.

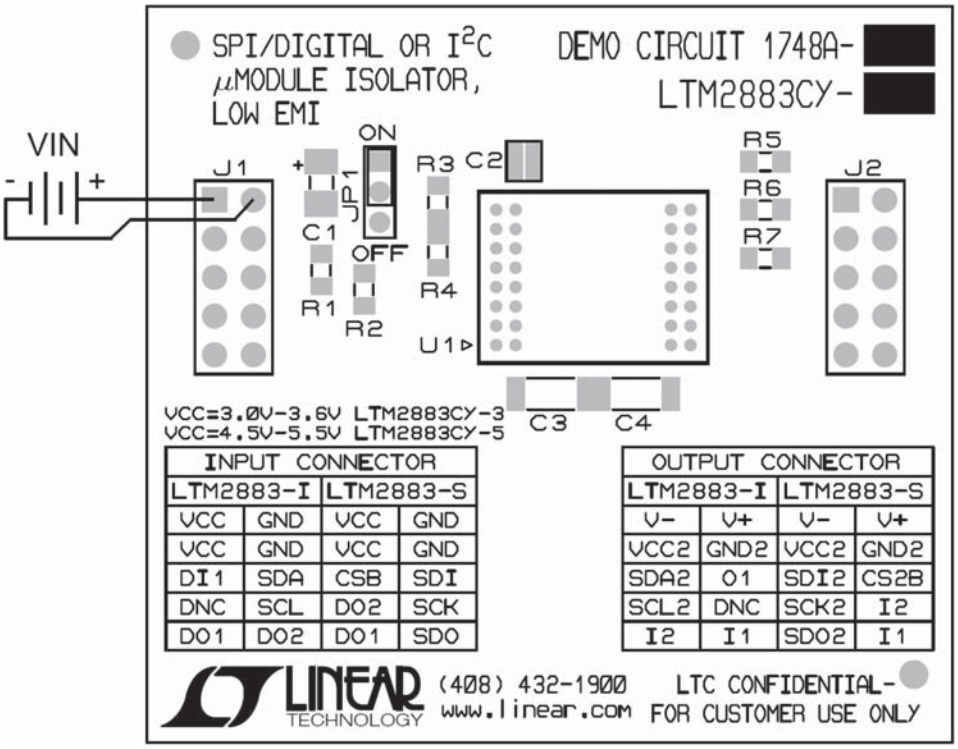
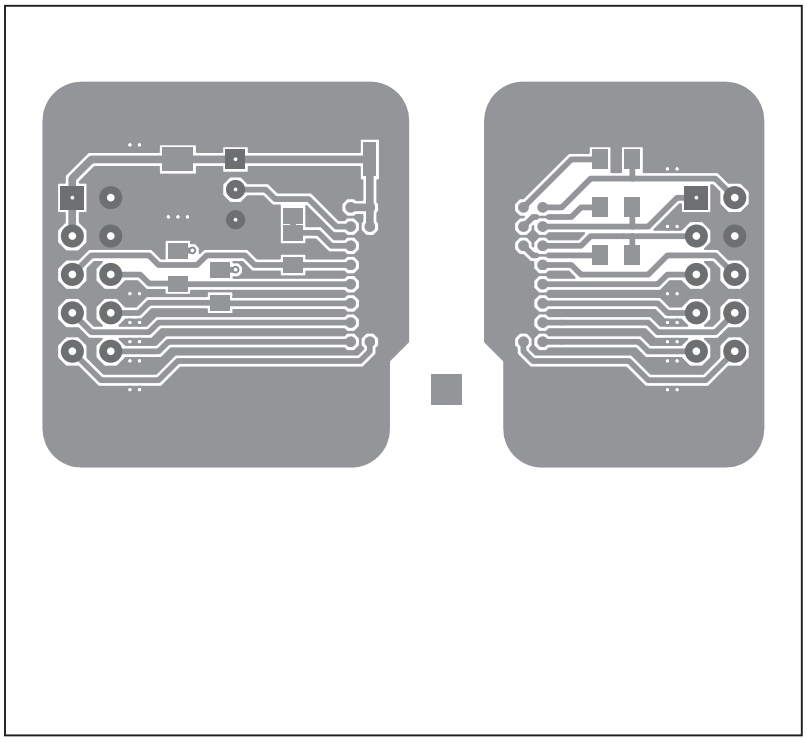
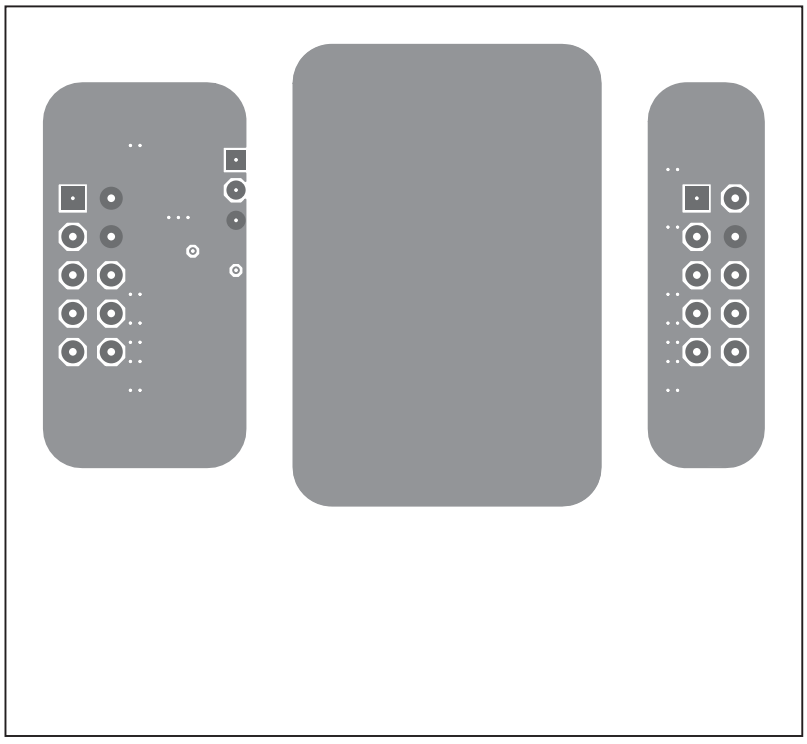


Figure 2. Demo Board Setup

PCB LAYOUT

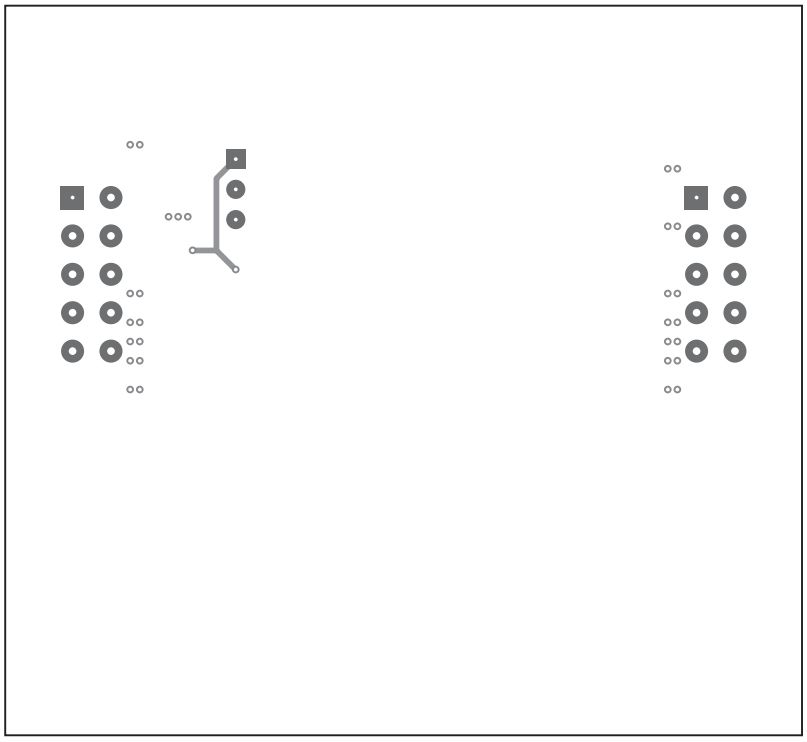


Layer 1. Top Layer

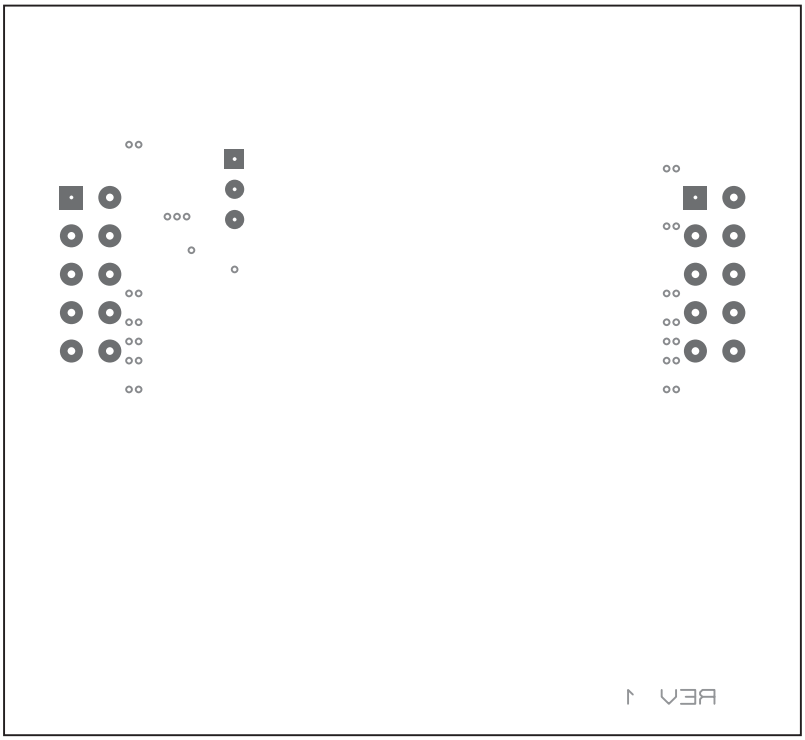


Layer 2. Ground Plane

PCB LAYOUT



Layer 3. Signal Layer

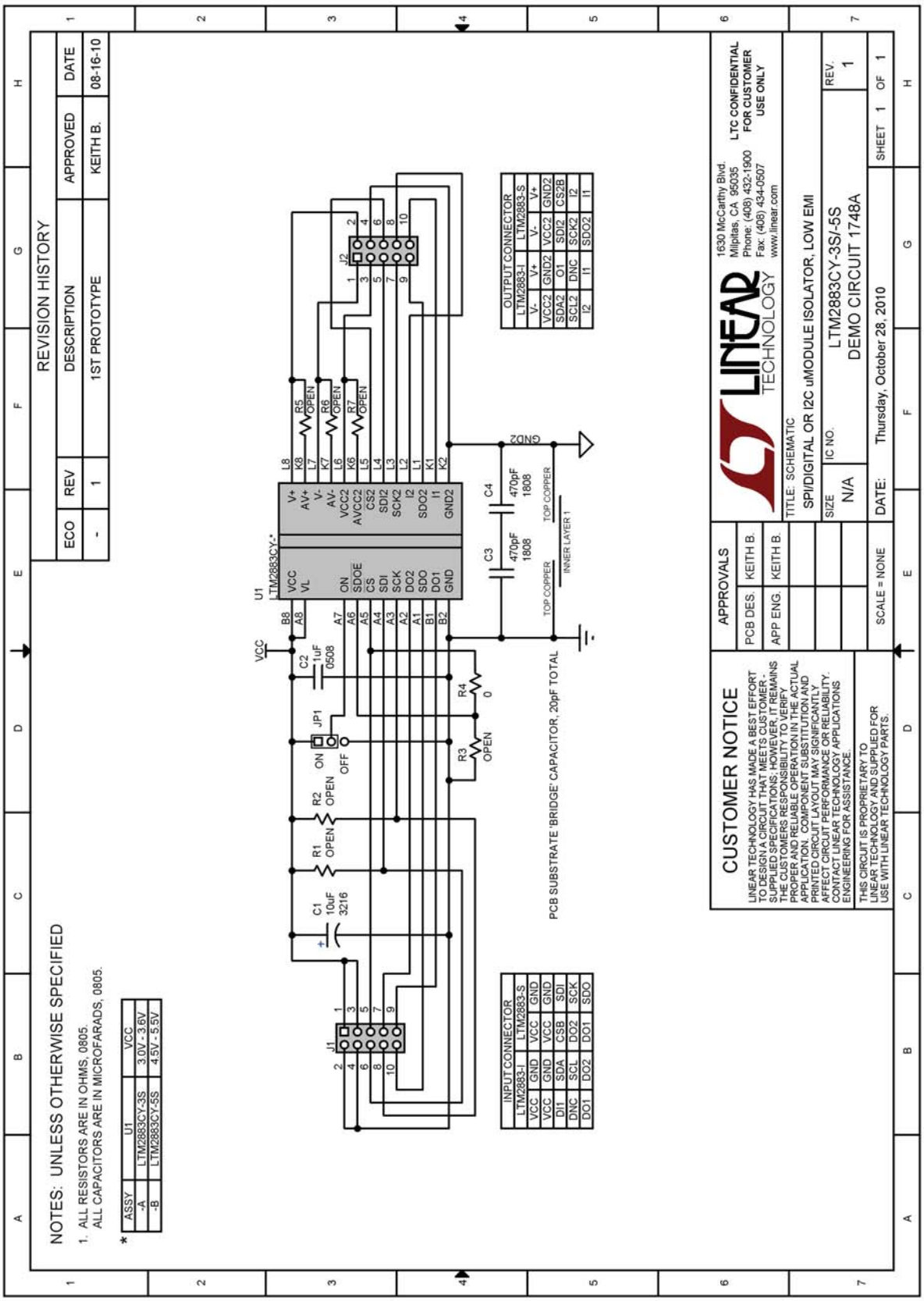


Layer 4. Bottom Layer

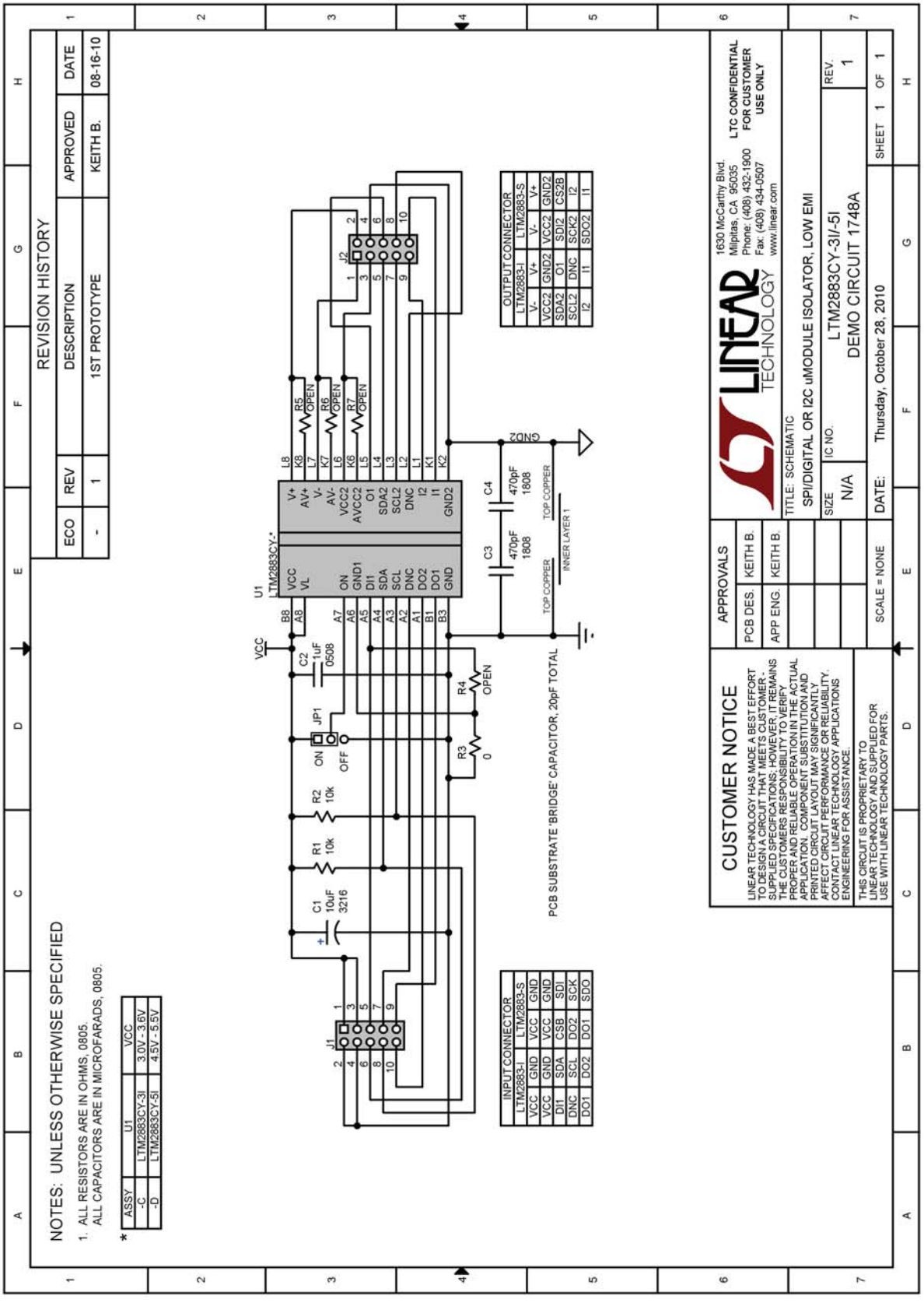
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	1	U1-A	IC, LTM2883CY-3S	Linear Technology LTM2883CY-3S#PBF
	1	U1-B	IC, LTM2883CY-5S	Linear Technology LTM2883CY-5S#PBF
	1	U1-C	IC, LTM2883CY-3I	Linear Technology LTM2883CY-3I#PBF
	1	U1-D	IC, LTM2883CY-5I	Linear Technology LTM2883CY-5I#PBF
Hardware/Components (For Demo Board Only)				
2	1	C1	Capacitor, Tantalum 10µF 10V 20% TAJA	AVX TAJA106M010RNJ
3	1	C2	Capacitor, Ceramic 1µF 10V 20% 0508	Murata LLL219R71A105MA01L
4	2	C3, C4	Capacitor, Ceramic 470pF 250VAC 10% 1808	Murata GA342QR7GF471KW01L
5	2	J1, J2	0.1" Double Row Header, 5 × 2 Pin	Samtec TSW-105-22-G-D
6	2	J1, J2	0.1" Ferrite Plate, 5 × 2 Hole	Fair Rite 2644247101
7	1	J2	Connection, Filtered, DSUB 9-Pin	Kobiconn 152-3609
8	1	JP1	2mm Single Row Header, 3-Pin	Samtec TMM-103-02-L-S
9	1	JP1	Shunt	Samtec 2SN-BK-G
10	1	R1-C	Resistor, Chip 10kΩ 1% 0805	Yageo RC0805FR-0710KL
	1	R1-D	Resistor, Chip 10kΩ 1% 0805	Yageo RC0805FR-0710KL
11	1	R2-C	Resistor, Chip 10kΩ 1% 0805	Yageo RC0805FR-0710KL
	1	R2-D	Resistor, Chip 10kΩ 1% 0805	Yageo RC0805FR-0710KL
12	1	R3-C	Resistor, Chip 0 0805	Yageo RC0805FR-070RL
	1	R3-D	Resistor, Chip 0 0805	Yageo RC0805FR-070RL
13	1	R4-A	Resistor, Chip 0 0805	Yageo RC0805FR-070RL
	1	R4-B	Resistor, Chip 0 0805	Yageo RC0805FR-070RL

SCHEMATIC DIAGRAM (DC1748A-A/DC1748A-B)



SCHEMATIC DIAGRAM (DC1748A-C/DC1748A-D)



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This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

Mailing Address:

Linear Technology
1630 McCarthy Blvd.
Milpitas, CA 95035