

## CLOCK MULTIPLIER WITH DELAY CONTROL AND PHASE ALIGNMENT

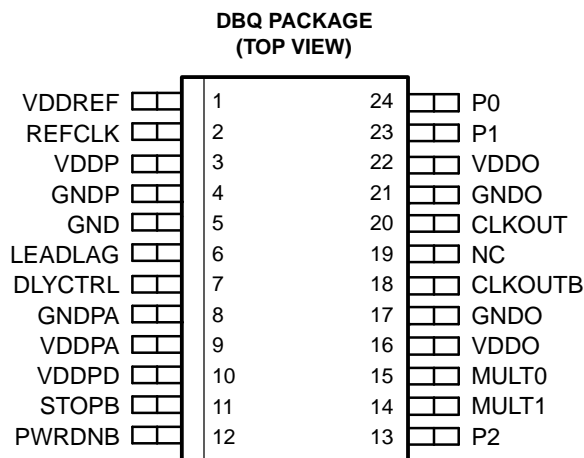
### (Not Recommended for New Designs Use CDCF5801A as a Replacement)

#### FEATURES

- **Low-Jitter Clock Multiplier:**  $\times 1$ ,  $\times 2$ ,  $\times 4$ ,  $\times 8$
- **Programmable Bidirectional Delay Steps of 1.3 mUI**
- **Output Frequency Range of 25 MHz to 280 MHz**
- **Input Frequency Range of 12.5 MHz to 240 MHz**
- **Low Jitter Generation**
- **Single-Ended REFCLK Input With Adjustable Trigger Level (Works With LVTTTL, HSTL, and LVPECL)**
- **Differential/Single-Ended Output**
- **Output Can Drive LVPECL, LVDS, and LVTTTL**
- **Three Power Operating Modes to Minimize Power**
- **Low Power Consumption (< 190 mW at 280 MHz/3.3 V)**
- **Packaged in a Shrink Small-Outline Package (DBQ)**
- **No External Components Required for PLL**
- **Spread Spectrum Clock Tracking Ability to Reduce EMI (SSC)**

#### APPLICATIONS

- **Video Graphics**
- **Gaming Products**
- **Datacom**
- **Telecom**
- **Noise Cancellation Created by FPGAs**



#### DESCRIPTION

The CDCF5801 provides clock multiplication from a reference clock (REFCLK) signal with the unique capability to delay or advance the CLKOUT/CLKOUTB with steps of only 1.3 mUI through a phase aligner. For every rising edge on the DLYCTRL pin the CLKOUT is delayed by a 1.3-mUI step size as long as the LEADLAG input detects a low signal at the time of the DLYCTRL rising edge. Similarly for every rising edge on the DLYCTRL pin the CLKOUT is advanced by a 1.3-mUI step size as long as the LEADLAG pin is high during the transition. This unique capability allows the device to phase align (zero delay) between CLKOUT/CLKOUTB and any one other CLK in the system by feeding the clocks that need to be aligned to the DLYCTRL and the LEADLAG pins. Also it provides the capability to program a fixed delay by providing the proper number of edges on the DLYCTRL pin, while strapping the LEADLAG pin to dc high or low. Further possible applications are:

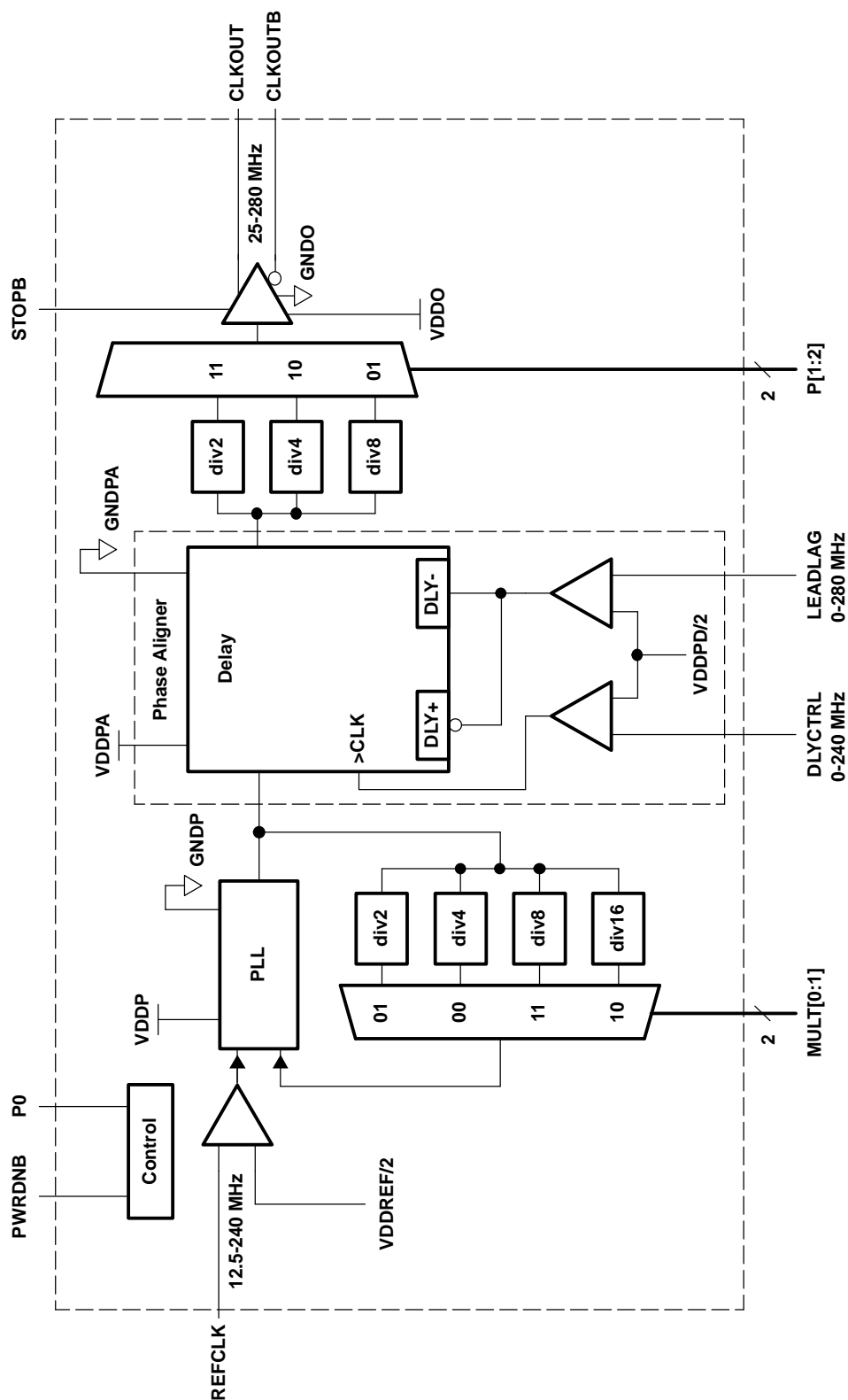
- Aligning the rising edge of the output clock signal to the input clock rising edge
- Avoiding PLL instability in applications that require very long PLL feedback lines
- Isolation of jitter and digital switching noise
- Limitation of jitter in systems with good ppm frequency stability



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The CDCF5801 provides clock multiplication and division from a reference clock (REFCLK) signal. The device is optimized to have extremely low jitter impact from input to output. The predivider pins MULT[0:1] and post-divider pins P[0:2] provide selection for frequency multiplication and division ratios, generating CLKOUT/CLOUTKB frequencies ranging from 25 MHz to 280 MHz with clock input references (REFCLK) ranging from 12.5 MHz to 240 MHz. See [Table 1](#) for detailed frequency support. The selection of pins MULT[0:1] and P[1:2] determines the multiplication value of 1, 2, 4, or 8. The CDCF5801 offers several power-down/high-impedance modes, selectable by pins P0, STOPB and PWRDN. Another unique capability of the CDCF5801 is the high sensitivity and wide common-mode range of the clock-input pin REFCLK by varying the voltage on the VDDREF pin. The clock signal outputs CLKOUT and CLKOUTB can be used independently to generate single-ended clock signals. The CLKOUT/CLKOUTB outputs can also be combined to generate a differential output signal suitable for LVDS, LVPECL, or HSTL/SSTL signaling. The CDCF5801 is characterized for operation over free-air temperatures of -40°C to 85°C.

# FUNCTIONAL BLOCK DIAGRAM



**TERMINAL FUNCTIONS**

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
CLKOUT CLKOUTB	2018	O	Output CLK signal (low-noise CMOS) Complementary output CLK signal (low-noise CMOS)
DLYCTRL	7	I	Every rising edge on this pin delays/advances the CLKOUT/CLKOUTB signal by 1/768 <sup>th</sup> of the CLKOUT/CLKOUTB period (1.3 mUI). (E.g., for a 90-degree delay or advancement one needs to provide 192 rising edges). See <a href="#">Table 3</a> .
GND	5		GND for VDDREF and VDDPD
GNDO	17, 21		GND for the output pins (CLKOUT, CLKOUTB)
GNDP	4		GND for the PLL
GNDPA	8		GND for phase aligner, digital logic, and inputs P[0:2], MULT[0:1], STOPB, PWRDNB
LEADLAG	6	I	Controls whether the output CLK is delayed or advanced relative to REFCLK. See <a href="#">Table 3</a> .
MULT0 MULT1	15 14	I	PLL multiplication factor select. See <a href="#">Table 1</a> . MULT[0:1] = 10: ×16 MULT[0:1] = 11: ×8 MULT[0:1] = 00: ×4 MULT[0:1] = 01: ×2
NC	19		Not connected; leave pin floating or tied to GND.
P0	24	I	Mode control pins (see <a href="#">Table 1</a> ) 0 - Normal operation 1 - High-Z outputs and other special settings
P1	23	I	Post divider control (see <a href="#">Table 1</a> ) P[1:2] = 11: div2 P[1:2] = 10: div4 P[1:2] = 01: div8
P2	13		
PWRDNB	12	I	Active-low power-down state. CLKOUT/CLKOUTB goes low, See <a href="#">Table 2</a> . 0 - IC in power down 1 - Normal operation
REFCLK	2	I	Reference input clock
STOPB	11	I	Active low output disabler, PLL and PA still running, CLKOUT and CLKOUTB goes to a dc value as listed in <a href="#">Table 2</a> . 0 - Outputs disabled 1 - Normal operation
VDDO	16, 22		VDD for the output pin (CLKOUT, CLKOUTB) and power down circuit
VDDP	3		VDD for PLL and input buffer
VDDPA	9		VDD for phase aligner, digital logic, and inputs P[0:2], MULT[0:1], and STOPB
VDDPD	10		Reference voltage for inputs LEADLAG and DLYCTRL
VDDREF	1		Reference voltage for REFCLK

Table 1. Input-to-Output Settings

INPUT-TO-OUTPUT MULTIPLICATION-RATIO	INPUT FREQUENCY (MHz)		OUTPUT FREQUENCY (MHz)		PREDIVIDER		POST DIVIDER			NOTE
	FROM	TO	FROM	TO	MULT0	MULT1	P0	P1	P2	
8	12.5	35	100	280	1	0	0	1	1	Normal operation <sup>(1)</sup>
4	12.5	39	50	156	1	0		1	0	
	25	70	100	280	1	1		1	1	
2	12.5	39	25	78	1	0		0	1	
	25	78	50	156	1	1		1	0	
	50	140	100	280	0	0		1	1	
1	25	78	25	78	1	1		0	1	
	50	156	50	156	0	0		1	0	
	100	240	100	240	0	1		1	1	
CLKOUT high-impedance					X	X	1	0	0	Special mode of operation
CLOCKOUTB high-impedance										
CLKOUT = high					X	X		0	1	
CLKOUTB = high										
CLKOUT = P2					X	X		1	X	
CLKOUTB = P2										

(1) There is some overlapping of the input frequency ranges for multiplication ratios of 1, 2, and 4. For example, an input frequency of 30 MHz for a multiplication ratio of four falls within both the 12.5 to 39-MHz range and the 25 to 70-MHz range. For best device operation in a case such as this, always select the input frequency range nearer to the top of the table.

## PLL DIVIDER/MULTIPLIER SELECTION

Table 2. Power Down Modes

STATE	PWRDNB	STOPB	CLKOUT and CLKOUTB
Power down	0	X	GNDO
Clock stop	1	0	V <sub>O</sub> , STOP
Normal	1	1	See <a href="#">Table 1</a>

Table 3. Programmable Delay and Phase Alignment

DLYCTR	NOTE	LEADLAG	CLKOUT and CLKOUTB
Each rising edge+	For every 32 edges, there are one or two edges for which the phase aligner does not update the phase. Therefore, CLKOUT phase is not updated for every 32 <sup>nd</sup> edge. The frequency of the DLYCTRL pin should always be equal to or less than the frequency of the LEADLAG pin.	HI	Advanced by one step: step size: 1/768 of the CLKOUT period (1.3 mUI) at P[1:2] = 11 1/1536 of the CLKOUT period (0.65 mUI) at P[1:2] = 10 1/3072 of the CLKOUT period (0.325 mUI) at P[1:2] = 01
Each rising edge+		LO	Delayed by one step: step size: 1/768 of the CLKOUT period (1.3 mUI) at P[1:2] = 11 1/1536 of the CLKOUT period (0.65 mUI) at P[1:2] = 10 1/3072 of the CLKOUT period (0.325 mUI) at P[1:2] = 01

**ABSOLUTE MAXIMUM RATINGS**over operating free-air temperature (unless otherwise noted)<sup>(1)</sup>

$V_{DDx}^{(2)}$	Supply voltage range	-0.5 V to 4 V
	Voltage range at any output terminal	-0.5 V to $V_{DD} + 0.5$ V
	Voltage range at any input terminal	-0.5 V to $V_{DD} + 0.5$ V
$T_{stg}$	Storage temperature range	-65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

- (1) Stresses beyond those listed under „absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under „recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the GND terminals.

**POWER DISSIPATION RATING TABLE**

PACKA GE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR <sup>(1)</sup> ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ POWER RATING
DBQ	830 mW	8.3 mW/°C	332 mW

- (1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

**RECOMMENDED OPERATING CONDITIONS**

		MIN	NOM	MAX	UNIT
VDDP, VDDPA, VDDO	Supply voltage	3	3.3	3.6	V
$V_{IH}$ (CMOS)	High-level input voltage	0.7 VDD			V
$V_{IL}$ (CMOS)	Low-level input voltage			0.3 VDD	V
$V_{IL}$ (DLYCTRL, LEADLAG)	Input signal low voltage		$\frac{VDDPD}{2} - 0.2$		V
$V_{IH}$ (DLYCTRL, LEADLAG)	Input signal high voltage		$\frac{VDDPD}{2} + 0.2$		V
(VDDPD)	Input reference voltage for DLYCNTRL and LEADLAG	1.2		VDD	V
$I_{OH}$	High-level output current			-16	mA
$I_{OL}$	Low-level output current			16	mA
(VDDREF) (see Application section)	Input reference voltage for REFCLK	1.2		VDD	V
$V_{IL}$ (see Application section)	REFCLK input low voltage		$\frac{VDDREF}{2} - 0.2$		V
$V_{IH}$ (see Application section)	REFCLK input high voltage		$\frac{VDDREF}{2} + 0.2$		V
$T_A$	Operating free-air temperature	-40		85	°C

**TIMING REQUIREMENTS**

	PARAMETER	MIN	MAX	UNIT
$F_{mod}$	Input frequency of modulation, (if driven by SSC CLKIN)		33	kHz
	Modulation index, nonlinear maximum 0.5%		0.6%	
SR	Input slew rate	1	4	V/ns
	Input duty cycle on REFCLK	40%	60%	
	Input frequency on REFCLK	12.5	240	MHz
	Output frequency on CLKOUT and CLKOUTB	25	280	MHz
	Allowable frequency on DLYCTRL		240	MHz

**TIMING REQUIREMENTS (continued)**

PARAMETER	MIN	MAX	UNIT
Allowable frequency on LEADLAG		280	MHz
Allowable duty cycle on DLYCTRL and LEADLAG pins	25%	75%	

**ELECTRICAL CHARACTERISTICS**

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS <sup>(1)</sup>		MIN		TYP <sup>(2)</sup>		MAX	UNIT
V <sub>O(STOP)</sub>	Output voltage during Clkstop mode		See <a href="#">Figure 1</a>		1.1				2	V
V <sub>O(X)</sub>	Output crossing-point voltage		See <a href="#">Figure 1</a> and <a href="#">Figure 4</a>		$\frac{V_{DDO}}{2} - 0.2$		$\frac{V_{DDO}}{2} + 0.2$			V
V <sub>O</sub>	Output voltage swing (V <sub>OH</sub> - V <sub>OL</sub> )		See <a href="#">Figure 1</a>		1.7				2.9	V
V <sub>IK</sub>	Input clamp voltage		V <sub>DD</sub> = 3 V, I <sub>I</sub> = -18 mA						-1.2	V
V <sub>OH</sub>	High-level output voltage		V <sub>DD</sub> = 3 to 3.6 V, See <a href="#">Figure 1</a>		2	2.5			V	
			V <sub>DD</sub> = 3 V, I <sub>OH</sub> = -16 mA		2.2					
V <sub>OL</sub>	Low-level output voltage		V <sub>DD</sub> = 3 to 3.6 V, See <a href="#">Figure 1</a>		0.4		0.6		V	
			V <sub>DD</sub> = 3 V, I <sub>OH</sub> = 16 mA		0.5					
I <sub>OH</sub>	High-level output current		V <sub>DD</sub> = 3.135 V, V <sub>O</sub> = 1 V		-32	-52			mA	
			V <sub>DD</sub> = 3.3 V, V <sub>O</sub> = 1.65 V		-51					
			V <sub>DD</sub> = 3.465 V, V <sub>O</sub> = 3.135 V		-14.5 -21					
I <sub>OL</sub>	Low-level output current		V <sub>DD</sub> = 3.135 V, V <sub>O</sub> = 1.95 V		43	61.5			mA	
			V <sub>DD</sub> = 3.3 V, V <sub>O</sub> = 1.65 V		65					
			V <sub>DD</sub> = 3.465 V, V <sub>O</sub> = 0.4 V		25.5 40					
I <sub>OZ</sub>	High-impedance-state output current		P0 = 1, P1 = P2 = 0				±10		μA	
I <sub>OZ(STOP)</sub>	High-impedance-state output current during Clk Stop		Stop = 0, V <sub>O</sub> = GND or V <sub>DD</sub>				±100		μA	
I <sub>OZ(PD)</sub>	High-impedance-state output current in power-down state		PWRDNB = 0, V <sub>O</sub> = GND or V <sub>DD</sub>		-10		100		μA	
I <sub>IH</sub>	High-level input current	REFCLK; STOPB; PWRDNB; P[0:2]; MULT[0:1]; DLYCTRL; LEADLAG	V <sub>DD</sub> = 3.6 V, V <sub>I</sub> = V <sub>DD</sub>				10		μA	
I <sub>IL</sub>			V <sub>DD</sub> = 3.6 V, V <sub>I</sub> = 0				-10		μA	
Z <sub>O</sub>	Output impedance (single ended)	High state	R <sub>I</sub> at I <sub>O</sub> -14.5 mA to -16.5 mA		15	35	50		Ω	
		Low state	R <sub>I</sub> at I <sub>O</sub> 14.5 mA to 16.5 mA		10	17	35			
I <sub>REF</sub>	Reference current	V <sub>DDREF</sub> ; VDDPD	V <sub>DD</sub> = 3.6 V	PWRDNB = 0			50		μA	
				PWRDNB = 1			0.5		mA	
C <sub>I</sub>	Input capacitance		V <sub>I</sub> = V <sub>DD</sub> or GND		2				pF	
C <sub>O</sub>	Output capacitance		V <sub>O</sub> = GND or V <sub>DD</sub>		3				pF	
I <sub>DD(PD)</sub>	Supply current in power-down state		REFCLK = 0 MHz to 280 MHz; PWRDNB = 0; STOPB = 1				4		mA	
I <sub>DD(CLKSTOP)</sub>	Supply current in CLK stop state		BUSCLK configured for 280 MHz				44		mA	
I <sub>DD(NORMAL)</sub>	Supply current (normal operation mode)		BUSCLK 280 MHz, MULT[0:1] = 10; P[0:2] = 011; Load , See <a href="#">Figure 1</a>				75		mA	

(1) V<sub>DD</sub> refers to any of the following; VDDP, VDDREF, VDDO, VDDPD, and VDDPA(2) All typical values are at V<sub>DD</sub> = 3.3 V, T<sub>A</sub> = 25°C.

**JITTER SPECIFICATION**over recommended free-air temperature range and  $V_{CC}$  range (unless otherwise noted)

PARAMETER		TEST CONDITIONS					TYP (ps)	MAX (ps)
		REFCLK (MHz)	CLKOUT (MHz)	MULT[0:1]	P[0:2]	NOTES		
t <sub>(jitter)</sub>	Period rms (1-sigma jitter, full frequency band)	25	25	11	001	Phase aligner running (CLKOUT tight to LEADLAG; REFCLK tight to DLYCTRL). All typical values are at VDD = 3.3 V, T <sub>A</sub> = 25°C.	20	48
	Period p-p						120	225
	Cycle to cycle +						70	165
	Cycle to cycle -						70	165
	RMS phase jitter (accumulated, 100 kHz-12.5 MHz)						80	160
	Period rms (1-sigma jitter, full frequency band)	50	50	11	001		7	15
	Period p-p						37	75
	Cycle to cycle +						27	55
	Cycle to cycle -						27	55
	RMS phase jitter (accumulated, 100 kHz-25 MHz)						27	65
	Period rms (1-sigma jitter, full frequency band)	100	100	00	010		5	14
	Period p-p						30	65
	Cycle to cycle +						24	55
	Cycle to cycle -						24	55
	RMS phase jitter (accumulated, 100 kHz-40 MHz)						35	65
	Period rms (1-sigma jitter, full frequency band)	156	156	00	010		4	8
	Period p-p						20	40
	Cycle to cycle +						17	40
	Cycle to cycle -						17	40
	RMS phase jitter (accumulated, 100 kHz-40 MHz)						15	35
	Period rms (1-sigma jitter, full frequency band)	200	200	01	011		8	15
	Period p-p						38	60
	Cycle to cycle +						5	55
	Cycle to cycle -						35	55
	RMS phase jitter (accumulated, 100 kHz-40 MHz)						30	60



**JITTER SPECIFICATION (continued)**over recommended free-air temperature range and  $V_{CC}$  range (unless otherwise noted)

PARAMETER		TEST CONDITIONS					TYP (ps)	MAX (ps)
		REFCLK (MHz)	CLKOUT (MHz)	MULT[0:1]	P[0:2]	NOTES		
t <sub>(jitter)</sub>	Period rms (1-sigma jitter, full frequency band)	25	200	10	011	Phase aligner not running (LEADLAG = 0, DLYCTRL = 0). All typical values are at VDD = 3.3 V, T <sub>A</sub> = 25°C.	4	11
	Period p-p						20	48
	Cycle to cycle +						16	45
	Cycle to cycle -						16	45
	Period rms (1-sigma jitter, full frequency band)	25	100	10	010		4	11
	Period p-p						22	55
	Cycle to cycle +						15	45
	Cycle to cycle -						15	45
	Period rms (1-sigma jitter, full frequency band)	70	280	11	011		4	11
	Period p-p						18	48
	Cycle to cycle +						15	45
	Cycle to cycle -						15	45
	Period rms (1-sigma jitter, full frequency band)	25	50	10	001		6	16
	Period p-p						34	75
	Cycle to cycle +						20	65
	Cycle to cycle -						20	65
	Period rms (1-sigma jitter, full frequency band)	78	156	11	010		3	11
	Period p-p						15	44
	Cycle to cycle +						13	40
	Cycle to cycle -						13	40
	Period rms (1-sigma jitter, full frequency band)	62.5	125	00	011		6	20
	Period p-p						35	80
	Cycle to cycle +						25	75
	Cycle to cycle -						25	75

**SWITCHING CHARACTERISTICS**

over recommended operating free-air temperature range (unless otherwise noted)

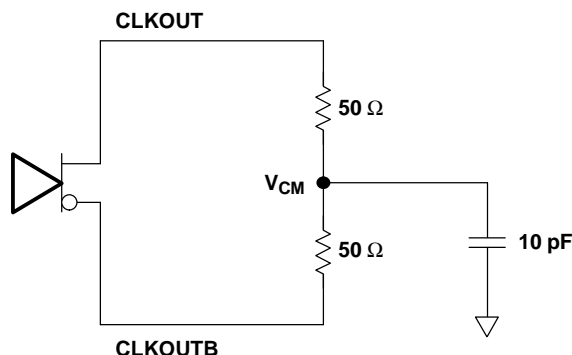
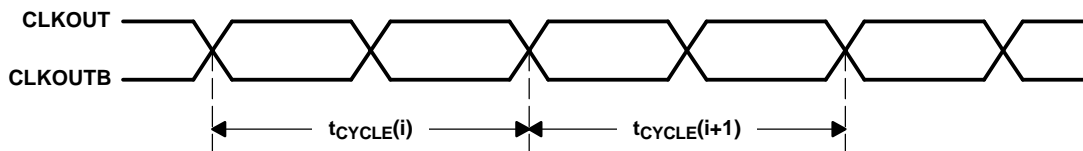
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(DC)}$	Output duty cycle over 1000 cycles	See <a href="#">Figure 3</a>	42%		58%	
$t_r, t_f$	Output rise and fall times (measured at 20%-80% of output voltage)	See <a href="#">Figure 5</a>	150	250	350	ps

**STATE TRANSITION LATENCY SPECIFICATIONS**

PARAMETER		FROM	TO	TEST CONDITION	MIN	TYP	MAX	UNIT
$t_{(powerup)}$	Delay time, PWRDNB $\uparrow$ to CLKOUT / CLKOUTB settled	Power down	Normal	See <a href="#">Figure 6</a>			3	ms
	Delay time, PWRDNB $\uparrow$ to internal PLL and clock are on and settled						3	

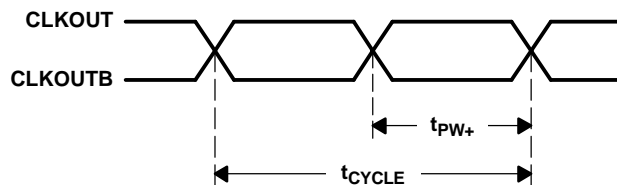
**STATE TRANSITION LATENCY SPECIFICATIONS (continued)**

PARAMETER		FROM	TO	TEST CONDITION	MIN	TYP	MAX	UNIT
$t_{(VDDpowerup)}$	Delay time, power up to CLKOUT output settled	$V_{DD}$	Normal	See Figure 6			3	ms
	Delay time, power up to internal PLL and clock are on and settled						3	
$t_{(MULT)}$	MULT0 and MULT1 change to CLKOUT output resettled	Normal	Normal	See Figure 7			1	ms
$t_{(CLKON)}$	STOPB $\uparrow$ to CLKOUT glitch-free clock edges	CLK stop	Normal	See Figure 8			10	ns
$t_{(CLKSETL)}$	STOPB $\uparrow$ to CLKOUT output settled to within 50 ps of the phase before STOPB was disabled	CLK stop	Normal	See Figure 8			20	cycles
$t_{(CLKOFF)}$	STOPB $\downarrow$ to CLKOUT output disabled	Normal	CLK stop	See Figure 8			5	ns
$t_{(powerdown)}$	Delay time, PWRDNB $\downarrow$ to the device in the power-down mode	Normal	Power down	See Figure 6			1	ms
$t_{(STOP)}$	Maximum time in CLKSTOP (STOPB = 0) before reentering normal mode (STOPB = 1)	STOPB	Normal	See Figure 8	100			$\mu$ s
$t_{(ON)}$	Minimum time in normal mode (STOPB = 1) before reentering CLKSTOP (STOPB = 0)	Normal	CLK stop	See Figure 8	100			ms

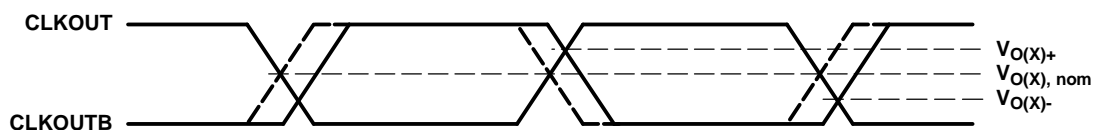
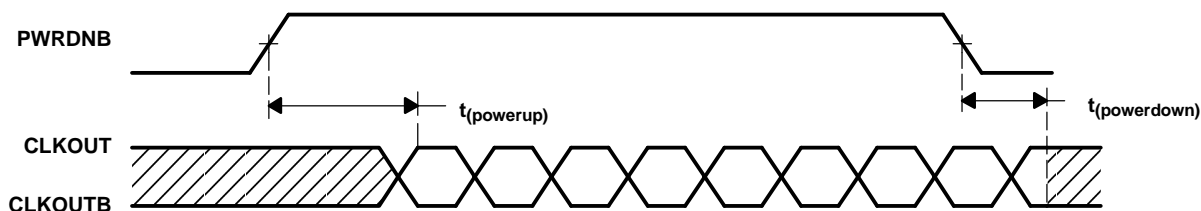
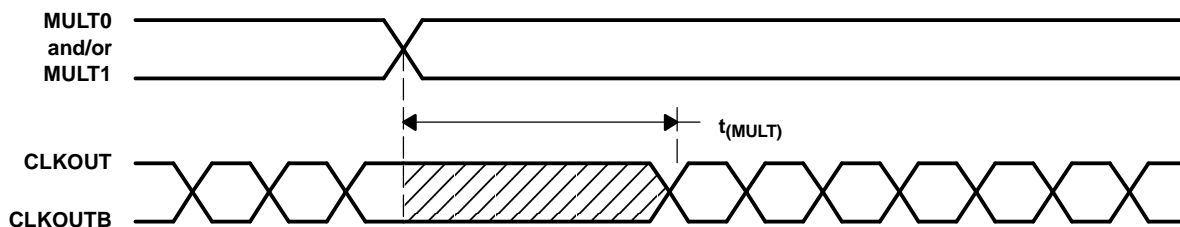
**PARAMETER MEASUREMENT INFORMATION****TESTING CONDITIONS****Figure 1. Test Load and Voltage Definitions  $V_{OH}$ ,  $V_{OL}$ ,  $V_{O(STOP)}$** 

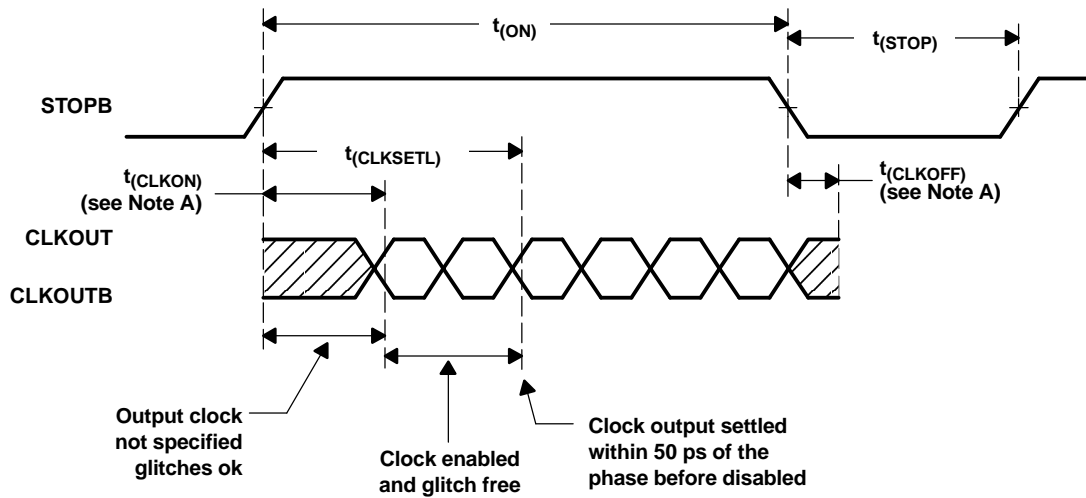
Cycle-to-Cycle Jitter ( $t_{(jitter)}$ ) =  $|t_{CYCLE(i)} - t_{CYCLE(i+1)}|$  over 1000 consecutive cycles

**Figure 2. Cycle-to-Cycle Jitter**

**PARAMETER MEASUREMENT INFORMATION (continued)**

$$\text{Duty Cycle} = (t_{PW+}/t_{\text{CYCLE}})$$

**Figure 3. Output Duty Cycle****Figure 4. Crossing Point Voltage****Figure 5. Voltage Waveforms****Figure 6. PWRDNB Transition Timings****Figure 7. MULT Transition Timings**

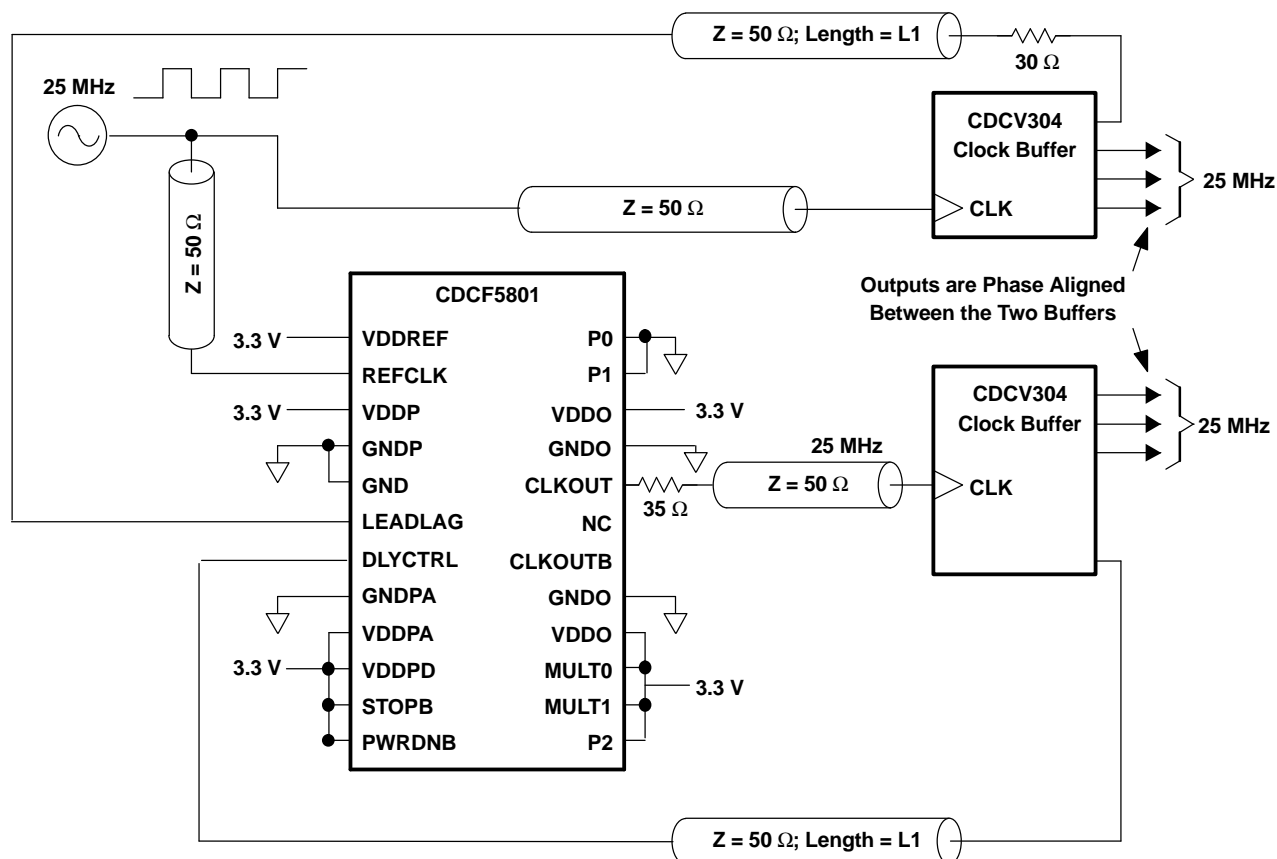
**PARAMETER MEASUREMENT INFORMATION (continued)**

A.  $V_{ref} = V_O \pm 200 \text{ mV}$

**Figure 8. STOPB Transition Timings**

**APPLICATION INFORMATION****APPLICATION EXAMPLE**

The following figure shows an example of using the CDCF5801 as a phase aligner de-skewing the unknown buffer delay of the two CDCV304s in the circuit. This circuitry would not be possible with a simple PLL because the feedback of the PLL would have the second CDCV304 in the loop, causing instability of the PLL due to a long delay.

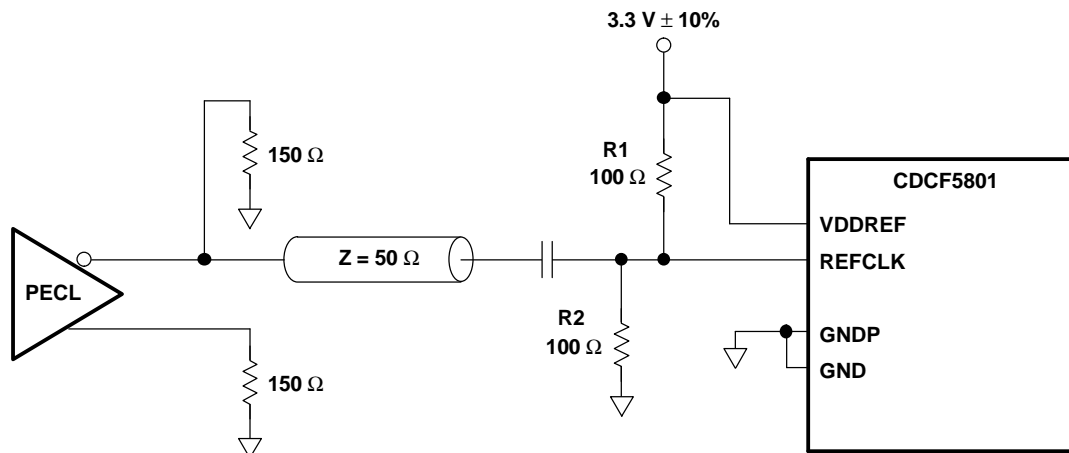
**Figure 9. Application Example****NOTE:**

If an active element (microcontroller, ASIC, DSP, FPYA, DSP, etc.) is used in the CDCF5801 CLKOUT to DLYCTRL feedback loop, see application report SCAA075.

**SELECTING VDDREF**

Generally, VDDREF can be set to any value between 1.2 V and VDD. The setting of VDDREF directly influences the trigger voltage of the input. Special care must be taken when using small signal swings to drive the CDCF5801 input (e.g., PECL). It is recommended to connect VDDREF directly to VDD, ac-couple the REFCLK input, and rebias the signal.

The following circuit is recommended to drive the CDCF5801 from a differential clock signal like PECL.

**APPLICATION INFORMATION (continued)**

- A. NOTE: If more signal swing is required and an unterminated transmission is on option, then R1 and R2 can both be replaced with 10-k $\Omega$  resistors.

**Revision History**

DATE	REV	PAGE	SECTION	DESCRIPTION
29 JUL 05	E	13	Application Example	Changed first paragraph and changed P2 connection in Figure 9
18 DEC 04	D	–	–	Unknown
17 FEB 04	C	–	–	Unknown
15 OCT 03	B	–	–	Unknown
9 OCT 03	A	–	–	Unknown
16 SEP 03	*	–	–	Original version

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CDCF5801DBQ	NRND	SSOP	DBQ	24	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CDCF5801	
CDCF5801DBQG4	NRND	SSOP	DBQ	24	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CDCF5801	
CDCF5801DBQR	NRND	SSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CDCF5801	
CDCF5801DBQRG4	NRND	SSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CDCF5801	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCF5801DBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDC5801DBQR	SSOP	DBQ	24	2500	367.0	367.0	38.0

DBQ (R-PDSO-G24)

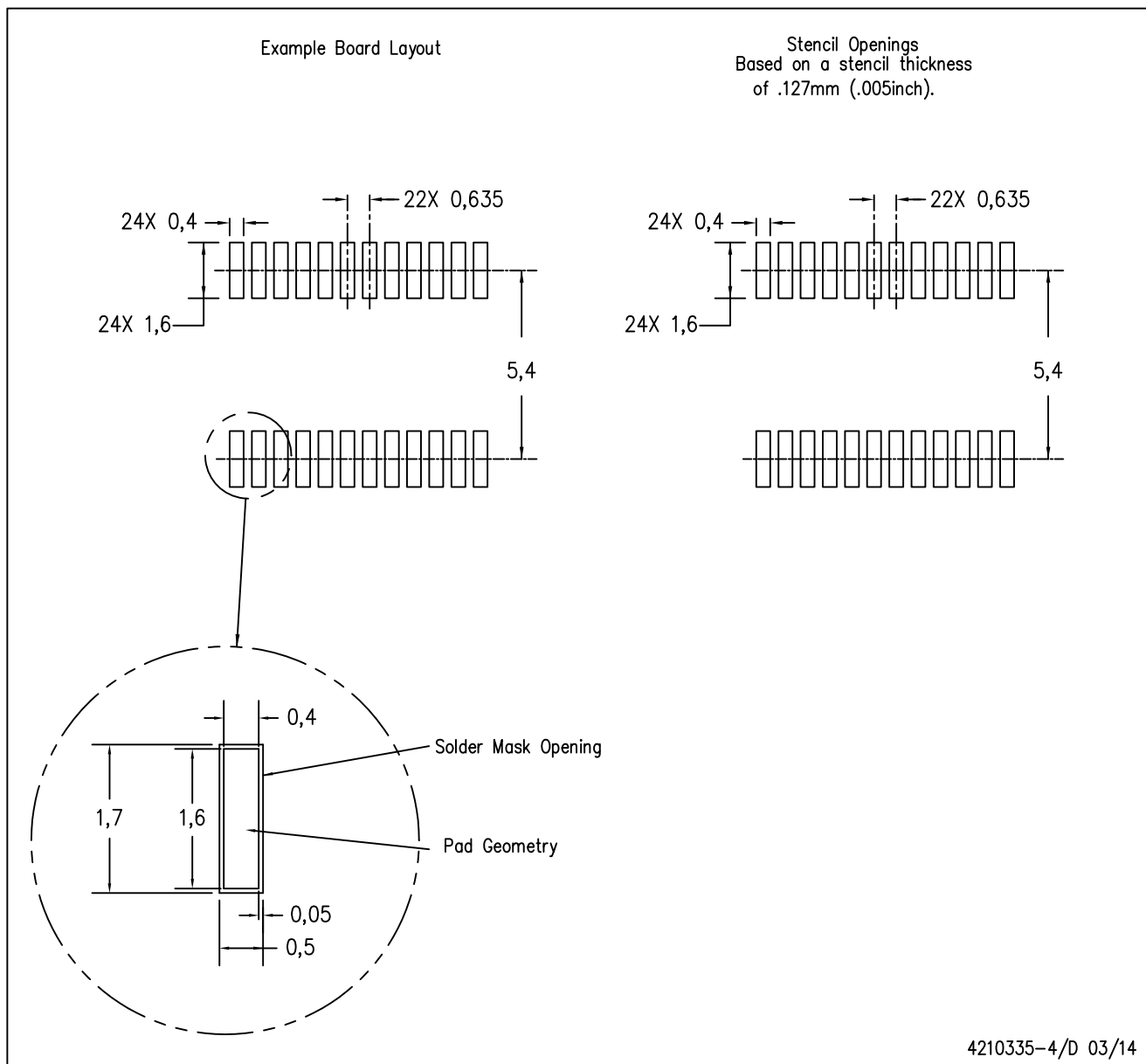
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
  - D. Falls within JEDEC MO-137 variation AE.

DBQ (R-PDSO-G24)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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