



N-channel 650 V, 0.175 Ω , 17 A ultra low gate charge MDmesh™ V Power MOSFET in PowerFLAT™ 8x8 HV package

Datasheet — production data

Features

Order code	V_{DS} @ T_{Jmax}	$R_{DS(on)}$ max	I_D
STL21N65M5	710 V	< 0.190 Ω	17 A ⁽¹⁾

1. The value is rated according to $R_{thj-case}$

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

This device is an N-channel MDmesh™ V Power MOSFET based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

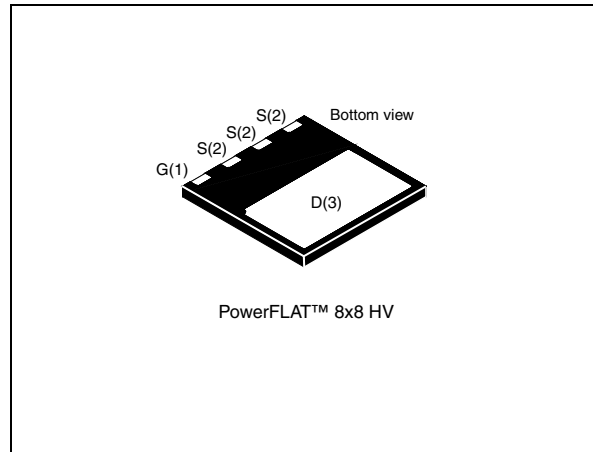


Figure 1. Internal schematic diagram

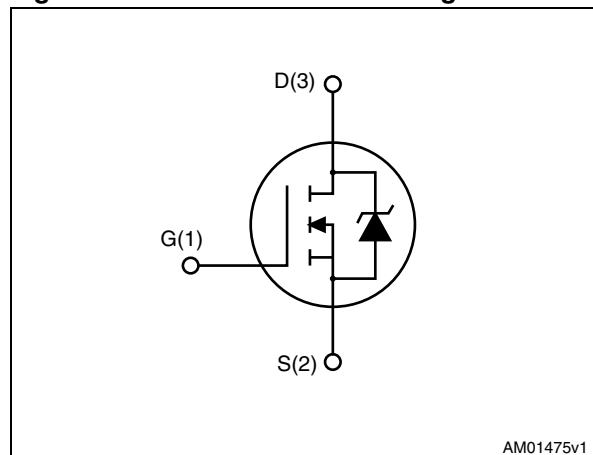


Table 1. Device summary

Order code	Marking	Package	Packaging
STL21N65M5	21N65M5	PowerFLAT™ 8x8 HV	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	650	V
V_{GS}	Gate-source voltage	± 25	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	17	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	11	A
$I_{DM}^{(1),(2)}$	Drain current (pulsed)	68	A
$I_D^{(3)}$	Drain current (continuous) at $T_{amb} = 25\text{ }^\circ\text{C}$	2.7	A
$I_D^{(3)}$	Drain current (continuous) at $T_{amb} = 100\text{ }^\circ\text{C}$	1.7	A
$I_{DM}^{(2),(3)}$	Drain current (pulsed)	10.8	A
$P_{TOT}^{(3)}$	Total dissipation at $T_{amb} = 25\text{ }^\circ\text{C}$	3	W
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	125	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	5	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	400	mJ
$dv/dt^{(4)}$	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	- 55 to 150	$^\circ\text{C}$
T_j	Max. operating junction temperature	150	$^\circ\text{C}$

1. The value is rated according to $R_{thj-case}$.
2. Pulse width limited by safe operating area.
3. When mounted on FR-4 board of 1 inch^2 , 2oz Cu.
4. $I_{SD} \leq 17\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{Peak} < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	1	$^\circ\text{C}/\text{W}$
$R_{thj-amb}^{(1)}$	Thermal resistance junction-amb max	45	$^\circ\text{C}/\text{W}$

1. When mounted on 1 inch^2 FR-4 board, 2 oz Cu.

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	650			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 650\text{ V}$ $V_{DS} = 650\text{ V}$, $T_C = 125\text{ °C}$			1 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 25\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 8.5\text{ A}$		0.175	0.190	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	1950 46 3	-	pF pF pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{DS} = 0\text{ to }520\text{ V}$, $V_{GS} = 0$	-	133	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related		-	44	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	2.5	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 520\text{ V}$, $I_D = 8.5\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 16)	-	44 12 17	-	nC nC nC

1. $C_{oss\text{ eq.}}$ time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. $C_{oss\text{ eq.}}$ energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(off)}$	Turn-off delay time	$V_{DD} = 400\text{ V}$, $I_D = 11\text{ A}$,		37		ns
t_r	Rise time	$R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$	-	10	-	ns
t_c	Cross time	(see Figure 17),		24		ns
t_f	Fall time	(see Figure 20)		12		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		17	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				68	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 17\text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 17\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	-	294		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 100\text{ V}$ (see Figure 17)		4		μC
I_{RRM}	Reverse recovery current			28		A
t_{rr}	Reverse recovery time	$I_{SD} = 17\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	-	340		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 100\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$		5		μC
I_{RRM}	Reverse recovery current	(see Figure 17)		29		A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

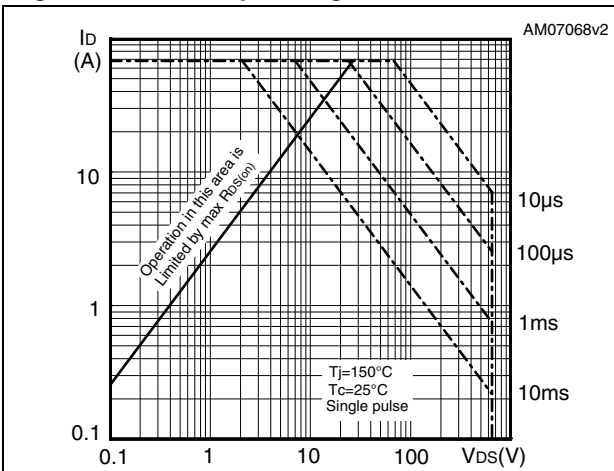


Figure 3. Thermal impedance

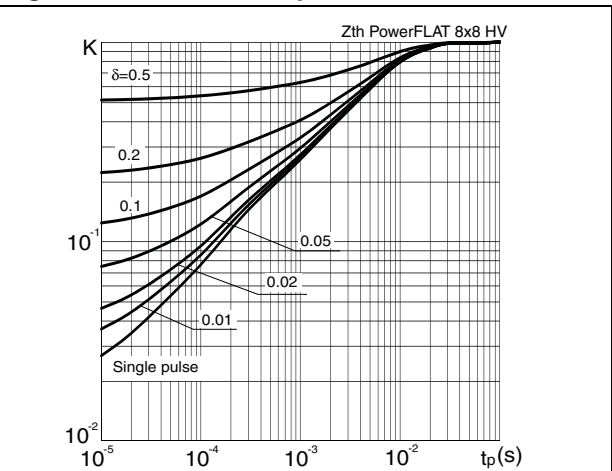


Figure 4. Output characteristics

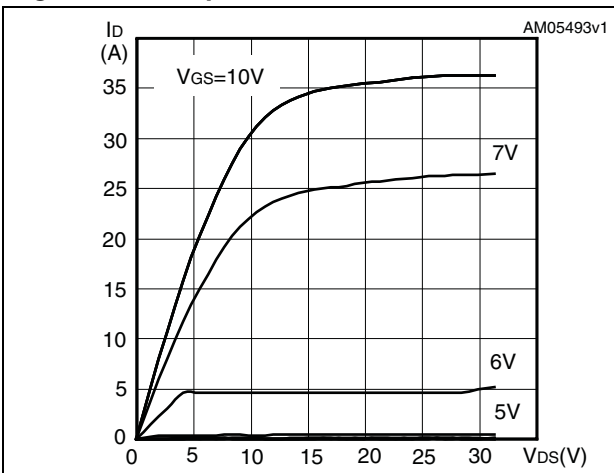


Figure 5. Transfer characteristics

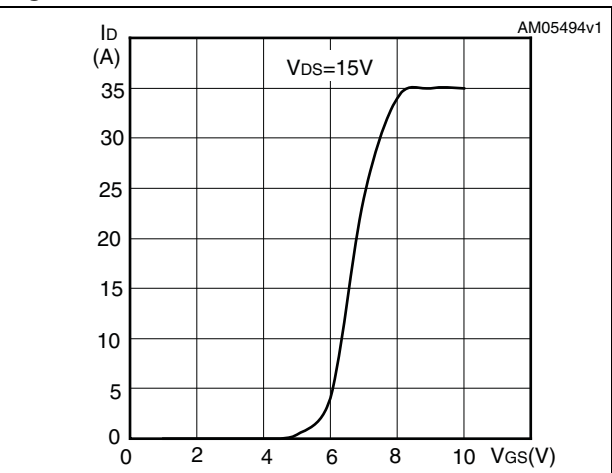


Figure 6. Gate charge vs gate-source voltage

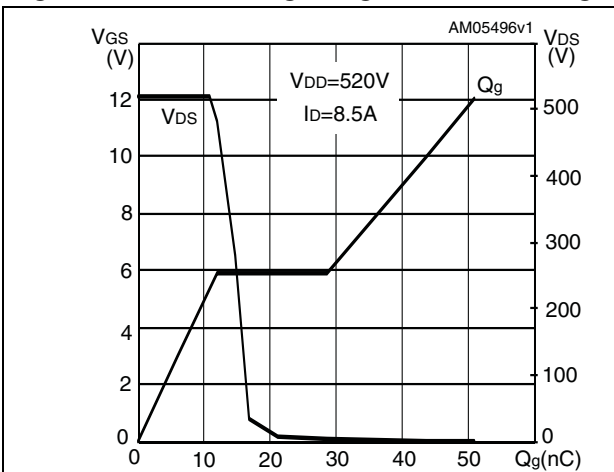


Figure 7. Static drain-source on-resistance

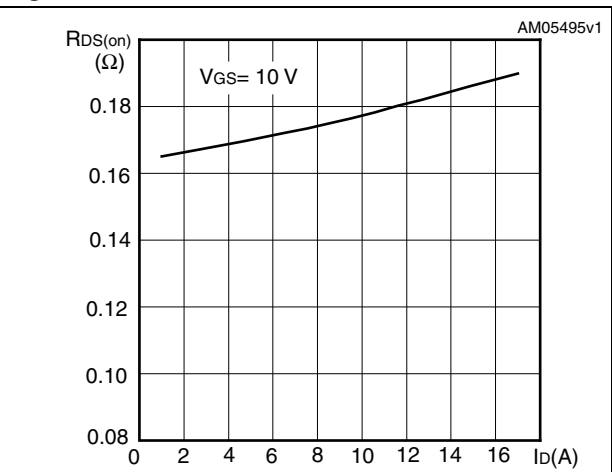


Figure 8. Output capacitance stored energy Figure 9. Capacitance variations

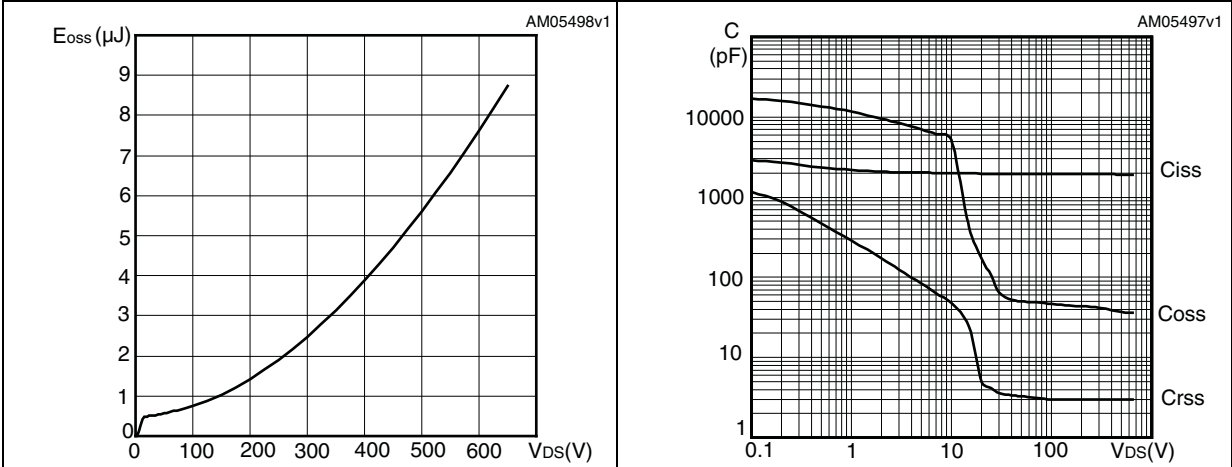


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on-resistance vs temperature

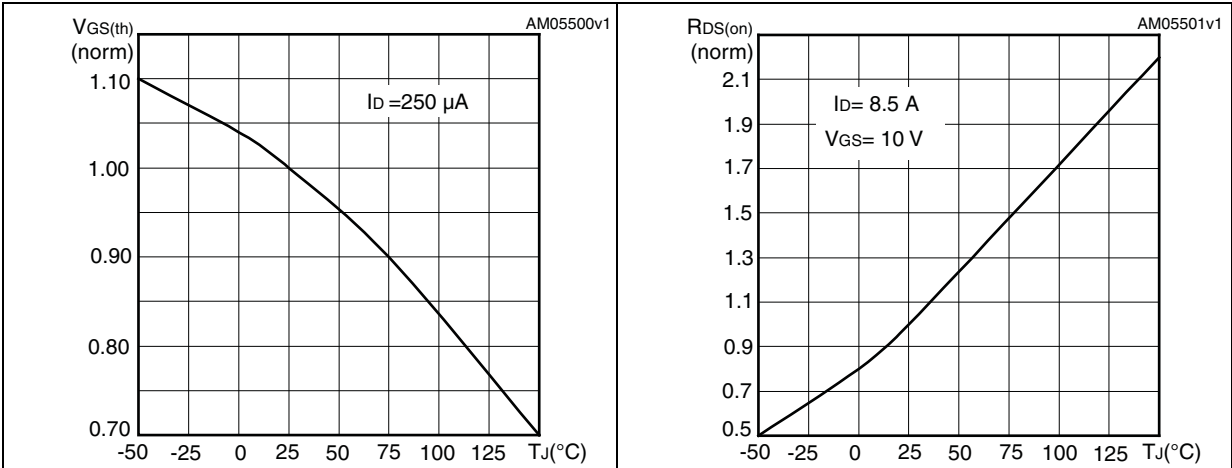


Figure 12. Source-drain diode forward characteristics Figure 13. Normalized V_{DS} vs temperature

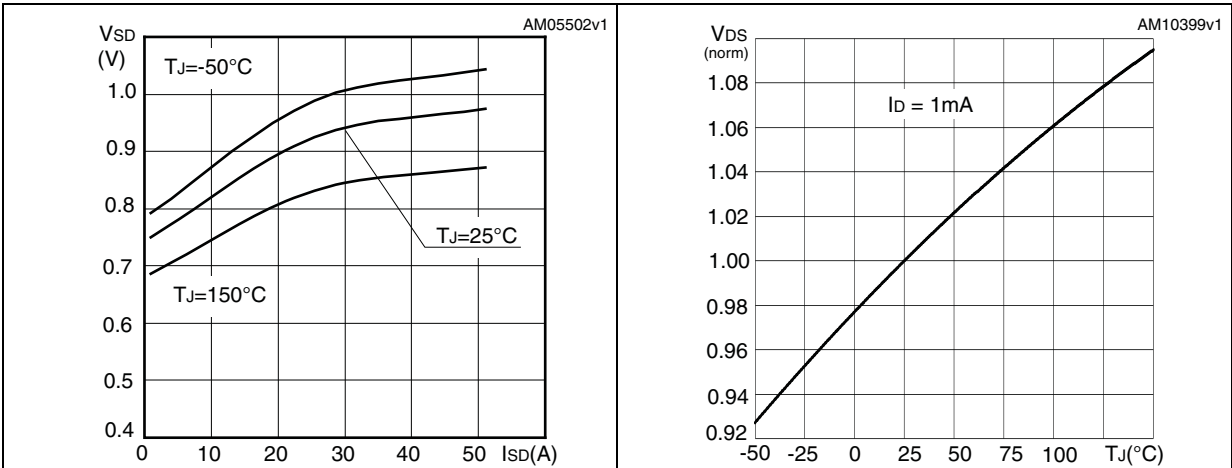
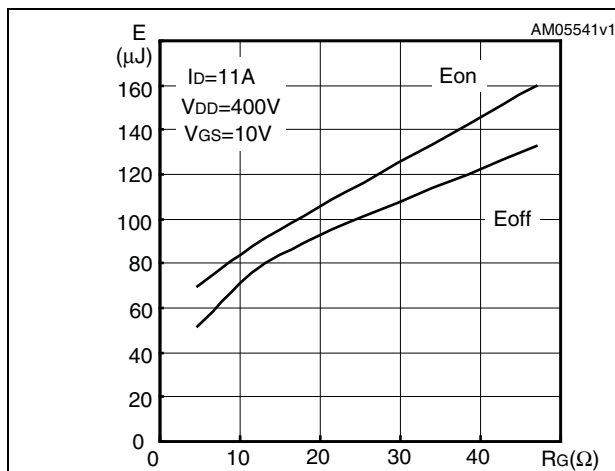


Figure 14. Switching losses vs gate resistance
(1)



1. E_{on} including reverse recovery of a SiC diode

3 Test circuits

Figure 15. Switching times test circuit for resistive load

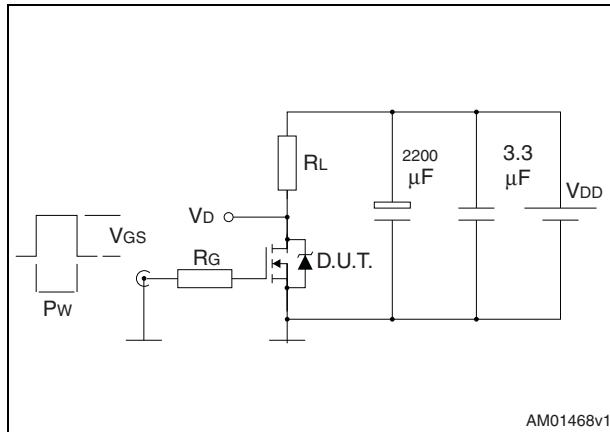


Figure 16. Gate charge test circuit

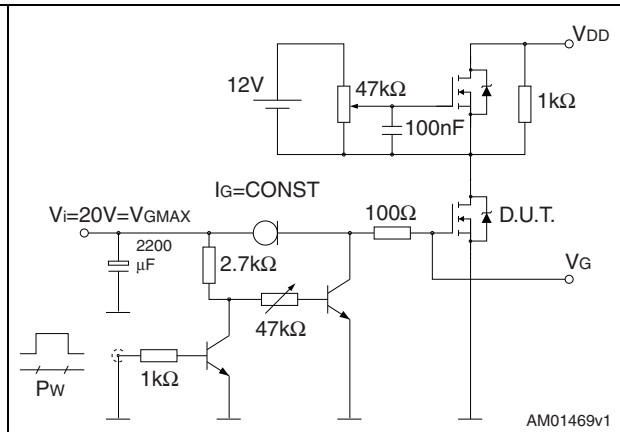


Figure 17. Test circuit for inductive load switching and diode recovery times

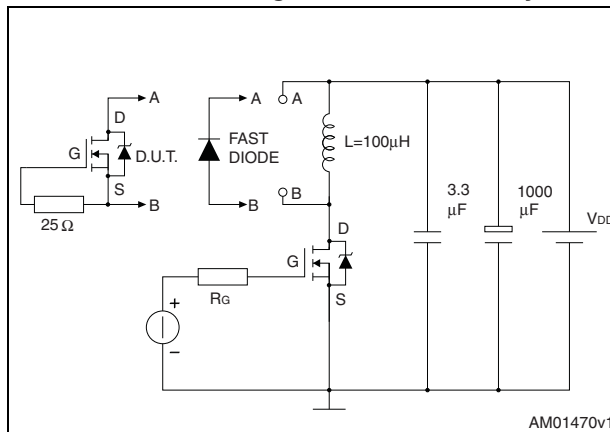


Figure 18. Unclamped inductive load test circuit

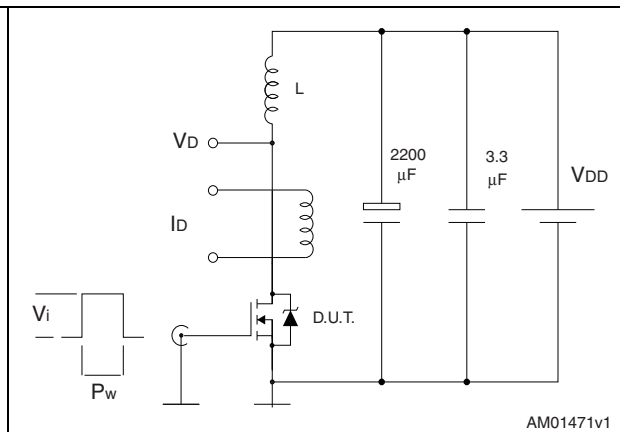


Figure 19. Unclamped inductive waveform

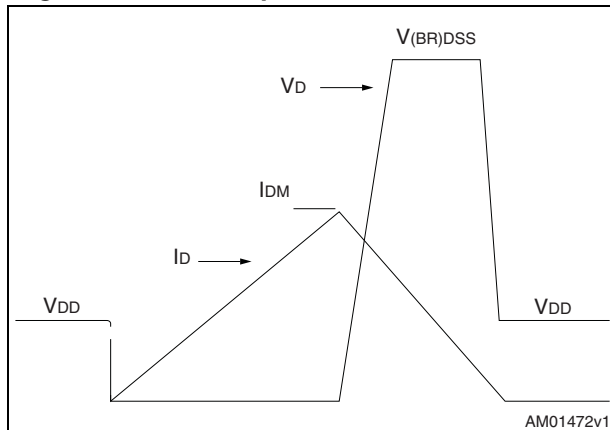
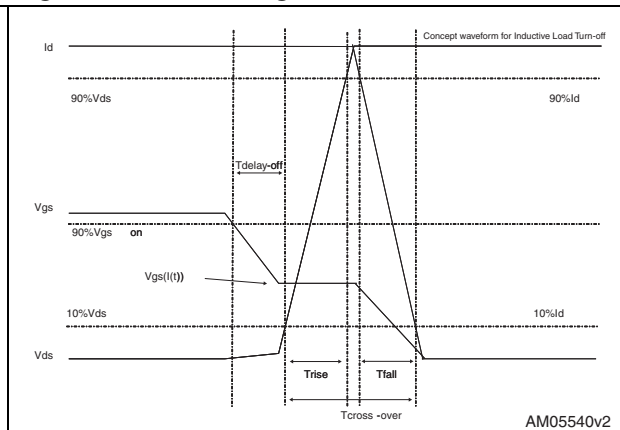


Figure 20. Switching time waveform



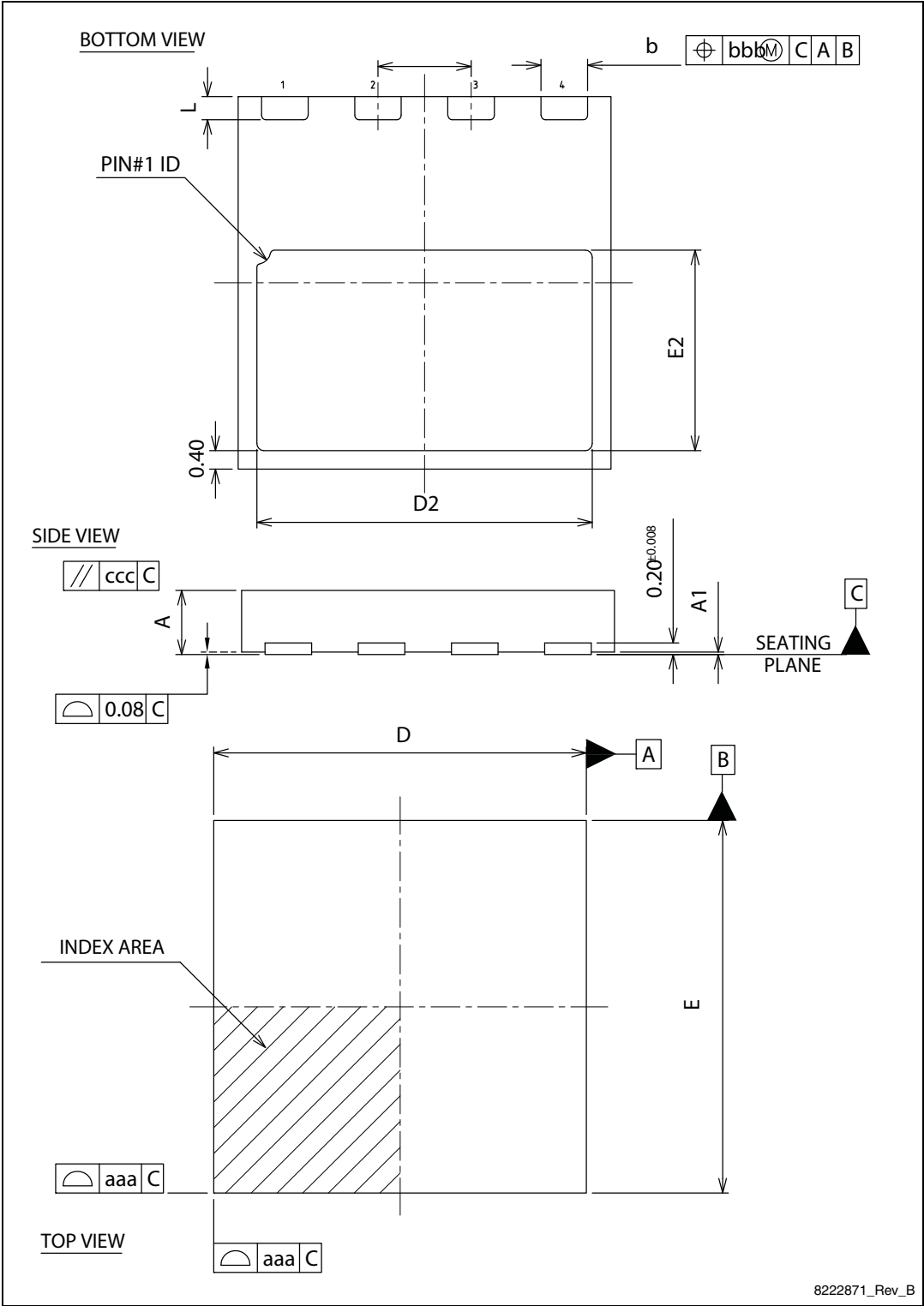
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. PowerFLAT™ 8x8 HV mechanical data

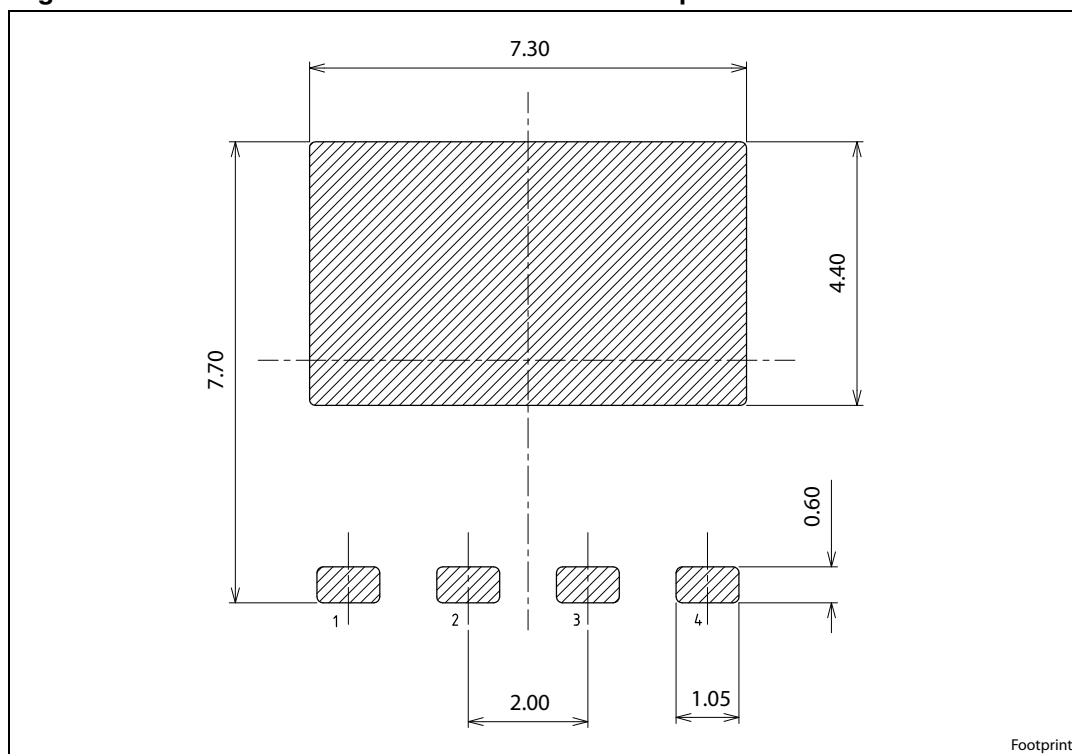
Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.95	1.00	1.05
D		8.00	
E		8.00	
D2	7.05	7.20	7.30
E2	4.15	4.30	4.40
e		2.00	
L	0.40	0.50	0.60
aaa		0.10	
bbb		0.10	
ccc		0.10	

Figure 21. PowerFLAT™ 8x8 HV drawing mechanical data



8222871_Rev_B

Figure 22. PowerFLAT™ 8x8 HV recommended footprint



5 Packaging mechanical data

Figure 23. PowerFLAT™ 8x8 HV tape

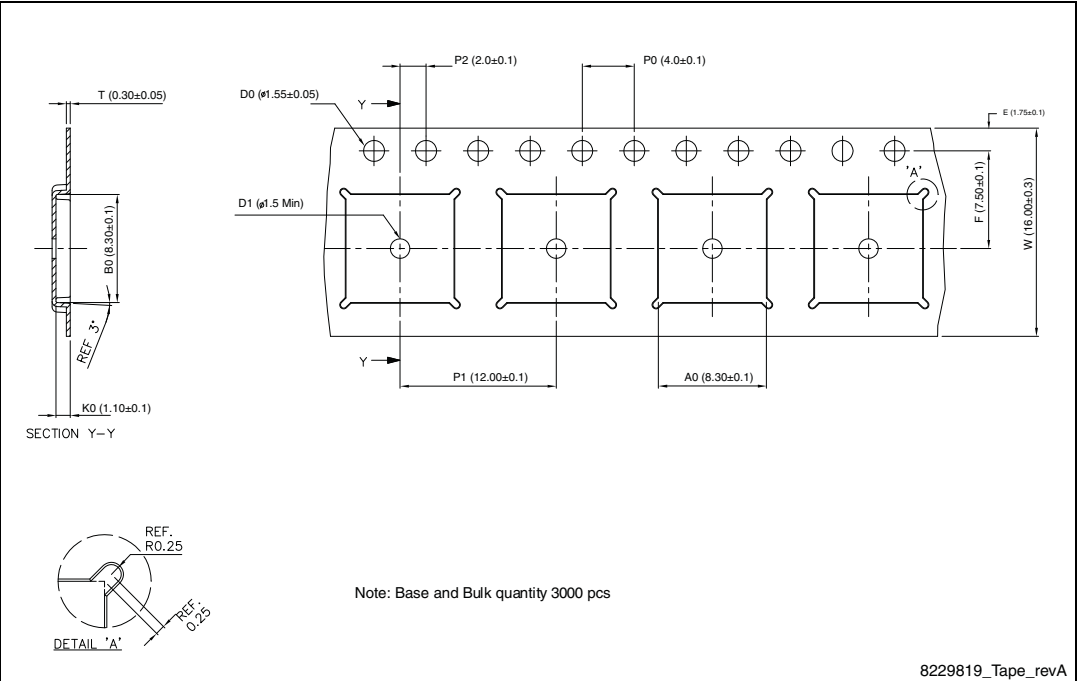
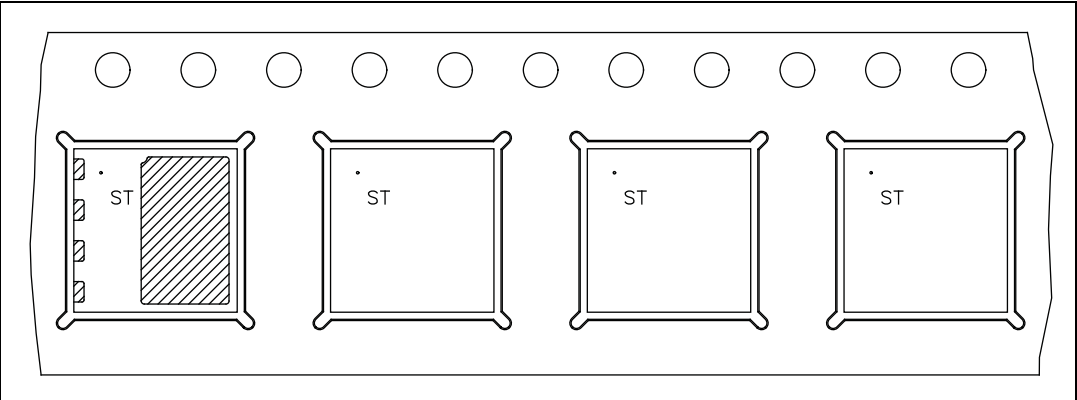


Figure 24. PowerFLAT™ 8x8 HV package orientation in carrier tape



Technical drawing of a reel-to-reel tape reel, showing front, side, and detail views.

Front View (Left): Shows a circular reel with three slots. Key dimensions include:

- Overall diameter: $\phi 330.0 \pm 0.20$
- Slot width: $4.0W \times 10.0D$ CUT SLOT (3 PLCS)
- Slot depth: 10.0
- Slot spacing: 6.5 ± 0.18
- Slot angle: 120°
- Slot radius: $R57.7$
- Slot thickness: 2.0
- Slot position: $\phi 21.2$
- Slot offset: 1.0
- Slot angle: 60°
- Slot radius: $R4.6$
- Slot thickness: 0.6
- Slot position: $\phi 13.1 \pm 0.13$

Side View (Bottom): Shows the profile of the reel. Key dimensions include:

- Overall height: 18.4 ± 0.20
- Slot height: 2.7 ± 0.14
- Slot depth: 0.6
- Slot width: $\phi 100 \pm 0.20$
- Slot spacing: 2.0
- Slot position: $\phi 330.0 \pm 0.20$

Detail View (Right): Shows a close-up of the slot. Key dimensions include:

- Slot width: 6.5 ± 0.18
- Slot depth: 0.6
- Slot position: $\phi 13.1 \pm 0.13$
- Slot radius: $R113$
- Slot thickness: 2.0
- Slot angle: 120°
- Slot radius: $R50$
- Slot thickness: 0.6
- Slot position: $\phi 21.2$
- Slot offset: 1.0
- Slot angle: 60°
- Slot radius: $R4.6$
- Slot thickness: 0.6
- Slot position: $\phi 13.1 \pm 0.13$

Reference: SEE DETAIL C

6 Revision history

Table 9. Document revision history

Date	Revision	Changes
28-Apr-2010	1	First release.
14-Jun-2010	2	$R_{DS(on)}$ typical value has been corrected.
14-Mar-2011	3	Figure 2: Safe operating area , Figure 3: Thermal impedance and Figure 7: Static drain-source on-resistance have been updated.
18-May-2011	4	$R_{DS(on)}$ limits in Table 4 have been updated.
29-May-2011	5	Section 4: Package mechanical data has been updated. Added new section: Section 5: Packaging mechanical data . Minor text changes.

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