SLG59H1010V

A 13.3 mΩ, 5 A, Integrated Power Switch with 12V/24V Input Lockout Select and MOSFET Current Monitor Output

General Description

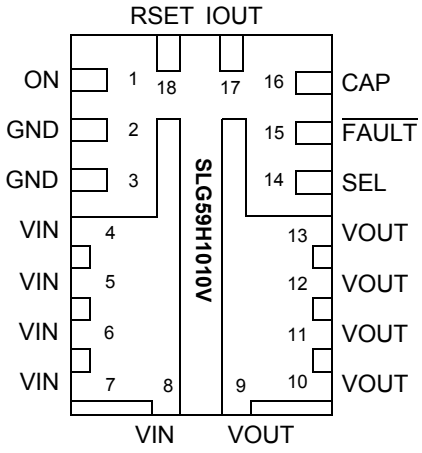
The SLG59H1010V is a high-performance 13.3 mΩ NMOS power switch designed to control 12 V or 24 V power rails up to 5A. Using a proprietary MOSFET design, the SLG59H1010V achieves a stable 13.3 mΩ RDS_{ON} across a wide input/supply voltage range and over temperature. Using Silego's proprietary CuFET™ technology, the SLG59H1010V package also exhibits a low thermal resistance for high-current operation.

Designed to operate over a -40°C to 85°C range, the SLG59H1010V is available in a low thermal resistance, RoHS-compliant, 1.6 x 3.0 mm STQFN package.

Features

- Wide Operating Supply Voltage: 12 V or 24 V
- Maximum Continuous Switch Current: 5 A
- Automatic nFET SOA Protection
- High-performance MOSFET Switch
  - Low RDS_{ON}: 13.3 mΩ at V_{IN} = 24 V
  - Low $\Delta RDS_{ON}/\Delta V_{IN}$: <0.05 mΩ/V
  - Low $\Delta RDS_{ON}/\Delta T$: <0.06 mΩ/°C
- Pin-programmable 12V/24V Input Overvoltage and Undervoltage Lockout
- Capacitor-programmable Inrush Current Control
- Two stage Current Limit Protection:
  - Resistor-programmable Active Current Limit
  - Internal Short-circuit Current limit
- Open Drain $\overline{FAULT}$ Signaling
- MOSFET Current Analog Output Monitor: 10 µA/A
- Fast 4 kΩ Output Discharge
- Pb-Free / Halogen-Free / RoHS Compliant Packaging

Pin Configuration

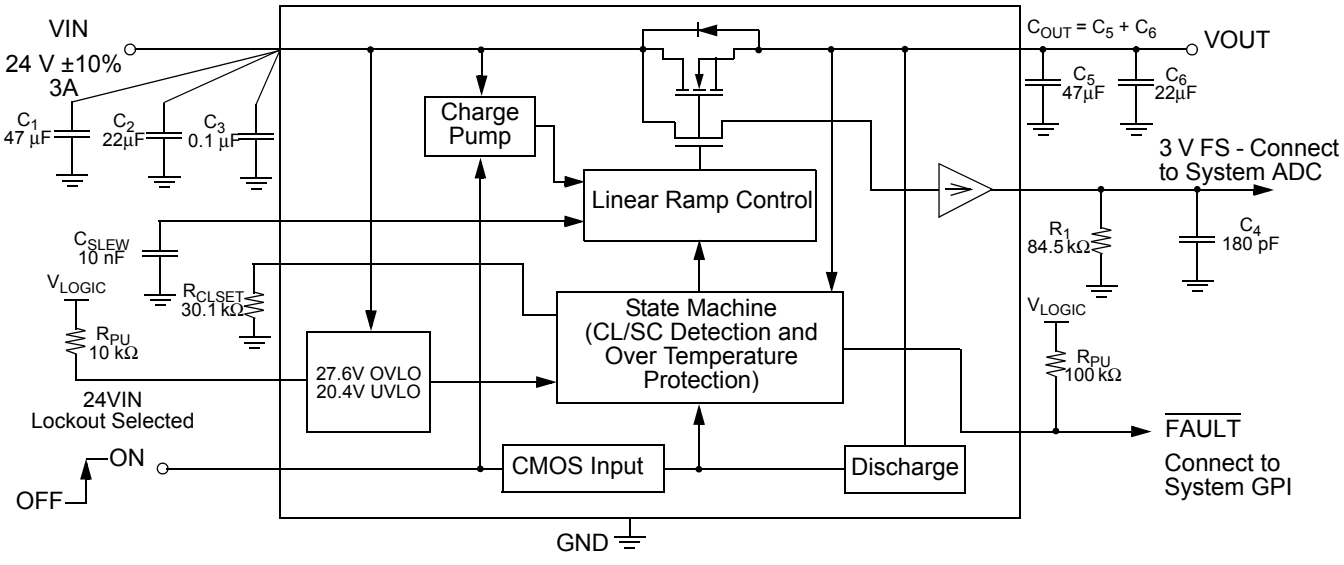


18-pin STQFN
1.6 x 3.0 mm, 0.40mm pitch
(Top View)

Applications

- Power-Rail Switching
- Multifunction Printers
- Large-format Copiers
- Telecommunications Equipment
- High-performance Computing
  - 12 V and 24 V Point-of-Load Power Distribution
- Motor Drives

Block Diagram and 3 A Typical Application Circuit



Pin Description

Pin #	Pin Name	Type	Pin Description
1	ON	Input	A low-to-high transition on this pin initiates the operation of the SLG59H1010V's state machine. ON is an asserted HIGH, level-sensitive CMOS input with V_{IL} < 0.3 V and VIH > 0.9 V. As the ON pin input circuit does not have an internal pull-down resistor, connect this pin to a general-purpose output (GPO) of a microcontroller, an application processor, or a system controller – do not allow this pin to be open-circuited.
2	GND	GND	Pin 2 is a low-current GND terminal for the SLG59H1010V. Connect directly to Pin 3
3	GND	GND	Pin 3 is the main ground connection for the SLG59H1010V's internal charge pump, its gate drive and current-limit circuits as well as its internal state machine. Therefore, use a short, stout connection from Pin 3 to the system's analog or power plane.
4-8	VIN	MOSFET	VIN supplies the power for the operation of the SLG59H1010V, its internal control circuitry, and the drain terminal of the nFET power switch. With 5 pins fused together at VIN, connect a 47 µF (or larger) low-ESR capacitor from this pin to ground. Capacitors used at VIN should be rated at 50 V or higher.
9-13	VOUT	MOSFET	Source terminal of n-channel MOSFET (5 pins fused for VOUT). Connect a 47 µF (or larger) low-ESR capacitor from this pin to ground. Capacitors used at VOUT should be rated at 50 V or higher.
14	SEL	Input	As a low logic-level CMOS input with V_{IL} < 0.3 V and V_{IH} > 1.65 V, SEL selects one of two undervoltage/overvoltage lockout windows. When SEL = LOW, the V_{IN} undervoltage/overvoltage lockout window is set for 12 V ±10% applications. When SEL = HIGH, the V_{IN} undervoltage/overvoltage lockout window is set for 24 V ±10% applications. See the Electrical Characteristics table for additional information.
15	$\overline{\text{FAULT}}$	Output	An open drain output, $\overline{\text{FAULT}}$ is asserted within $TFAULT_{LOW}$ when a V_{IN} undervoltage, V_{IN} overvoltage, a current-limit, a nFET SOA, or an over-temperature condition is detected. $\overline{\text{FAULT}}$ is deasserted within $TFAULT_{HIGH}$ when the fault condition is removed. Connect an 100 kΩ external resistor from the $\overline{\text{FAULT}}$ pin to local system logic supply.
16	CAP	Output	A low-ESR, stable dielectric, ceramic surface-mount capacitor connected from CAP pin to GND sets the V_{OUT} slew rate and overall turn-on time of the SLG59H1010V. For best performance, the range for CAP values are 10 nF ≤ CAP ≤ 20 nF – please see typical characteristics for additional information. Capacitors used at the CAP pin should be rated at 10 V or higher. See equation for selecting capacitor and start-up slewing.
17	IOUT	Output	IOUT is the SLG59H1010V's power MOSFET load current monitor output. As an analog output current, this signal when applied to a ground-reference resistor generates a voltage proportional to the current through the n-channel MOSFET. The IOUT transfer characteristic is typically 10 µA/A with a voltage compliance range of 0.5 V ≤ V(IOUT) ≤ 4V. Optimal IOUT linearity is exhibited for 0.5 A ≤ IDS ≤ 5 A. In addition, it is recommended to bypass the IOUT pin to GND with a 0.18 nF capacitor.
18	RSET	Input	A 1%-tolerance, metal-film resistor between 18 kΩ and 95 kΩ sets the SLG59H1010V's active current limit. A 95 kΩ resistor sets the SLG59H1010V's active current limit to 1 A and a 18 kΩ resistor sets the active current limit to 5 A.

Ordering Information

Part Number	Type	Production Flow
SLG59H1010V	STQFN 18L FC	Industrial, -40 °C to 85 °C
SLG59H1010VTR	STQFN 18L FC (Tape and Reel)	Industrial, -40 °C to 85 °C

Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IN} to GND	Power Switch Input Voltage to GND	Continuous	-0.3	--	30	V
		Maximum pulsed VIN, pulse width <0.1s	--	--	32	V
V_{OUT} to GND	Power Switch Output Voltage to GND		-0.3	--	VIN	V
ON, SEL, CAP, RSET, IOUT, and $\overline{FAULT}$ to GND	ON, SEL, CAP, RSET, IOUT, and FAULT Pin Voltages to GND		-0.3	--	7	V
T_S	Storage Temperature		-65	--	150	°C
ESD_{HBM}	ESD Protection	Human Body Model	2000	--	--	V
ESD_{CDM}	ESD Protection	Charged Device Model	500	--	--	V
MSL	Moisture Sensitivity Level			1		
θ_{JA}	Thermal Resistance	1.6 x 3.0 mm 18L STQFN; Determined with the device mounted onto a 1 in^2, 1 oz. copper pad of FR-4 material	--	40	--	°C/W
MOSFET IDS_{CONT}	Continuous Current from VIN to VOUT	T_J < 150°C	--	--	5	A
MOSFET IDS_{PEAK}	Peak Current from VIN to VOUT	Maximum pulsed switch current, pulse width < 1 ms	--	--	6	A

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

12 V ≤ V_{IN} ≤ 24 V; CIN = 47 µF, T_A = -40°C to 85°C, unless otherwise noted. Typical values are at T_A = 25°C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating Input Voltage		10.8	--	26.4	V
$V_{IN(OVLO)}$	VIN Overvoltage Lockout Threshold	V_{IN} ↑; SEL = HIGH	26.5	27	28.5	V
		V_{IN} ↑; SEL = LOW	13.3	13.7	14.5	V
$V_{IN(UVLO)}$	VIN Undervoltage Lockout Threshold	V_{IN} ↓; SEL = HIGH	19.5	20.5	21.5	V
		V_{IN} ↓; SEL = LOW	9.7	10.2	10.7	V
I_Q	Quiescent Supply Current	ON = HIGH; I_{DS} = 0 A	--	0.5	0.6	mA
I_{SHDN}	OFF Mode Supply Current	ON = LOW; I_{DS} = 0 A	--	1	3	µA
RDS_{ON}	Static Drain to Source ON Resistance	T_A = 25°C; I_{DS} = 0.1 A	--	13.3	14.5	mΩ
		T_A = 85°C; I_{DS} = 0.1 A	--	17.2	18	mΩ
I_{LIMIT}	Active Current Limit, I_{ACL}	V_{OUT} > 0.5 V; R_{SET} = 30.1 kΩ	3.0	3.19	3.5	A
	Short-circuit Current Limit, I_{SCL}	V_{OUT} < 0.5 V	--	0.5	-	A
T_{ACL}	Active Current Limit Response Time	R_{SET} = 51.6 kΩ	--	120	--	µs
R_{DSCHRG}	Output Discharge Resistance		3.5	4.4	5.3	kΩ

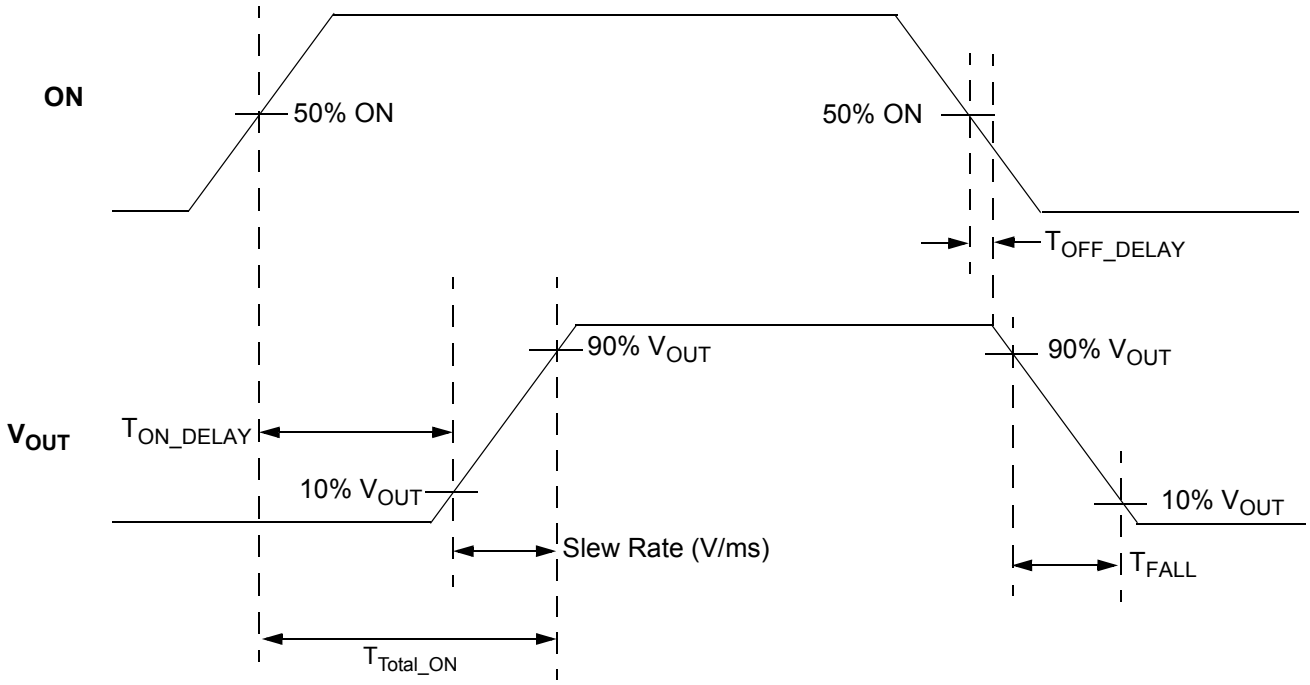
Electrical Characteristics (continued)

12 V ≤ V_{IN} ≤ 24 V; CIN = 47 µF, T_A = -40°C to 85°C, unless otherwise noted. Typical values are at T_A = 25°C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
I_{OUT}	MOSFET Current Analog Monitor Output	I_{LOAD} = 1 A	9.3	10	10.9	µA
		I_{LOAD} = 3 A	28.5	30	31.7	µA
T_{IOUT}	I_{OUT} Response Time to Change in Main MOSFET Current	C_{IOUT} = 180 pF; Step load 0 to 2.4 A; 0% to 90% I_{OUT}	--	45	--	µs
CAP_{OUT}	Output Capacitive Load to GND		47	--	--	µF
T_{ON_Delay}	ON Delay Time	50% ON to 10% V_{OUT} ↑; V_{IN} = 12 V; CAP = 10 nF; R_{LOAD} = 100 Ω, C_{LOAD} = 10 µF	480	600	720	µs
		50% ON to 10% V_{OUT} ↑; V_{IN} = 24 V; CAP = 10 nF; R_{LOAD} = 100 Ω, C_{LOAD} = 10µF	0.8	1.0	1.2	ms
T_{Total_ON}	Total Turn-on Time	50% ON to 90% V_{OUT} ↑	Set by External CAP[1]			ms
		50% ON to 90% V_{OUT} ↑; V_{IN} = 12 V; CAP = 10 nF; R_{LOAD} = 100 Ω, C_{LOAD} = 10 µF	2.9	3.6	4.3	ms
		50% ON to 90% V_{OUT} ↑; V_{IN} = 24 V; CAP = 10 nF; R_{LOAD} = 100 Ω, C_{LOAD} = 10 µF	5.7	7.1	8.5	ms
$V_{OUT(SR)}$	VOUT Slew rate	10% V_{OUT} to 90% V_{OUT} ↑	Set by External CAP[1]			V/ms
		10% V_{OUT} to 90% V_{OUT} ↑; V_{IN} = 12 V or 24 V; CAP = 10 nF; R_{LOAD} = 100 Ω, C_{LOAD} = 10 µF	2.7	3.2	3.9	V/ms
T_{OFF_Delay}	OFF Delay Time	50% ON to V_{OUT} ↓; R_{LOAD} = 100 Ω, No C_{LOAD}	--	15	--	µs
T_{Fall}	VOUT Fall Time	ON = HIGH-to-LOW; R_{LOAD} = 100 Ω, No C_{LOAD}	10.4	12.7	15	µs
$TFAULT_{LOW}$	$\overline{FAULT}$ Assertion Time	Current-limit Detection to FAULT↓; I_{ACL} = 1 A; V_{IN} = 24 V; R_{SET} = 95 kΩ; switch in 20 Ω load	--	80	--	µs
$TFAULT_{HIGH}$	$\overline{FAULT}$ De-assertion Time	Delay to FAULT↑ after fault condition is removed; I_{ACL} = 1 A; V_{IN} = 24 V; R_{SET} = 95 kΩ; switch out 20 Ω load	--	180	--	µs
$\overline{FAULT}_{VOL}$	$\overline{FAULT}$ Output Low Voltage	$I_{\overline{FAULT}}$ = 1 mA	--	0.2	--	V
ON_VIH	ON Pin Input High Voltage		0.9	--	5	V
ON_VIL	ON Pin Input Low Voltage		-0.3	0	0.3	V
SEL_VIH	SEL pin Input High Voltage		1.65	--	4.5	V
SEL_VIL	SEL pin Input Low Voltage		-0.3	--	0.3	V
$I_{ON(Leakage)}$	ON Pin Leakage Current	1 V ≤ ON ≤ 5 V or ON = GND	--	--	1	µA
$THERM_{ON}$	Thermal Protection Shutdown Threshold		--	125	--	°C
$THERM_{OFF}$	Thermal Protection Restart Threshold		--	100	--	°C

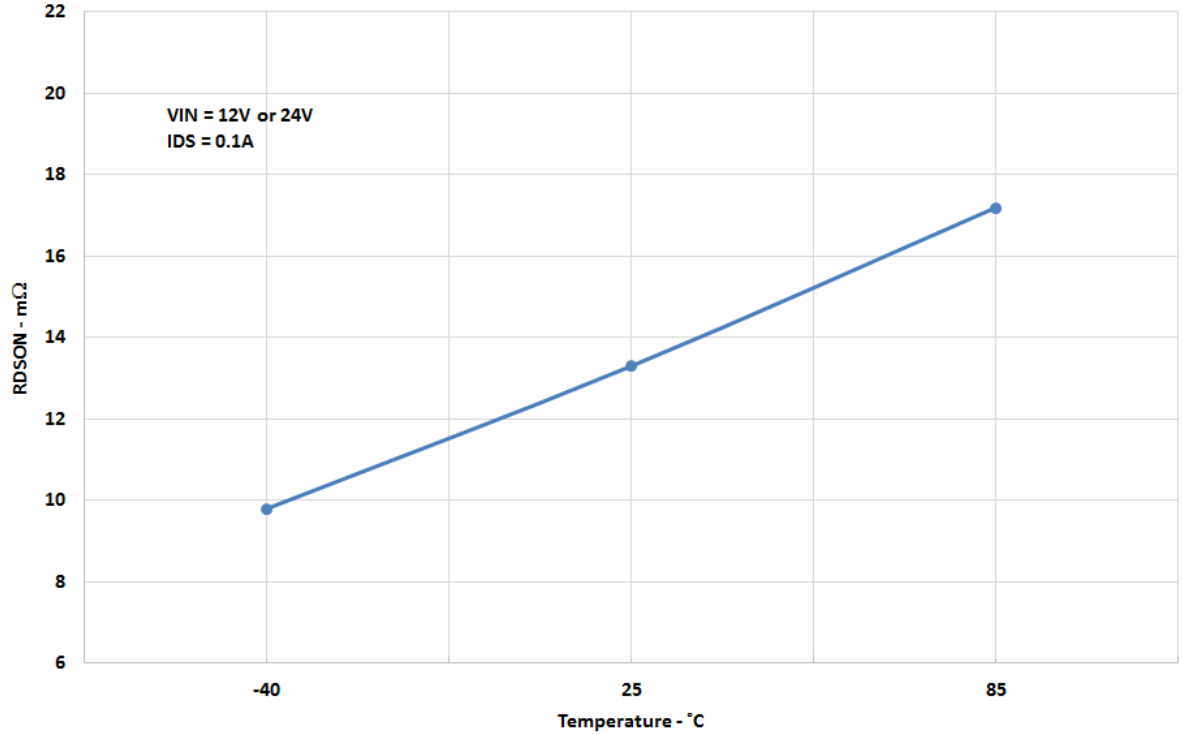
Notes:
1. Refer to typical Timing Parameter vs. CAP performance charts for additional information.

T_{Total_ON}, T_{ON_Delay} and Slew Rate Measurement Timing Details

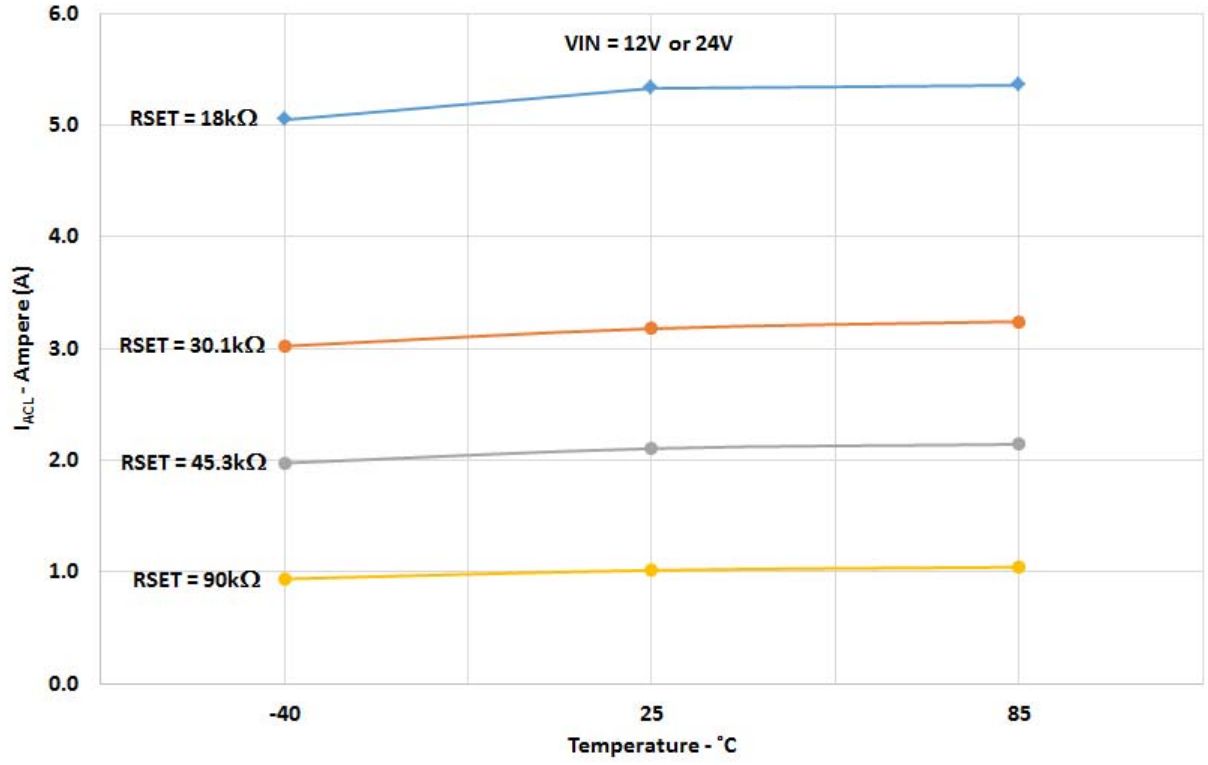


Typical Performance Characteristics

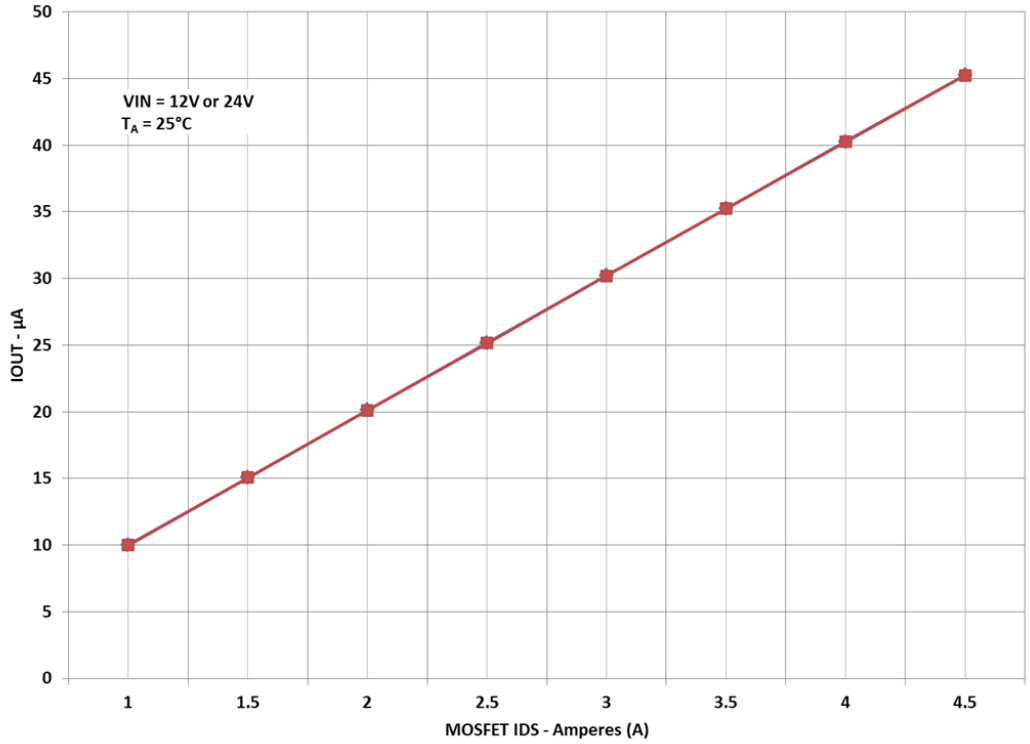
RDS_{ON} vs. Temperature and V_{IN}



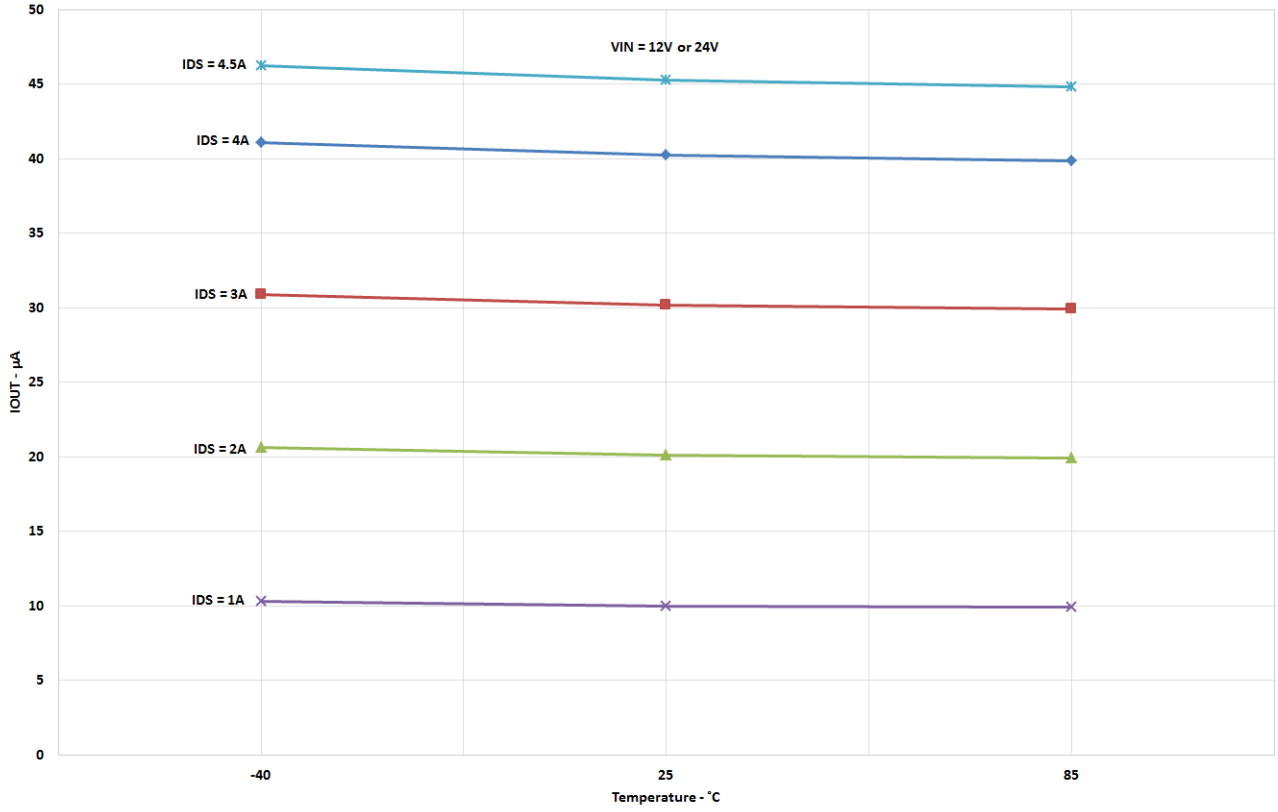
I_{ACL} vs. Temperature and R_{SET}



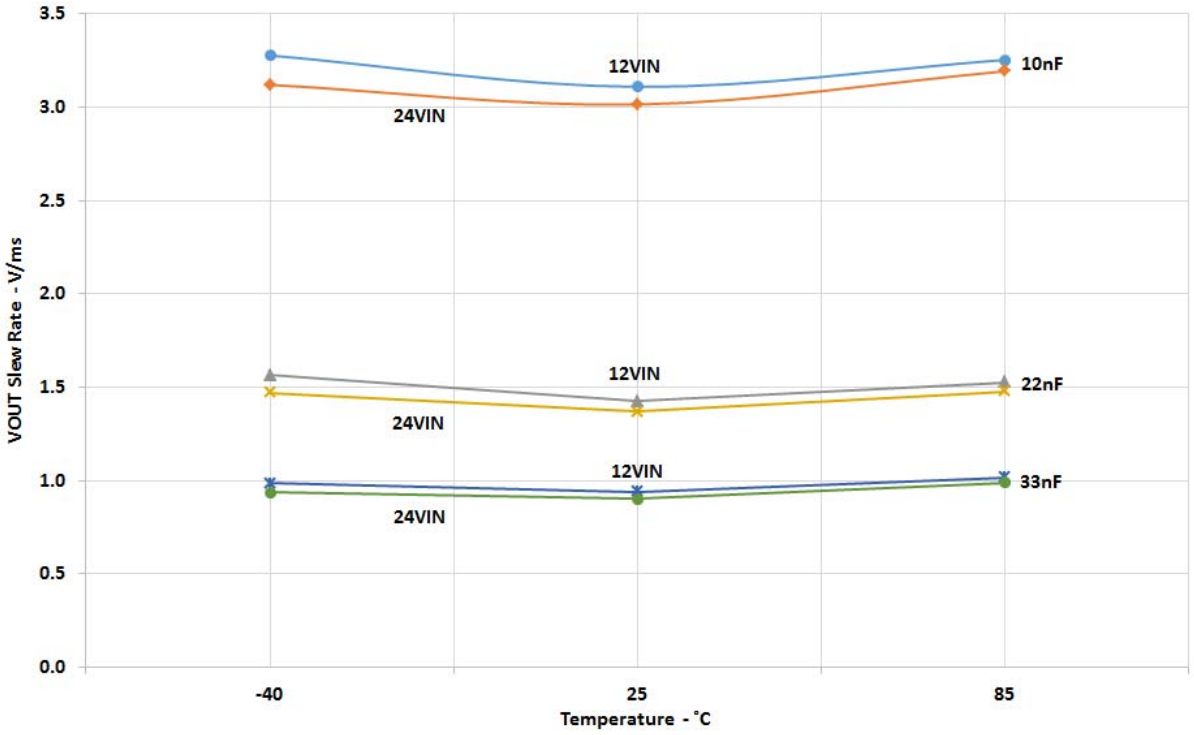
I_{OUT} vs. MOSFET IDS and V_{IN}



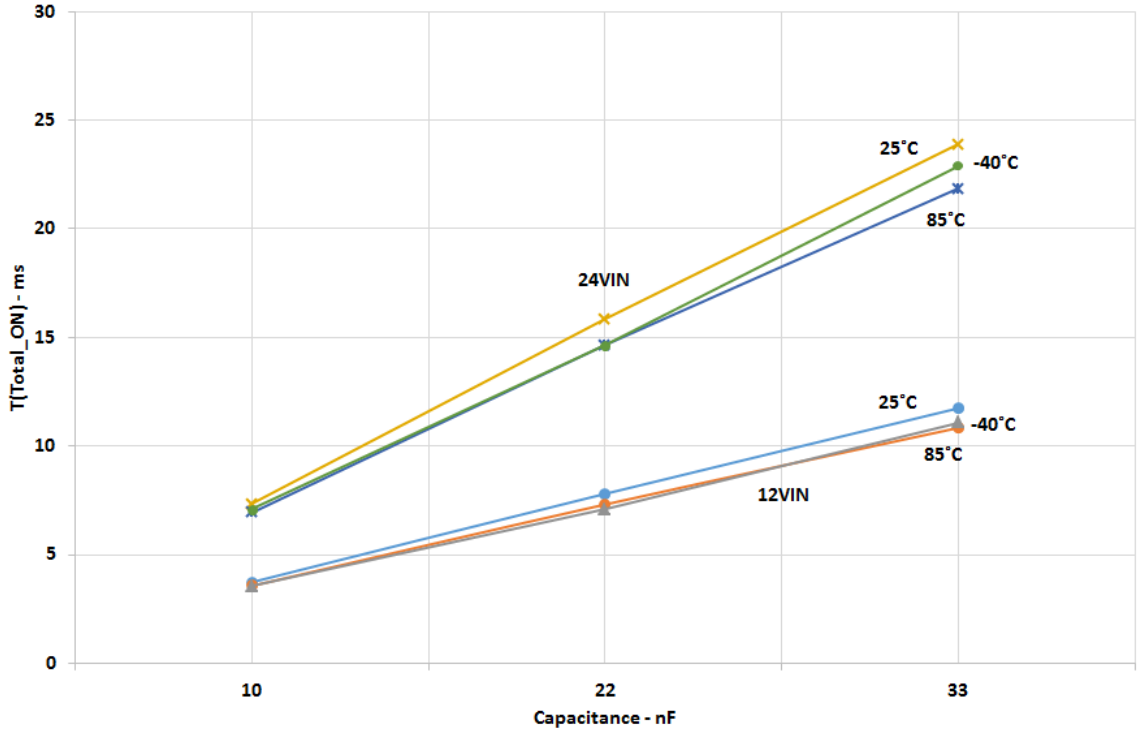
I_{OUT} vs. Temperature and MOSFET IDS



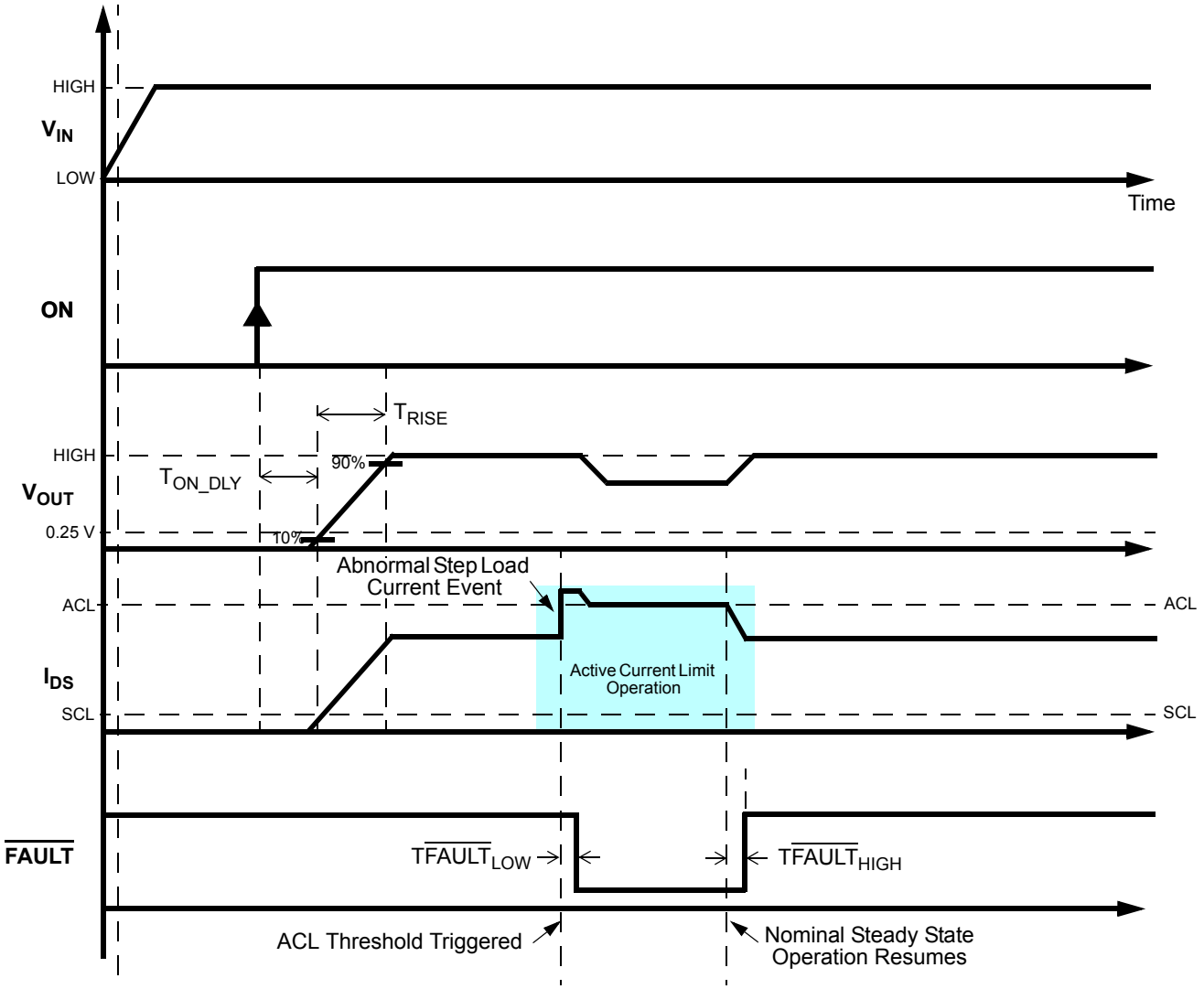
V_{OUT} Slew Rate vs. Temperature, V_{IN}, and C_{SLEW}



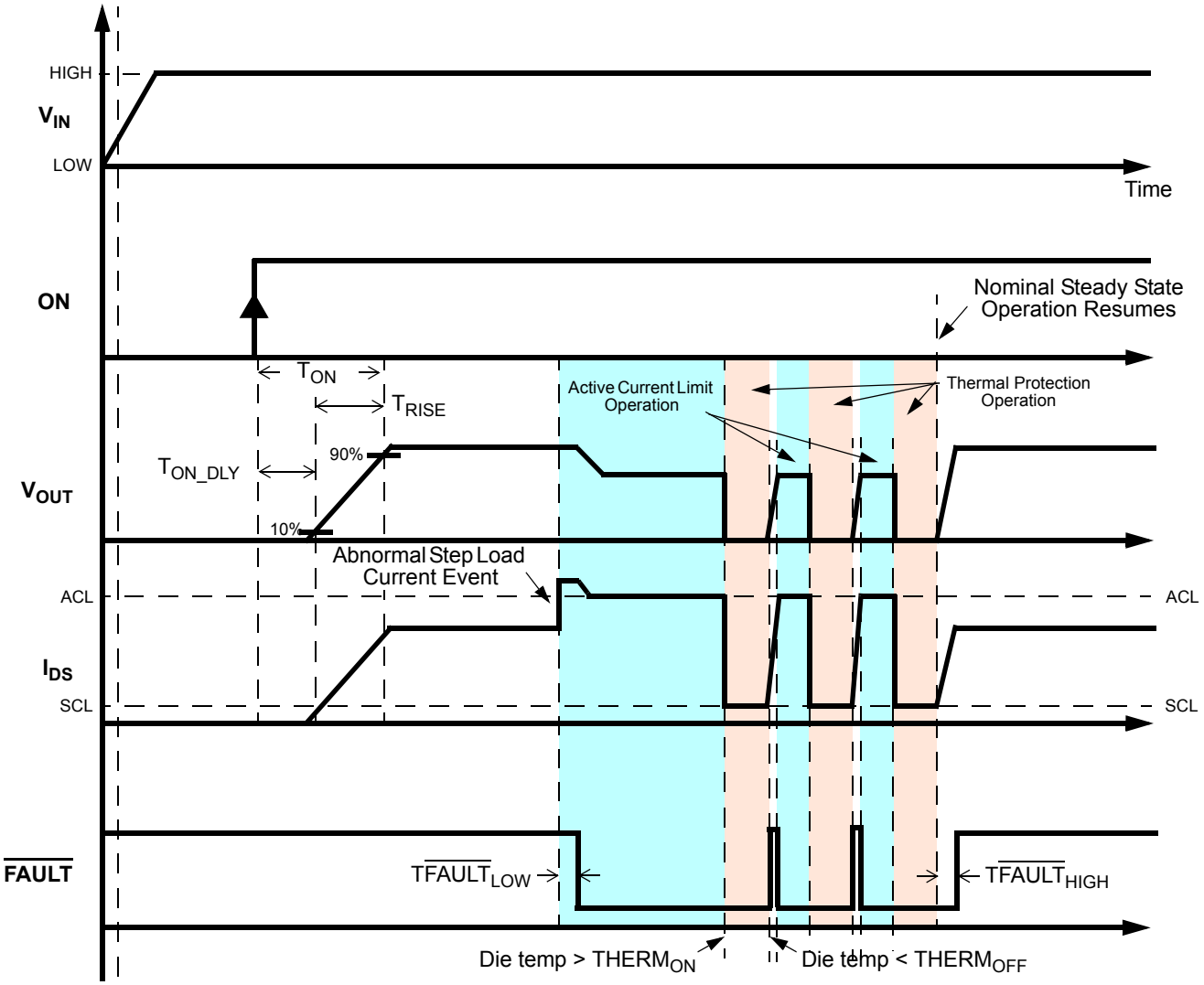
T_{Total_ON} vs. C_{SLEW} , V_{IN}, and Temperature



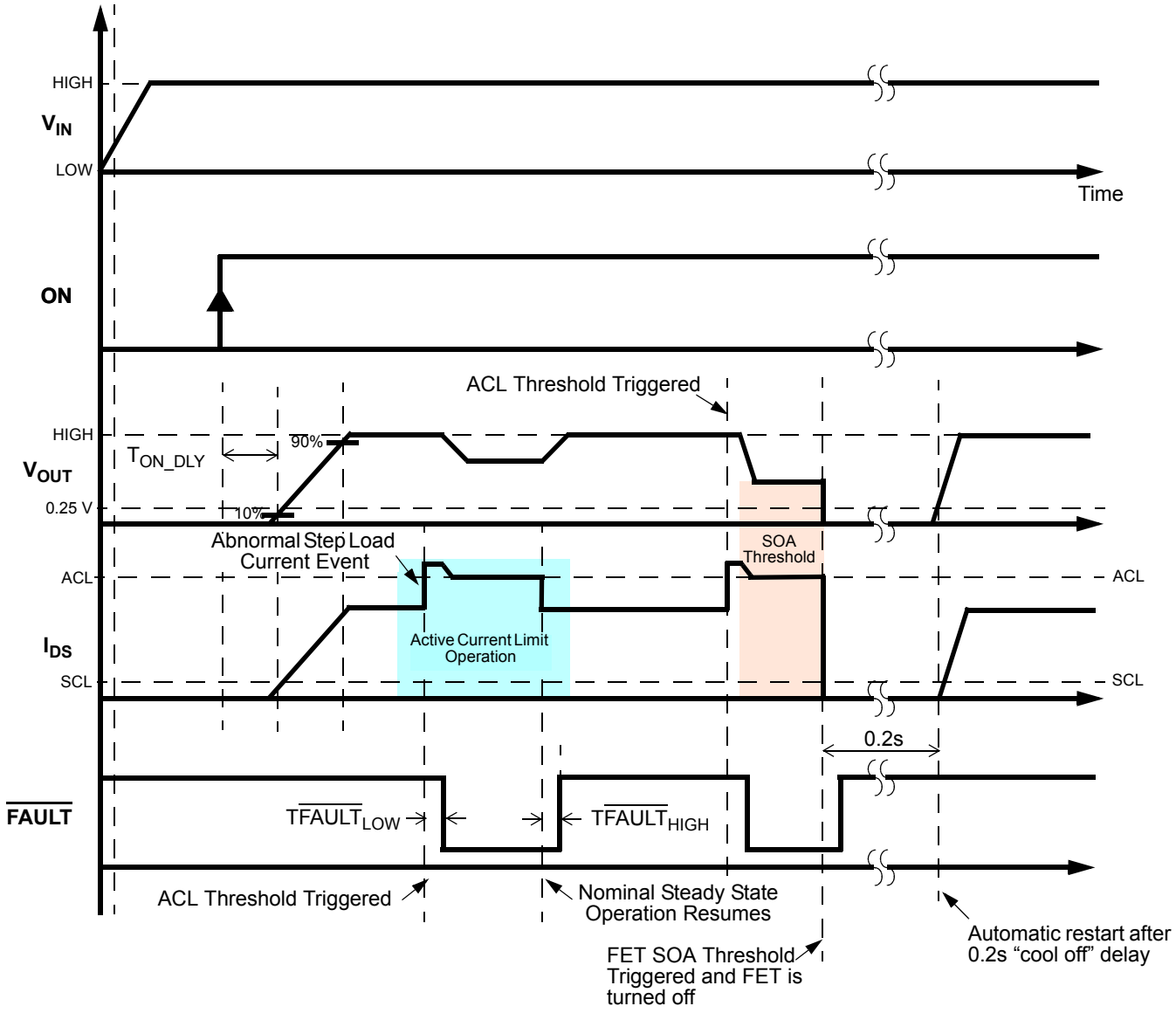
Timing Diagram - Basic Operation including Active Current Limit Protection



Timing Diagram - Active Current Limit & Thermal Protection Operation



Timing Diagram - Basic Operation including Active Current + Internal FET SOA Protection



Applications Information

HFET1 Safe Operating Area Explained

Silego's HFET1 integrated power controllers incorporate a number of internal protection features that prevents them from damaging themselves or any other circuit or subcircuit downstream of them. One particular protection feature is their Safe Operation Area (SOA) protection. SOA protection is automatically activated under overpower and, in some cases, under overcurrent conditions. Overpower SOA is activated if package power dissipation exceeds an internal 5W threshold longer than 2.5 ms. HFET1 devices will quickly switch off (open circuit) upon overpower detection and automatically resume (close) nominal operation once overpower condition no longer exists.

One possible way to have an overpower condition trigger SOA protection is when HFET1 products are enabled into heavy output resistive loads and/or into large load capacitors. It is under these conditions to follow carefully the "Safe Start-up Loading" guidance in the Applications section of the datasheet. During an overcurrent condition, HFET1 devices will try to limit the output current to the level set by the external RSET resistor. Limiting the output current, however, causes an increased voltage drop across the FET's channel because the FET's RDS_{ON} increased as well. Since the FET's RDS_{ON} is larger, package power dissipation also increases. If the resultant increase in package power dissipation is higher/equal than 5 W for longer than 2.5 ms, internal SOA protection will be triggered and the FET will open circuit (switch off). Every time SOA protection is triggered, all HFET1 devices will automatically attempt to resume nominal operation after 160 ms.

Safe Start-up Condition

SLG59H1010V has built-in protection to prevent over-heating during start-up into a heavy load. Overloading the VOUT pin with a capacitor and a resistor may result in non-monotonic VOUT ramping. In general, under light loading on VOUT, VOUT ramping can be controlled with C_{SLEW} value. The following equation serves as a guide:

$$C_{SLEW} = \frac{T_{RAMP}}{V_{IN}} \times 4.9\,\mu A \times \frac{20}{3}$$

where
T_{RAMP} = Total ramping time for V_{OUT} to reach V_{IN}
V_{IN} = Input Voltage
C_{SLEW} = Capacitor value for CAP pin

When capacitor and resistor loading on VOUT during start up, the following tables will ensure VOUT ramping is monotonic without triggering internal protection:

Safe Start-up Loading for V_{IN} = 24 V (Monotonic Ramp)			
Slew Rate (V/ms)	**C_{SLEW} Control (nF)**	**C_{LOAD} (µF)**	**R_{LOAD} (Ω)**
0.5	66.7	500	80
1.0	33.3	250	80
1.5	22.2	160	80
2.0	16.7	120	80
2.5	13.3	100	80

Safe Start-up Loading for V_{IN} = 12 V (Monotonic Ramp)			
Slew Rate (V/ms)	**C_{SLEW} Control (nF)**	**C_{LOAD} (µF)**	**R_{LOAD} (Ω)**
1	33.3	500	20
2	16.7	250	20
3	11.1	160	20
4	8.3	120	20
5	6.7	100	20

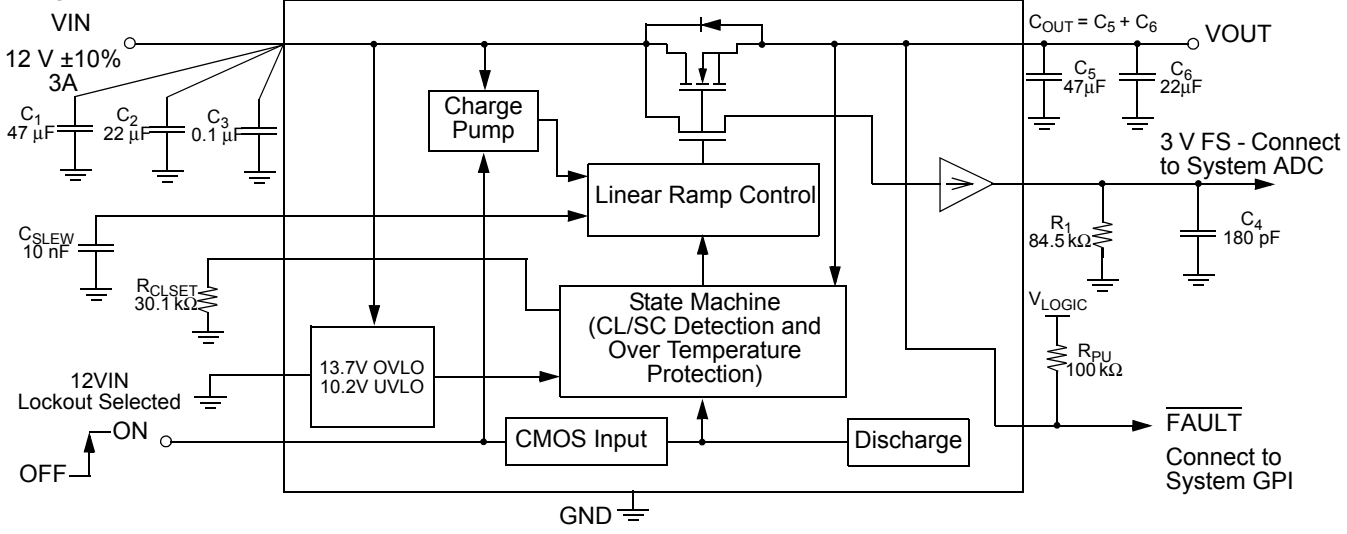
Setting the SLG59H1010V's Active Current Limit

RSET (kΩ)	Active Current Limit (A)
95	1
45	2
30	3
18	5

Configuring the SLG59H1010V for 12VIN Lockout Applications

To configure the SLG59H1010V for conditioned 12 V ±10% V_{IN} applications is simply a matter of connecting the SEL pin to GND as shown in *Figure A*. For other V_{IN} lockout window applications, please consult Silego for additional information.

Figure A.



24VIN and 12VIN Lockout Window Thresholds

Shown in *Figure B* and *Figure C* are the two sets of V_{IN} overvoltage/undervoltage lockout windows – one for conditioned 24 V ±10% V_{IN} systems and the second for conditioned 12 V ±10% V_{IN} systems. The SLG59H1010V's lockout thresholds represent a ±5% distribution around each respective typical voltage threshold. To avoid lockout threshold collision with nominal operation, the SLG59H1010V's V_{IN} (OV, min) and V_{IN} (UV, max) thresholds were set 0.1V correspondingly higher than the system's nominal V_{IN}(H) or lower than the system's VIN(L) range.

Figure B.

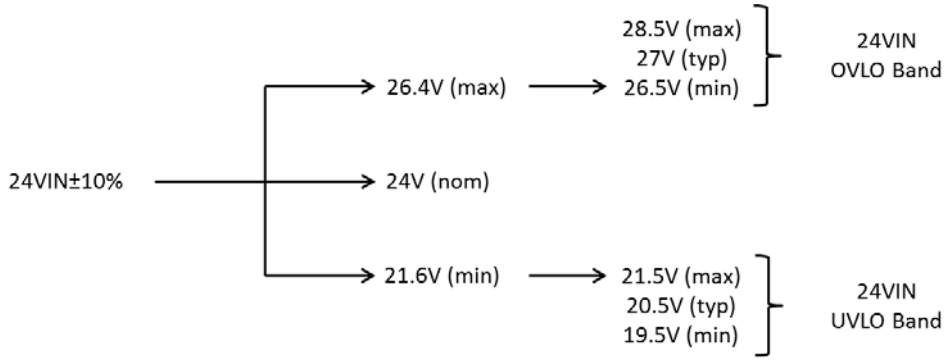
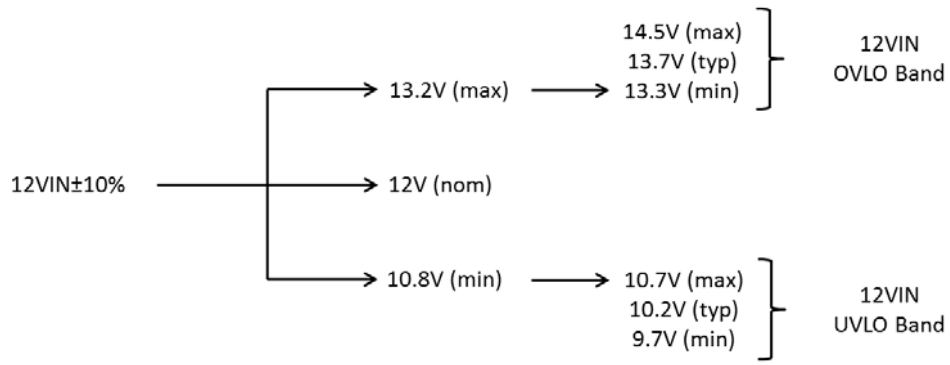


Figure C.



Power Dissipation

The junction temperature of the SLG59H1010V depends on different factors such as board layout, ambient temperature, and other environmental factors. The primary contributor to the increase in the junction temperature of the SLG59H1010V is the power dissipation of its power MOSFET. Its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$PD = RDS_{ON} \times I_{OUT}^2$$

where:

PD = Power dissipation, in Watts (W)
RDS_{ON} = Power MOSFET ON resistance, in Ohms (Ω)
I_{OUT} = Output current, in Amps (A)

and

$$T_J = PD \times \theta_{JA} + T_A$$

where:

T_J = Junction temperature, in Celsius degrees (°C)
θ_{JA} = Package thermal resistance, in Celsius degrees per Watt (°C/W)
T_A = Ambient temperature, in Celsius degrees (°C)

Power Dissipation (continued)

In current-limit mode, the SLG59H1010V's power dissipation can be calculated by taking into account the voltage drop across the power switch (V_{IN}-V_{OUT}) and the magnitude of the output current in current-limit mode (I_{ACL}):

$$PD = (V_{IN}\text{-}V_{OUT}) \times I_{ACL} \text{ or}$$

$$PD = (V_{IN} - (R_{LOAD} \times I_{ACL})) \times I_{ACL}$$

where:

PD = Power dissipation, in Watts (W)
V_{IN} = Input Voltage, in Volts (V)
R_{LOAD} = Load Resistance, in Ohms (Ω)
I_{ACL} = Output limited current, in Amps (A)
$V_{OUT} = R_{LOAD} \times I_{ACL}$

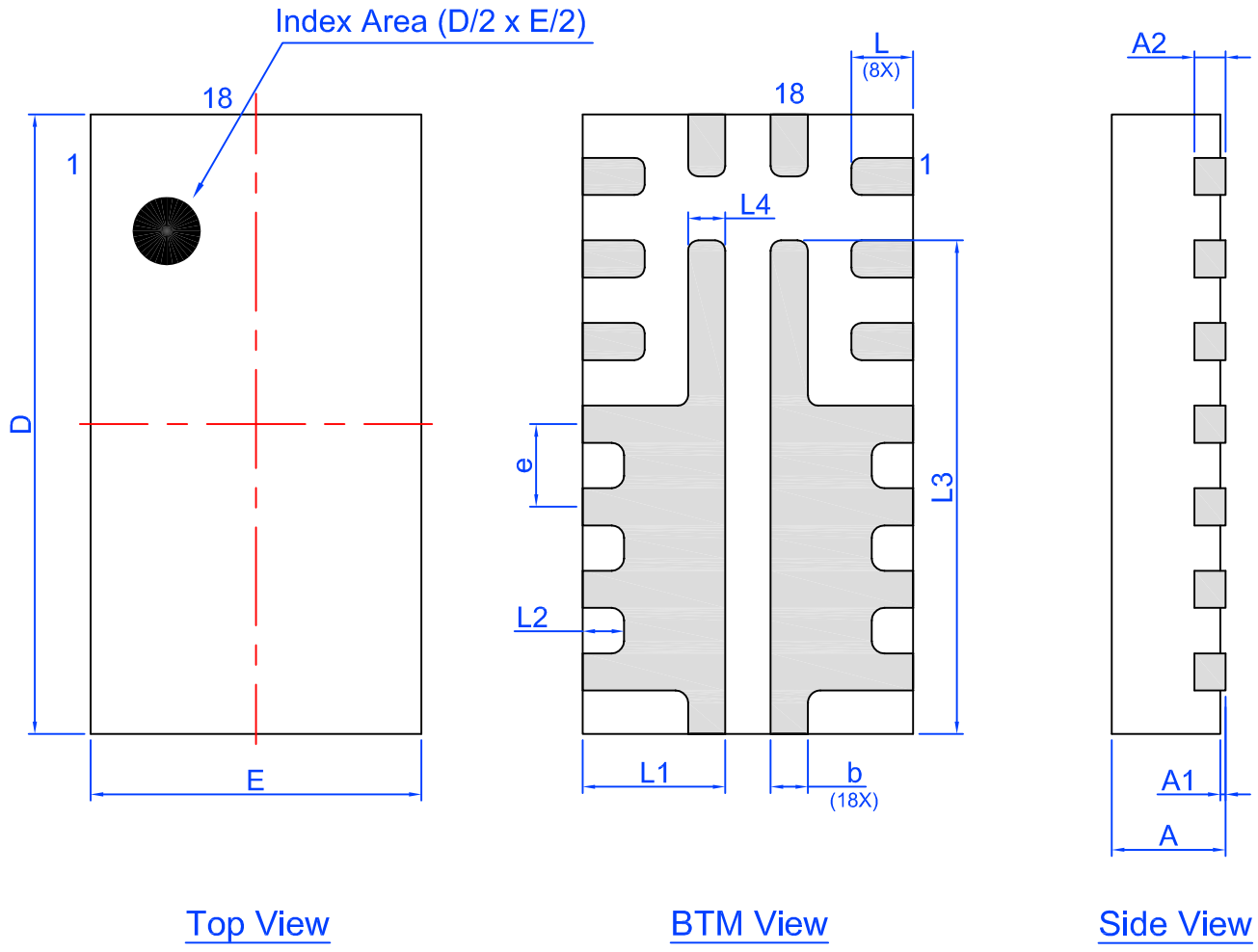
Package Top Marking System Definition

1010V - Part ID Field
WW - Date Code Field[1]
NNN - Lot Traceability Code Field[1]
A - Assembly Site Code Field [2]
RR - Part Revision Code Field[2]

Note 1: Each character in code field can be alphanumeric A-Z and 0-9
Note 2: Character in code field can be alphabetic A-Z

Package Drawing and Dimensions

18 Lead TQFN Package 1.6 x 3 mm (Fused Lead)
JEDEC MO-220, Variation WCEE

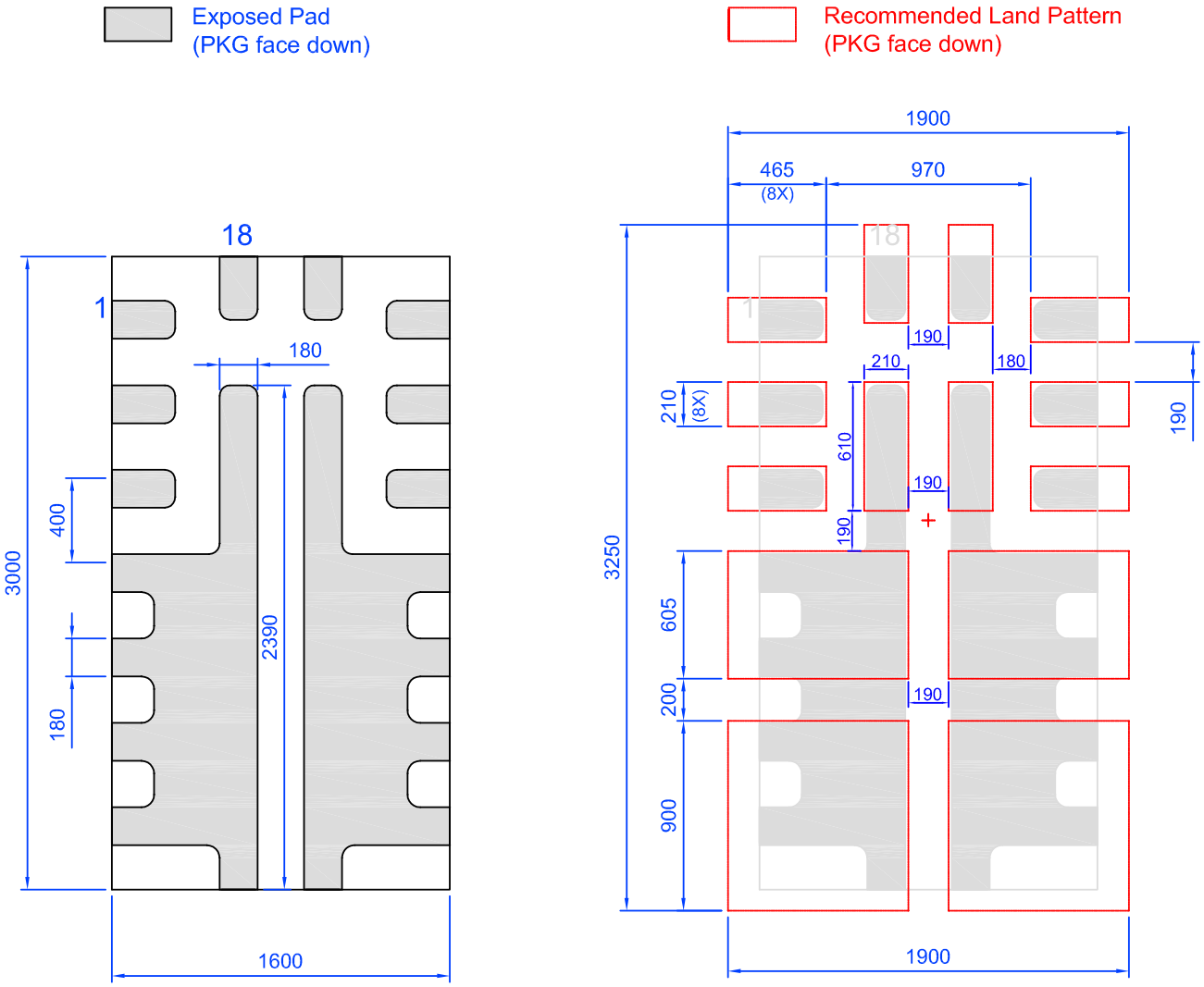


Top View BTM View Side View

Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.95	3.00	3.05
A1	0.005	-	0.05	E	1.55	1.60	1.65
A2	0.10	0.15	0.20	L	0.25	0.30	0.35
b	0.13	0.18	0.23	L1	0.64	0.69	0.74
e	0.40 BSC			L2	0.15	0.20	0.25
L3	2.34	2.39	2.44	L4	0.13	0.18	0.23

SLG59H1010V 18-pin STQFN PCB Landing Pattern



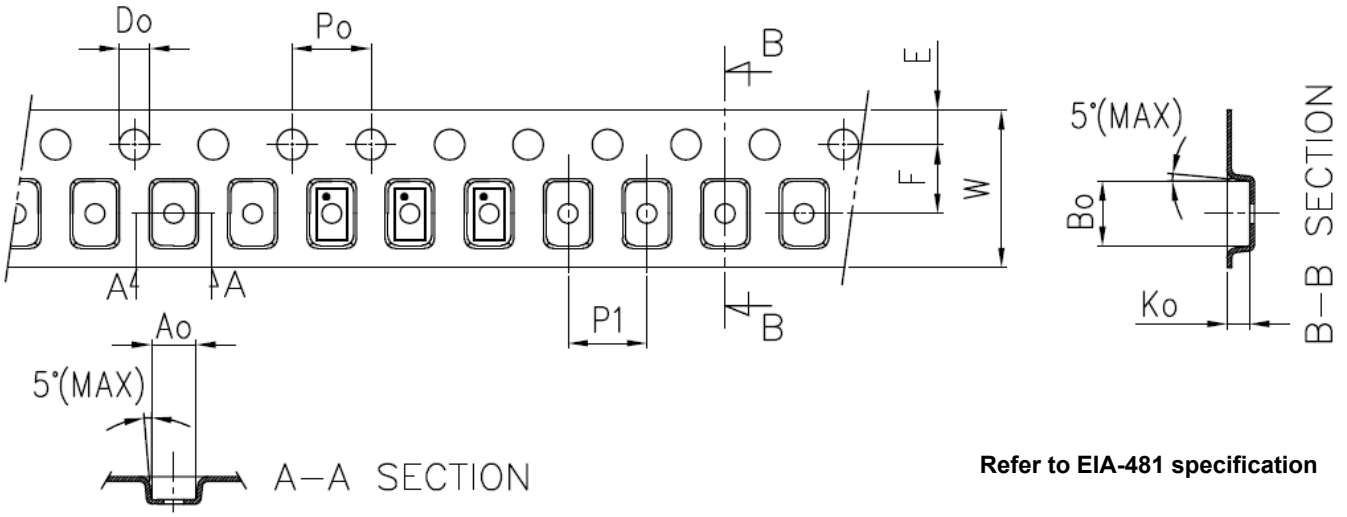
Note: All dimensions shown in micrometers (µm)

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 18L 0.4P FC Green	18	1.6 x 3 x 0.55	3,000	3,000	178 / 60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 18L 0.4P FC Green	1.78	3.18	0.76	4	4	1.5	1.75	3.5	8



Refer to EIA-481 specification

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.64 mm^3 (nominal). More information can be found at www.jedec.org.

Revision History

Date	Version	Change
2/24/2017	1.00	Production Release