



# PMGD290UCEA

20 / 20 V, 725 / 500 mA N/P-channel Trench MOSFET

28 March 2014

Product data sheet

## 1. General description

Complementary N/P-channel enhancement mode Field-Effect Transistor (FET) in a very small SOT363 Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

## 2. Features and benefits

- Very fast switching
- Trench MOSFET technology
- 2 kV ESD protection
- AEC-Q101 qualified

## 3. Applications

- Relay driver
- High-speed line driver
- Low-side loadswitch
- Switching circuits
- Automotive applications

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<strong>TR1 (N-channel), Static characteristics</strong>							
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}$ ; $I_D = 500 \text{ mA}$ ; $T_j = 25 \text{ }^\circ\text{C}$		-	290	380	$\text{m}\Omega$
<strong>TR2 (P-channel), Static characteristics</strong>							
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -4.5 \text{ V}$ ; $I_D = -400 \text{ mA}$ ; $T_j = 25 \text{ }^\circ\text{C}$		-	670	850	$\text{m}\Omega$
<strong>TR1 (N-channel)</strong>							
$V_{DS}$	drain-source voltage	$T_j = 25 \text{ }^\circ\text{C}$		-	-	20	V
$V_{GS}$	gate-source voltage			-8	-	8	V
$I_D$	drain current	$V_{GS} = 4.5 \text{ V}$ ; $T_{amb} = 25 \text{ }^\circ\text{C}$	[1]	-	-	725	mA
<strong>TR2 (P-channel)</strong>							
$V_{DS}$	drain-source voltage	$T_j = 25 \text{ }^\circ\text{C}$		-	-	-20	V

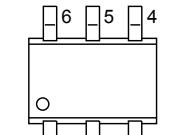
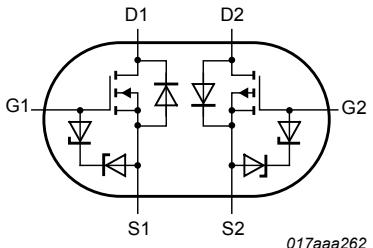
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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{GS}$	gate-source voltage			-8	-	8	V
$I_D$	drain current	$V_{GS} = -4.5$ V; $T_{amb} = 25$ °C	[1]	-	-	-500	mA

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm<sup>2</sup>.

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1	 <b>TSSOP6 (SOT363)</b>	 017aaa262
2	G1	gate TR1		
3	D2	drain TR2		
4	S2	source TR2		
5	G2	gate TR2		
6	D1	drain TR1		

## 6. Ordering information

Table 3. Ordering information

Type number	Package			Version
	Name	Description		
PMGD290UCEA	TSSOP6	plastic surface-mounted package; 6 leads		SOT363

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PMGD290UCEA	[1] YD%

[1] % = placeholder for manufacturing site code

## 8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

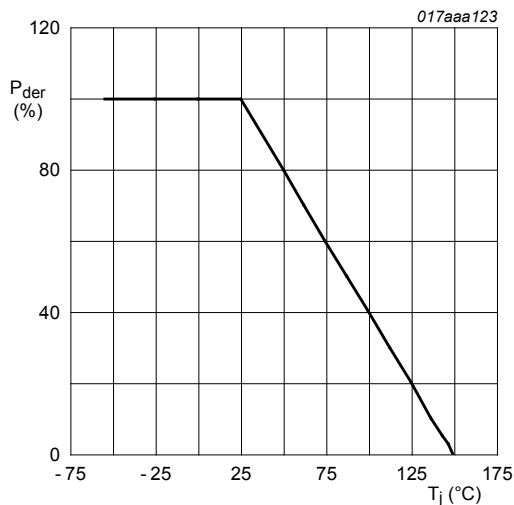
Symbol	Parameter	Conditions		Min	Max	Unit
<b>TR1 (N-channel)</b>						
$V_{DS}$	drain-source voltage	$T_j = 25$ °C		-	20	V
$V_{GS}$	gate-source voltage			-8	8	V

Symbol	Parameter	Conditions		Min	Max	Unit
$I_D$	drain current	$V_{GS} = 4.5 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$	[1]	-	725	mA
		$V_{GS} = 4.5 \text{ V}; T_{amb} = 100 \text{ }^\circ\text{C}$	[1]	-	450	mA
$I_{DM}$	peak drain current	$T_{amb} = 25 \text{ }^\circ\text{C}$ ; single pulse; $t_p \leq 10 \text{ } \mu\text{s}$		-	3	A
$P_{tot}$	total power dissipation	$T_{amb} = 25 \text{ }^\circ\text{C}$	[2]	-	280	mW
			[1]	-	320	mW
		$T_{sp} = 25 \text{ }^\circ\text{C}$		-	990	mW
<b>TR1 (N-channel), Source-drain diode</b>						
$I_S$	source current	$T_{amb} = 25 \text{ }^\circ\text{C}$	[1]	-	370	mA
<b>TR1 N-channel), ESD maximum rating</b>						
$V_{ESD}$	electrostatic discharge voltage	HBM	[3]	-	2000	V
<b>TR2 (P-channel)</b>						
$V_{DS}$	drain-source voltage	$T_j = 25 \text{ }^\circ\text{C}$		-	-20	V
$V_{GS}$	gate-source voltage			-8	8	V
$I_D$	drain current	$V_{GS} = -4.5 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$	[1]	-	-500	mA
		$V_{GS} = -4.5 \text{ V}; T_{amb} = 100 \text{ }^\circ\text{C}$	[1]	-	-320	mA
$I_{DM}$	peak drain current	$T_{amb} = 25 \text{ }^\circ\text{C}$ ; single pulse; $t_p \leq 10 \text{ } \mu\text{s}$		-	-2	A
$P_{tot}$	total power dissipation	$T_{amb} = 25 \text{ }^\circ\text{C}$	[2]	-	280	mW
			[1]	-	320	mW
		$T_{sp} = 25 \text{ }^\circ\text{C}$		-	990	mW
<b>TR2 (P-channel), Source-drain diode</b>						
$I_S$	source current	$T_{amb} = 25 \text{ }^\circ\text{C}$	[1]	-	-370	mA
<b>TR2 (P-channel), ESD maximum rating</b>						
$V_{ESD}$	electrostatic discharge voltage	HBM	[3]	-	2000	V
<b>Per device</b>						
$P_{tot}$	total power dissipation	$T_{amb} = 25 \text{ }^\circ\text{C}$	[2]	-	445	mW
$T_j$	junction temperature			-55	150	$^\circ\text{C}$
$T_{amb}$	ambient temperature			-55	150	$^\circ\text{C}$
$T_{stg}$	storage temperature			-65	150	$^\circ\text{C}$

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1  $\text{cm}^2$ .

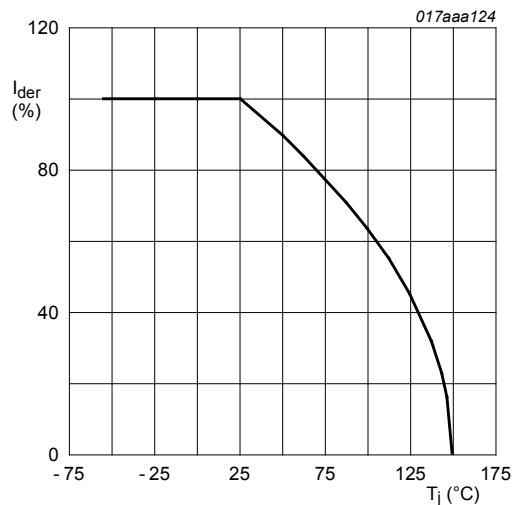
[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper; tin-plated and standard footprint.

[3] Measured between all pins.



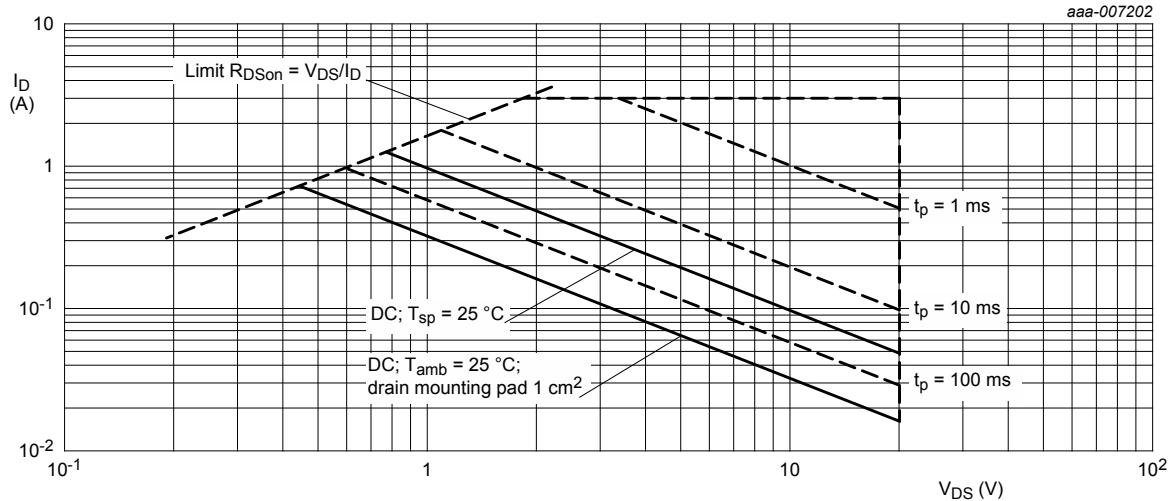
**Fig. 1. Normalized total power dissipation as a function of junction temperature**

$$P_{der} = \frac{P_{tot}}{P_{tot}(25^\circ\text{C})} \times 100 \%$$



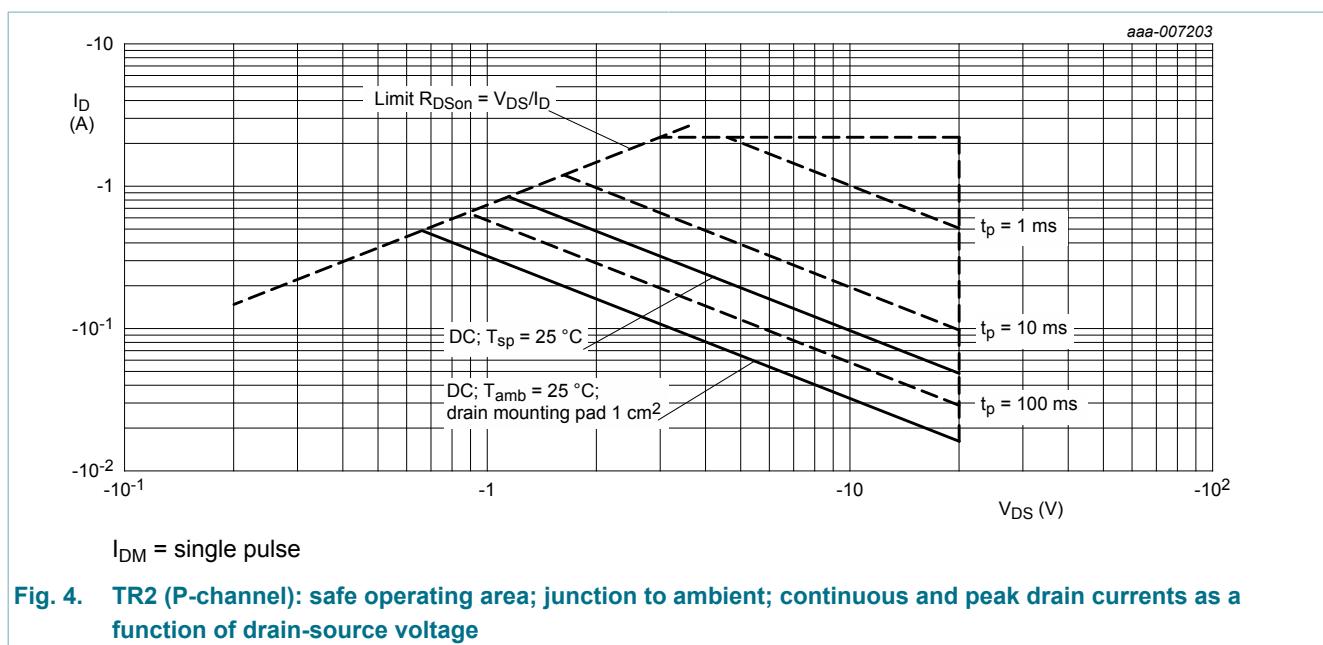
**Fig. 2. Normalized continuous drain current as a function of junction temperature**

$$I_{der} = \frac{I_D}{I_D(25^\circ\text{C})} \times 100 \%$$



$I_{DM}$  = single pulse

**Fig. 3. TR1 (N-channel): safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage**



**Fig. 4. TR2 (P-channel): safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage**

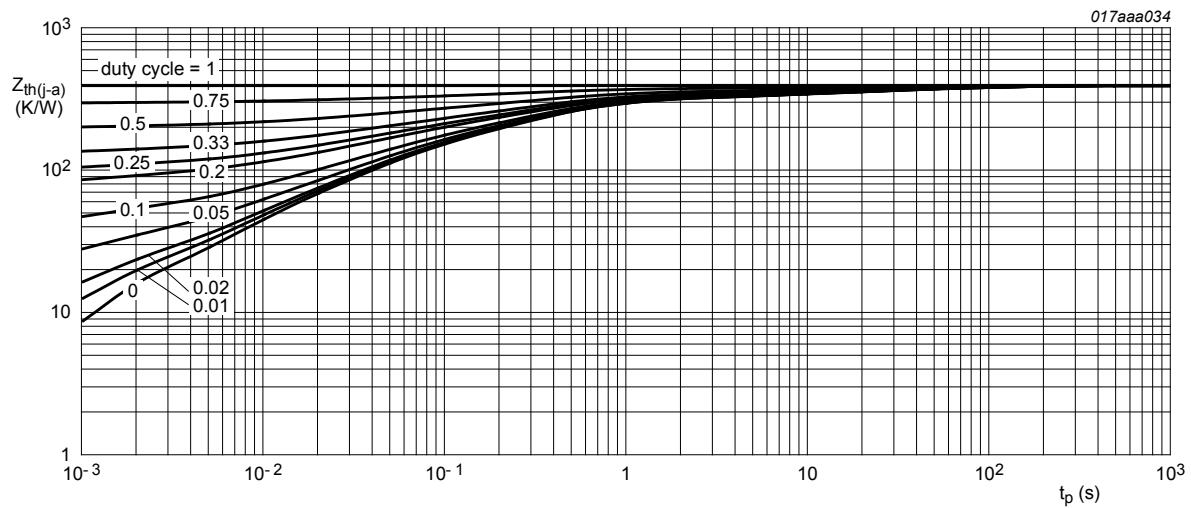
## 9. Thermal characteristics

**Table 6. Thermal characteristics**

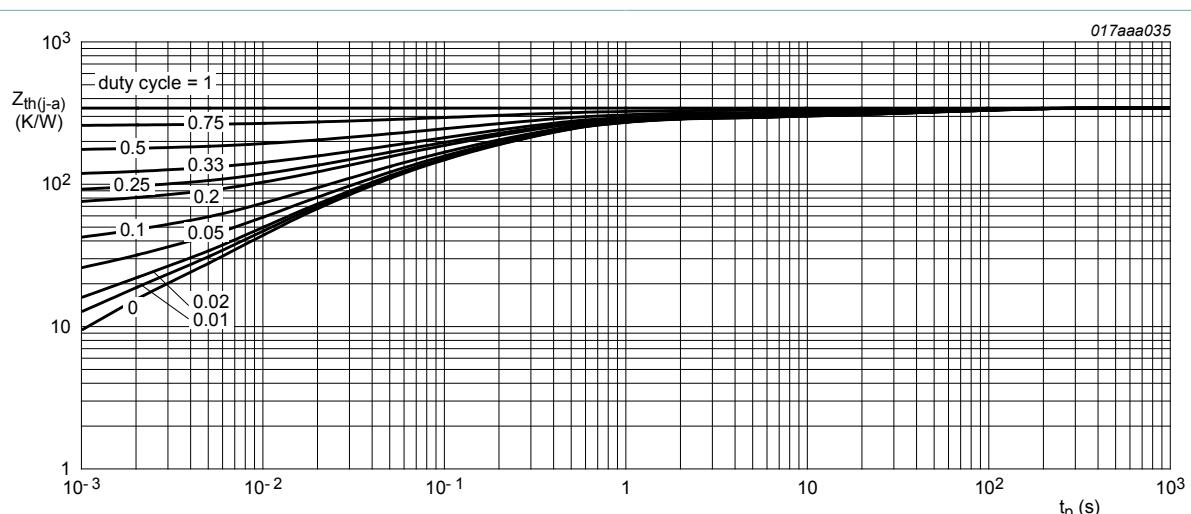
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>TR1 (N-channel)</b>							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	390	445	K/W
			[2]	-	340	390	K/W
<b>TR2 (P-channel)</b>							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	390	445	K/W
			[2]	-	340	390	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	-	130	K/W
<b>Per device</b>							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	300	K/W

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper; tin-plated and standard footprint.

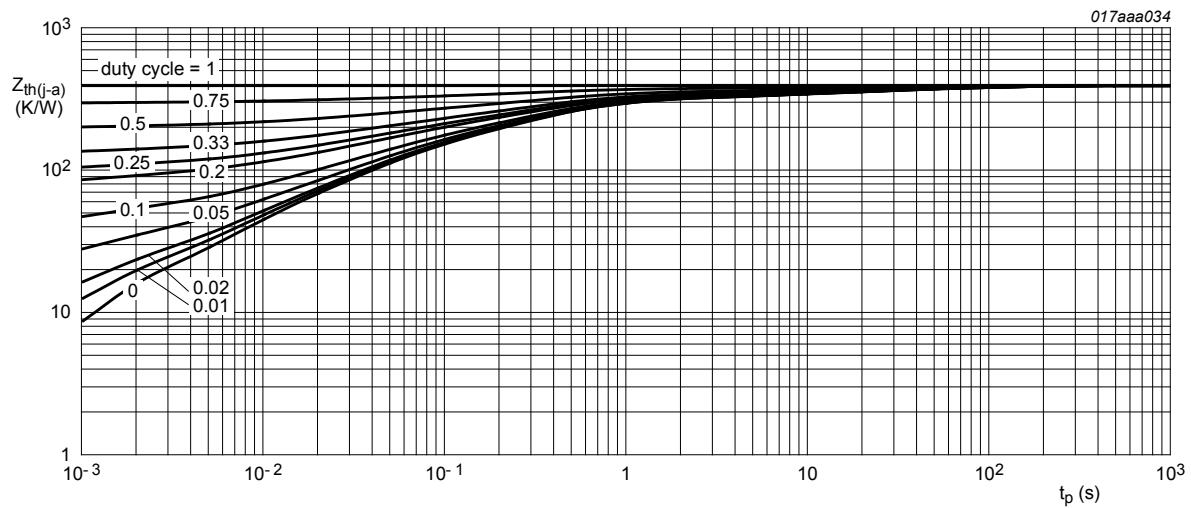
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain  $1 \text{ cm}^2$ .



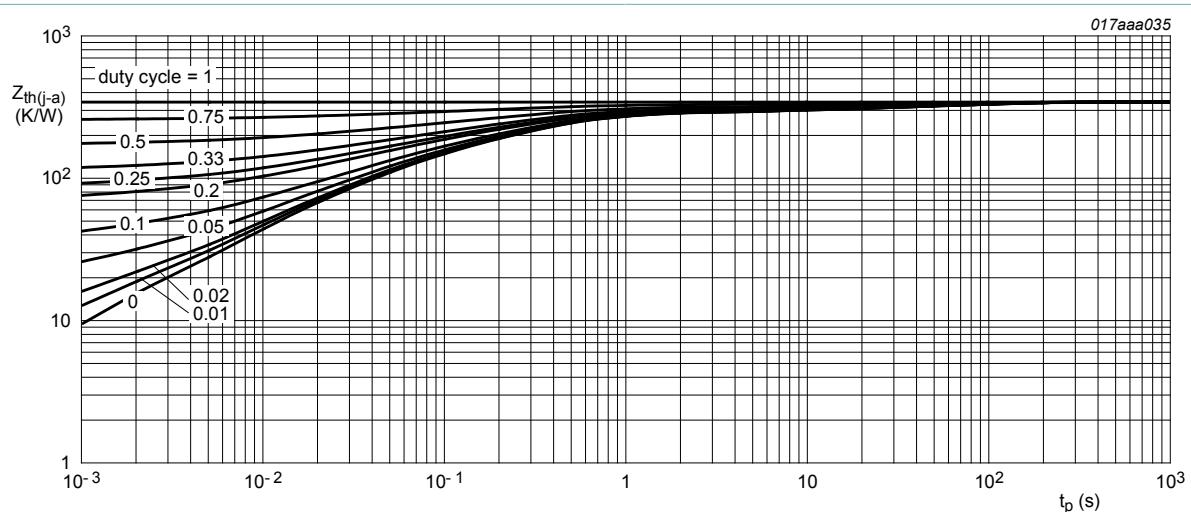
**Fig. 5. TR1: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**



**Fig. 6. TR1: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**



**Fig. 7. TR2: transient thermal impedance from junction to ambient as a function of pulse duration; typical values**



**Fig. 8. TR2: transient thermal impedance from junction to ambient as a function of pulse duration; typical values**

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>TR1 (N-channel), Static characteristics</b>							
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25^\circ C$		20	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = 250 \mu A; V_{DS} = V_{GS}; T_j = 25^\circ C$		0.5	0.75	0.95	V
$I_{DSS}$	drain leakage current	$V_{DS} = 20 V; V_{GS} = 0 V; T_j = 25^\circ C$		-	-	1	$\mu A$
		$V_{DS} = 20 V; V_{GS} = 0 V; T_j = 150^\circ C$		-	-	10	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 8 V; V_{DS} = 0 V; -40^\circ C < T_j < 150^\circ C$		-	-	10	$\mu A$
		$V_{GS} = -8 V; V_{DS} = 0 V; -40^\circ C < T_j < 150^\circ C$		-	-	-10	$\mu A$
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 4.5 V; I_D = 500 mA; T_j = 25^\circ C$		-	290	380	$m\Omega$
		$V_{GS} = 4.5 V; I_D = 500 mA; T_j = 150^\circ C$		-	460	610	$m\Omega$
		$V_{GS} = 2.5 V; I_D = 200 mA; T_j = 25^\circ C$		-	420	620	$m\Omega$
		$V_{GS} = 1.8 V; I_D = 10 mA; T_j = 25^\circ C$		-	0.6	1.1	$\Omega$
$g_{fs}$	transfer conductance	$V_{DS} = 10 V; I_D = 200 mA; T_j = 25^\circ C$		-	1.6	-	S
<b>TR1 (N-channel), Dynamic characteristics</b>							
$Q_{G(tot)}$	total gate charge	$V_{DS} = 10 V; I_D = 500 mA; V_{GS} = 4.5 V; T_j = 25^\circ C$		-	0.45	0.68	nC
$Q_{GS}$	gate-source charge			-	0.15	-	nC
$Q_{GD}$	gate-drain charge			-	0.15	-	nC
$C_{iss}$	input capacitance	$V_{DS} = 10 V; f = 1 MHz; V_{GS} = 0 V; T_j = 25^\circ C$		-	55	83	pF
$C_{oss}$	output capacitance			-	15	-	pF
$C_{rss}$	reverse transfer capacitance			-	7	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 10 V; R_L = 250 \Omega; V_{GS} = 4.5 V; R_{G(ext)} = 6 \Omega; T_j = 25^\circ C$		-	6	12	ns
$t_r$	rise time			-	4	-	ns
$t_{d(off)}$	turn-off delay time			-	86	172	ns
$t_f$	fall time			-	31	-	ns
<b>TR1 (N-channel), Source-drain diode characteristics</b>							
$V_{SD}$	source-drain voltage	$I_S = 300 mA; V_{GS} = 0 V; T_j = 25^\circ C$		0.48	0.77	1.2	V
<b>TR2 (P-channel), Static characteristics</b>							
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu A; V_{GS} = 0 V; T_j = 25^\circ C$		-20	-	-	V

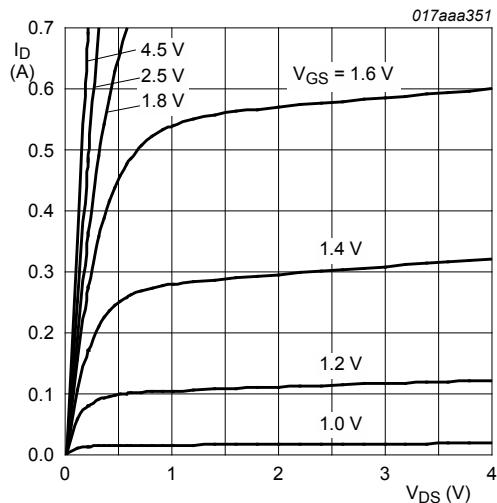
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{GSth}$	gate-source threshold voltage	$I_D = -250 \mu A; V_{DS} = V_{GS}; T_j = 25^\circ C$		-0.5	-0.8	-1.3	V
$I_{DSS}$	drain leakage current	$V_{DS} = -20 V; V_{GS} = 0 V; T_j = 25^\circ C$		-	-	-1	$\mu A$
		$V_{DS} = -20 V; V_{GS} = 0 V; T_j = 150^\circ C$		-	-	-10	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 8 V; V_{DS} = 0 V; -40^\circ C < T_j < 150^\circ C$		-	-	10	$\mu A$
		$V_{GS} = -8 V; V_{DS} = 0 V; -40^\circ C < T_j < 150^\circ C$		-	-	-10	$\mu A$
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -4.5 V; I_D = -400 mA; T_j = 25^\circ C$		-	670	850	$m\Omega$
		$V_{GS} = -4.5 V; I_D = -400 mA; T_j = 150^\circ C$		-	1.1	1.4	$\Omega$
		$V_{GS} = -2.5 V; I_D = -200 mA; T_j = 25^\circ C$		-	1.2	1.5	$\Omega$
		$V_{GS} = -1.8 V; I_D = -10 mA; T_j = 25^\circ C$		-	1.8	2.8	$\Omega$
$g_{fs}$	transfer conductance	$V_{DS} = -10 V; I_D = -200 mA; T_j = 25^\circ C$		-	610	-	$mS$

**TR2 (P-channel), Dynamic characteristics**

$Q_{G(tot)}$	total gate charge	$V_{DS} = -10 V; I_D = -400 mA; V_{GS} = -4.5 V; T_j = 25^\circ C$		-	0.76	1.14	nC
$Q_{GS}$	gate-source charge			-	0.28	-	nC
$Q_{GD}$	gate-drain charge			-	0.18	-	nC
$C_{iss}$	input capacitance	$V_{DS} = -10 V; f = 1 MHz; V_{GS} = 0 V; T_j = 25^\circ C$		-	58	87	pF
$C_{oss}$	output capacitance			-	21	-	pF
$C_{rss}$	reverse transfer capacitance			-	12	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -10 V; R_L = 250 \Omega; V_{GS} = -4.5 V; R_{G(ext)} = 6 \Omega; T_j = 25^\circ C$		-	18	36	ns
$t_r$	rise time			-	30	-	ns
$t_{d(off)}$	turn-off delay time			-	80	160	ns
$t_f$	fall time			-	72	-	ns

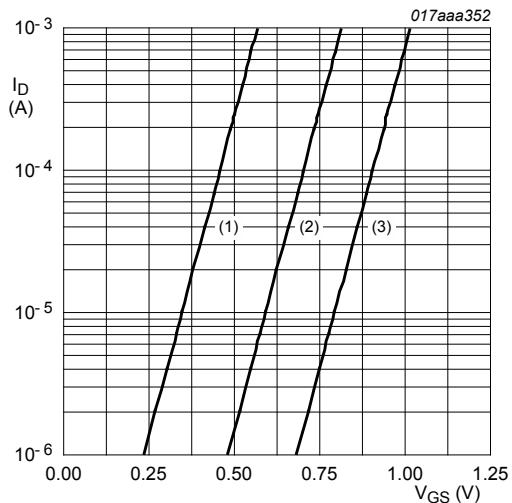
**TR2 (P-channel), Source-drain diode characteristics**

$V_{SD}$	source-drain voltage	$I_S = -300 mA; V_{GS} = 0 V; T_j = 25^\circ C$		-0.48	-0.84	-1.2	V
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$T_j = 25^\circ\text{C}$

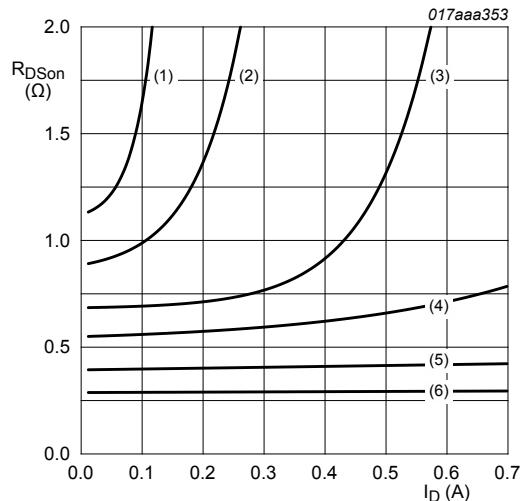
**Fig. 9. TR1; Output characteristics: drain current as a function of drain-source voltage; typical values**



$T_j = 25^\circ\text{C}; V_{DS} = 5\text{ V}$

- (1) minimum values
- (2) typical values
- (3) maximum values

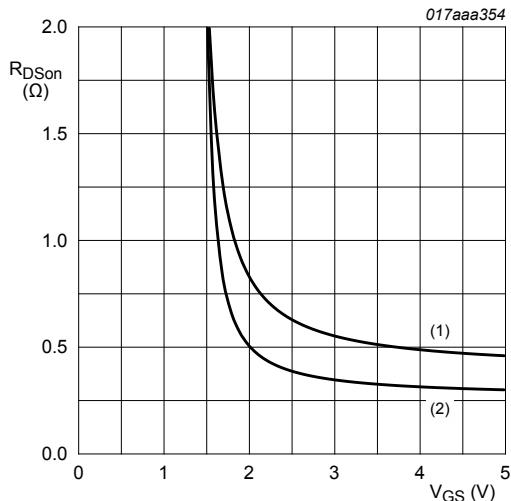
**Fig. 10. TR1; Sub-threshold drain current as a function of gate-source voltage**



$T_j = 25^\circ\text{C}$

- (1)  $V_{GS} = 1.3\text{ V}$
- (2)  $V_{GS} = 1.4\text{ V}$
- (3)  $V_{GS} = 1.6\text{ V}$
- (4)  $V_{GS} = 1.8\text{ V}$
- (5)  $V_{GS} = 2.5\text{ V}$
- (6)  $V_{GS} = 4.5\text{ V}$

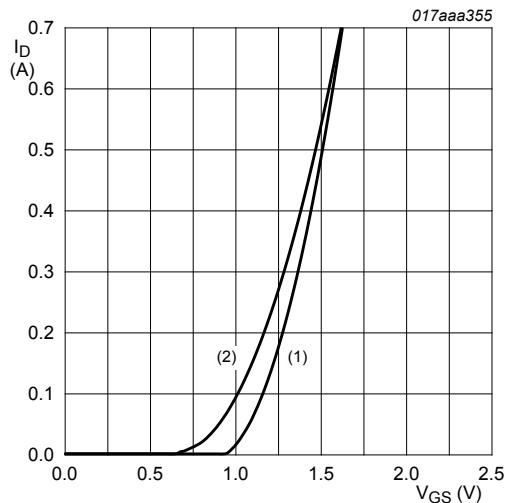
**Fig. 11. TR1; Drain-source on-state resistance as a function of drain current; typical values**



$I_D = 400\text{ mA}$

- (1)  $T_j = 150^\circ\text{C}$
- (2)  $T_j = 25^\circ\text{C}$

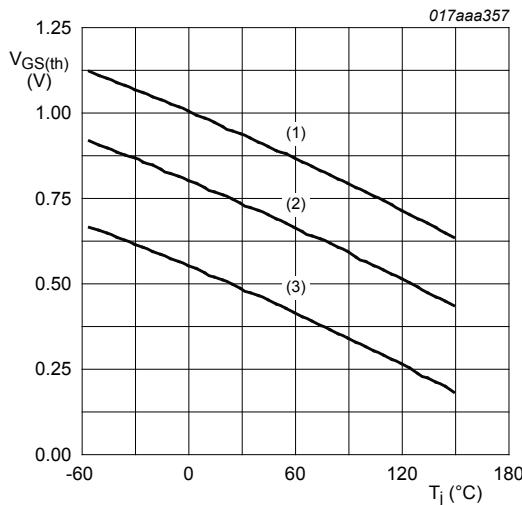
**Fig. 12. TR1; Drain-source on-state resistance as a function of gate-source voltage; typical values**



$V_{DS} > I_D \times R_{DSon}$

- (1)  $T_j = 25^\circ\text{C}$
- (2)  $T_j = 150^\circ\text{C}$

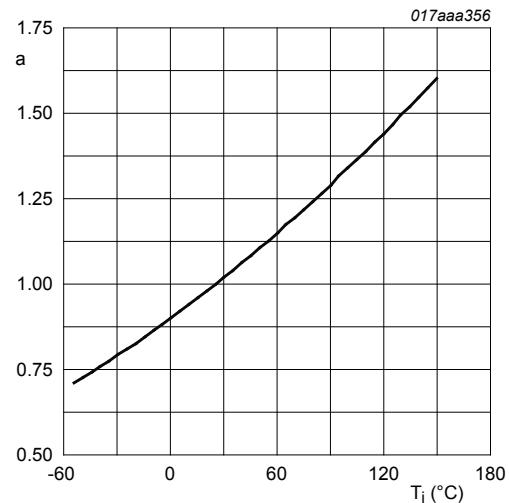
**Fig. 13. TR1; Transfer characteristics: drain current as a function of gate-source voltage; typical values**



$I_D = 0.25 \text{ mA}; V_{DS} = V_{GS}$

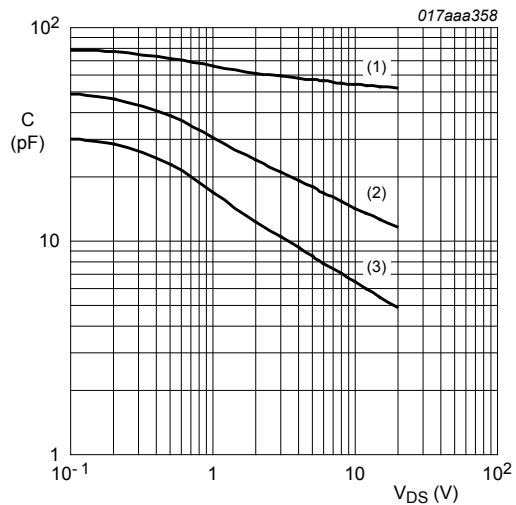
- (1) maximum values
- (2) typical values
- (3) minimum values

**Fig. 15. TR1; Gate-source threshold voltage as a function of junction temperature**



**Fig. 14. TR1; Normalized drain-source on-state resistance as a function of junction temperature; typical values**

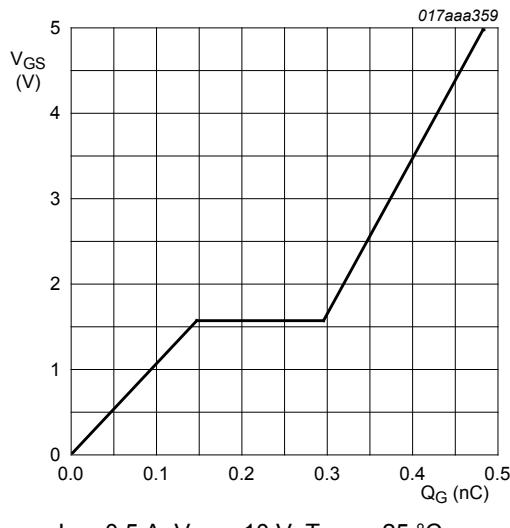
$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$



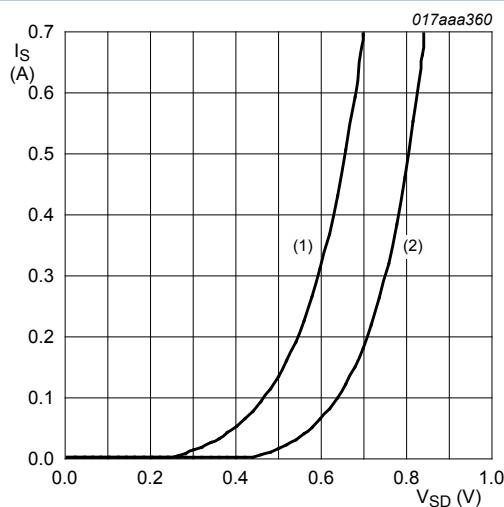
$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$

- (1)  $C_{iss}$
- (2)  $C_{oss}$
- (3)  $C_{rss}$

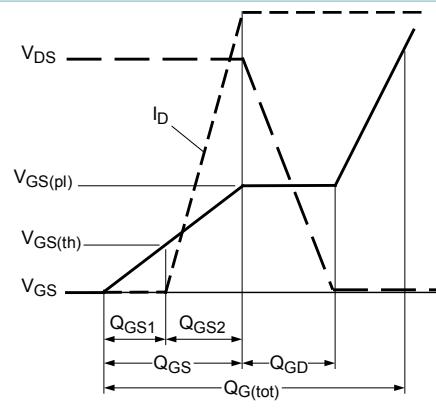
**Fig. 16. TR1; Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



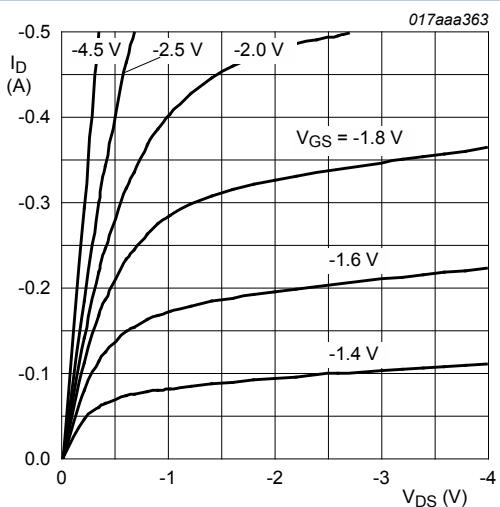
**Fig. 17. TR1; Gate-source voltage as a function of gate charge; typical values**



**Fig. 19. TR1; Source current as a function of source-drain voltage; typical values**



**Fig. 18. Gate charge waveform definitions**



**Fig. 20. TR2; Output characteristics: drain current as a function of drain-source voltage; typical values**

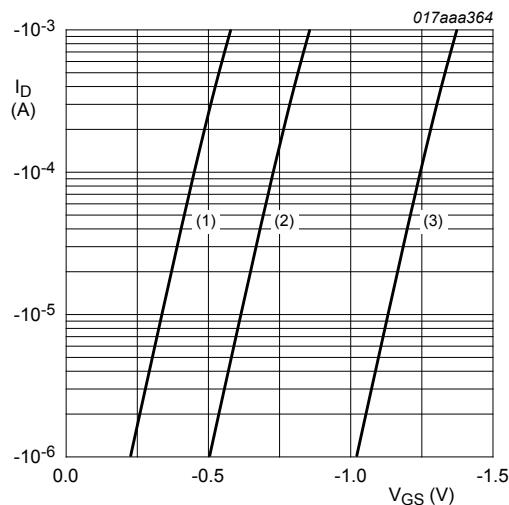


Fig. 21. TR2; Sub-threshold drain current as a function of gate-source voltage

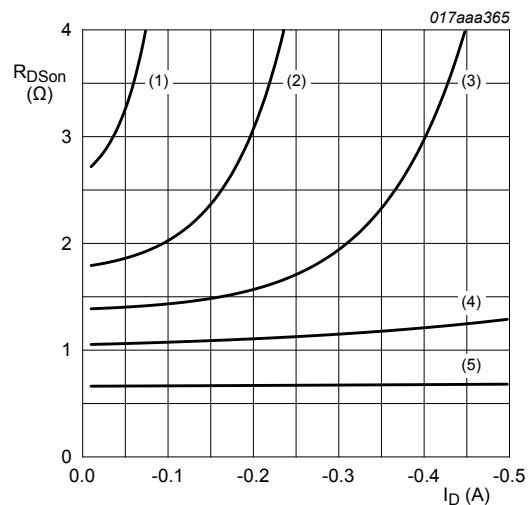


Fig. 22. TR2; Drain-source on-state resistance as a function of drain current; typical values

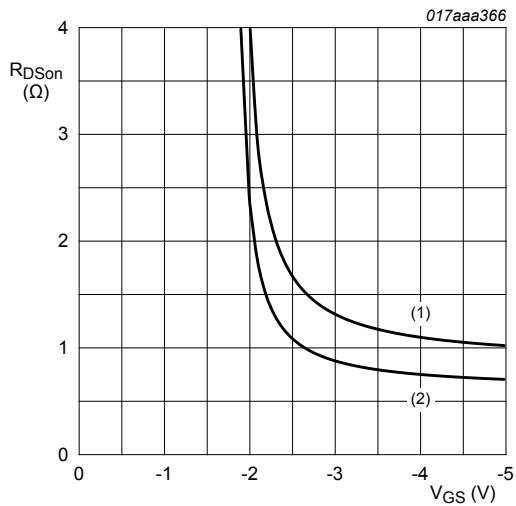


Fig. 23. TR2; Drain-source on-state resistance as a function of gate-source voltage; typical values

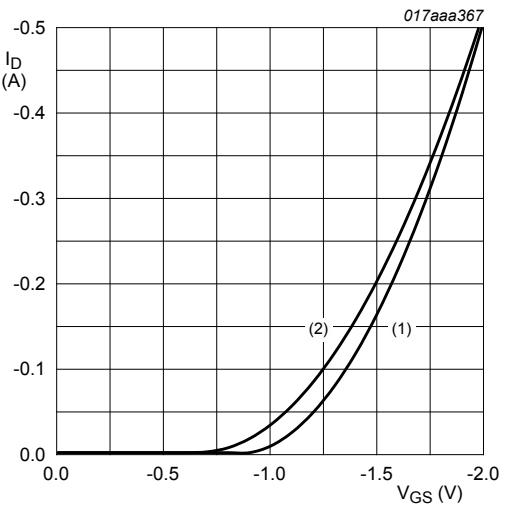
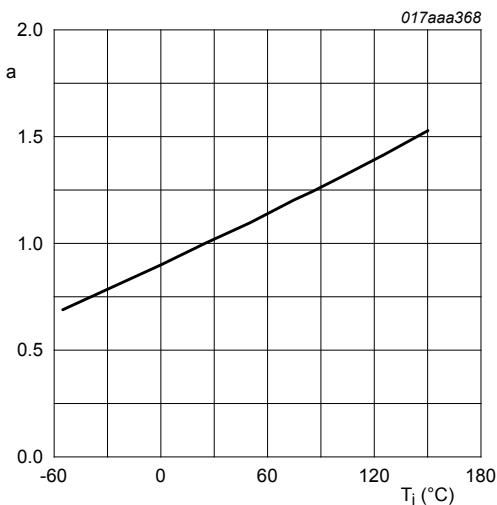
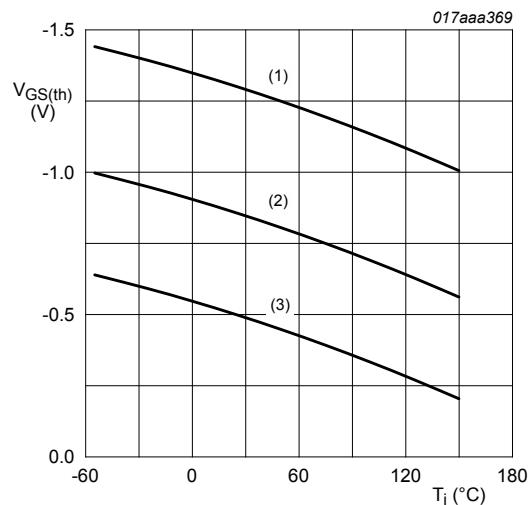


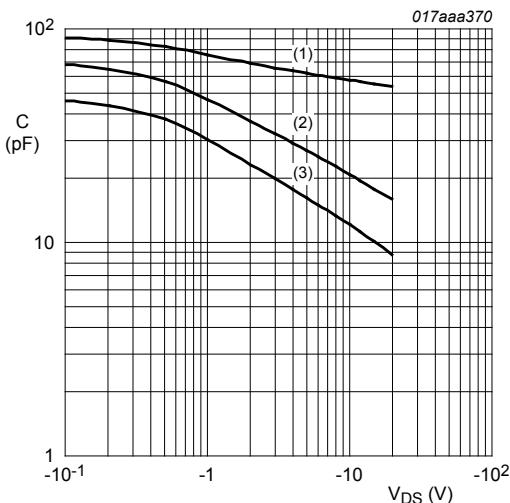
Fig. 24. TR2; Transfer characteristics: drain current as a function of gate-source voltage; typical values



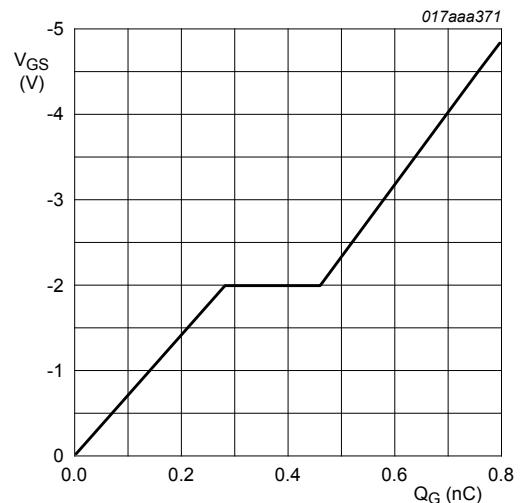
**Fig. 25. TR2; Normalized drain-source on-state resistance as a function of ambient temperature; typical values**



**Fig. 26. TR2; Gate-source threshold voltage as a function of junction temperature**



**Fig. 27. TR2; Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



**Fig. 28. TR2; Gate-source voltage as a function of gate charge; typical values**

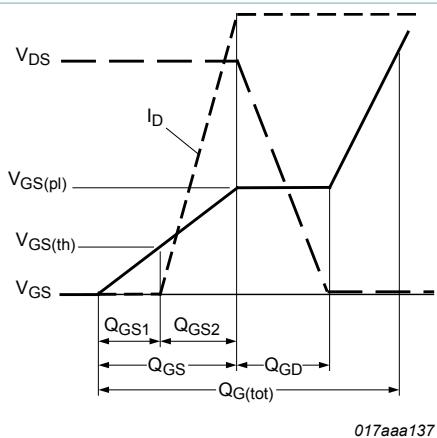


Fig. 29. Gate charge waveform definitions

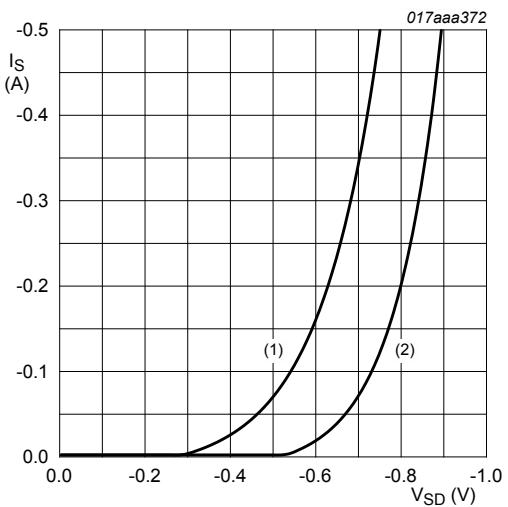


Fig. 30. TR2; Source current as a function of source-drain voltage; typical values

## 11. Test information

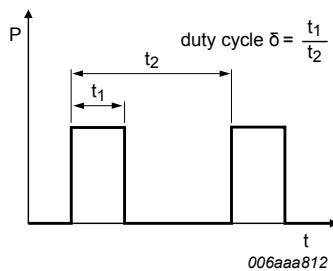


Fig. 31. Duty cycle definition

### 11.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

## 12. Package outline

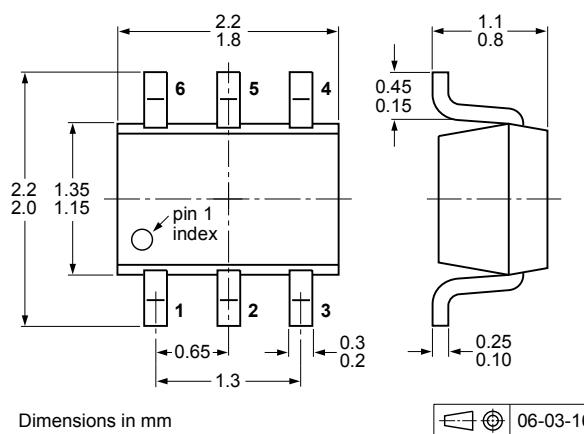


Fig. 32. Package outline TSSOP6 (SOT363)

## 13. Soldering

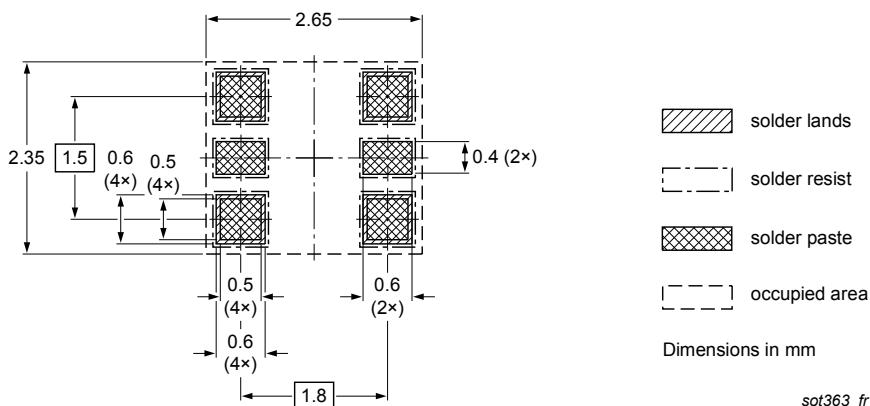


Fig. 33. Reflow soldering footprint for TSSOP6 (SOT363)

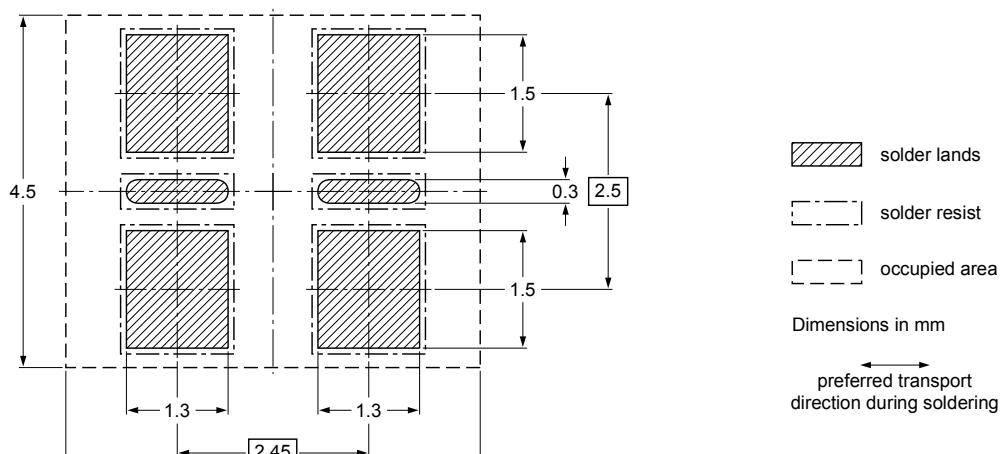


Fig. 34. Wave soldering footprint for TSSOP6 (SOT363)

## 14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMGD290UCEA v.3	20140328	Product data sheet	-	PMGD290UCEA v.2
Modifications:	<ul style="list-style-type: none"><li>Table 7: <math>I_{GSS}</math> parameter unit corrected</li></ul>			
PMGD290UCEA v.2	20130418	Product data sheet	-	PMGD290UCEA v.1
PMGD290UCEA v.1	20130415	Product data sheet	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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