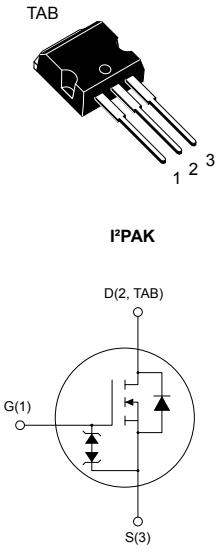


## N-channel 600 V, 0.230 $\Omega$ typ., 13 A MDmesh™ M2 EP Power MOSFET in an I<sup>2</sup>PAK package

### Features



Order code	V <sub>DS</sub>	R <sub>D(on)</sub> max.	I <sub>D</sub>
STI20N60M2-EP	600 V	0.278 $\Omega$	13 A

- Extremely low gate charge
- Excellent output capacitance (C<sub>oss</sub>) profile
- Very low turn-off switching losses
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications
- Tailored for very high frequency converters ( $f > 150$  kHz)

### Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 enhanced performance (EP) technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance, optimized switching characteristics with very low turn-off switching losses, rendering it suitable for the most demanding very high frequency converters.

Product status link	
<a href="#">STI20N60M2-EP</a>	
Product summary	
<b>Order code</b>	
Order code	STI20N60M2-EP
Marking	20N60M2EP
Package	I <sup>2</sup> PAK
Packing	Tube

## 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	13	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	8	A
$I_{DM}^{(1)}$	Drain current (pulsed)	52	A
$P_{TOT}$	Total dissipation at $T_C = 25^\circ\text{C}$	110	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	V/ns
$T_J$	Operating junction temperature range	- 55 to 150	$^\circ\text{C}$
$T_{stg}$	Storage temperature range		

1. Pulse width limited by safe operating area.
2.  $I_{SD} \leq 13 \text{ A}$ ,  $di/dt \leq 400 \text{ A}/\mu\text{s}$ ;  $V_{DS \text{ peak}} < V_{(BR)DSS}$ ;  $V_{DD} = 400 \text{ V}$ .
3.  $V_{DS} \leq 480 \text{ V}$

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.14	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	62.5	$^\circ\text{C}/\text{W}$

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$ )	2.7	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25^\circ\text{C}$ , $I_D = I_{AR}$ ; $V_{DD} = 50 \text{ V}$ )	138	mJ

## 2 Electrical characteristics

$T_C = 25^\circ\text{C}$  unless otherwise specified

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	600			V
$I_{\text{DSS}}$	Zero gate voltage	$V_{GS} = 0 \text{ V}, V_{DS} = 600 \text{ V}$			1	$\mu\text{A}$
	Drain current	$V_{GS} = 0 \text{ V}, V_{DS} = 600 \text{ V}, T_C = 125^\circ\text{C}^{(1)}$			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 25 \text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	3.25	4	4.75	V
$R_{DS(\text{on})}$	Static drain-source on-resistance	$V_{GS} = 10 \text{ V}, I_D = 6.5 \text{ A}$		0.230	0.278	$\Omega$

1. Defined by design, not subject to production test.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100 \text{ V}, f = 1 \text{ MHz}, V_{GS} = 0 \text{ V}$	-	787	-	pF
$C_{oss}$	Output capacitance		-	50	-	
$C_{rss}$	Reverse transfer capacitance		-	1.2	-	
$C_{oss \text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0 \text{ to } 480 \text{ V}, V_{GS} = 0 \text{ V}$	-	89	-	pF
$R_G$	Intrinsic gate resistance	$f = 1 \text{ MHz}, I_D = 0 \text{ A}$	-	5.9	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 480 \text{ V}, I_D = 13 \text{ A}, V_{GS} = 0 \text{ to } 10 \text{ V}$ (see Figure 15. Test circuit for gate charge behavior)	-	22	-	nC
$Q_{gs}$	Gate-source charge		-	3.5	-	
$Q_{gd}$	Gate-drain charge		-	10.5	-	

1.  $C_{oss \text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 6. Switching energy**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$E_{\text{off}}$	Turn-off energy (from 90% $V_{GS}$ to 0% $I_D$ )	$V_{DD} = 400 \text{ V}, I_D = 2 \text{ A}, R_G = 4.7 \Omega, V_{GS} = 10 \text{ V}$	-	7.2	-	$\mu\text{J}$
		$V_{DD} = 400 \text{ V}, I_D = 5 \text{ A}, R_G = 4.7 \Omega, V_{GS} = 10 \text{ V}$	-	20.4	-	$\mu\text{J}$

**Table 7. Switching times**

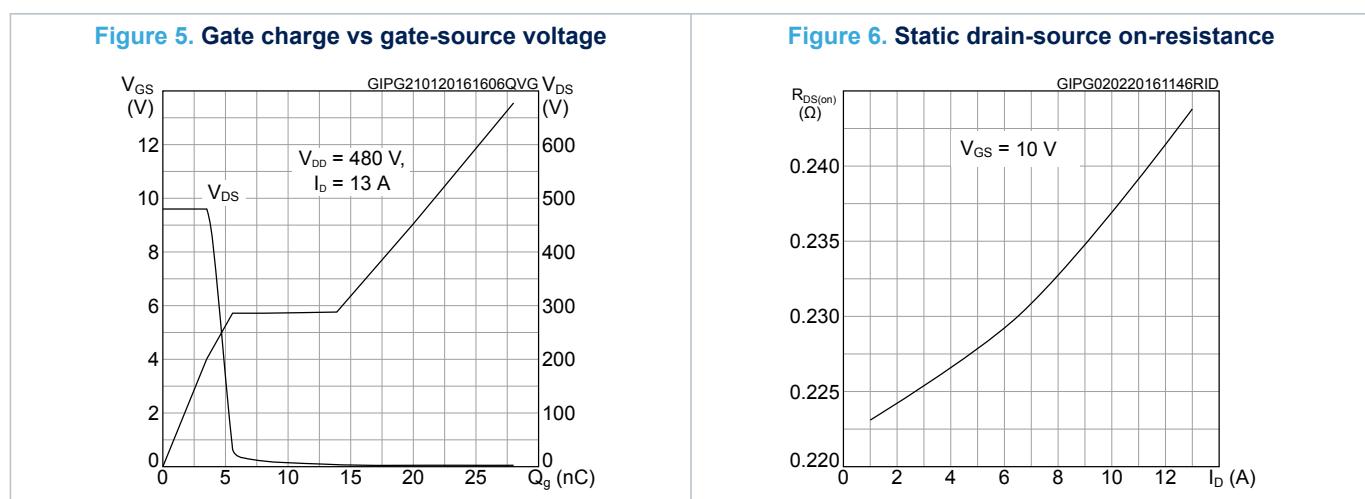
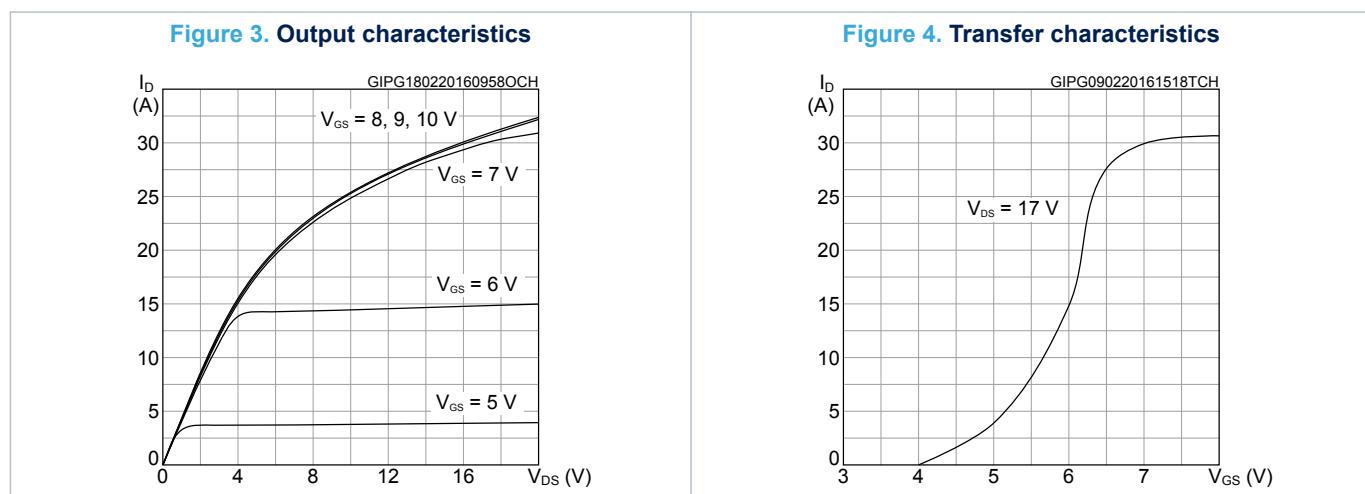
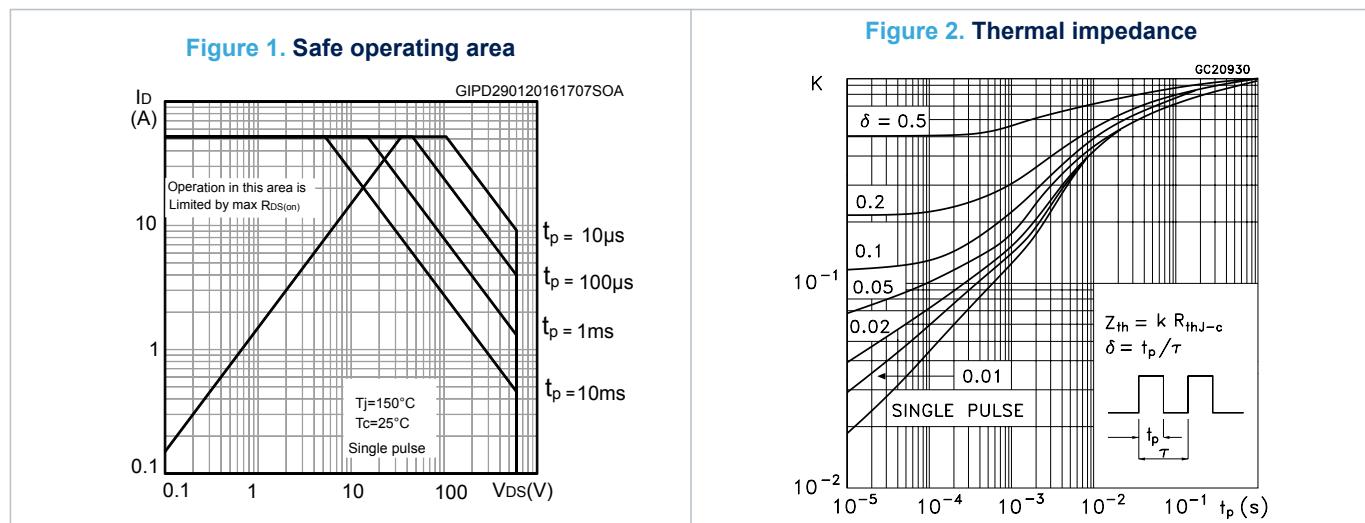
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300 \text{ V}, I_D = 6.5 \text{ A}, R_G = 4.7 \Omega, V_{GS} = 10 \text{ V}$ (see <a href="#">Figure 14. Test circuit for resistive load switching times</a> and <a href="#">Figure 19. Switching time waveform</a> )	-	10.5	-	ns
$t_r$	Rise time		-	5.2	-	ns
$t_{d(off)}$	Turn-off delay time		-	41	-	ns
$t_f$	Fall time		-	8	-	ns

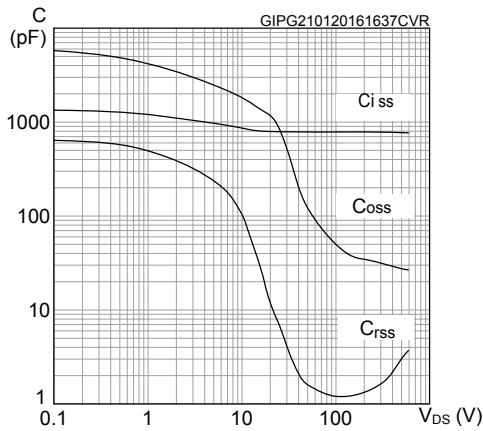
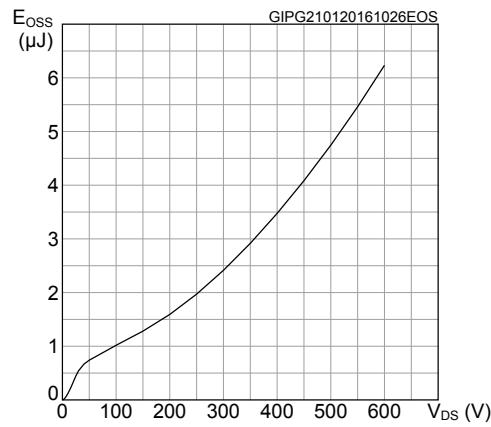
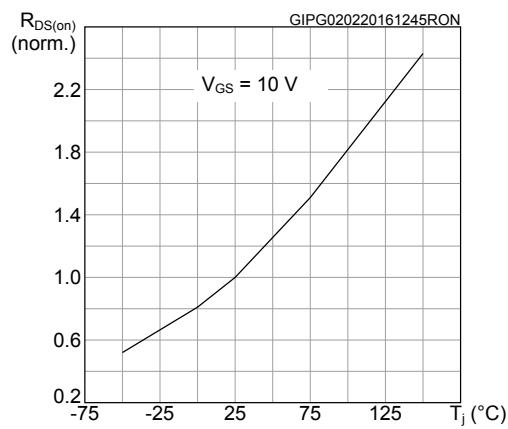
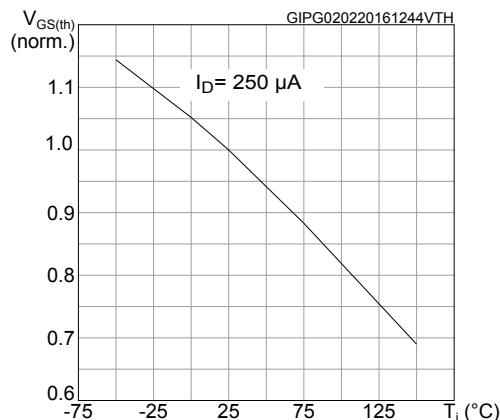
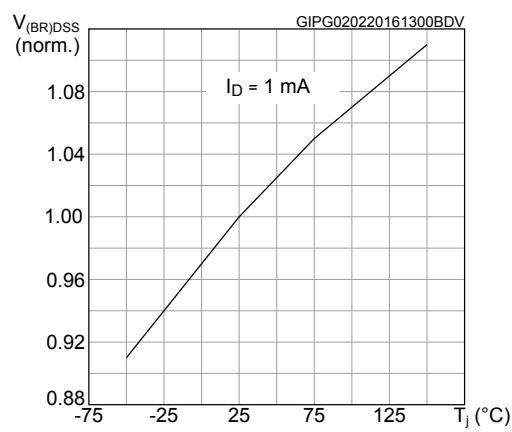
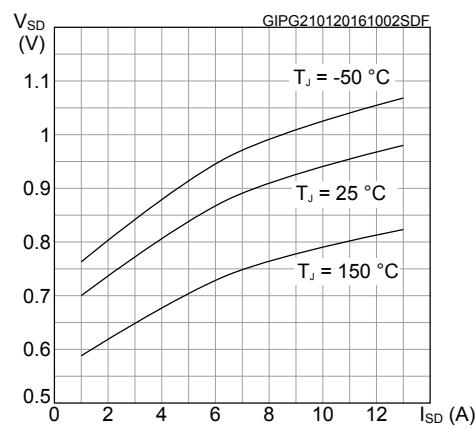
**Table 8. Source-drain diode**

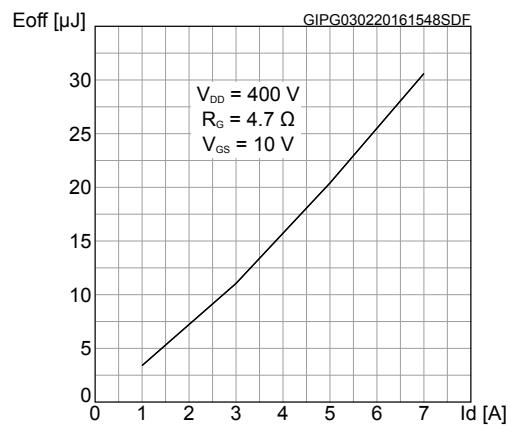
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		13	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		52	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0 \text{ V}, I_{SD} = 13 \text{ A}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 13 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s}, V_{DD} = 60 \text{ V}$ (see <a href="#">Figure 16. Test circuit for inductive load switching and diode recovery times</a> )	-	230		ns
$Q_{rr}$	Reverse recovery charge	$T_j = 150^\circ\text{C}$ (see <a href="#">Figure 16. Test circuit for inductive load switching and diode recovery times</a> )	-	2.3		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	20		A
$t_{rr}$	Reverse recovery time		-	287		ns
$Q_{rr}$	Reverse recovery charge		-	2.9		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	20.2		A

1. Pulse width is limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

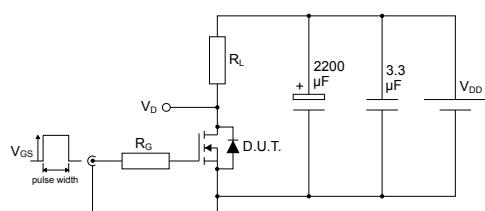


**Figure 7. Capacitance variations**

**Figure 8. Output capacitance stored energy**

**Figure 9. Normalized on-resistance vs temperature**

**Figure 10. Normalized gate threshold voltage vs temperature**

**Figure 11. Normalized V\_(BR)DSS vs temperature**

**Figure 12. Source-drain diode forward characteristics**


**Figure 13. Turn-off switching energy vs drain current**

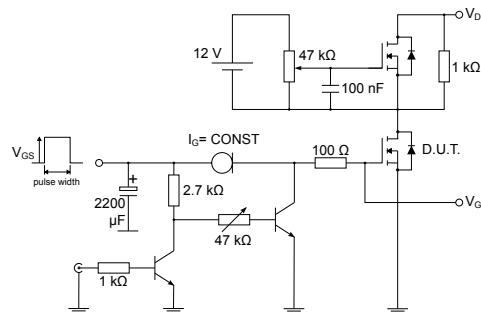
### 3 Test circuits

**Figure 14.** Test circuit for resistive load switching times



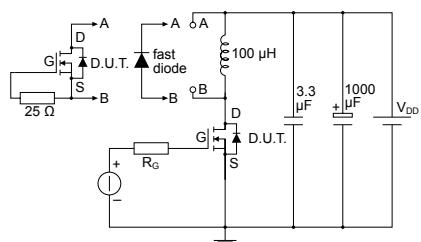
AM01468v1

**Figure 15.** Test circuit for gate charge behavior



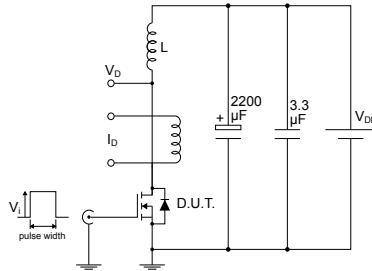
AM01469v1

**Figure 16.** Test circuit for inductive load switching and diode recovery times



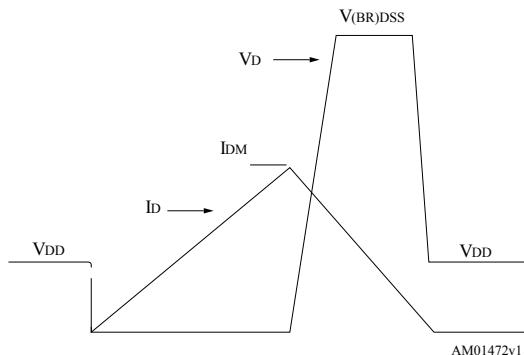
AM01470v1

**Figure 17.** Unclamped inductive load test circuit



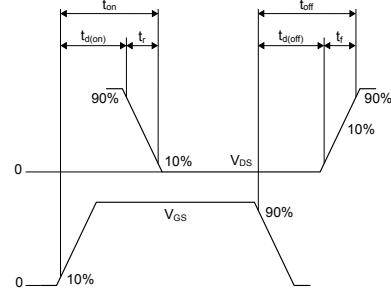
AM01471v1

**Figure 18.** Unclamped inductive waveform



AM01472v1

**Figure 19.** Switching time waveform



AM01473v1

**4**

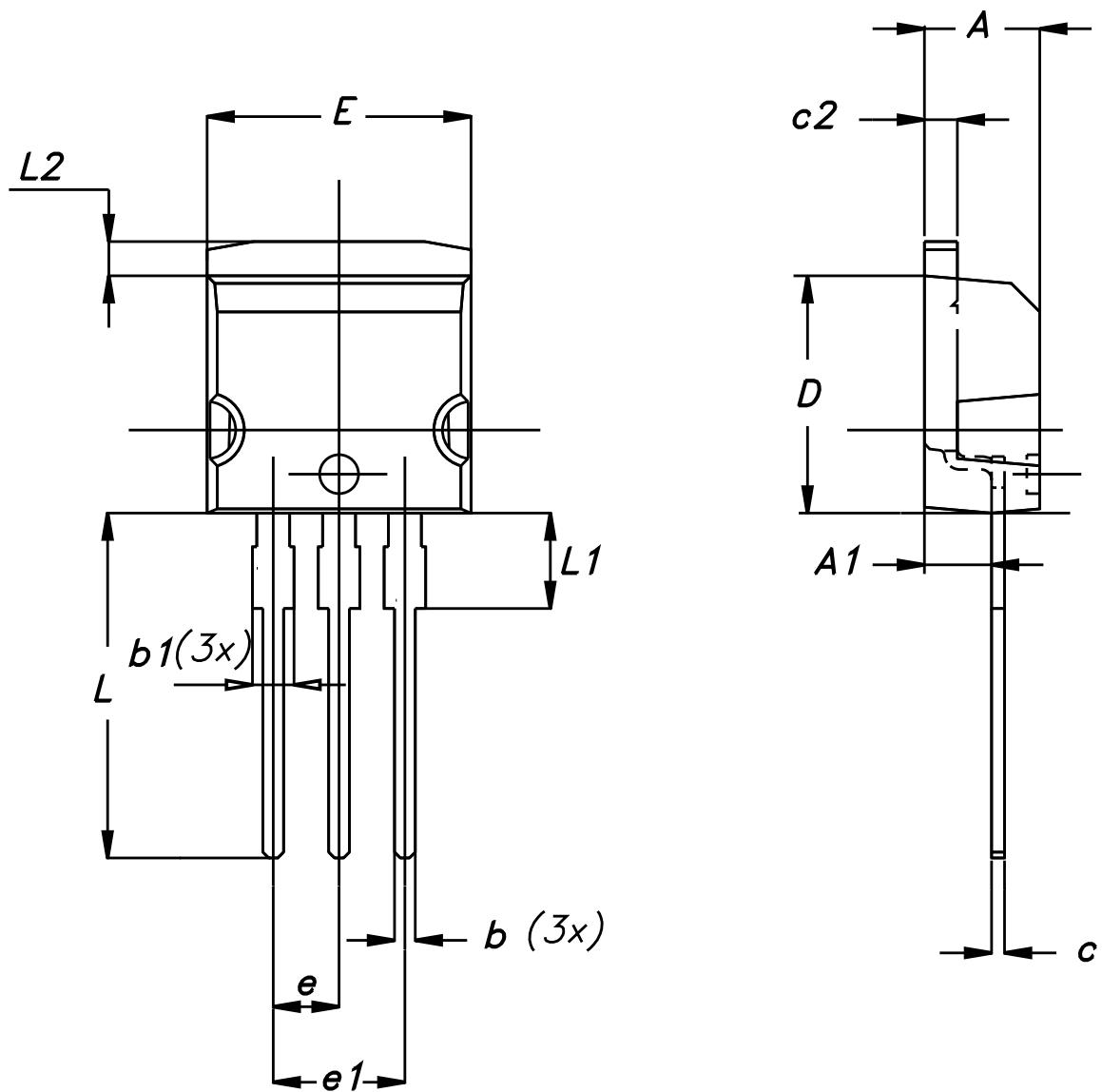
## Package information

---

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

#### 4.1 TO-220 package information

Figure 20. I<sup>2</sup>PAK package outline



0004982\_Rev\_H

Table 9. I<sup>2</sup>PAK package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40	-	4.60
A1	2.40	-	2.72
b	0.61	-	0.88
b1	1.14	-	1.70
c	0.49	-	0.70
c2	1.23	-	1.32
D	8.95	-	9.35
e	2.40	-	2.70
e1	4.95	-	5.15
E	10	-	10.40
L	13	-	14
L1	3.50	-	3.93
L2	1.27	-	1.40

## Revision history

**Table 10. Document revision history**

Date	Revision	Changes
20-Mar-2018	1	First release, the part number previously included in DS11505. The document status is production data.
04-Jun-2018	2	Modified <a href="#">Table 1. Absolute maximum ratings</a> and <a href="#">Table 8. Source-drain diode</a> . Minor text changes.

## Contents

<b>1</b>	<b>Electrical ratings .....</b>	<b>2</b>
<b>2</b>	<b>Electrical characteristics.....</b>	<b>3</b>
<b>2.1</b>	Electrical characteristics (curves) .....	5
<b>3</b>	<b>Test circuits .....</b>	<b>8</b>
<b>4</b>	<b>Package information.....</b>	<b>9</b>
<b>4.1</b>	TO-220 package information .....	9
	<b>Revision history .....</b>	<b>12</b>

**IMPORTANT NOTICE – PLEASE READ CAREFULLY**

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2018 STMicroelectronics – All rights reserved