Backlight Driver for 5 LEDs with SemPulse™ Interface

POWER MANAGEMENT

Features

- Input supply voltage range — 2.9V to 5.5V
- Very high efficiency charge pump driver system with three modes — 1x, 1.5x and 2x
- Five programmable current sinks — 0mA to 25mA
- Up to three LED grouping options
- Fade-in/fade-out feature for main LED bank
- Charge pump frequency — 250kHz
- SemPulse single wire interface
- Backlight current accuracy — ±1.5% typical
- Backlight current matching — ±0.5% typical
- LED float detection
- Automatic sleep mode (LEDs off) — I_Q = 60µA (typ.)
- Shutdown current — 0.1µA (typical)
- Ultra-thin package — 2 x 2 x 0.6 (mm)
- Fully WEEE and RoHS compliant

Applications

- Cellular phones, smart phones, and PDAs
- LCD modules
- Portable media players
- Digital cameras
- Personal navigation devices
- Display/keypad backlighting and LED indicators

Description

The SC657 is a high efficiency charge pump LED driver using Semtech's proprietary charge pump technology. Performance is optimized for use in single-cell Li-ion battery applications.

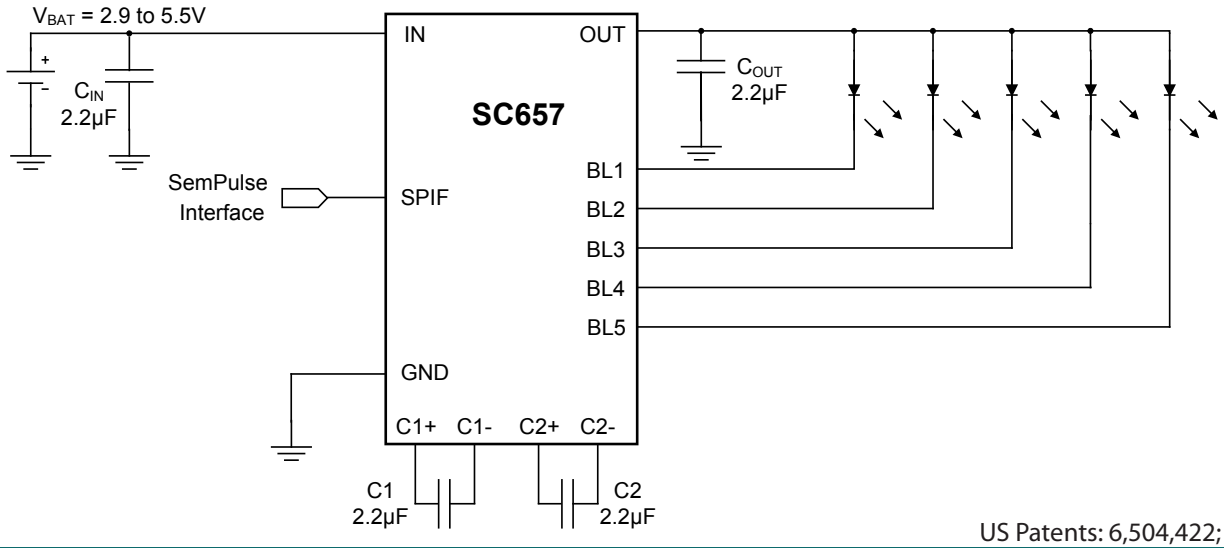
The charge pump provides backlight current utilizing five matched current sinks. The load and supply conditions determine whether the charge pump operates in 1x, 1.5x, or 2x mode. An optional fading feature that gradually adjusts the backlight current is provided to simplify control software.

The SC657 uses the proprietary SemPulse™ single wire interface to control all functions of the device, including backlight currents. The single wire interface minimizes microcontroller and interface pin counts. The five LEDs can be grouped in up to three separate banks that can be independently controlled.

The SC657 enters sleep mode when all the LED drivers are disabled. In this mode, the quiescent current is reduced while the device continues to monitor the SemPulse interface.

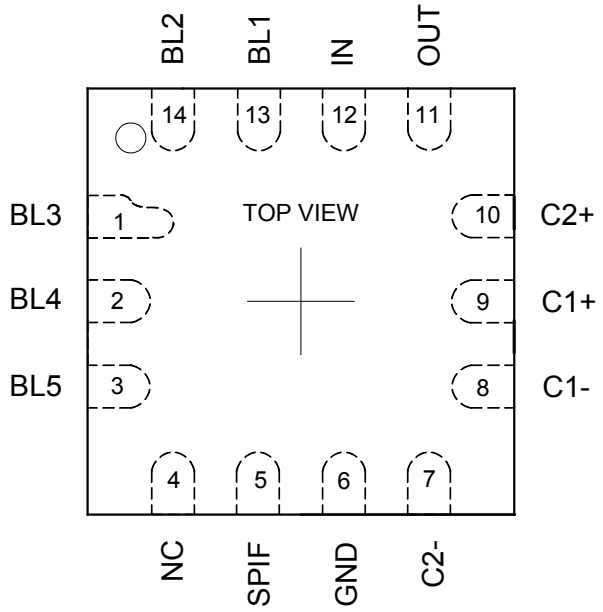
With a 2 x 2 (mm) package and four small capacitors, the SC657 provides a complete LED driver solution with a minimal PCB footprint.

Typical Application Circuit



US Patents: 6,504,422; 6,794,926

Pin Configuration



MLPQ-UT-14; 2x2, 14 LEAD

θ_{JA} = 127°C/W

Ordering Information

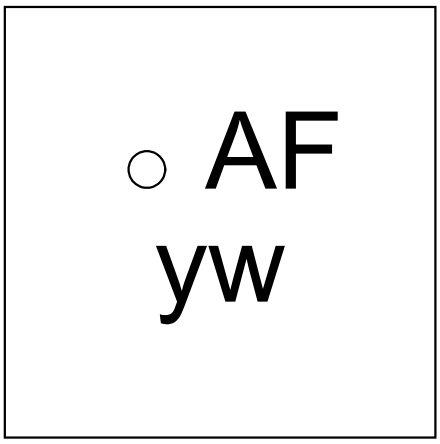
Device	Package
SC657ULTRT[1][2]	MLPQ-UT-14 2×2
SC657EVB	Evaluation Board

Notes:

(1) Available in tape and reel only. A reel contains 3,000 devices.

(2) Lead-free package only. Device is WEEE and RoHS compliant.

Marking Information



AF = Marking code for SC657

yw = Date Code

SEMTECH

Absolute Maximum Ratings

IN, OUT (V) ..... -0.3 to +6.0
C1+, C2+ (V) ..... -0.3 to (V_{OUT} + 0.3)
Pin Voltage — All Other Pins (V) ..... -0.3 to (V_{IN} + 0.3)
OUT Short Circuit Duration ..... Continuous
ESD Protection Level[1] (kV) 2

Recommended Operating Conditions

Ambient Temperature Range (°C) ..... -40 ≤ T_A ≤ +85
Input Voltage (V) ..... 2.9 ≤ V_{IN} ≤ 5.5
Output Voltage (V) ..... 2.5 ≤ V_{OUT} ≤ 5.25
Voltage Difference between any two LEDs (V) .. ΔV_F < 1.0[2]

Thermal Information

Thermal Resistance, Junction to Ambient[3] (°C/W) .. 127
Maximum Junction Temperature (°C) ..... +150
Storage Temperature Range (°C) ..... -65 to +150
Peak IR Reflow Temperature (10s to 30s) (°C) ..... +260

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:
(1) Tested according to JEDEC standard JESD22-A114
(2) $\Delta V_{F(max)}$ = 1.0V when V_{IN} = 2.9V, higher V_{IN} supports higher $\Delta V_{F(max)}$
(3) Calculated from package in still air, mounted to 3 x 4.5 (in), 4 layer FR4 PCB per JESD51 standards.

Electrical Characteristics

Unless otherwise noted, T_A = +25°C for Typ, -40°C to +85°C for Min and Max, $T_{J(MAX)}$ = 125°C, V_{IN} = 3.7 V, C_{IN} = C_1 = C_2 = C_{OUT} = 2.2µF (ESR = 0.03Ω)[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Shutdown Current	$I_{Q(OFF)}$			0.1	2	µA
Total Quiescent Current	I_Q	All outputs disabled, SPIF = V_{IN}[2]		60	100	µA
		Charge pump enabled, 1x Mode, all LEDs on, I_{BLn} = 0.5mA		1.6		mA
		Charge pump in 1x mode, 2.9V <V_{IN} < 4.2V, all LEDs on, I_{BLn} = 25mA		4.8		
		Charge pump in 1.5x, 2x mode, 2.9V <V_{IN} < 4.2V, all LEDs on, I_{BLn} = 25mA		5.9		
Maximum Total Output Current	$I_{OUT(MAX)}$	V_{IN} > 2.9V, sum of all active LED currents, $V_{OUT(MAX)}$ = 4.2V	125			mA
Backlight Current Setting	I_{BLn}	Nominal setting for BL1 thru BL5	0		25	mA
Backlight Current Matching	I_{BL-BL}	I_{BLn} = 12mA[3]	-3.5	±0.5	+3.5	%
Backlight Current Accuracy	I_{BL_ACC}	I_{BLn} = 12mA	-8	±1.5	+8	%

Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
1x Mode to 1.5x Mode Falling Transition Input Voltage	$V_{TRANS1x}$	I_{OUT} = 50mA, I_{BLn} = 10mA, V_{OUT} = 3.2V		3.25		V
1.5x Mode to 1x Mode Hysteresis	V_{HYST1x}	I_{OUT} = 50mA, I_{BLn} = 10mA, V_{OUT} = 3.2V		250		mV
1.5x Mode to 2x Mode Falling Transition Input Voltage	$V_{TRANS1.5x}$	I_{OUT} = 50mA, I_{BLn} = 10mA, V_{OUT} = 4.0V[4]		3.13		V
Current Sink Off-State Leakage Current	$I_{BLn(off)}$	$V_{IN} = V_{BLn}$ = 4.2V		0.1	1	µA
Charge Pump Frequency	f_{PUMP}	V_{IN} = 3.2V		250		kHz
Output Short Circuit Current Limit	$I_{OUT(SC)}$	OUT pin shorted to GND		60		mA
		V_{OUT} > 2.5V		300		
Under Voltage Lockout	$V_{UVLO-OFF}$	Increasing V_{IN}		2.7		V
	$V_{UVLO-HYS}$	Hysteresis		800		mV
Over-Voltage Protection	V_{OVP}	OUT pin open circuit, $V_{OUT} = V_{OVP}$, rising threshold		5.7	6.0	V
Over-Temperature	T_{OT}	Rising temperature		160		°C
OT Hysteresis	T_{OT-HYS}			20		°C

Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SemPulse Interface						
Input High Threshold	V_{IH}	V_{IN} = 5.5V	1.6			V
Input Low Threshold	V_{IL}	V_{IN} = 2.9V			0.4	V
Input High Current	I_{IH}	V_{IN} = 5.5V	-1		+1	µA
Input Low Current	I_{IL}	V_{IN} = 5.5V	-1		+1	µA
Start up Time(5)	t_{SU}	Only required when leaving shutdown mode	1			ms
Bit Pulse Duration(6)	t_{HI}		0.75		250	µs
Duration Between Pulses(6)	t_{LO}		0.75		250	µs
Hold Time - Address(6)	t_{HOLDA}	Software limit — SPIF must be held high for this amount of time to latch the data	550		5000	µs
Hold Time - Data(6)	t_{HOLDD}	Software limit — SPIF must be held high for this amount of time to latch the address	550			µs
Bus Reset Time (6)	t_{BR}	Software Limit — SPIF must be held high for this amount of time to force a bus system reset	12			ms
Shutdown Time (7)	t_{SD}	Software Limit — SPIF must be held low for this amount of time to disable device	10			ms

Notes:

(1) Capacitors are MLCC of X5R type. Production tested with higher value capacitors than the application requires

(2) SPIF is high for more than 10ms to place serial bus in standby mode

(3) Current matching is defined as $\pm [I_{BL(MAX)} - I_{BL(MIN)}] / [I_{BL(MAX)} + I_{BL(MIN)}]$.

(4) Test voltage is V_{OUT} = 4.2V — a relatively extreme LED voltage — to force a transition during test. Typically V_F = 3.2V for white LEDs.

(5) The SemPulse start-up time is the minimum time that the SPIF pin must be held high to enable the part before starting communication.

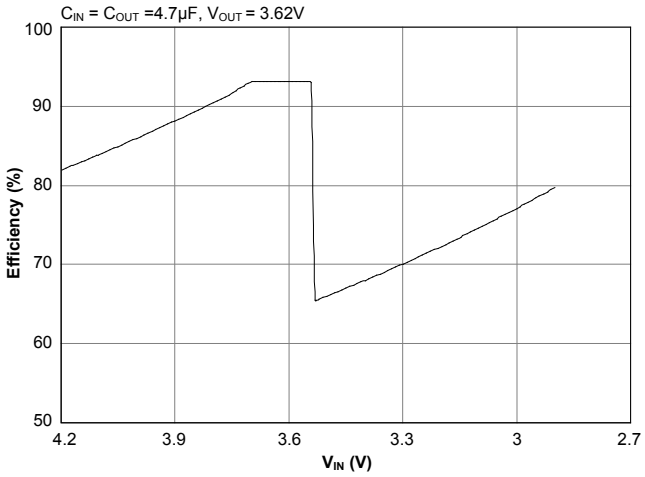
(6) The source driver used to provide the SemPulse Output must meet these limits.

(7) The SemPulse shutdown time is the minimum time that the SPIF pin must be pulled low to shut the part down.

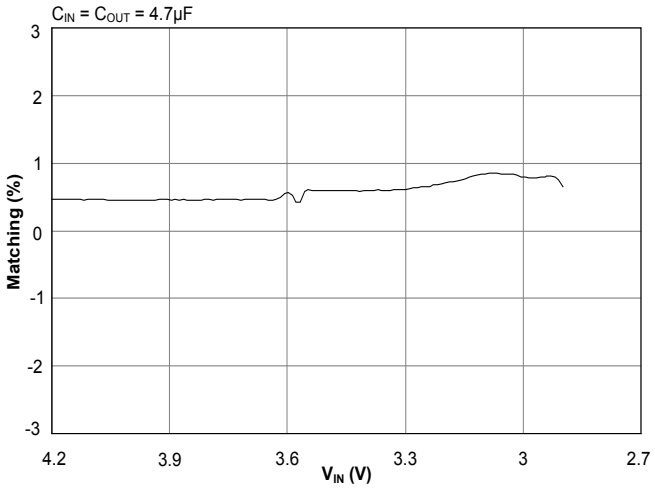
Typical Characteristics

All data taken with T_A = +25 °C, V_{IN} = 3.7V, C_{IN} = C_1 = C_2 = C_{OUT} = 2.2µF (ESR = 0.03Ω) unless otherwise noted.

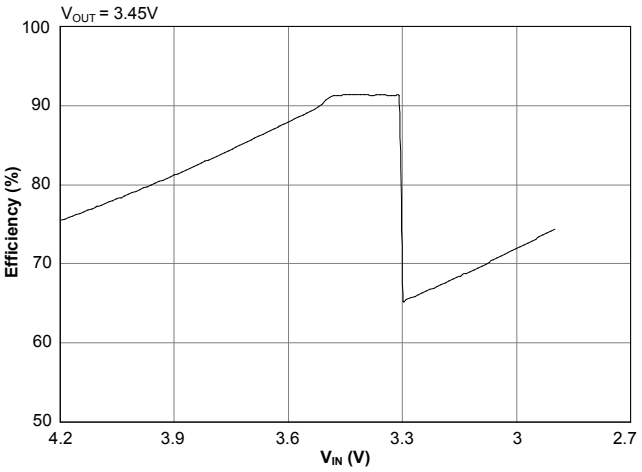
Backlight Efficiency (5 LEDs) — 25mA Each



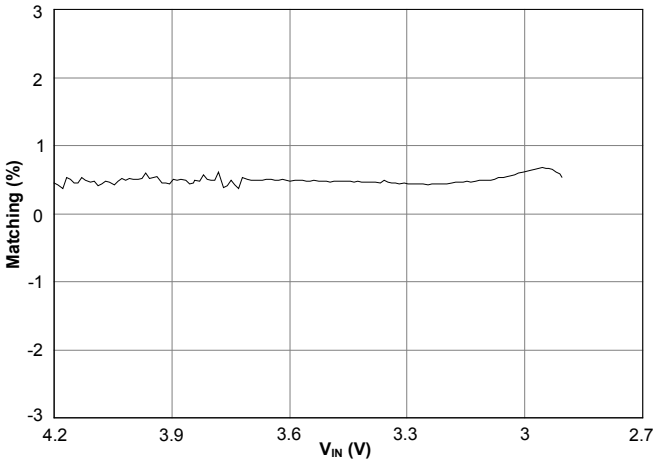
Backlight Matching (5 LEDs) — 25mA Each



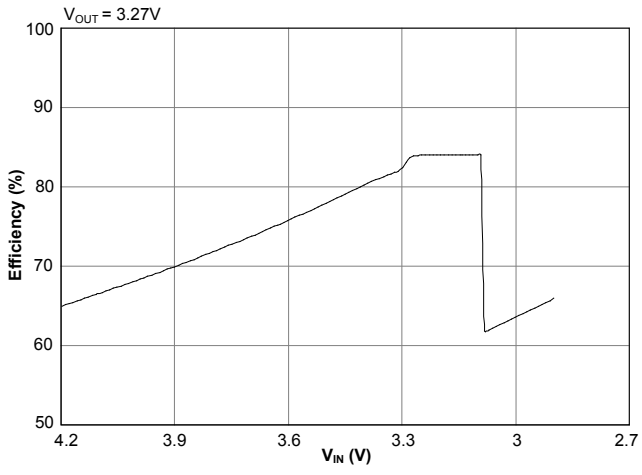
Backlight Efficiency (5 LEDs) — 12mA Each



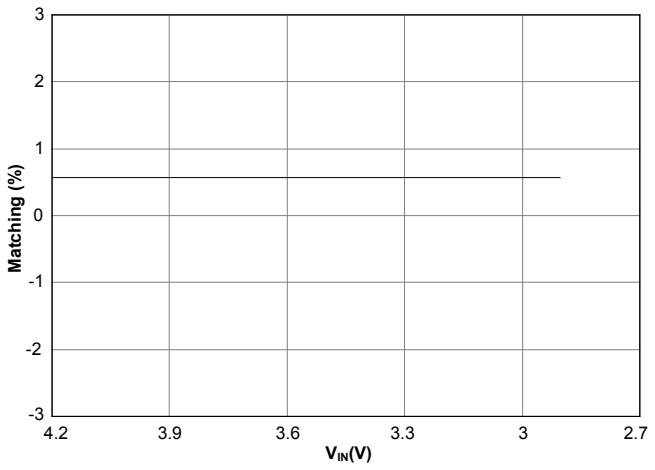
Backlight Matching (5 LEDs) — 12mA Each



Backlight Efficiency (5 LEDs) — 4.5mA Each

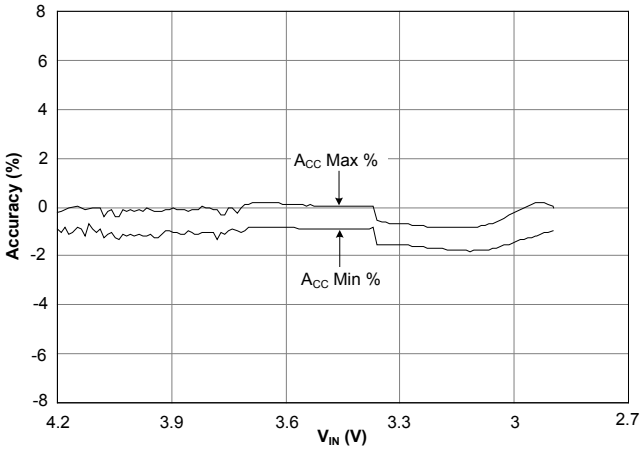


Backlight Matching (5 LEDs) — 4.5mA Each

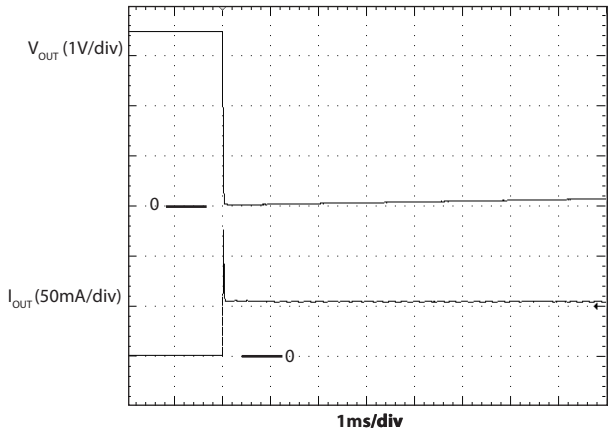


Typical Characteristics (continued)

Backlight Accuracy (5 LEDs) — 12mA Each

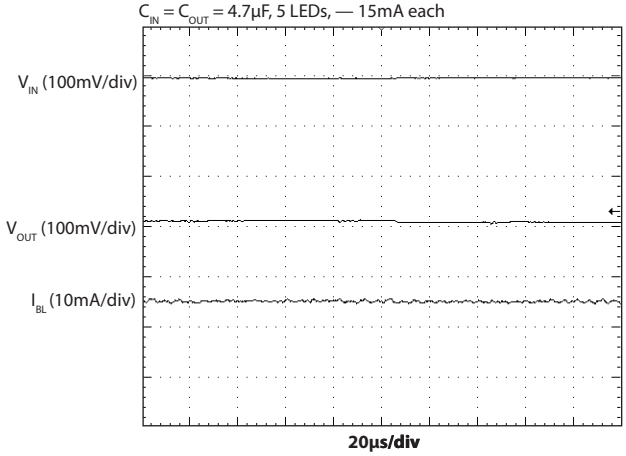


Output Short Circuit Current Limit



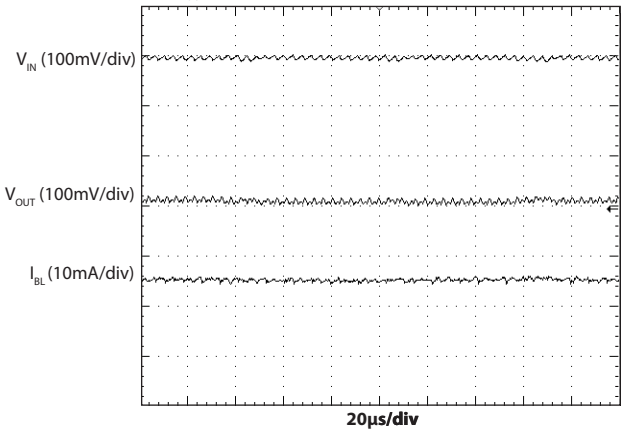
Ripple — 1x Mode

$C_{IN} = C_{OUT} = 4.7\mu F$, 5 LEDs, — 15mA each



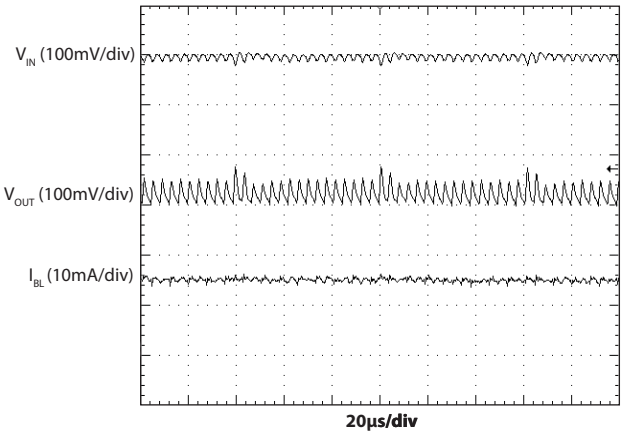
Ripple — 1.5x Mode

$C_{IN} = C_{OUT} = 4.7\mu F$, V_{IN} = 2.9V, 5 LEDs, — 15mA each

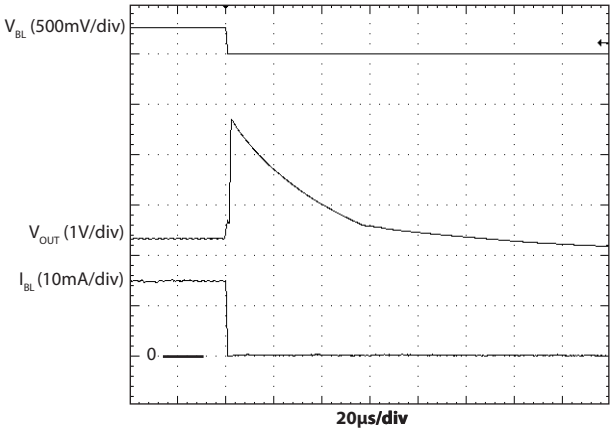


Ripple — 2x Mode

$C_{IN} = C_{OUT} = 4.7\mu F$, V_{IN} = 2.9V, 5 LEDs — 15mA each



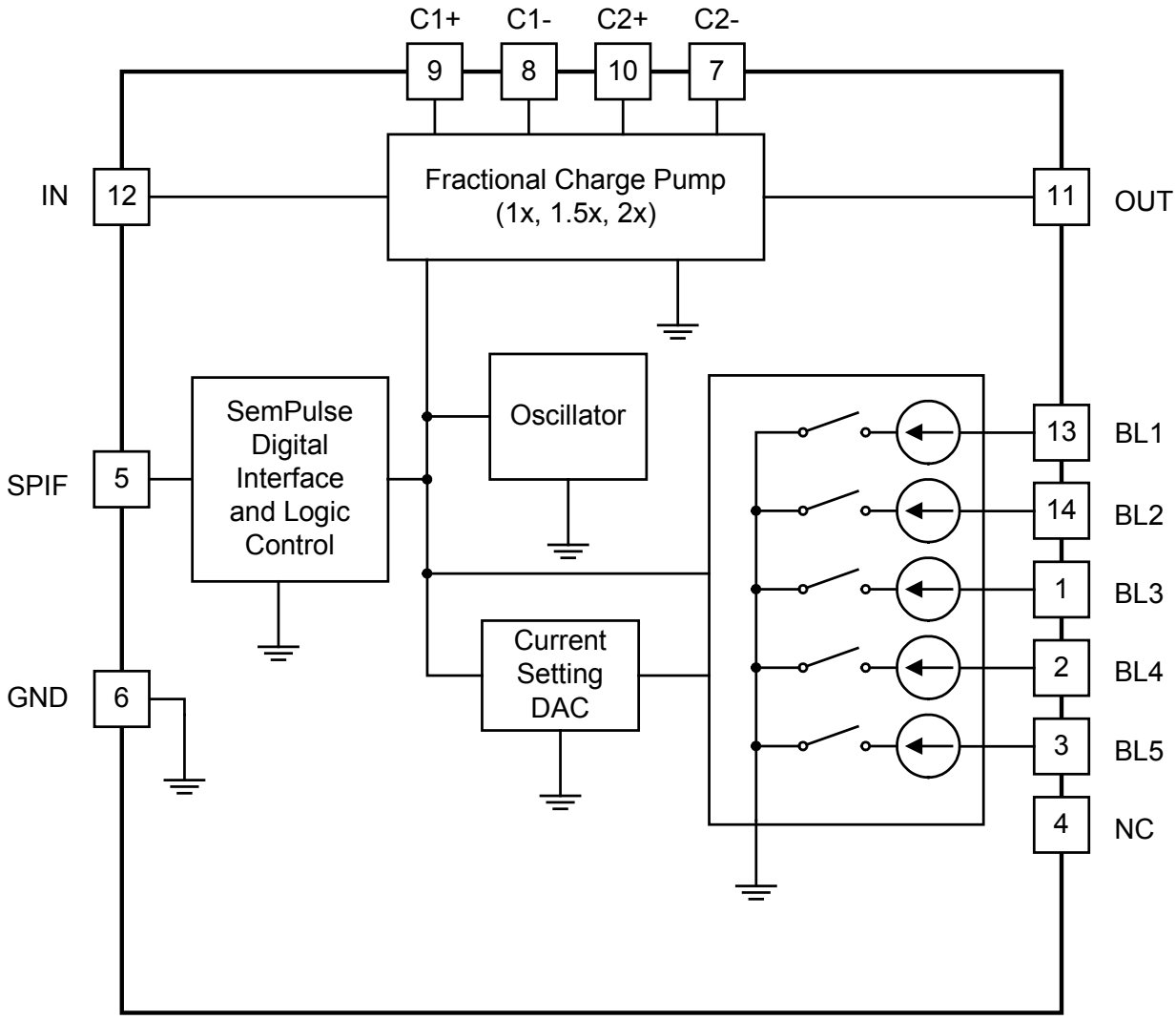
Output Open Circuit Protection



Pin Descriptions

Pin #	Pin Name	Pin Function
1	BL3	Current sink output for main backlight LED 3 — leave this pin open if unused
2	BL4	Current sink output for main backlight LED 4 — leave this pin open if unused
3	BL5	Current sink output for main backlight LED 5 — leave this pin open if unused
4	NC	No connection
5	SPIF	SemPulse single wire interface pin — used to enable/disable the device and to configure all registers (refer to Register Map and SemPulse Interface sections)
6	GND	Ground pin
7	C2-	Negative connection to bucket capacitor 2
8	C1-	Negative connection to bucket capacitor 1
9	C1+	Positive connection to bucket capacitor 1
10	C2+	Positive connection to bucket capacitor 2
11	OUT	Charge pump output — all LED anode pins should be connected to this pin
12	IN	Battery voltage input
13	BL1	Current sink output for main backlight LED 1 — leave this pin open if unused
14	BL2	Current sink output for main backlight LED 2 — leave this pin open if unused

Block Diagram



Applications Information

General Description

This design is optimized for handheld applications supplied from a single Li-ion cell and includes the following key features:

- A high efficiency fractional charge pump that supplies power to all LEDs
- Five matched current sinks that control LED backlighting current, providing 0mA to 25mA per LED
- LEDs can be grouped in up to three independently controlled banks

High Current Fractional Charge Pump

The backlight outputs are supported by a high efficiency, high current fractional charge pump output. The charge pump multiplies the input voltage by 1x, 1.5x, or 2x. The charge pump switches at a fixed frequency of 250kHz in 1.5x and 2x modes and is disabled in 1x mode to save power and improve efficiency.

The mode selection circuit automatically selects the mode as 1x, 1.5x, or 2x based on circuit conditions such as LED voltage, input voltage, and load current. The 1x mode is the most efficient of the three modes, followed by 1.5x and 2x modes. Circuit conditions such as low input voltage, high output current, or high LED voltage place a higher demand on the charge pump output. A higher numerical mode (1.5x or 2x) may be needed momentarily to maintain regulation at the OUT pin during intervals of high demand. The charge pump responds to momentary high demands, setting the charge pump to the optimum mode to deliver the output voltage and load current while optimizing efficiency. Hysteresis is provided to prevent mode toggling.

The charge pump requires two bucket capacitors for proper operation. One capacitor must be connected between the C1+ and C1- pins and the other must be connected between the C2+ and C2- pins as shown in the Typical Application Circuit diagram. These capacitors should be equal in value, with a minimum capacitance of 1µF to support the charge pump current requirements. The device also requires at least 1µF of capacitance on the IN pin and at least 1µF of capacitance on the OUT pin to minimize noise and support the output current requirements of up to 90mA. For output currents higher than 90mA, a nominal value of 4.7µF is recommended for C_{OUT} and C_{IN}. Capacitors with X7R or X5R ceramic dielectric are strongly recommended for their low ESR and superior temperature and voltage characteristics. Y5V capacitors should not be used as their temperature coefficients make them unsuitable for this application.

It is important to ensure the minimum capacitance value of each capacitor does not drop below 1µF. This may require the use of 2.2µF capacitors to be sure that the degradation of capacitance due to DC voltage does not cause the capacitance to go below 1µF.

LED Backlight Current Sinks

The backlight current is set via the SemPulse interface. The current is regulated to a value between 0mA and 25mA. The step size varies depending upon the current setting. Between 0mA and 5mA, the step size is 0.5mA. The step size increases to 1mA for settings between 5mA and 21mA. Steps are 2mA between 21mA and 25mA. The variation in step size allows finer adjustment for dimming functions in the low current setting range and coarse adjustment at higher current settings where small current changes are not visibly noticeable in LED brightness. A zero setting is also included to allow the current sink to be disabled by writing to either the enable bit or the current setting register for maximum flexibility.

All backlight current sinks have matched currents, even when there is a variation in the forward voltages (ΔV_F) of the LEDs. A ΔV_F difference of 1.0V is supported when the input voltage is at 2.9V. Higher ΔV_F LED mis-match is supported when V_{IN} is higher than 2.9V. All current sink outputs are compared and the lowest output is used for setting the voltage regulation at the OUT pin. This is done to ensure that sufficient bias exists for all LEDs.

The backlight LEDs default to the off state upon power-up. For backlight applications using less than five LEDs, any unused output must be left open and the unused LED must remain disabled. When writing to the backlight enable register, a zero (0) must be written to the corresponding bit of any unused output.

Applications Information (continued)

Backlight Quiescent Current

The quiescent current required to operate all backlights is reduced when the backlight current is set to 4.0mA or less. This feature results in higher efficiency under light-load conditions. Further reduction in quiescent current will result from using fewer than the maximum number of LEDs.

LED Banks

The LEDs can be grouped in up to three independently controlled LED banks. Using the SemPulse interface, the five LED drivers can be grouped as described in the Backlight Grouping Configuration subsection. The banks can be used to provide up to three different current options. This can be useful for controlling keypad, display, and auxiliary backlight operation from one SC657 device.

The LED banks provide versatility by allowing backlights to be controlled independently. For example, applications that have a main and sub display may also need to supply an indicator LED. The three bank option allows the SC657 to control each function with different current settings. Another application involves backlighting two displays and a keypad, each requiring different brightness settings. A third scenario requires supplying different brightness levels to different types of LEDs (such as RGB) to create display effects. In all applications, the brightness level for each LED can be set independently.

Backlight Fade-in / Fade-out Function

The SC657 contains bits that control the fade state of the main bank. When enabled, the fade function causes the backlight settings to step from their current state to the next programmed state as soon as the new state is stored in its register. For example, if the backlight is set at 25mA and the next setting is the off state, the backlight will step from 25mA down to 0mA using all settings at the fade rate specified by the bits in register 04h. The same is true when turning on or increasing the backlight current — the backlight current will step from the present level to the new level at the step rate defined in register 04h. This process applies to the main display only.

The fade rate may be changed dynamically when a fade operation is active by writing new values to the fade register. When a new backlight level is written during an ongoing fade operation, the fade will be redirected to the new value from the present state. An ongoing fade operation may be cancelled by disabling fade which will result in the backlight current changing immediately to the final value. If fade is disabled, the current level will change immediately without the fade delay.

The state diagram in Figure 1 describes the fade operation. More details can be found in the Register Map section.

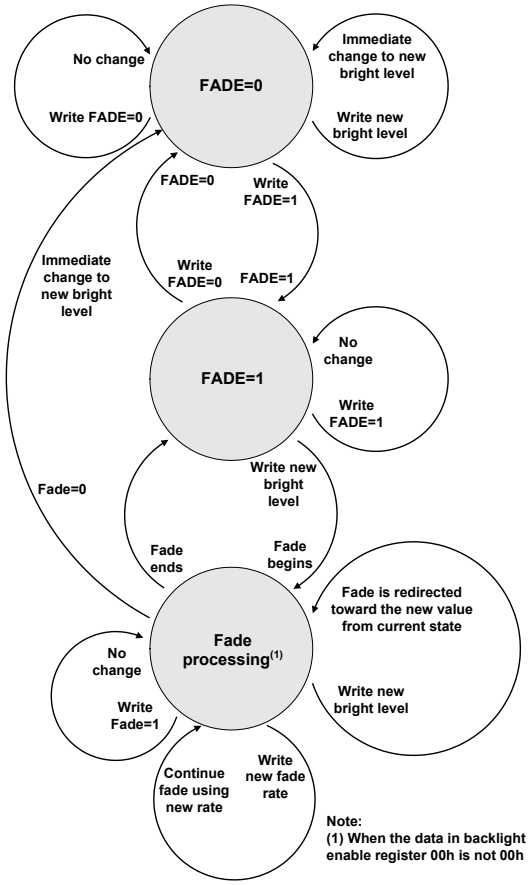


Figure 1 — State Diagram for Fade Function

Fade-In from Off State

When the initial state of the main backlight current register is 00h (the data value for 0mA), fading to an on state is accomplished by following the steps listed in Table 1. Following these steps explicitly will ensure that the fade-in operation will proceed with no interruption at the rate specified in the Main Fade register (04h). This procedure must be followed regardless of which backlight grouping

Applications Information (continued)

configuration is being used. Note that it is only necessary to set the BLEN bits for the main display.

Table 1 — Fade-In from Off State

Command Sequence	Action	Data
1. Disable fade	Write to register 04h	00h
2. Set Main back-lights to 0.5mA	Write to register 01h	04h
3. Enable fade	Write to register 04h	01h, 02h, or 03h
4. Set BLEN bits	Write to register 00h	Any value from 01h through 3Fh
5. Set new value of backlight current	Write to register 01h	Any value from 05h through 1Fh

Fade-Out from any On State to Off State

Fading the backlight LEDs from any active state to the off state follows a simple procedure. The sequence of commands for this action is shown in Table 2. Following these steps explicitly will ensure that the fade-out operation will proceed with no interruption at the rate specified in the Main Fade register (04h). This procedure must be followed regardless of the backlight grouping configuration.

Table 2 — Fade-Out from any On State to Off State

Command Sequence	Action	Data
1. Enable fade	Write to register 04h	01h, 02h, or 03h
2. Set Main back-lights to 0mA	Write to register 01h	00h

Fading Between Different On States

Fading from one backlight level to another (up or down) also follows a simple procedure. The sequence of commands for this action is shown in Table 3. Following these steps explicitly will ensure that the fade-in/fade-out operation will proceed with no interruption at the rate specified in the Main Fade register (04h). This procedure must be followed regardless of the backlight grouping configuration.

Table 3 — Fading between Different On States

Command Sequence	Action	Data
1. Enable fade	Write to register 04h	01h, 02h, or 03h
2. Set new value of backlight current	Write to register 01h	Any value from 05h through 1Fh

Additional Information

For more details about the Fade-in/Fade-out function, refer to the *SC657 Backlight Driver Software User's Guide* and *SemPulse Interface Specification* document and to the associated software drivers available for this device (contact your sales office for more details).

Shutdown Mode

The device is disabled when the SPIF pin is held low for the shutdown time specified in the electrical characteristics section. All registers are reset to default condition at shutdown.

Sleep Mode

When all LEDs are disabled, sleep mode is activated. This is a reduced current mode that helps minimize overall current consumption by disabling the clock and the charge pump while continuing to monitor the serial interface for commands. An additional current savings can be obtained by putting the serial interface in standby mode (see SemPulse Interface, Standby Mode).

Protection Features

The SC657 provides several protection features to safeguard the device from catastrophic failures. These features include:

- Output Open Circuit Protection
- Over-Temperature Protection
- Charge Pump Output Current Limit
- LED Float Detection

Output Open Circuit Protection

Over-Voltage Protection (OVP) at the OUT pin prevents the charge pump from producing an excessively high output voltage. In the event of an open circuit between the OUT pin and all current sinks (no loads connected), the charge pump runs in open loop and the voltage rises up to the

Applications Information (continued)

OVP limit. OVP operation is hysteretic, meaning the charge pump will momentarily turn off until V_{OUT} is sufficiently reduced. The maximum OVP threshold is 6.0V, allowing the use of a ceramic output capacitor rated at 6.3V.

Over-Temperature Protection

The Over-Temperature (OT) protection circuit prevents the device from overheating and experiencing a catastrophic failure. When the junction temperature exceeds 160°C, the device goes into thermal shutdown with all outputs disabled until the junction temperature is reduced. All register information is retained during thermal shutdown. Hysteresis of 20°C is provided to ensure that the device cools sufficiently before re-enabling.

Charge Pump Output Current Limit

The device limits the charge pump current at the OUT pin. If the OUT pin is shorted to ground, or V_{OUT} is lower than 2.5V, the typical output current limit is 60mA. The output current is limited to 300mA when over loaded resistively with V_{OUT} greater than 2.5V.

LED Float Detection

Float detect is a fault detection feature of the LED backlight outputs. If an output is programmed to be enabled and an open circuit fault occurs at any backlight output, that output will be disabled to prevent a sustained output OVP condition from occurring due to the resulting open loop. Float detect ensures device protection but does not ensure optimum performance. Unused LED outputs must be disabled to prevent an open circuit fault from occurring.

Thermal Management

Although the SC657 can provide up to 125mA output current, the maximum thermal temperature and the thermal resistance (θ_{JA}) of the package and layout may limit the output current. Thermal resistance can be lowered by following the recommended layout guidelines in PCB Layout Considerations, as illustrated in Figure 2.

PCB Layout Considerations

Following fundamental layout rules is critical for achieving the performance specified in the Electrical Characteristics table. The following guidelines are recommended when developing a PCB layout:

- Place all capacitors (C1, C2, CIN, and COUT) as close to the device as possible.
- All charge pump current passes through the IN/OUT and the bucket capacitor connection pins. Ensure that all connections to these pins make the of wide traces so that the resistive drop on each connection is minimized.
- Make all ground connections to a solid ground plane as shown in the example layout .

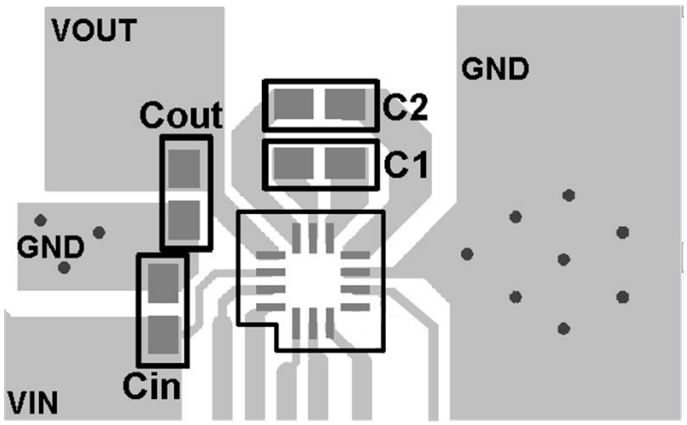


Figure 2 — Suggested Layout

SemPulse™ Interface

Introduction

SemPulse is a write-only single wire interface. It provides the capability to access up to 32 registers that control device functionality. Two sets of pulse trains are transmitted via the SPIF pin. The first pulse set is used to set the desired address. After the bus is held high for the address hold period, the next pulse set is used to write the data value. After the data pulses are transmitted, the bus is held high again for the data hold period to signify the data write is complete. At this point the device latches the data into the address that was selected by the first set of pulses. See the SemPulse Timing Diagrams for descriptions of all timing parameters.

Chip Enable/Disable

The device is enabled when the SemPulse interface pin (SPIF) is pulled high for greater than t_{SU}. If the SPIF pin is pulled low again for more than t_{SD}, the device will be disabled.

Address Writes

The first set of pulses can range between 0 and 31 (or 1 to 32 rising edges) to set the desired address. After the pulses are transmitted, the SPIF pin must be held high for t_{HOLDA} to signal to the slave device that the address write is finished. If the pulse count is between 0 and 31 and the line is held high for t_{HOLDA}, the address is latched as the destination for the next data write. If the SPIF pin is not held high for t_{HOLDA}, the slave device will continue to count pulses. Note that if t_{HOLDA} exceeds its maximum specification, the bus will reset. This means that the communication is ignored and the bus resumes monitoring the pin, expecting the next pulse set to be an address. If the total exceeds 31 pulses, SPIF must be held high until the bus reset time t_{BR} is exceeded before commencing communication.

Data Writes

After the bus has been held high for the minimum address hold period, the next set of pulses are used to write the data value. The total number of pulses can range from 0 to 63 (or 1 to 64 rising edges) since there are a total of 6 register bits per register. Just like with the address write, the data write is only accepted if the bus is held high for t_{HOLDD} when the pulse train is completed. If the proper hold time is not received, the interface will keep counting pulses until the hold time is detected. If the total exceeds 63 pulses, the write will be ignored and the bus will reset after the next valid hold time is detected. After the bus has been held high for t_{HOLDD}, the bus will expect the next pulse set to be an address write. Note that this is the same effect as the bus reset that occurs when t_{HOLDA} exceeds its maximum specification. For this reason, there is no maximum limit on t_{HOLDD} — the bus simply waits for the next valid address to be transmitted.

Multiple Writes

It is important to note that this single-wire interface requires the address to be paired with its corresponding data. If it is desired to write multiple times to the same address, the address must always be re-transmitted prior to the corresponding data. If it is only transmitted one time and followed by multiple data transmissions, every other block of data will be treated like a new address. The result will be invalid data writes to incorrect addresses. Note that multiple writes only need to be separated by the minimum t_{HOLDD} for the slave to interpret them correctly. As long as t_{HOLDA} between the address pulse set and the data pulse set is less than its maximum specification but greater than its minimum, multiple pairs of address and data pulse counts can be made with no detrimental effects.

Standby Mode

Once data transfer is completed, the SPIF line must be returned to the high state for at least 10ms to return to the standby mode. In this mode, the SPIF line remains idle while monitoring for the next command. This mode allows the device to minimize current consumption between commands. Once the device has returned to standby mode, the bus is automatically reset to expect the address pulses as the next data block. This safeguard is intended to reset the bus to a known state (waiting for the beginning of a write sequence) if the delay exceeds the reset threshold.

SemPulse™ Interface (continued)

SemPulse Timing Diagrams

The SemPulse single wire interface is used to enable or disable the device and configure all registers (see Figure 3). The timing parameters refer to the digital I/O electrical specifications.

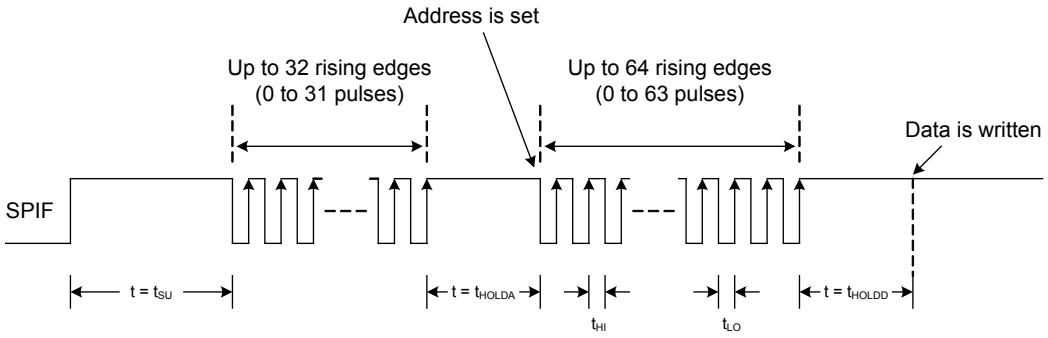


Figure 3 — Uniform Timing Diagram for SemPulse Communication

Timing Example 1

In this example (see Figure 4), the slave chip receives two sets of pulses to set the address and data, and the pulses experience interrupts that cause the pulse width to be nonuniform. Note that as long as the maximum high and low times are satisfied and the hold times are within specification, the data transfer is completed regardless of the number of interrupts that delay the transmission.

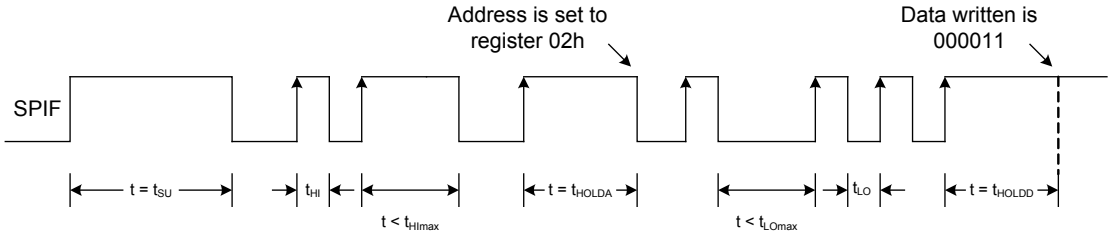


Figure 4 — SemPulse Data Write with Non-Uniform Pulse Widths

Timing Example 2

In this example (see Figure 5), the slave chip receives two sets of pulses to set the address and data, but an interrupt occurs during a pulse that causes it to exceed the minimum address hold time. The write is meant to be the value 03h in register 05h, but instead it is interpreted as the value 02h written to register 02h. The extended pulse that is delayed by the interrupt triggers a false address detection, causing the next pulse set to be interpreted as the data set. To avoid any problems with timing, make sure that all pulse widths comply with their timing requirements as outlined in this datasheet.

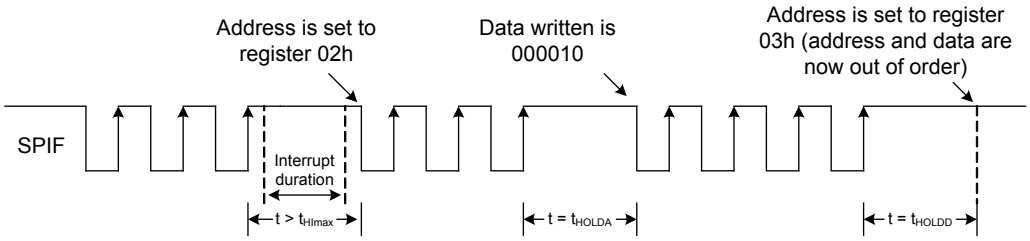


Figure 5 — Faulty SemPulse Data Write Due to Extended Interrupt Duration

Register Map(1)

Address	D5	D4	D3	D2	D1	D0	Reset Value	Description
00h	0(2)	BLEN5	BLEN4	BLEN3	BLEN2	BLEN1	00h	Backlight Enable
01h	0(2)	MBL4	MBL3	MBL2	MBL1	MBL0	00h	Main Backlight Current
02h	0(2)	SBL4	SBL3	SBL2	SBL1	SBL0	00h	Sub Backlight Current
03h	0(2)	TBL4	TBL3	TBL2	TBL1	TBL0	00h	Third Backlight Current
04h	0(2)	0(2)	0(2)	0(2)	MFADE1	MFADE0	00h	Main Fade
05h	0(2)	0(2)	0(2)	MB2	MB1	MB0	00h	Backlight Grouping Configuration

Notes:
(1) all registers are write-only.
(2) 0 = always write a 0 to these bits

Definition of Registers and Bits

BL Enable Control Register (00h)

This register enables each individual LED.

Bit D5

This bit is unused and is always a zero, so the maximum pulse count for this register is 31.

BLEN5 — BLEN1 [D4:D0]

These active high bits enable the five backlight drivers. Each LED can be controlled independently.

Register and Bit Definitions (continued)

Main Backlight Current Control Register (01h)

This register is used to set the currents for the backlight current sinks assigned to the Main Backlight Group. This group can also be used to control red LEDs for limited RGB control. These current sinks need to be enabled in the Backlight Enable Control register to be active.

Bit D5

This bit is unused and is always a zero, so the maximum pulse count for this register is 31.

MBL4 — MBL0 [D4:D0]

These bits are used to set the current for the main backlight current sinks. All enabled main backlight current sinks will sink the same current, as shown in Table 4.

Table 4 — Main Backlight Current Settings

MBL4	MBL3	MBL2	MBL1	MBL0	Backlight Current (mA)
0	0	0	0	0	0
0	0	0	0	1	See note 1
0	0	0	1	0	See note 1
0	0	0	1	1	See note 1
0	0	1	0	0	0.5
0	0	1	0	1	1.0
0	0	1	1	0	1.5
0	0	1	1	1	2.0
0	1	0	0	0	2.5
0	1	0	0	1	3.0
0	1	0	1	0	3.5
0	1	0	1	1	4.0
0	1	1	0	0	4.5
0	1	1	0	1	5.0
0	1	1	1	0	6.0
0	1	1	1	1	7.0
1	0	0	0	0	8.0
1	0	0	0	1	9.0
1	0	0	1	0	10
1	0	0	1	1	11
1	0	1	0	0	12
1	0	1	0	1	13
1	0	1	1	0	14
1	0	1	1	1	15
1	1	0	0	0	16
1	1	0	0	1	17
1	1	0	1	0	18
1	1	0	1	1	19
1	1	1	0	0	20
1	1	1	0	1	21
1	1	1	1	0	23
1	1	1	1	1	25

(1) Reserved for future use

Register and Bit Definitions (continued)

Sub Backlight Current Control Register (02h)

This register is used to set the currents for the backlight current sinks assigned to the Sub Backlight Group. This group can also be used to control green LEDs for limited RGB control. These current sinks need to be enabled in the Backlight Enable Control register to be active.

Bit D5

This bit is unused and is always a zero, so the maximum pulse count for this register is 31.

SBL4 — SBL0 [D4:D0]

These bits are used to set the current for the sub backlight current sinks. All enabled sub backlight current sinks will sink the same current, as shown in Table 5.

Table 5 — Sub Backlight Current Settings

SBL4	SBL3	SBL2	SBL1	SBL0	Backlight Current (mA)
0	0	0	0	0	0
0	0	0	0	1	See note 1
0	0	0	1	0	See note 1
0	0	0	1	1	See note 1
0	0	1	0	0	0.5
0	0	1	0	1	1.0
0	0	1	1	0	1.5
0	0	1	1	1	2.0
0	1	0	0	0	2.5
0	1	0	0	1	3.0
0	1	0	1	0	3.5
0	1	0	1	1	4.0
0	1	1	0	0	4.5
0	1	1	0	1	5.0
0	1	1	1	0	6.0
0	1	1	1	1	7.0
1	0	0	0	0	8.0
1	0	0	0	1	9.0
1	0	0	1	0	10
1	0	0	1	1	11
1	0	1	0	0	12
1	0	1	0	1	13
1	0	1	1	0	14
1	0	1	1	1	15
1	1	0	0	0	16
1	1	0	0	1	17
1	1	0	1	0	18
1	1	0	1	1	19
1	1	1	0	0	20
1	1	1	0	1	21
1	1	1	1	0	23
1	1	1	1	1	25

(1) Reserved for future use

Register and Bit Definitions (continued)

Third Backlight Current Control Register (03h)

This register is used to set the currents for the backlight current sinks assigned to the Third Backlight Group. This group can also be used to control blue LEDs for limited RGB control. These current sinks need to be enabled in the Backlight Enable Control register to be active.

Bit D5

This bit is unused and is always a zero, so the maximum pulse count for this register is 31.

TBL4 — TBL0 [D4:D0]

These bits are used to set the current for the third backlight current sinks. All enabled third backlight current sinks will sink the same current, as shown in Table 6.

Table 6 — Third Backlight Current Control Bits

TBL4	TBL3	TBL2	TBL1	TBL0	Backlight Current (mA)
0	0	0	0	0	0
0	0	0	0	1	See note 1
0	0	0	1	0	See note 1
0	0	0	1	1	See note 1
0	0	1	0	0	0.5
0	0	1	0	1	1.0
0	0	1	1	0	1.5
0	0	1	1	1	2.0
0	1	0	0	0	2.5
0	1	0	0	1	3.0
0	1	0	1	0	3.5
0	1	0	1	1	4.0
0	1	1	0	0	4.5
0	1	1	0	1	5.0
0	1	1	1	0	6.0
0	1	1	1	1	7.0
1	0	0	0	0	8.0
1	0	0	0	1	9.0
1	0	0	1	0	10
1	0	0	1	1	11
1	0	1	0	0	12
1	0	1	0	1	13
1	0	1	1	0	14
1	0	1	1	1	15
1	1	0	0	0	16
1	1	0	0	1	17
1	1	0	1	0	18
1	1	0	1	1	19
1	1	1	0	0	20
1	1	1	0	1	21
1	1	1	1	0	23
1	1	1	1	1	25

(1) Reserved for future use

Register and Bit Definitions (continued)

Main Fade Control (04h)

This register sets the fade status and rate for the main backlight group.

Bits [D5:D2]

These bits are unused and are always zeros, so the maximum pulse count for this register is 3.

MFADE1, MFADE0[D1:D0]

These bits are used to enable and set the rise/fall rate between two backlight currents as follows in Table 7.

Table 7 — Main Display Fade Control Bits

MFADE1	MFADE0	Fade Feature Rise/Fall Rate (ms/step)
0	0	OFF
0	1	8
1	0	16
1	1	32

The number of steps used to change the backlight current will be equal to the change in binary count of bits MBL[4:0].

When a new backlight current is set, the backlight current will change from its current value to a new value set by bits MBL[4:0] at the rate determined by MFADE1 and MFADE0 bits. The total fade time is determined by the number of steps between old and new backlight values, in Table 4, multiplied by the rate of fade in ms/step.

Backlight Grouping Configuration (05h)

This register assigns the LEDs to the back light bank configurations.

Bits [D5:D3]

These bits are unused and are always zeros, so the maximum pulse count for this register is 7.

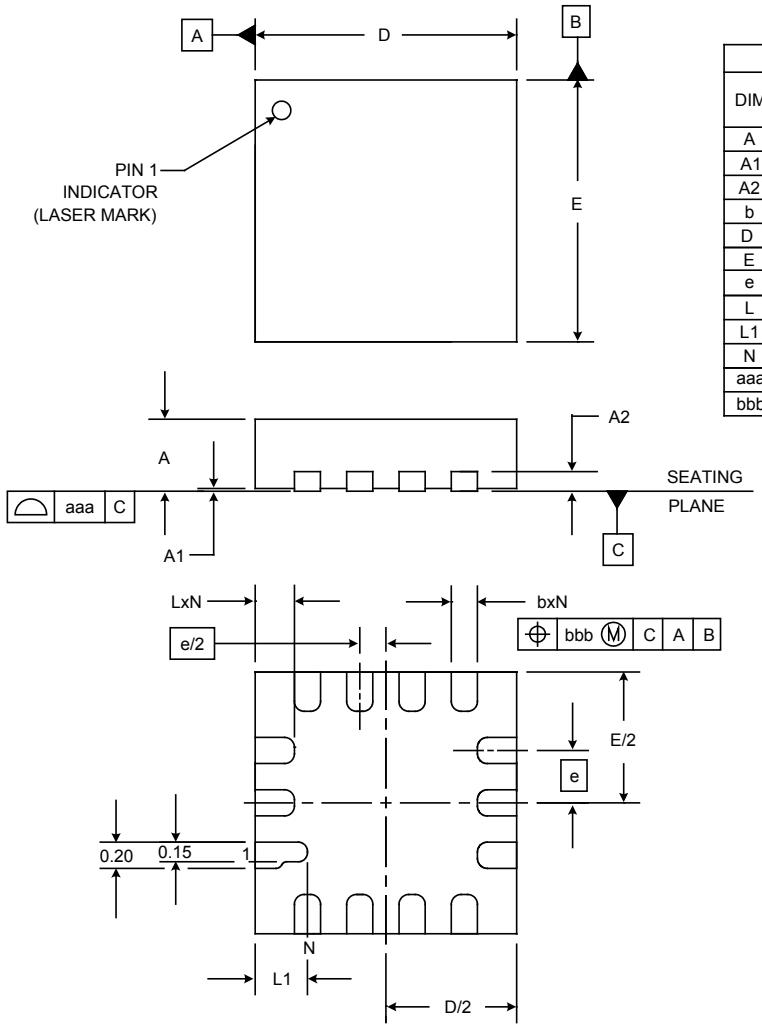
MB2, MB1 and MB0 [D2:D0]

These bits are used to set the number of LED drivers dedicated to each backlight group. This allows the device to drive up to three different sets of LEDs with different current settings. Note that any driver assigned to any LED group can still be disabled independently if not needed. The code set by these bits determines how the LED drivers are assigned among the three LED groups according to the assignments listed in Table 8. Default state for each of these three bits is "0" (all LEDs assigned to main display).

Table 8 — Backlight Grouping Configuration

MB2	MB1	MB0	Main Display LED Drivers	Sub Display LED Drivers	Third Display LED Drivers
0	0	0	BL1-BL5		
0	0	1	BL1-BL3	BL4-BL5	
0	1	0	BL1-BL2	BL3-BL4	BL5
0	1	1	BL1-BL2, BL5	BL3	BL4
1	0	0	BL1-BL3	BL4-BL5	
1	0	1	BL1-BL4	BL5	
1	1	X	BL1-BL5		

Outline Drawing — MLPQ-UT-14 2x2

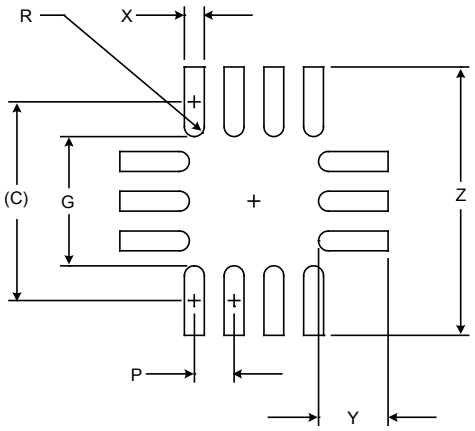


DIM	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.020	-	.024	0.50	-	0.60
A1	.000	-	.002	0.00	-	0.05
A2		(.006)			(0.152)	
b	.006	.008	.010	0.15	0.20	0.25
D	.077	.079	.081	1.95	2.00	2.05
E	.077	.079	.081	1.95	2.00	2.05
e		.016 BSC			0.40 BSC	
L	.010	.012	.014	0.25	0.30	0.35
L1	.014	.016	.018	0.35	0.40	0.45
N		14			14	
aaa		.003			0.08	
bbb		.004			0.10	

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

Land Pattern — MLPQ-UT-14 2x2



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.079)	(2.00)
G	.055	1.40
P	.016	0.40
R	.004	0.10
X	.008	0.20
Y	.024	0.60
Z	.102	2.60

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
   CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR
   COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. SQUARE PACKAGE - DIMENSIONS APPLY IN BOTH " X " AND " Y " DIRECTIONS.
4. PIN 1 PAD CAN BE SHORTER THAN THE ACTUAL PACKAGE LEAD TO AVOID
   SOLDER BRIDGING BETWEEN PINS 1 & 14.

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