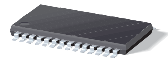


DUAL INPUT BUS 9-A OUTPUT SYNCHRONOUS BUCK PWM SWITCHER WITH INTEGRATED FETs (SWIFT™)

FEATURES

- **Low Voltage Separate Power Bus**
- **15-mΩ MOSFET Switches for High Efficiency at 9-A Continuous Output**
- **Adjustable Output Voltage**
- **Externally Compensated With 1% Internal Reference Accuracy**
- **Fast Transient Response**
- **Wide PWM Frequency: Adjustable 280 kHz to 700 kHz**
- **Load Protected at Thermal Shutdown**
- **Integrated Solution Reduces Board Area and Total Cost**

APPLICATIONS

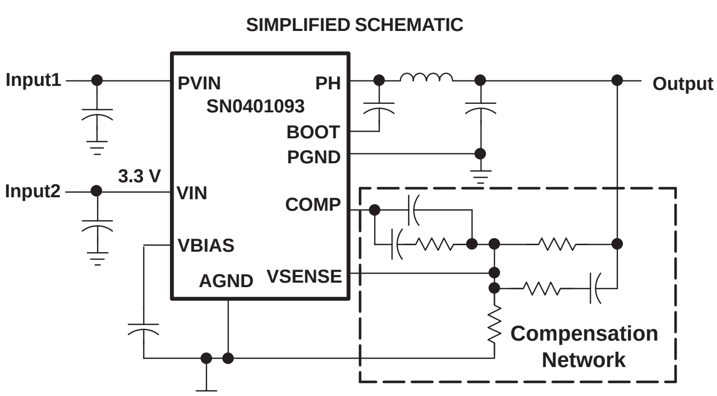
- **Low-Voltage, High-Density Systems With Power Distribution at 1.0 V**
- **Point of Load Regulation for High Performance DSPs, FPGAs, ASICs and Microprocessors**
- **Broadband, Networking and Optical Communications Infrastructure**

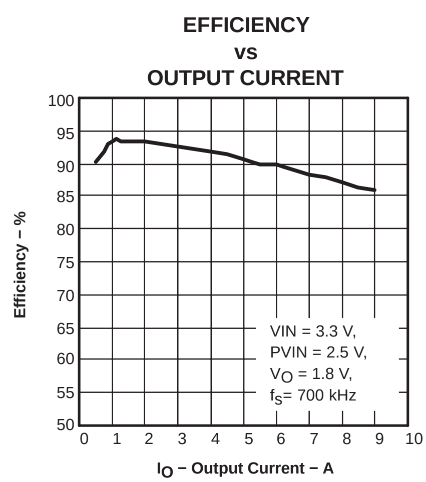
DESCRIPTION

As a member of the SWIFT™ family of dc/dc regulators, the SN0401093 low-input voltage high-output current synchronous buck PWM converter integrates all required active components. Included on the substrate with the listed features are a true, high performance, voltage error amplifier that enables maximum performance under transient conditions and flexibility in choosing the output filter L and C components; an under-voltage-lockout circuit to prevent start-up until the VIN input voltage reaches 3 V; an internally and externally set slow-start circuit to limit in-rush currents; and a power good output useful for processor/logic reset, fault signaling, and supply sequencing.

The SN0401093 is available in a thermally enhanced 28-pin TSSOP (PWP) PowerPAD™ package, which eliminates bulky heatsinks.

SIMPLIFIED SCHEMATIC





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	OUTPUT VOLTAGE	PACKAGE	PART NUMBER
−40°C to 85°C	Adjustable down to 0.9 V	Plastic HTSSOP (PWP)[1]	SN0401093PWP

(1) The PWP package is also available taped and reeled. Add an R suffix to the device type (i.e., SN0401093PWPR). See the application section of the data sheet for PowerPAD drawing and layout information.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted[1]

		SN0401093	UNIT
Input voltage range, V_I	SS/ENA	−0.3 to 7	V
	RT	−0.3 to 6	
	VSENSE	−0.3 to 4	
	PVIN, VIN	−0.3 to 4.5	
	BOOT	−0.3 to 10	
Output voltage range, V_O	VBIAS, COMP, PWRGD	−0.3 to 7	V
	PH	−0.6 to 6	
Source current, I_O	PH	Internally limited	
	COMP, VBIAS	6	mA
Sink current, I_S	PH	16	A
	COMP	6	mA
	SS/ENA, PWRGD	10	
Voltage differential	AGND to PGND	±0.3	V
Operating virtual junction temperature range, T_J		−40 to 125	°C
Storage temperature, T_{stg}		−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Input voltage, VIN, V_I	3		4	V
Power input voltage, PVIN	1.6		4.0	V
Operating junction temperature, T_J	−40		125	°C

DISSIPATION RATINGS[1][2]

PACKAGE	THERMAL IMPEDANCE JUNCTION-TO-AMBIENT	T_A = 25°C POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
28 Pin PWP with solder	18.8°C/W	5.32 W	2.93 W	2.13 W

(1) For more information on the PWP package, refer to TI technical brief, literature number SLMA002.
(2) Test board conditions:

1. 3” x 3”, 4 layers, thickness: 0.062”
2. 2.0 oz. copper traces and ground area located on the top of the PCB
3. 2.0 oz. copper ground area with V_{OUT} fill area and two signal traces on the bottom layer of the PCB
4. 2.0 oz. copper ground planes on the 2 internal layers
5. 12 thermal vias (see “Recommended Land Pattern” in applications section of this data sheet)

ELECTRICAL CHARACTERISTICS

T_J = –40°C to 125°C, VIN = 3 V to 4 V, PVIN = 1.6 V to 4.0 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE, VIN							
	Input voltage range, VIN			3.0		4.0	V
	Supply voltage range, PVIN		Output = 1.2 V	1.6		4.0	V
$I_{(Q)}$	Quiescent current	VIN	f_S = 350 kHz, RT open, PH pin open, PVIN = 1.8 V		6.3	10.0	mA
			SHUTDOWN, SS/ENA = 0 V, PVIN = 1.8 V		1	1.4	
		PVIN	f_S = 350 kHz, RT open, PH pin open, VIN = 3.3 V		4.0	7.0	mA
			SHUTDOWN, SS/ENA = 0 V, VIN = 3.3 V		< 100		µA
UNDER VOLTAGE LOCK OUT (VIN)							
	Start threshold voltage, UVLO				2.95	3.0	V
	Stop threshold voltage, UVLO			2.70	2.80		V
	Hysteresis voltage, UVLO				0.12		V
	Rising and falling edge deglitch, UVLO(1)				2.5		µs
BIAS VOLTAGE							
	Output voltage, VBIAS		$I_{(VBIAS)}$ = 0	2.70	2.80	2.90	V
	Output current, VBIAS (2)					100	µA
CUMULATIVE REFERENCE							
V_{ref}	Accuracy			0.882	0.891	0.900	V
REGULATION							
	Line regulation(1)		I_L = 4.5 A, f_S = 350 kHz, T_J = 85°C			0.07	%/V
	Load regulation(1)		I_L = 0 A to 9 A, f_S = 350 kHz, T_J = 85°C			0.03	%/A
OSCILLATOR							
	Internally set—free running frequency		RT open(1)	280	350	420	kHz
	Externally set—free running frequency range		RT = 180 kΩ (1% resistor to AGND)(1)	252	280	308	kHz
			RT = 100 kΩ (1% resistor to AGND)	460	500	540	
			RT = 68 kΩ (1% resistor to AGND)(1)	663	700	762	
	Ramp valley(1)				0.75		V
	Ramp amplitude (peak-to-peak)(1)				1		V
	Minimum controllable on time(1)					200	ns
	Maximum duty cycle(1)			90%			

(1) Specified by design
(2) Static resistive loads only

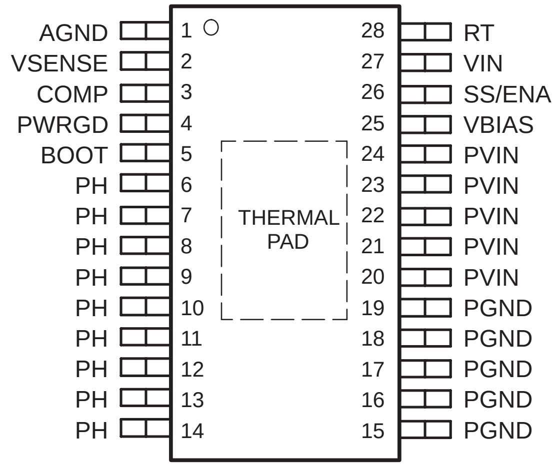
ELECTRICAL CHARACTERISTICS (continued)

T_J = –40°C to 125°C, VIN = 3 V to 4 V, PVIN = 1.6 V to 4.0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ERROR AMPLIFIER						
	Error amplifier open loop voltage gain	1 kΩ COMP to AGND(1)	90	110		dB
	Error amplifier unity gain bandwidth	Parallel 10 kΩ, 160 pF COMP to AGND(1)	3	5		MHz
	Error amplifier common mode input voltage range	Powered by internal LDO(1)	0		VBIAS	V
	Input bias current, VSENSE	VSENSE = V_{ref}		60	250	nA
	Output voltage slew rate (symmetric), COMP		1.0	1.4		V/µs
PWM COMPARATOR						
	PWM comparator propagation delay time, PWM comparator input to PH pin (excluding deadtime)	10-mV overdrive(1)		70	85	ns
SLOW-START/ENABLE						
	Enable threshold voltage, SS/ENA		0.82	1.2	1.4	V
	Enable hysteresis voltage, SS/ENA(1)			0.03		V
	Falling edge deglitch, SS/ENA(1)			2.5		µs
	Internal slow-start time		2.6	3.35	4.1	ms
	Charge current, SS/ENA	SS/ENA = 0 V	2	5	8	µA
	Discharge current, SS/ENA	SS/ENA = 0.2 V, VIN = 2.7 V	1	2	4	mA
POWER GOOD						
	Power good threshold voltage	VSENSE falling		90		$\%V_{ref}$
	Power good hysteresis voltage(1)			3		$\%V_{ref}$
	Power good falling edge deglitch(1)			35		µs
	Output saturation voltage, PWRGD	$I_{(sink)}$ = 2.5 mA		0.18	0.3	V
	Leakage current, PWRGD	VIN = 3.3 V			1	µA
THERMAL SHUTDOWN						
	Thermal shutdown trip point(1)		135	165		°C
	Thermal shutdown hysteresis(1)			10		°C
OUTPUT POWER MOSFETS						
$r_{DS(on)}$	Power MOSFET switches	VIN = 3 V		15	30	mΩ
		VIN = 3.6 V		14	28	

(1) Specified by design
(2) Static resistive loads only

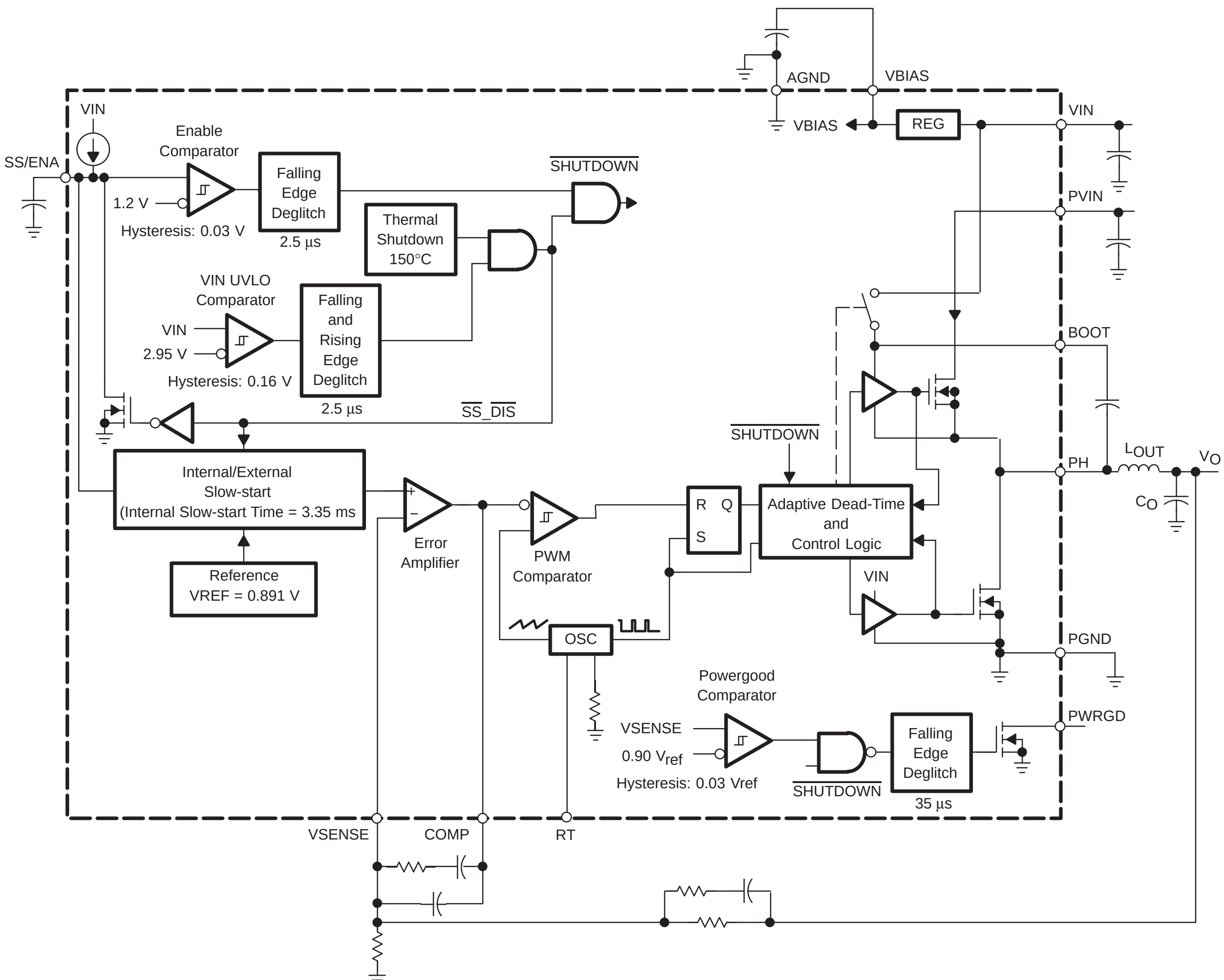
PWP PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
AGND	1	Analog ground. Return for compensation network/output divider, slow-start capacitor, VBIAS capacitor, and RT resistor. Connect PowerPAD to AGND.
BOOT	5	Bootstrap output. 0.022-µF to 0.1-µF low-ESR capacitor connected from BOOT to PH generates floating drive for the high-side FET driver.
COMP	3	Error amplifier output. Connect frequency compensation network from COMP to VSENSE
PGND	15−19	Power ground. High current return for the low-side driver and power MOSFET. Connect PGND with large copper areas to the input and output supply returns, and negative terminals of the input and output capacitors. A single point connection to AGND is recommended.
PH	6−14	Phase output. Junction of the internal high-side and low-side power MOSFETs, and output inductor.
PVIN	20−24	Input supply for the power MOSFET switches. Bypass PVIN pins to PGND pins close to device package with a high-quality, low-ESR 10-µF ceramic capacitor.
PWRGD	4	Power good open drain output. High when VSENSE ≥ 90% V_{ref}, otherwise PWRGD is low. Note that output is low when SS/ENA is low or the internal shutdown signal is active.
RT	28	Frequency setting resistor input. Connect a resistor from RT to AGND to set the switching frequency, f_S.
SS/ENA	26	Slow-start/enable input/output. Dual function pin which provides logic input to enable/disable device operation and capacitor input to externally set the start-up time.
VBIAS	25	Internal bias regulator output. Supplies regulated voltage to internal circuitry. Bypass VBIAS pin to AGND pin with a high-quality, low-ESR 0.1-µF to 1.0-µF ceramic capacitor.
VIN	27	Input supply for the internal bias regulator. An external capacitor of 1 µF to be connected to the VIN pin.
VSENSE	2	Error amplifier inverting input. Connect to output voltage compensation network/output divider.

INTERNAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

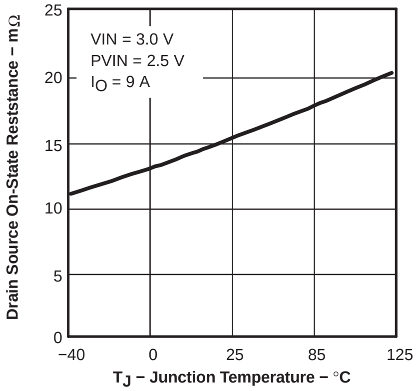


Figure 1

DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

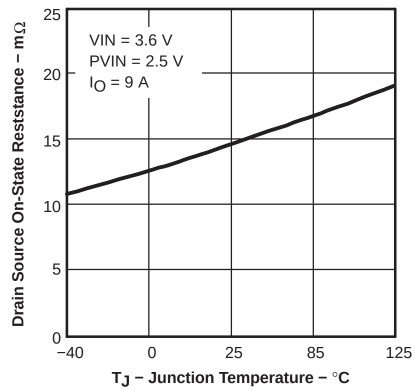


Figure 2

INTERNALLY SET OSCILLATOR FREQUENCY vs JUNCTION TEMPERATURE

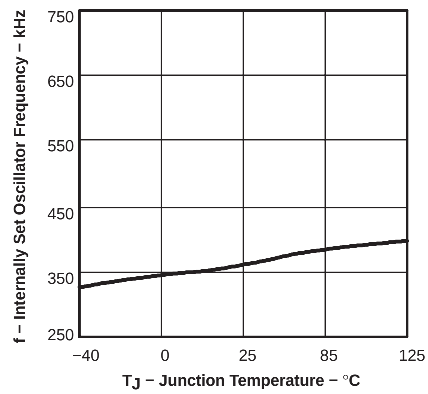


Figure 3

EXTERNALLY SET OSCILLATOR FREQUENCY vs JUNCTION TEMPERATURE

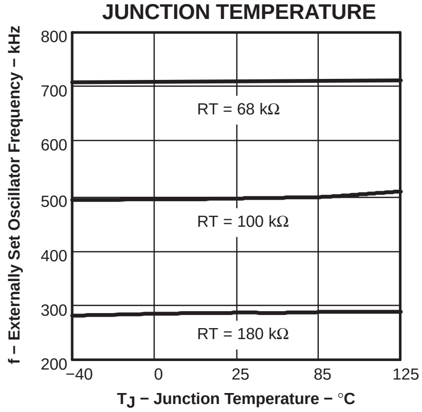


Figure 4

VOLTAGE REFERENCE vs JUNCTION TEMPERATURE

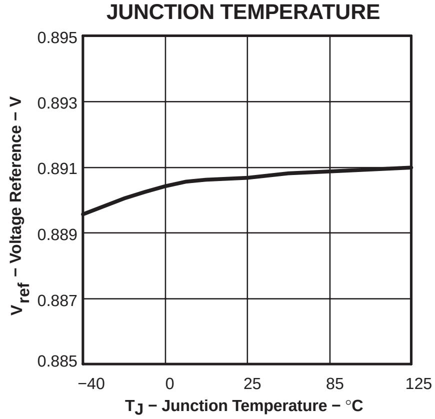


Figure 5

DEVICE POWER LOSSES vs LOAD CURRENT

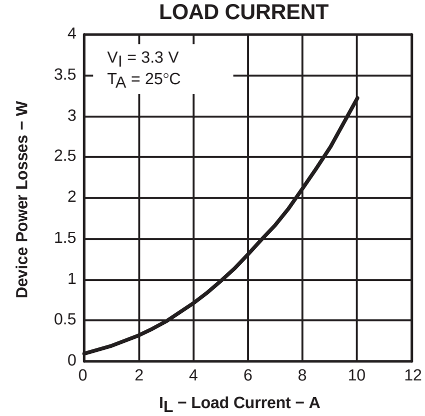


Figure 6

REFERENCE VOLTAGE vs INPUT VOLTAGE

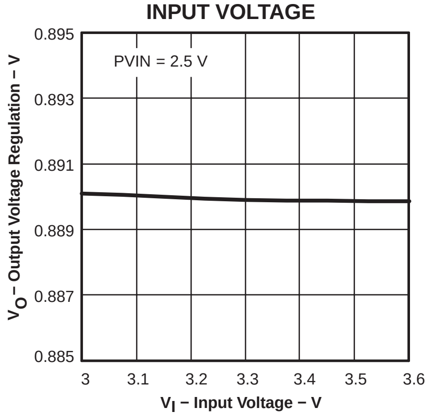


Figure 7

ERROR AMPLIFIER OPEN LOOP RESPONSE

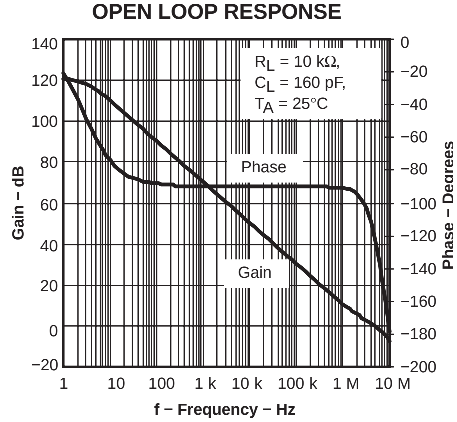


Figure 8

INTERNAL SLOW-START TIME vs JUNCTION TEMPERATURE

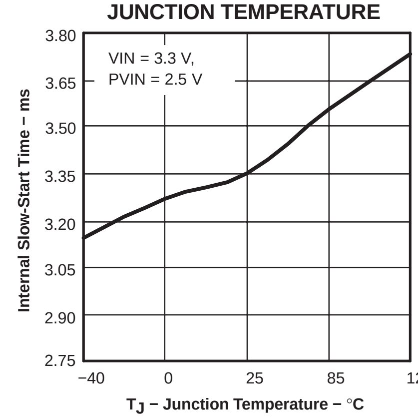


Figure 9

DETAILED DESCRIPTION

UNDERVOLTAGE LOCK OUT (UVLO)

The SN0401093 incorporates an under voltage lockout circuit to keep the device disabled when the input voltage (VIN) is insufficient. During power up, internal circuits are held inactive until VIN exceeds the nominal UVLO threshold voltage of 2.95 V. Once the UVLO start threshold is reached, device start-up begins. The device operates until VIN falls below the nominal UVLO stop threshold of 2.8 V. Hysteresis in the UVLO comparator, and a 2.5-µs rising and falling edge deglitch circuit reduce the likelihood of shutting the device down due to noise on VIN. UVLO with respect to VIN and not PVIN, see application note.

SLOW-START/ENABLE (SS/ENA)

The slow-start/enable pin provides two functions. First, the pin acts as an enable (shutdown) control by keeping the device turned off until the voltage exceeds the start threshold voltage of approximately 1.2 V. When SS/ENA exceeds the enable threshold, device start-up begins. The reference voltage fed to the error amplifier is linearly ramped up from 0 V to 0.891 V in 3.35 ms. Similarly, the converter output voltage reaches regulation in approximately 3.35 ms. Voltage hysteresis and a 2.5-µs falling edge deglitch circuit reduce the likelihood of triggering the enable due to noise.

The second function of the SS/ENA pin provides an external means of extending the slow-start time with a low-value capacitor connected between SS/ENA and AGND.

Adding a capacitor to the SS/ENA pin has two effects on start-up. First, a delay occurs between release of the SS/ENA pin and start-up of the output. The delay is proportional to the slow-start capacitor value and lasts until the SS/ENA pin reaches the enable threshold. The start-up delay is approximately:

$$t_d = C_{(SS)} \times \frac{1.2\ \text{V}}{5\ \mu\text{A}} \qquad (1)$$

Second, as the output becomes active, a brief ramp-up at the internal slow-start rate may be observed before the externally set slow-start rate takes control and the output rises at a rate proportional to the slow-start capacitor. The slow-start time set by the capacitor is approximately:

$$t_{(SS)} = C_{(SS)} \times \frac{0.7\ \text{V}}{5\ \mu\text{A}} \qquad (2)$$

The actual slow-start time is likely to be less than the above approximation due to the brief ramp-up at the internal rate.

VBIAS REGULATOR (VBIAS)

The VBIAS regulator provides internal analog and digital blocks with a stable supply voltage over variations in junction temperature and input voltage. A high quality, low-ESR, ceramic bypass capacitor is required on the VBIAS pin. X7R or X5R grade dielectrics are recommended because their values are more stable over temperature. The bypass capacitor must be placed close to the VBIAS pin and returned to AGND.

External loading on VBIAS is allowed, with the caution that internal circuits require a minimum VBIAS of 2.70 V, and external loads on VBIAS with ac or digital switching noise may degrade performance. The VBIAS pin may be useful as a reference voltage for external circuits. VBIAS is derived from the VIN pin, see the internal block diagram on page 6.

VOLTAGE REFERENCE

The voltage reference system produces a precise V_{ref} signal by scaling the output of a temperature stable bandgap circuit. During manufacture, the bandgap and scaling circuits are trimmed to produce 0.891 V at the output of the error amplifier, with the amplifier connected as a voltage follower. The trim procedure adds to the high precision regulation of the SN0401093, since it cancels offset errors in the scale and error amplifier circuits.

OSCILLATOR AND PWM RAMP

The oscillator frequency is set to an internally fixed value of 350 kHz. The oscillator frequency can be externally adjusted from 280 to 700 kHz by connecting a resistor between the RT pin to ground. The switching frequency is approximated by the following equation, where R is the resistance from RT to AGND:

$$\text{Switching Frequency} = \frac{100\ \text{k}\Omega}{R} \times 500\ [\text{kHz}] \qquad (3)$$

ERROR AMPLIFIER

The high performance, wide bandwidth, voltage error amplifier sets the SN0401093 apart from most dc/dc converters. The user is given the flexibility to use a wide range of output L and C filter components to suit the particular application needs. Type-2 or Type-3 compensation can be employed using external compensation components.

PWM CONTROL

Signals from the error amplifier output, oscillator, and current limit circuit are processed by the PWM control logic. Referring to the internal block diagram, the control logic includes the PWM comparator, OR gate, PWM latch, and portions of the adaptive dead-time and control-logic block. During steady-state operation below the current limit threshold, the PWM comparator output and oscillator pulse train alternately reset and set the PWM latch. Once the PWM latch is set, the low-side FET remains on for a minimum duration set by the oscillator pulse width. During this period, the PWM ramp discharges rapidly to its valley voltage. When the ramp begins to charge back up, the low-side FET turns off and high-side FET turns on. As the PWM ramp voltage exceeds the error amplifier output voltage, the PWM comparator resets the latch, thus turning off the high-side FET and turning on the low-side FET. The low-side FET remains on until the next oscillator pulse discharges the PWM ramp.

During transient conditions, the error amplifier output could be below the PWM ramp valley voltage or above the PWM peak voltage. If the error amplifier is high, the PWM latch is never reset, and the high-side FET remains on until the oscillator pulse signals the control logic to turn the high-side FET off and the low-side FET on. The device operates at its maximum duty cycle until the output voltage rises to the regulation set-point, setting VSENSE to approximately the same voltage as VREF. If the error amplifier output is low, the PWM latch is continually reset and the high-side FET does not turn on. The low-side FET remains on until the VSENSE voltage decreases to a range that allows the PWM comparator to change states. The SN0401093 is capable of sinking current continuously until the output reaches the regulation set-point.

If the current limit comparator trips for longer than 100 ns, the PWM latch resets before the PWM ramp exceeds the error amplifier output. The high-side FET turns off and low-side FET turns on to decrease the energy in the output inductor and consequently the output current. This process is repeated each cycle in which the current limit comparator is tripped.

DEAD-TIME CONTROL AND MOSFET DRIVERS

Adaptive dead-time control prevents shoot-through current from flowing in both N-channel power MOSFETs

during the switching transitions by actively controlling the turnon times of the MOSFET drivers. The high-side driver does not turn on until the voltage at the gate of the low-side FET is below 2 V. While the low-side driver does not turn on until the voltage at the gate of the high-side MOSFET is below 2 V.

The high-side and low-side drivers are designed with 300-mA source and sink capability to quickly drive the power MOSFETs gates. The low-side driver is supplied from VIN, while the high-side drive is supplied from the BOOT pin. A bootstrap circuit uses an external BOOT capacitor and an internal 2.5-Ω bootstrap switch connected between the VIN and BOOT pins. The integrated bootstrap switch improves drive efficiency and reduces external component count.

THERMAL SHUTDOWN

The device uses the thermal shutdown to turn off the power MOSFETs and disable the controller if the junction temperature exceeds 150°C. The device is released from shutdown automatically when the junction temperature decreases to 10°C below the thermal shutdown trip point, and starts up under control of the slow-start circuit.

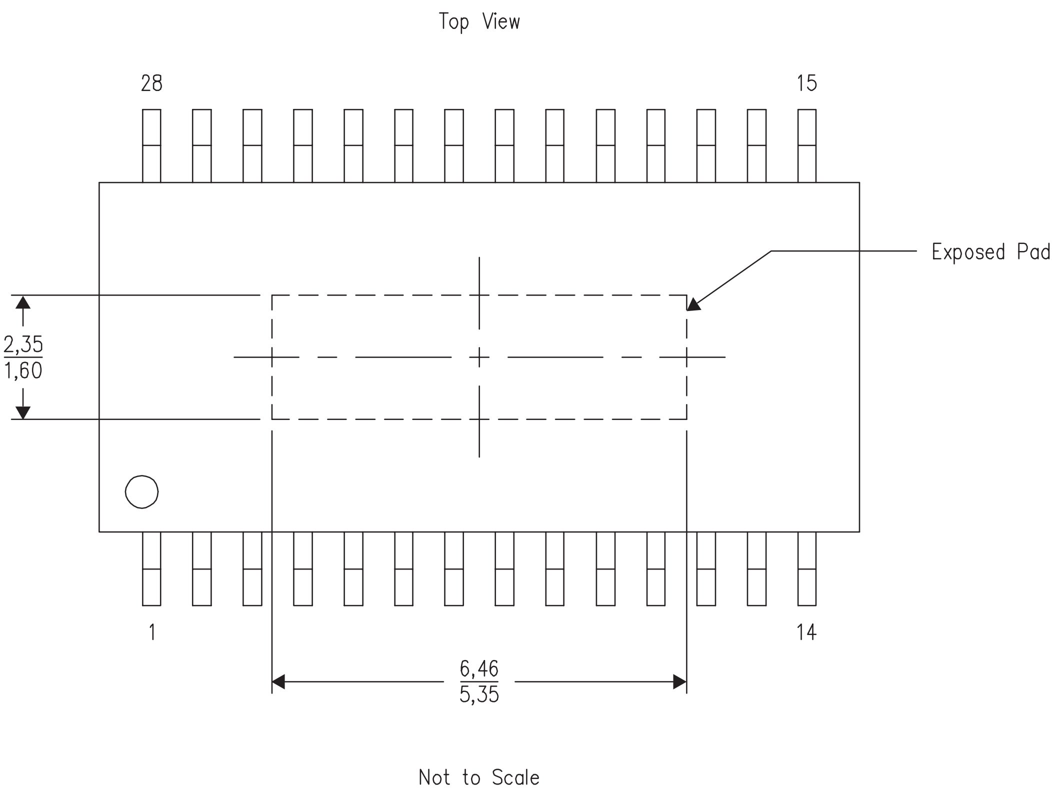
Thermal shutdown provides protection when an overload condition is sustained for several milliseconds. With a persistent fault condition, the device cycles continuously; starting up by control of the slow-start circuit, heating up due to the fault condition, and then shutting down upon reaching the thermal shutdown trip point. This sequence repeats until the fault condition is removed.

POWER-GOOD (PWRGD)

The power good circuit monitors for under voltage conditions on VSENSE. If the voltage on VSENSE is 10% below the reference voltage, the open-drain PWRGD output is pulled low. PWRGD is also pulled low if VIN is less than the UVLO threshold or SS/ENA is low. When VIN ≥ UVLO threshold, SS/ENA ≥ enable threshold, and VSENSE > 90% of V_{ref}, the open drain output of the PWRGD pin is high. A hysteresis voltage equal to 3% of V_{ref} and a 35 µs falling edge deglitch circuit prevent tripping of the power good comparator due to high frequency noise.

THERMAL PAD MECHANICAL DATA

PWP (R–PDSO–G28) **PowerPAD™ PLASTIC SMALL–OUTLINE**



PPTD032

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. For additional information on the PowerPAD™ package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, ***PowerPAD Thermally Enhanced Package***, Texas Instruments Literature No. SLMA002 and Application Brief, ***PowerPAD Made Easy***, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

PowerPAD is a trademark of Texas Instruments

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN0401093PWP	PREVIEW	HTSSOP	PWP	28		None	CU NIPDAU	Level-1-220C-UNLIM
SN0401093PWPR	PREVIEW	HTSSOP	PWP	28		None	CU NIPDAU	Level-1-220C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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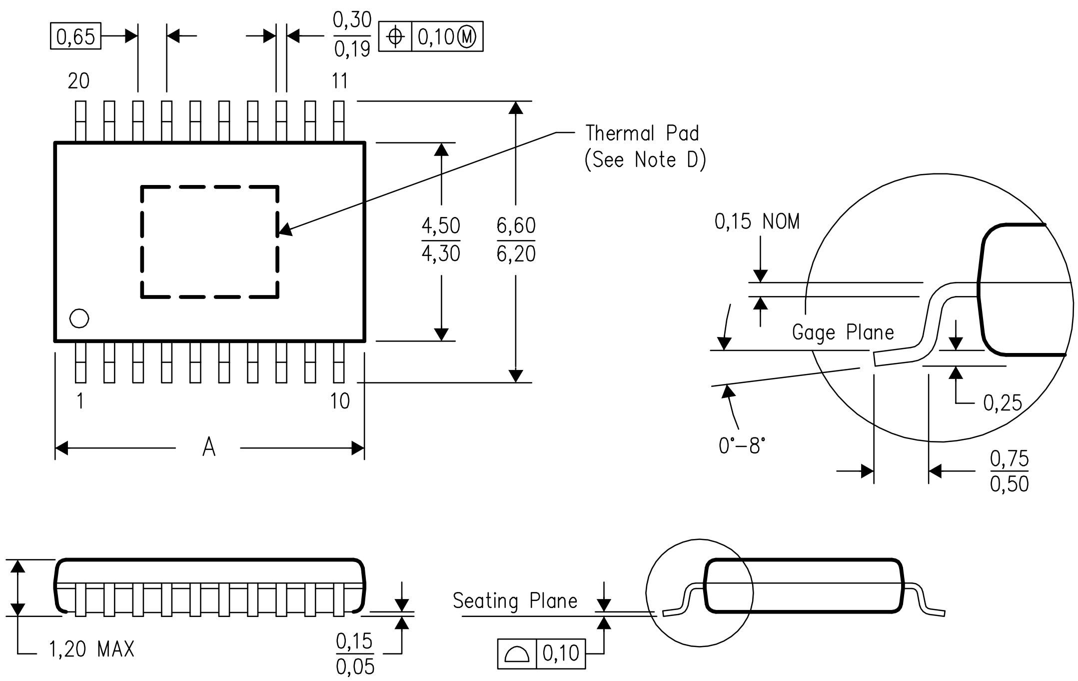
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PWP (R-PDSO-G**) PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE

20 PIN SHOWN



PINS ** / DIM	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/G 08/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
E. Falls within JEDEC MO-153

IMPORTANT NOTICE

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

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