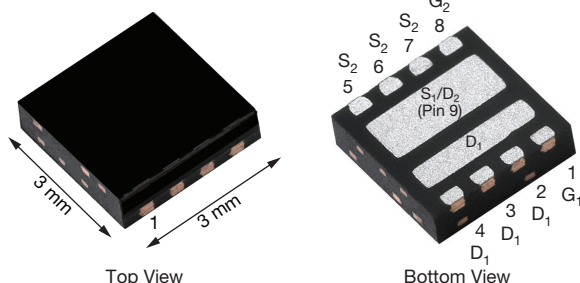


Dual N-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY

	V _{DS} (V)	R _{DS(on)} (Ω) MAX.	I _D (A)	Q _g (Typ.)
Channel-1 and Channel-2	30	0.0115 at V _{GS} = 10 V	30 ^a	4.5 nC
		0.0153 at V _{GS} = 4.5 V	27.5	

PowerPAIR® 3 x 3


Ordering Information:

SiZ342DT-T1-GE3 (lead (Pb)-free and halogen-free)

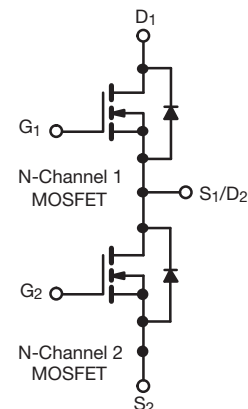
FEATURES

- PowerPAIR® optimizes high-side and low-side MOSFETs for synchronous buck converters
- TrenchFET® Gen IV power MOSFETs
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Synchronous buck
 - Battery charging
 - Computer system power
 - Graphic cards
- POL



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER	CHANNEL-1 AND CHANNEL-2		
	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	30	V
Gate-Source Voltage	V _{GS}	+20 / -16	
Continuous Drain Current (T _J = 150 °C)	I _D	30 ^a	A
		26.5	
		15.6 ^{b, c}	
		12.4 ^{b, c}	
Pulsed Drain Current (t = 100 μs)	I _{DM}	100	
Continuous Source Drain Diode Current	I _S	13.9	
		3.1 ^{b, c}	
Avalanche Current	I _{AS}	10	mJ
Single Pulse Avalanche Energy	E _{AS}	5	
Maximum Power Dissipation	P _D	16.7	W
		10.7	
		3.7 ^{b, c}	
		2.4 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

Notes

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- See solder profile (www.vishay.com/doc?73257). The PowerPAIR 3 x 3 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

**THERMAL RESISTANCE RATINGS**

PARAMETER		CHANNEL-1 AND CHANNEL-2			
		SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient ^{a, b}	$t \leq 10$ s	R_{thJA}	27	34	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	6	7.5	

Notes

- a. Surface mounted on 1" x 1" FR4 board.
b. Maximum under steady state conditions is 69 °C/W.

SPECIFICATIONS ($T_J = 25$ °C, unless otherwise noted)

PARAMETER	CHANNEL-1 AND CHANNEL-2					
	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0$ V, $I_D = 250$ μ A	30	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250$ μ A	-	20	-	mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250$ μ A	-	-5.6	-	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250$ μ A	1.2	-	2.4	V
Gate Source Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = +20$ V/ -16 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30$ V, $V_{GS} = 0$ V	-	-	1	μ A
		$V_{DS} = 30$ V, $V_{GS} = 0$ V, $T_J = 55$ °C	-	-	5	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \leq 5$ V, $V_{GS} = 10$ V	10	-	-	A
Drain-Source On-State Resistance ^b	$R_{DS(on)}$	$V_{GS} = 10$ V, $I_D = 14.4$ A	-	0.0084	0.0115	Ω
		$V_{GS} = 4.5$ V, $I_D = 13$ A	-	0.0111	0.0153	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15$ V, $I_D = 14.4$ A	-	37	-	S
Dynamic ^a						
Input Capacitance	C_{iss}	$V_{DS} = 15$ V, $V_{GS} = 0$ V, $f = 1$ MHz	-	650	-	pF
Output Capacitance	C_{oss}		-	236	-	
Reverse Transfer Capacitance	C_{rss}		-	20	-	
C_{rss} / C_{iss} Ratio			0.03	-	0.06	-
Total Gate Charge	Q_g	$V_{DS} = 15$ V, $V_{GS} = 10$ V, $I_D = 14.4$ A	-	10	20	nC
Gate-Source Charge	Q_{gs}	$V_{DS} = 15$ V, $V_{GS} = 4.5$ V, $I_D = 14.4$ A	-	4.5	9	
Gate-Drain Charge	Q_{gd}		-	2.1	-	
Output Charge	Q_{oss}		-	0.7	-	
			-	6.6	-	
Gate Resistance	R_g	$f = 1$ MHz	0.3	1.4	2.8	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15$ V, $R_L = 1.5$ Ω $I_D \equiv 10$ A, $V_{GEN} = 4.5$ V, $R_g = 1$ Ω	-	15	23	ns
Rise Time	t_r		-	50	75	
Turn-Off Delay Time	$t_{d(off)}$		-	16	24	
Fall Time	t_f		-	10	20	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15$ V, $R_L = 1.5$ Ω $I_D \equiv 10$ A, $V_{GEN} = 10$ V, $R_g = 1$ Ω	-	8	16	
Rise Time	t_r		-	15	23	
Turn-Off Delay Time	$t_{d(off)}$		-	17	26	
Fall Time	t_f		-	7	14	

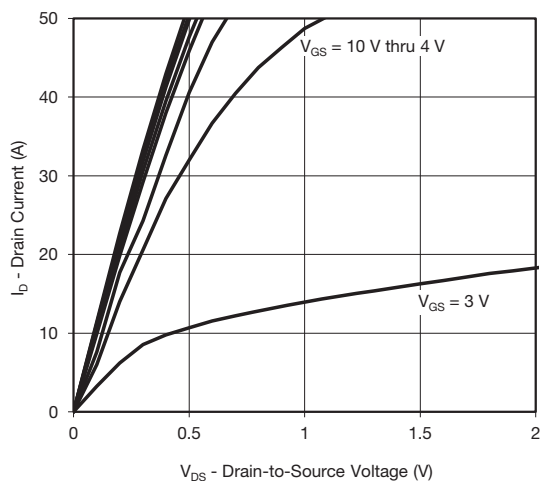
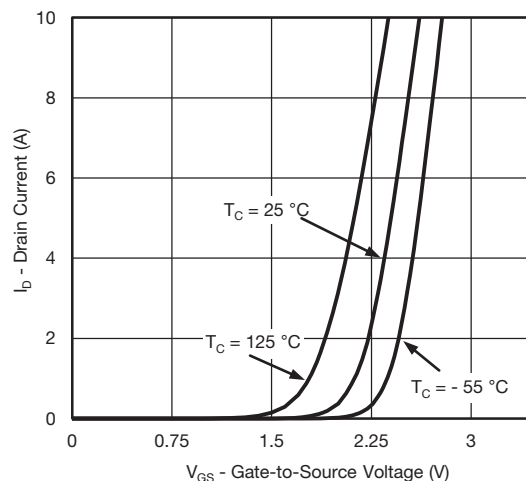
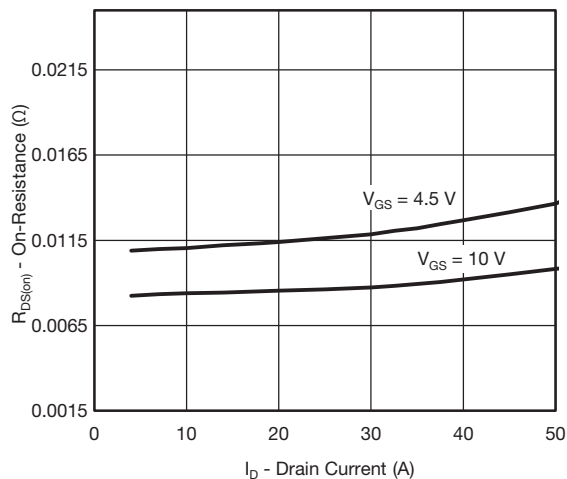
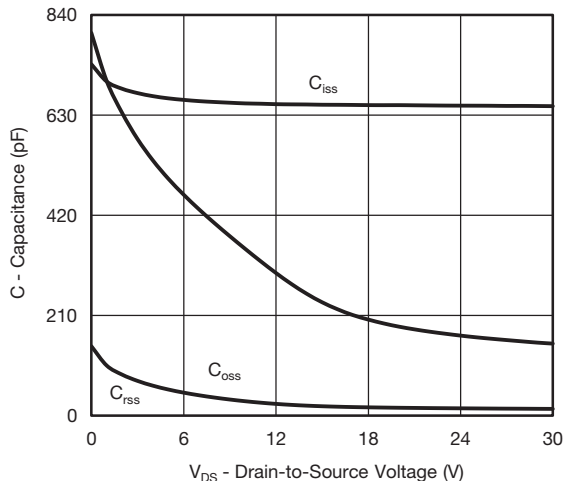
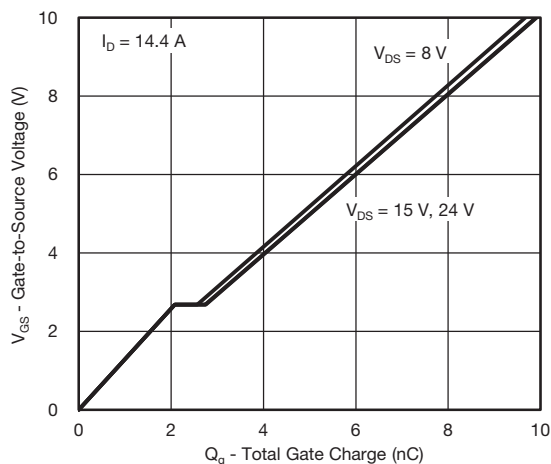
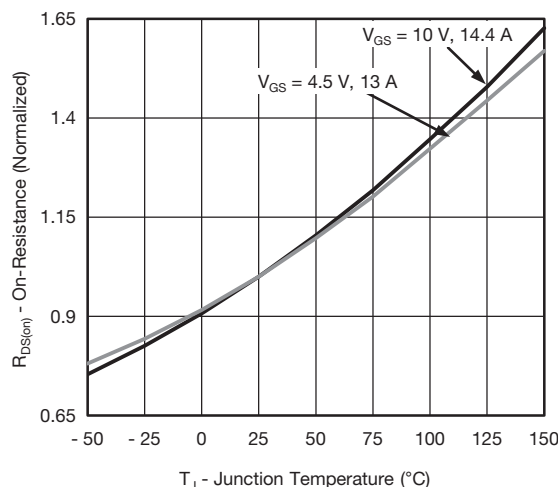
**SPECIFICATIONS** ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	CHANNEL-1 AND CHANNEL-2					
	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^{\circ}\text{C}$	-	-	13.9	A
Pulse Diode Forward Current ($t = 100\text{ }\mu\text{s}$)	I_{SM}		-	-	100	
Body Diode Voltage	V_{SD}	$I_S = 10\text{ A}$, $V_{GS} = 0\text{ V}$	-	0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 10\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^{\circ}\text{C}$	-	20	35	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	10	20	nC
Reverse Recovery Fall Time	t_a		-	12.5	-	ns
Reverse Recovery Rise Time	t_b		-	7.5	-	

Notes

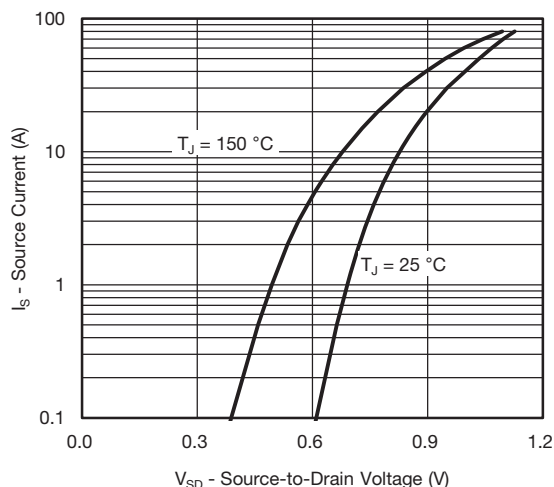
- Guaranteed by design, not subject to production testing.
- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

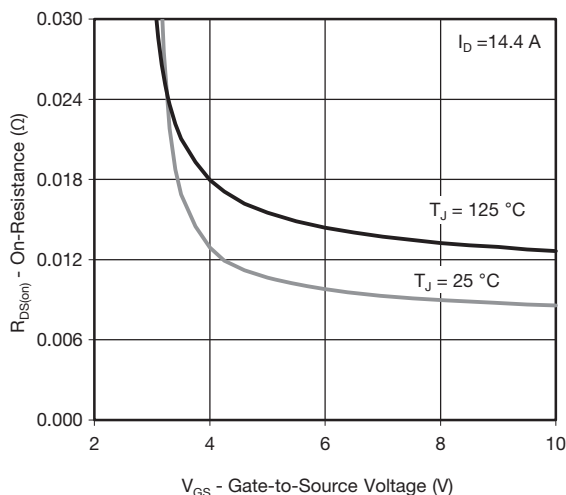
CHANNEL-1 AND CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature



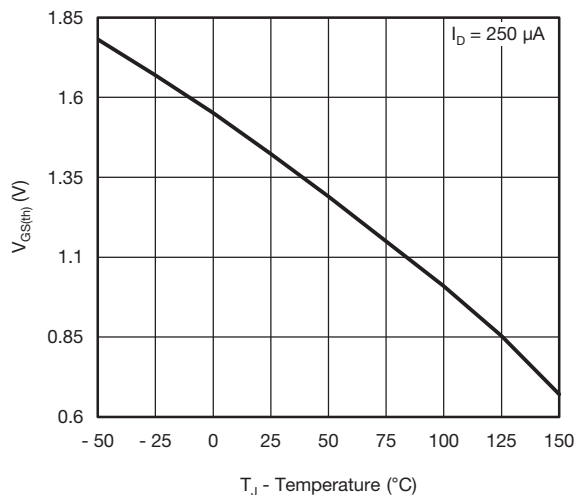
CHANNEL-1 AND CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



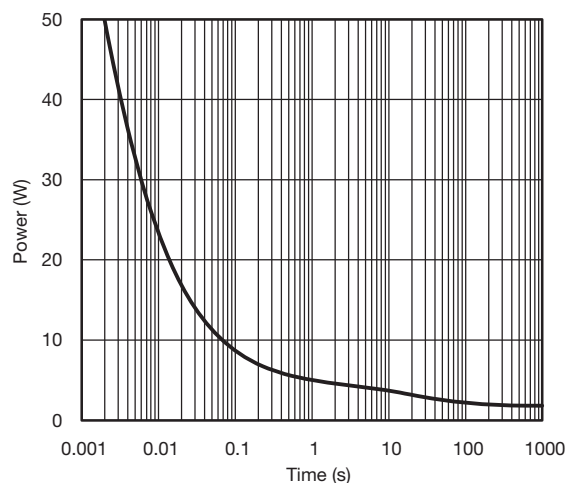
Source-Drain Diode Forward Voltage



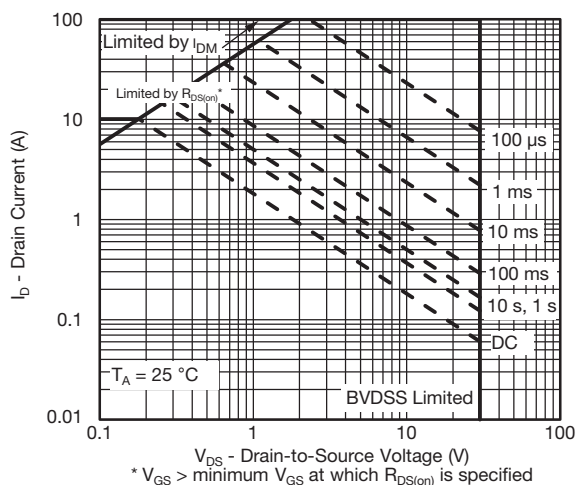
On-Resistance vs. Gate-to-Source Voltage



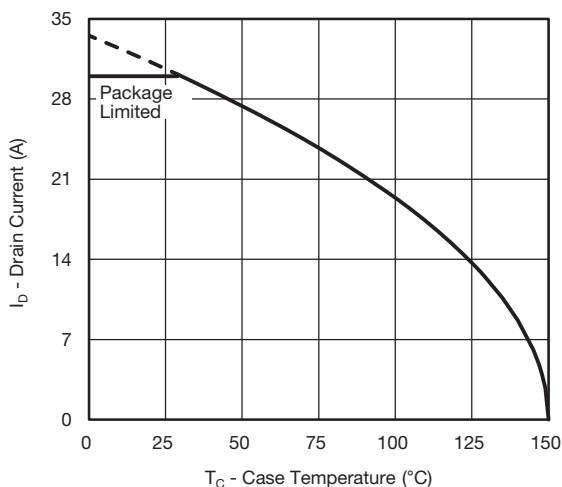
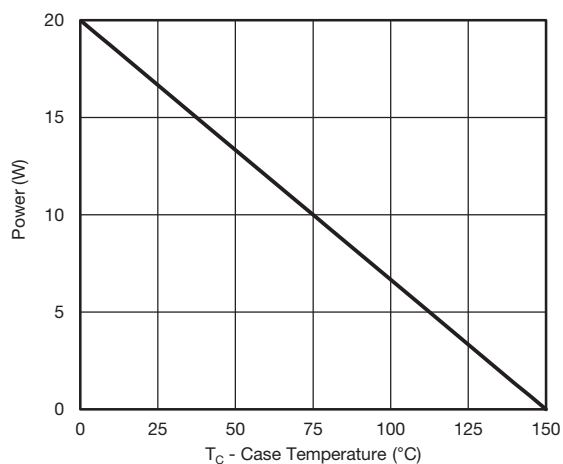
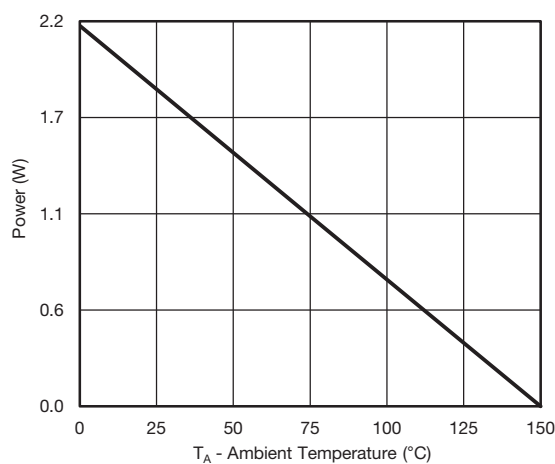
Threshold Voltage



Single Pulse Power (Junction-to-Ambient)



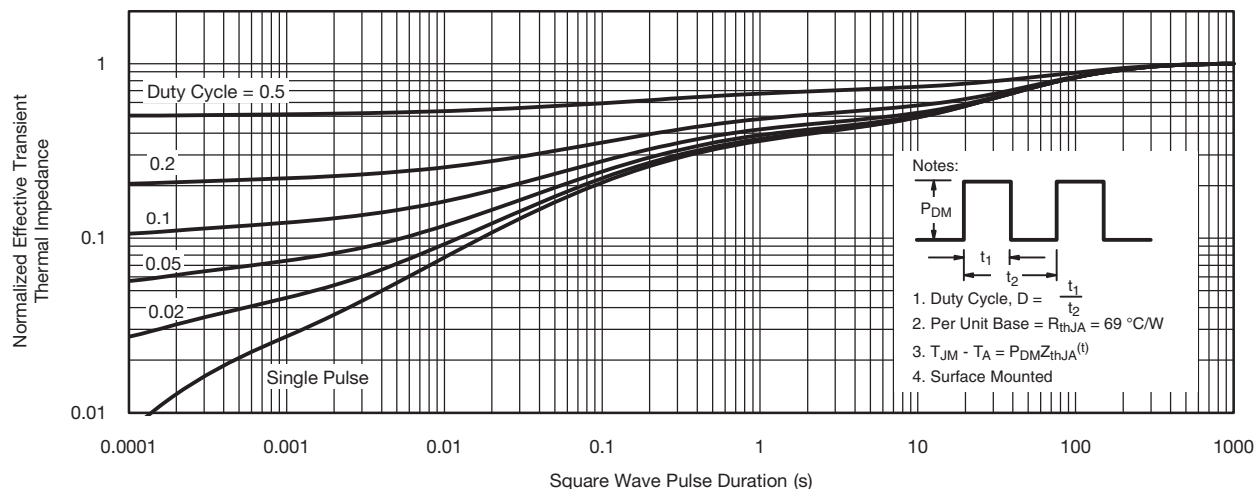
Safe Operating Area, Junction-to-Ambient

CHANNEL-1 AND CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Current Derating*

Power, Junction-to-Case

Power, Junction-to-Ambient

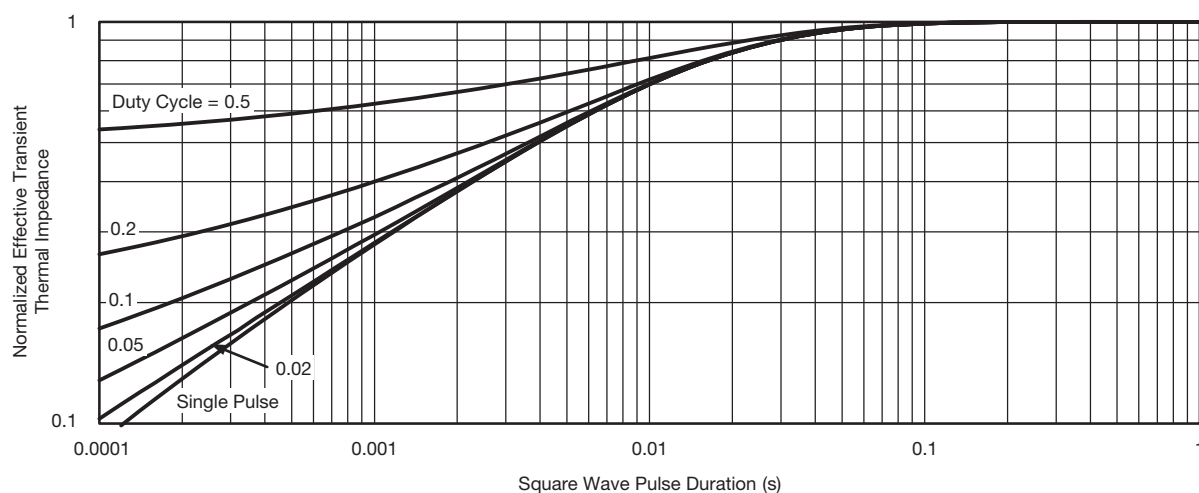
* The power dissipation P_D is based on $T_{J(max.)} = 150\text{ }^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



CHANNEL-1 AND CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

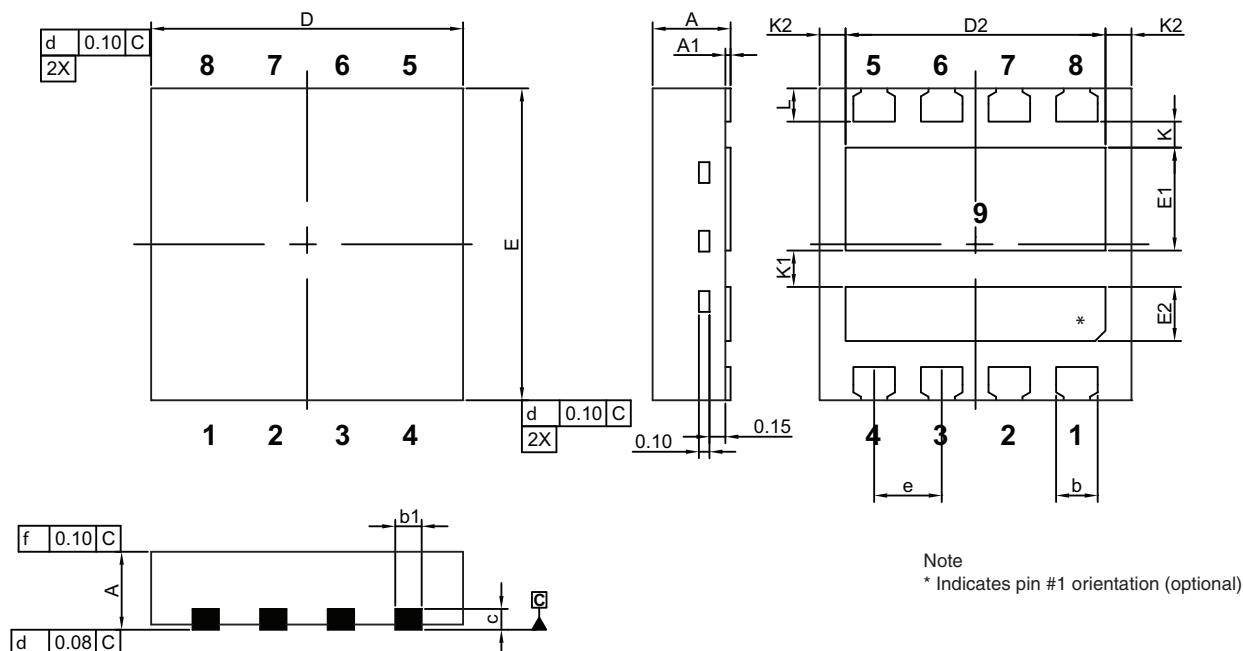


Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62949.



PowerPAIR® 3 x 3 Case Outline



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00		0.05	0.000		0.002
b	0.35	0.40	0.45	0.014	0.016	0.018
b1	0.20	0.25	0.38	0.008	0.010	0.015
C	0.18	0.20	0.23	0.007	0.008	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
D2	2.35	2.40	2.45	0.093	0.094	0.096
E	2.90	3.00	3.10	0.114	0.118	0.122
E1	0.94	0.99	1.04	0.037	0.039	0.041
E2	0.47	0.52	0.57	0.019	0.020	0.022
e	0.65 BSC			0.026 BSC		
K	0.25 typ.			0.010 typ.		
K1	0.35 typ.			0.014 typ.		
K2	0.30 typ.			0.012 typ.		
L	0.27	0.32	0.37	0.011	0.013	0.015
ECN: T12-0347-Rev. C, 18-Jun-12						
DWG: 5998						

Keep-Out 3.5 mm x 3.5 mm for non terminating traces



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