

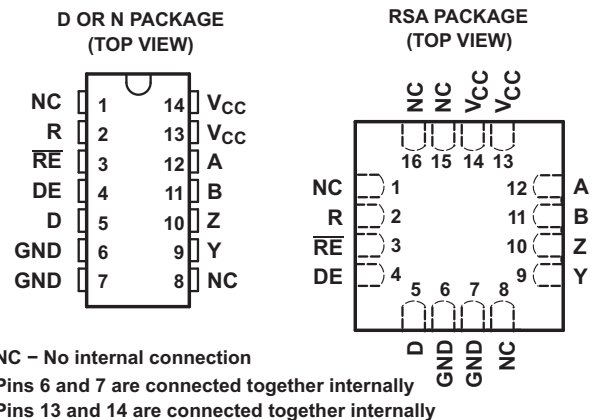
LOW-POWER RS-485 LINE DRIVER AND RECEIVER PAIRS

FEATURES

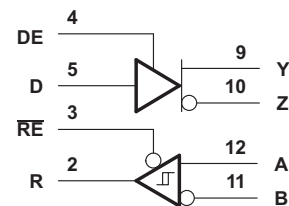
- Designed for High-Speed Multipoint Data Transmission Over Long Cables
- Operate With Pulse Durations as Low as 30 ns
- Low Supply Current . . . 5 mA Max
- Meet or Exceed the Requirements of ANSI Standard RS-485 and ISO 8482:1987(E)
- 3-State Outputs for Party-Line Buses
- Common-Mode Voltage Range of -7 V to 12 V
- Thermal Shutdown Protection Prevents Driver Damage From Bus Contention
- Positive and Negative Output Current Limiting
- Pin Compatible With the SN75ALS180

DESCRIPTION

The SN55LBC180, SN65LBC180 and SN75LBC180 differential driver and receiver pairs are monolithic integrated circuits designed for bidirectional data communication over long cables that take on the characteristics of transmission lines. They are balanced, or differential, voltage mode devices that meet or exceed the requirements of industry standards ANSI RS-485 and ISO 8482:1987(E). These devices are designed using TI's proprietary LinBiCMOS™ with the low-power consumption of CMOS and the precision and robustness of bipolar transistors in the same circuit.



logic diagram (positive logic)



ORDERING INFORMATION

| T_A | PACKAGE | PART NUMBER | PART MARKING |
|----------------|---------|---------------|--------------|
| 0°C to 70°C | PDIP | SN75LBC180N | SN75LBC180N |
| | SOIC | SN75LBC180D | 7LB180 |
| | QFN | SN75LBC180RSA | LB180 |
| -40°C to 85°C | PDIP | SN65LBC180N | 65LBC180N |
| | SOIC | SN65LBC180D | 6LB180 |
| | QFN | SN65LBC180RSA | BL180 |
| -55°C to 125°C | QFN | SN55LBC180RSA | SN55LBC180 |



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

The SN55LBC180, SN65LBC180 and SN75LBC180 combine a differential line driver and receiver with 3-state outputs and operate from a single 5-V supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected to function as a direction control. The driver differential outputs and the receiver differential inputs are connected to separate terminals for full-duplex operation and are designed to present minimum loading to the bus whether disabled or powered off ($V_{CC} = 0$). These parts feature a wide common-mode voltage range making them suitable for point-to-point or multipoint data-bus applications.

The devices also provide positive and negative output-current limiting and thermal shutdown for protection from line fault conditions. The line driver shuts down at a junction temperature of approximately 172°C.

The SN75LBC180 is characterized for operation over the commercial temperature range of 0°C to 70°C. The SN65LBC180 is characterized over the industrial temperature range of -40°C to 85°C.

The SN55LBC180 is characterized for operation over the military temperature range of -55°C to 125°C.

FUNCTION TABLES⁽¹⁾

| DRIVER | | | |
|---|--------------|-------------|---|
| INPUT D | ENABLE DE | OUTPUTS | |
| | | Y | Z |
| H | H | H | L |
| L | H | L | H |
| X | L | Z | Z |
| RECEIVER | | | |
| DIFFERENTIAL INPUTS A-B | ENABLE RE | OUTPUT R | |
| $V_{ID} \geq 0.2 \text{ V}$ | L | H | |
| $-0.2 \text{ V} < V_{ID} < 0.2 \text{ V}$ | L | ? | |
| $V_{ID} \leq -0.2 \text{ V}$ | L | L | |
| X | H | Z | |
| Open circuit | L | H | |

(1) H = high level, L = low level, ? = Indeterminate, X = irrelevant,
 Z = high impedance (off)

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| | | | UNIT | |
|-----------|---|---|------|----|
| V_{CC} | Supply voltage range ⁽²⁾ | –0.3 to 7 | V | |
| V_{BUS} | Bus voltage range (A, B, Y, Z) ⁽²⁾ | –10 to 15 | V | |
| | Voltage range at D, R, DE, \overline{RE} ⁽²⁾ | –0.3 to $V_{CC} + 0.5$ | V | |
| | Continuous total power dissipation ⁽³⁾ | Internally limited | | |
| | Total power dissipation | See Dissipation Rating Table | | |
| T_{stg} | Storage temperature range | –65 to 150 | °C | |
| I_O | Receiver output current range | –50 to 50 | mA | |
| ESD | Electrostatic discharge | HBM (Human Body Model) EIA/JESD22-A114 | ±4 | kV |
| | | MM (Machine Model) EIA/JESD22-A115 | 400 | V |
| | | CDM (Charge Device Model) EIA/JESD22-C101 | 1.5 | kV |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND.
- (3) The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature.

DISSIPATION RATING TABLE

| PACKAGE ⁽¹⁾ | $T_A \leq 25^\circ\text{C}$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 70^\circ\text{C}$ POWER RATING | $T_A = 85^\circ\text{C}$ POWER RATING | $T_A = 125^\circ\text{C}$ POWER RATING |
|------------------------|---|---|--|--|---|
| D | 950 mW | 7.6 mW/°C | 608 mW | 494 mW | — |
| N | 1150 mW | 9.2 mW/°C | 736 mW | 598 mW | — |
| RSA | 3333 mW | 26.67 mW/°C | 2133 mW | 1733 mW | 400 mW |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

RECOMMENDED OPERATING CONDITIONS

| | | | MIN | NOM | MAX | UNIT |
|-----------------------------|---|----------------------------|-------------------|-----|------|------|
| V_{CC} | Supply voltage | | 4.75 | 5 | 5.25 | V |
| V_{IH} | High-level input voltage | D, DE, and \overline{RE} | 2 | | | V |
| V_{IL} | Low-level input voltage | D, DE, and \overline{RE} | | | 0.8 | V |
| V_{ID} | Differential input voltage | | –6 ⁽¹⁾ | | 6 | V |
| V_O , V_I , or V_{IC} | Voltage at any bus terminal (separately or common mode) | A, B, Y, or Z | –7 ⁽¹⁾ | | 12 | V |
| I_{OH} | High-level output current | Y or Z | | | –60 | mA |
| | | R | | | –8 | |
| I_{OL} | Low-level output current | Y or Z | | | 60 | mA |
| | | R | | | 8 | |
| T_A | Operating free-air temperature | SN55LBC180 | –55 | | 125 | °C |
| | | SN65LBC180 | –40 | | 85 | |
| | | SN75LBC180 | 0 | | 70 | |

- (1) The algebraic convention where the least positive (more negative) limit is designated minimum, is used in this data sheet for the differential input voltage, voltage at any bus terminal, operating temperature, input threshold voltage, and common-mode output voltage.

DRIVER SECTION

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|------------------|---|---|---------------------------------------|-----|--------------------|-----------|---------------|
| V_{IK} | Input clamp voltage | $I_I = -18 \text{ mA}$ | | | | -1.5 | V |
| $ V_{OD} $ | Differential output voltage magnitude ⁽²⁾ | $R_L = 54 \Omega$, See Figure 1 | SN55LBC180 | 1 | 2.5 | 5 | V |
| | | | SN65LBC180 | 1.1 | 2.5 | 5 | |
| | | | SN75LBC180 | 1.5 | 2.5 | 5 | |
| | | $R_L = 60 \Omega$, See Figure 2 | SN55LBC180 | 1 | 2.5 | 5 | |
| | | | SN65LBC180 | 1.1 | 2 | 5 | |
| | | | SN75LBC180 | 1.5 | 2 | 5 | |
| $\Delta V_{OD} $ | Change in magnitude of differential output voltage ⁽³⁾ | See Figure 1 and Figure 2 | | | | ± 0.2 | V |
| V_{OC} | Common-mode output voltage | | | 1 | 2.5 | 3 | V |
| $\Delta V_{OC} $ | Change in magnitude of common-mode output voltage ⁽³⁾ | $R_L = 54 \Omega$, | See Figure 1 | | | ± 0.2 | V |
| I_O | Output current with power off | $V_{CC} = 0$, | $V_O = -7 \text{ V to } 12 \text{ V}$ | | | ± 100 | μA |
| I_{OZ} | High-impedance-state output current | $V_O = -7 \text{ V to } 12 \text{ V}$ | | | | ± 100 | μA |
| I_{IH} | High-level input current | $V_I = 2.4 \text{ V}$ | | | | 100 | μA |
| I_{IL} | Low-level input current | $V_I = 0.4 \text{ V}$ | | | | 100 | μA |
| I_{OS} | Short-circuit output current | $-7 \text{ V} \leq V_O \leq 12 \text{ V}$ | | | | ± 250 | mA |
| I_{CC} | Supply current | Receiver disabled | Outputs enabled | | | 5 | mA |
| | | | Outputs disabled | | | 3 | |

(1) All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^\circ\text{C}$.

(2) The minimum V_{OD} specification may not fully comply with ANSI RS-485 at operating temperatures below 0°C . System designers should take the possibly lower output signal into account in determining the maximum signal-transmission distance.

(3) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in the steady-state magnitude of V_{OD} and V_{OC} , respectively, that occur when the input is changed from a high level to a low level.

SWITCHING CHARACTERISTICS

$V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|-------------|-------------------------------------|----------------------|------------------------------|-----|-----|-----|------|
| $t_{d(OD)}$ | Differential output delay time | $R_L = 54 \Omega$, | See Figure 3 | 7 | 12 | 18 | ns |
| $t_{t(OD)}$ | Differential output transition time | | | 5 | 10 | 20 | ns |
| t_{PZH} | Output enable time to high level | $R_L = 110 \Omega$, | See Figure 4 | | | 35 | ns |
| t_{PZL} | Output enable time to low level | $R_L = 110 \Omega$, | See Figure 5 | | | 35 | ns |
| t_{PHZ} | Output disable time from high level | $R_L = 110 \Omega$, | See Figure 4 | | | 50 | ns |
| t_{PLZ} | Output disable time from low level | $R_L = 110 \Omega$, | See Figure 5 | | | 35 | ns |

SWITCHING CHARACTERISTICS (SN55LBC180)

$V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|-------------|-------------------------------------|----------------------|------------------------------|-----|-----|-----|------|
| $t_{d(OD)}$ | Differential output delay time | $R_L = 54 \Omega$, | See Figure 3 | | 15 | | ns |
| $t_{t(OD)}$ | Differential output transition time | | | | 21 | | ns |
| t_{PZH} | Output enable time to high level | $R_L = 110 \Omega$, | See Figure 4 | | 32 | | ns |
| t_{PHZ} | Output disable time from high level | | | | 55 | | |
| t_{PZL} | Output enable time to low level | $R_L = 110 \Omega$, | See Figure 5 | | 32 | | ns |
| t_{PLZ} | Output disable time from low level | | | | 20 | | |

RECEIVER SECTION

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|--|--|------------------|------|----------|---------------|
| V_{IT+} | Positive-going input threshold voltage | $I_O = -8 \text{ mA}$ | | | 0.2 | V |
| V_{IT-} | Negative-going input threshold voltage | $I_O = 8 \text{ mA}$ | -0.2 | | | V |
| V_{hys} | Hysteresis voltage ($V_{IT+} - V_{IT-}$) | | | 45 | | mV |
| V_{IK} | Enable-input clamp voltage | $I_I = -18 \text{ mA}$ | -1.5 | | | V |
| V_{OH} | High-level output voltage | $V_{ID} = 200 \text{ mV}$, $I_{OH} = -8 \text{ mA}$ | 3.5 | 4.5 | | V |
| V_{OL} | Low-level output voltage | $V_{ID} = -200 \text{ mV}$, $I_{OL} = 8 \text{ mA}$ | | 0.3 | 0.5 | V |
| I_{OZ} | High-impedance-state output current | $V_O = 0 \text{ V to } V_{CC}$ | | | ± 20 | μA |
| I_{IH} | High-level enable-input current | $V_{IH} = 2.4 \text{ V}$ | -50 | | | A |
| I_{IL} | Low-level enable-input current | $V_{IL} = 0.4 \text{ V}$ | -100 | | | μA |
| I_I | Bus input current | $V_I = 12 \text{ V}$, $V_{CC} = 5 \text{ V}$, Other input at 0 V | | 0.7 | 1 | mA |
| | | $V_I = 12 \text{ V}$, $V_{CC} = 0 \text{ V}$, Other input at 0 V | | 0.8 | 1 | |
| | | $V_I = -7 \text{ V}$, $V_{CC} = 5 \text{ V}$, Other input at 0 V | -0.8 | -0.5 | | |
| | | $V_I = -7 \text{ V}$, $V_{CC} = 0 \text{ V}$, Other input at 0 V | -0.8 | -0.5 | | |
| I_{CC} | Supply current | Driver disabled | Outputs enabled | | 5 | mA |
| | | | Outputs disabled | | 3 | |

SWITCHING CHARACTERISTICS

 $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------|---|--|-----|-----|-----|------|
| t_{PHL} | Propagation delay time, high- to low-level output | $V_{ID} = -1.5 \text{ V to } 1.5 \text{ V}$, See Figure 6 | 11 | 22 | 33 | ns |
| t_{PLH} | Propagation delay time, low- to high-level output | | 11 | 22 | 33 | ns |
| $t_{sk(p)}$ | Pulse skew ($ t_{PHL} - t_{PLH} $) | | 3 | | 6 | ns |
| t_t | Transition time | | 5 | | 8 | ns |
| t_{PZH} | Output enable time to high level | See Figure 7 | | | 35 | ns |
| t_{PZL} | Output enable time to low level | | | | 30 | ns |
| t_{PHZ} | Output disable time from high level | | | | 35 | ns |
| t_{PLZ} | Output disable time from low level | | | | 30 | ns |

SWITCHING CHARACTERISTICS (SN55LBC180)

 $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------|---|--|-----|-----|-----|------|
| t_{PHL} | Propagation delay time, high- to low-level output | $V_{ID} = -1.5 \text{ V to } 1.5 \text{ V}$, See Figure 6 | | 26 | | ns |
| t_{PLH} | Propagation delay time, low- to high-level output | | | 23 | | ns |
| $t_{sk(p)}$ | Pulse skew ($ t_{PHL} - t_{PLH} $) | | | 3 | | ns |
| $t_{sk(p)t}$ | Transition time | | | 4 | | ns |
| t_{PZH} | Output enable time to high level | See Figure 4 | | 30 | | ns |
| t_{PHZ} | Output disable time from high level | | | 26 | | ns |
| t_{PZL} | Output enable time to low level | | | 30 | | ns |
| t_{PLZ} | Output disable time from low level | | | 30 | | ns |

PARAMETER MEASUREMENT INFORMATION

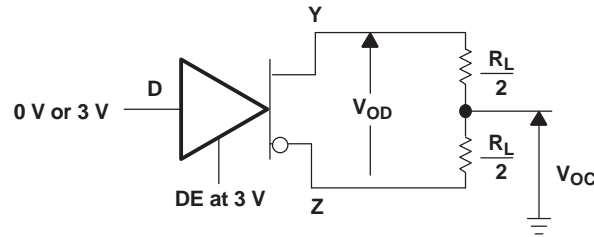


Figure 1. Differential and Common-Mode Output Voltages

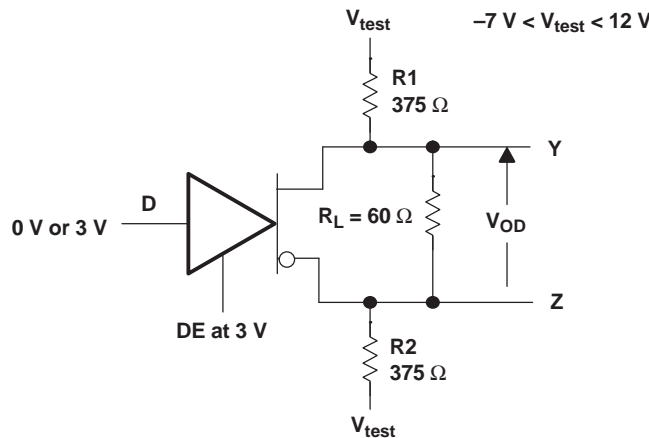
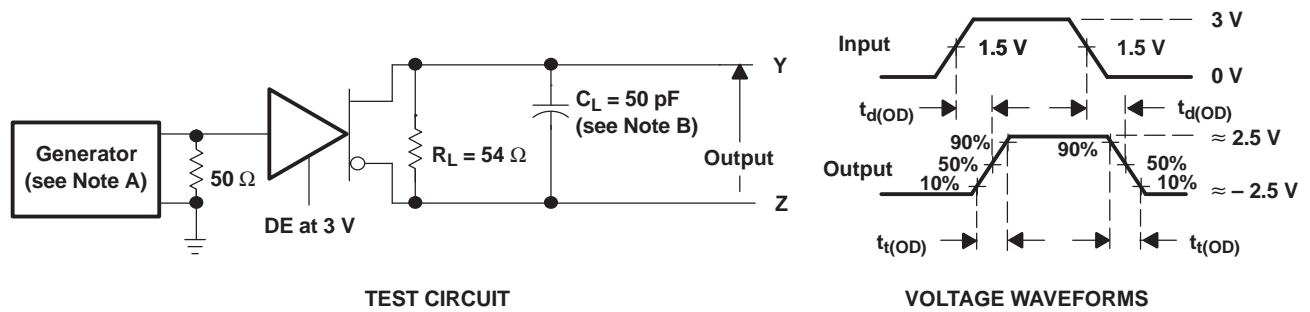


Figure 2. Driver V_{OD} Test Circuit



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR > 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
 B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Differential Output Delay and Transition Time Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

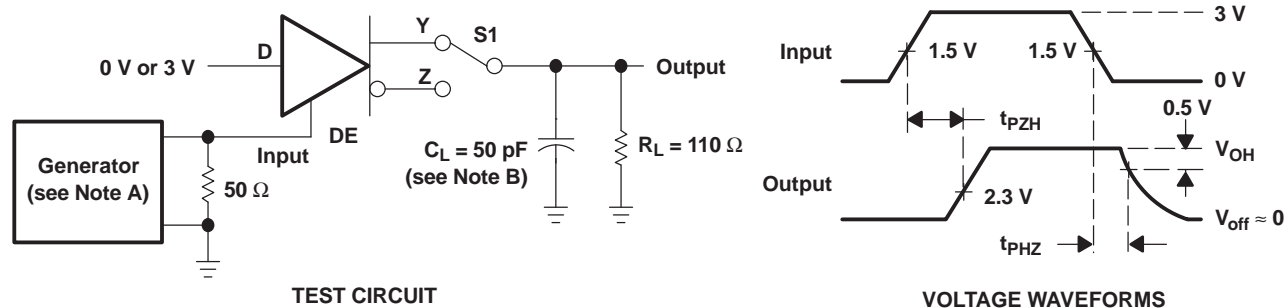


Figure 4. Driver Test Circuit and Enable and Disable Time Waveforms

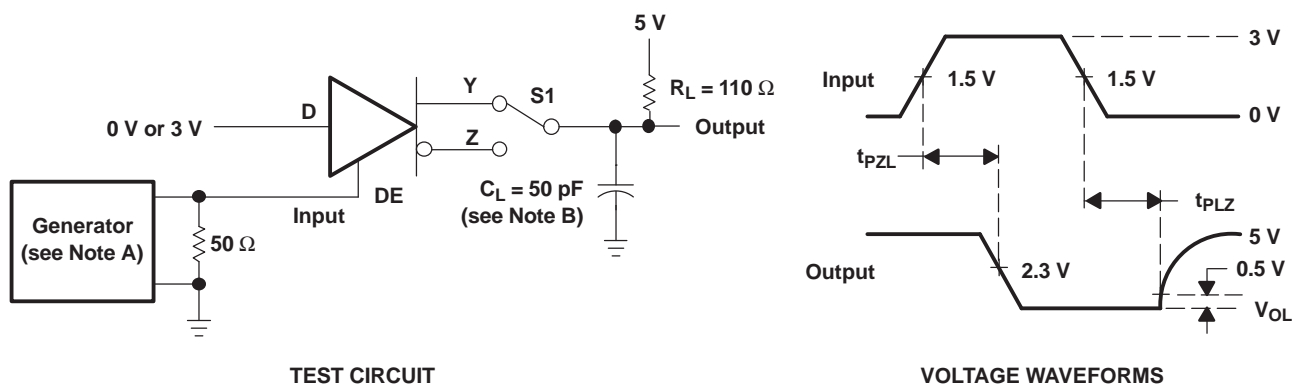
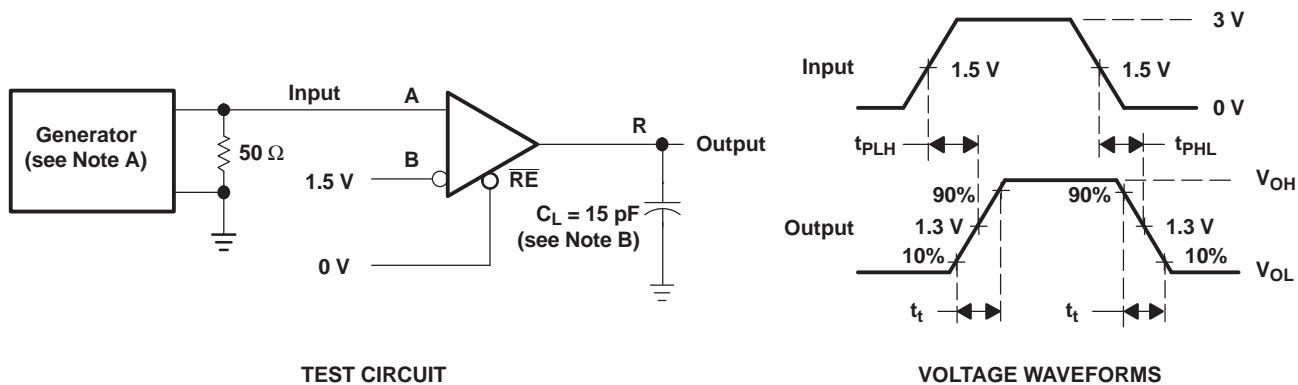


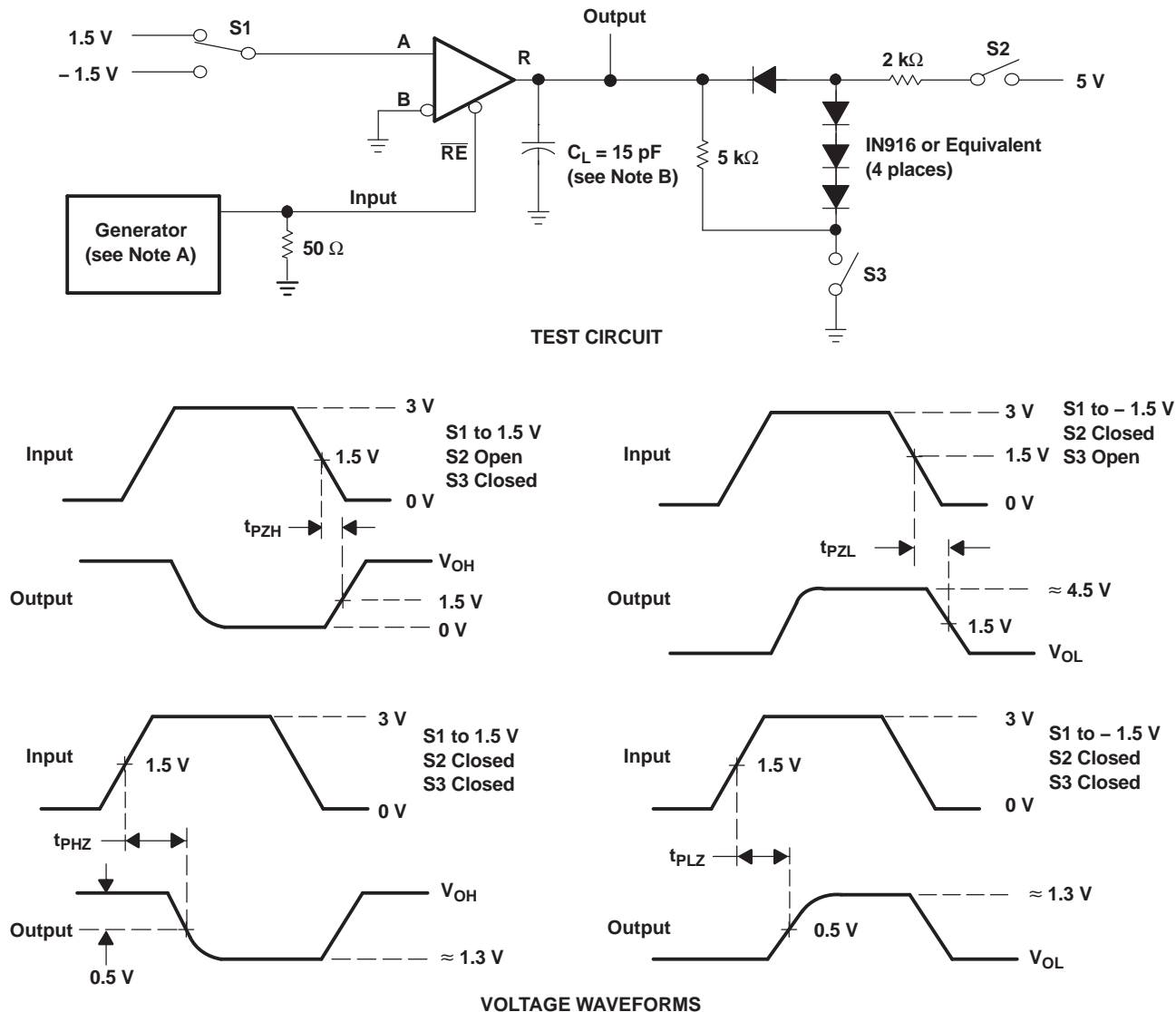
Figure 5. Driver Test Circuit and Enable and Disable Time Voltage Waveforms



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_o = 50 \Omega$.
B. C_L includes probe and jig capacitance.

Figure 6. Receiver Test Circuit and Propagation Delay Time Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

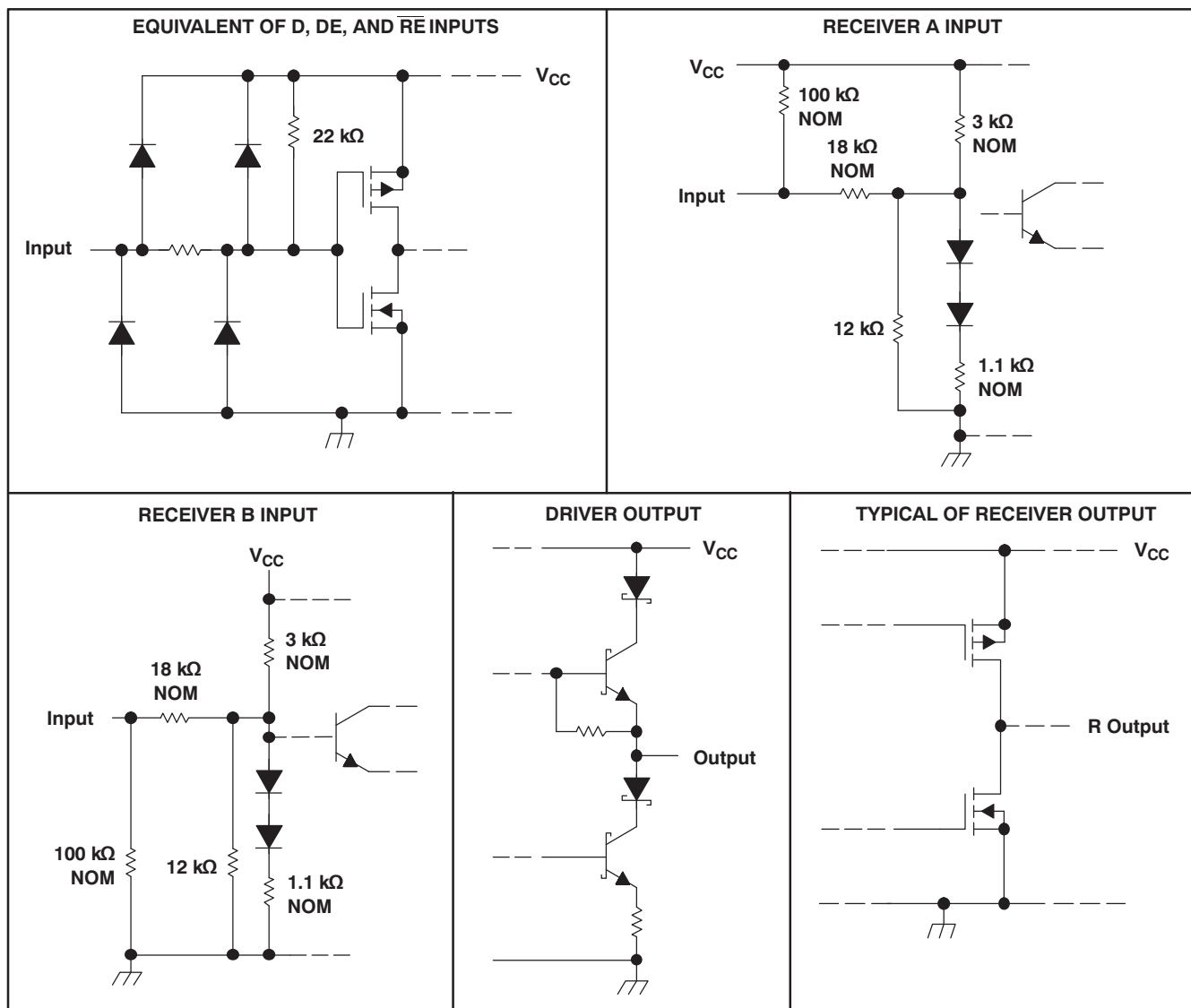


NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_O = 50 \Omega$.
 B. C_L includes probe and jig capacitance.

Figure 7. Receiver Output Enable and Disable Times

TYPICAL CHARACTERISTICS

SCHEMATICS OF INPUTS AND OUTPUTS



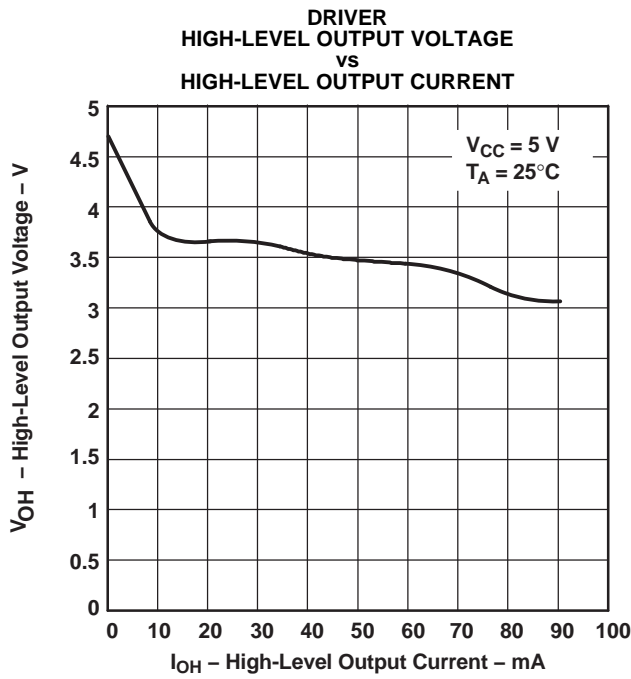


Figure 8.

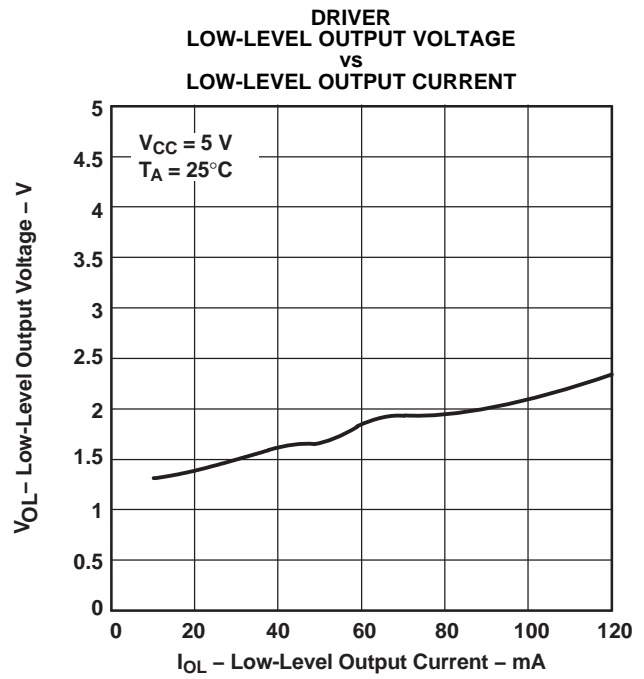


Figure 9.

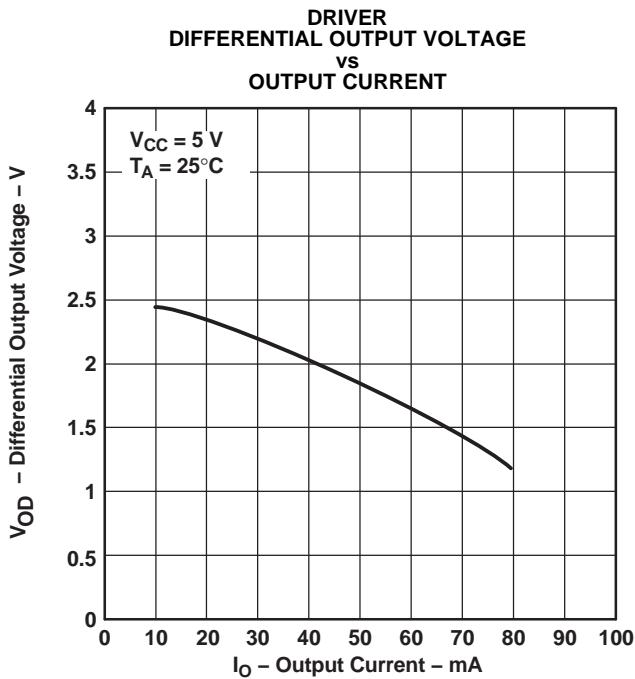


Figure 10.

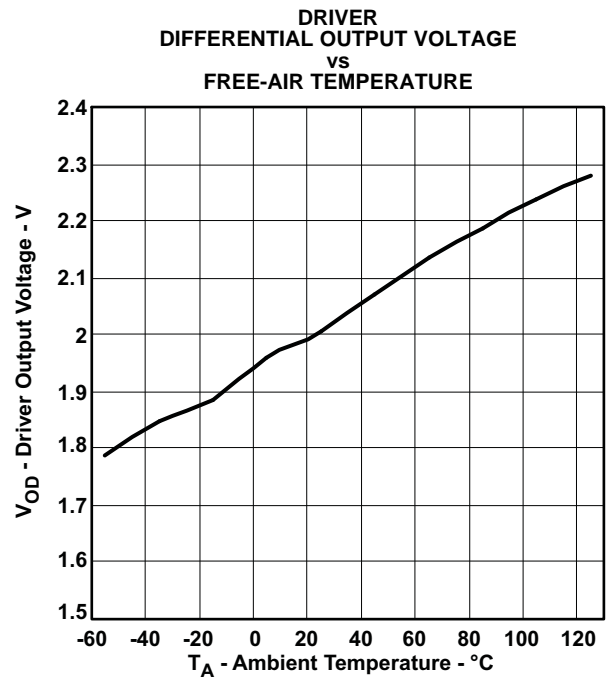


Figure 11.

DRIVER DIFFERENTIAL DELAY TIMES vs FREE-AIR TEMPERATURE

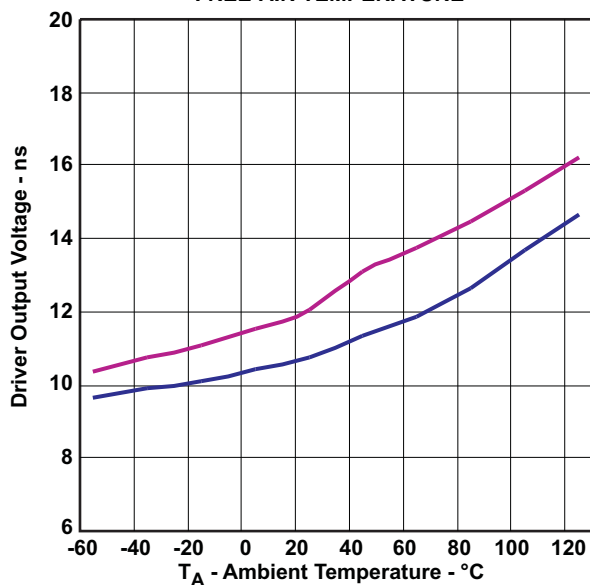


Figure 12.

DRIVER OUTPUT CURRENT vs SUPPLY VOLTAGE

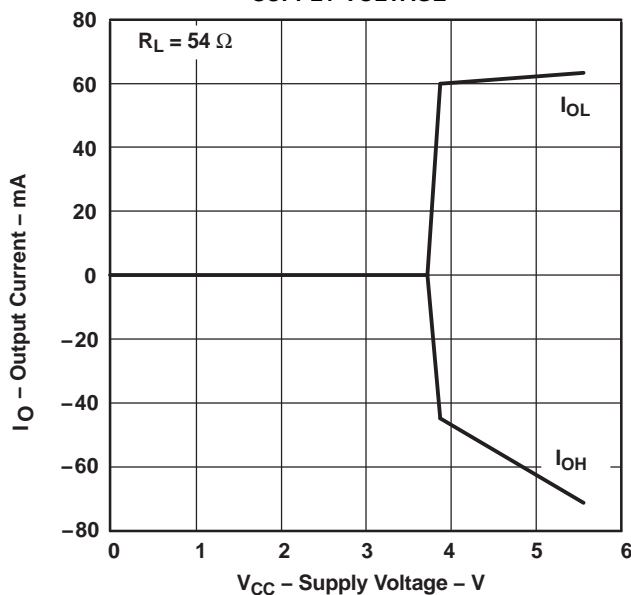


Figure 13.

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

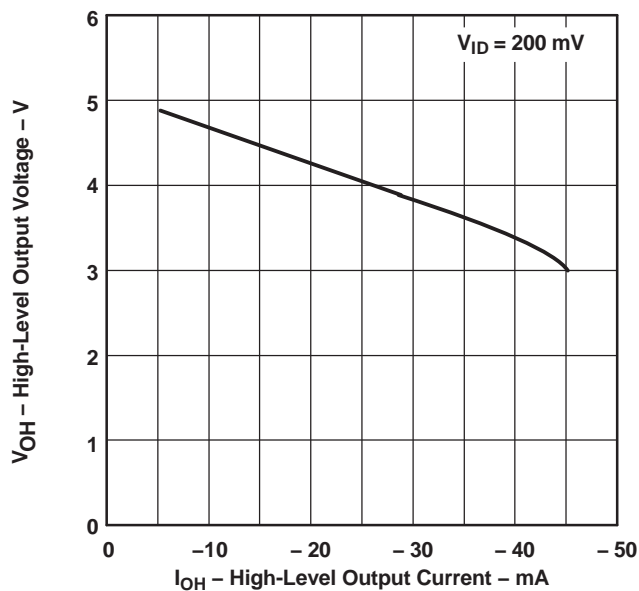


Figure 14.

RECEIVER LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

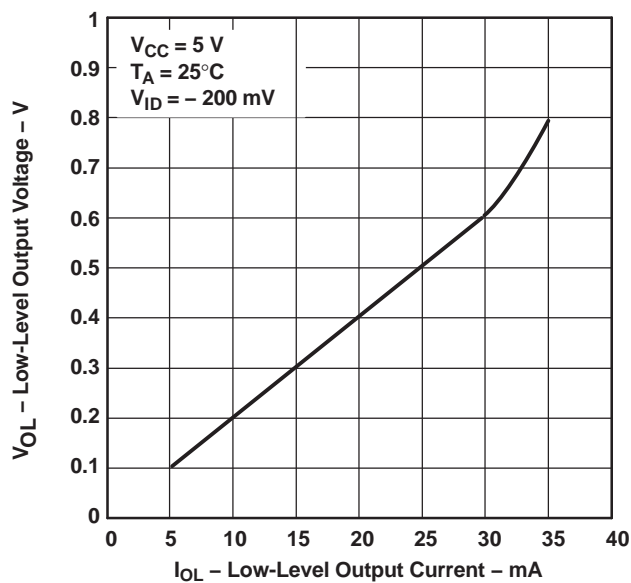
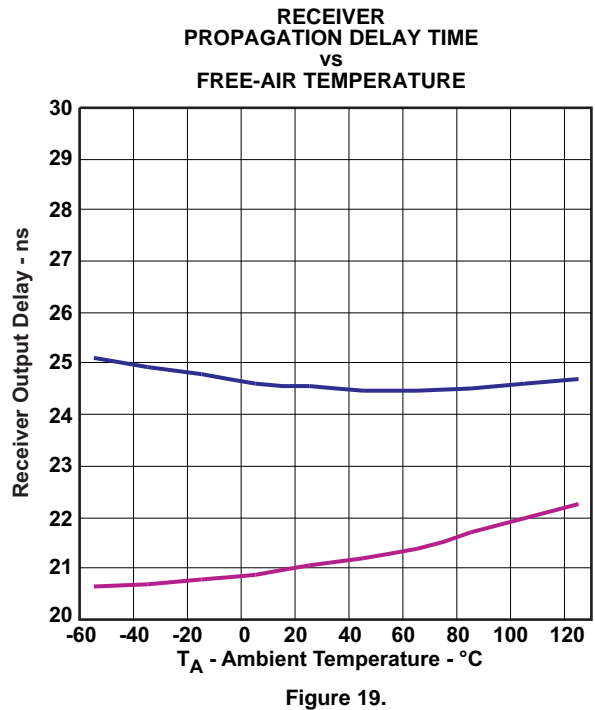
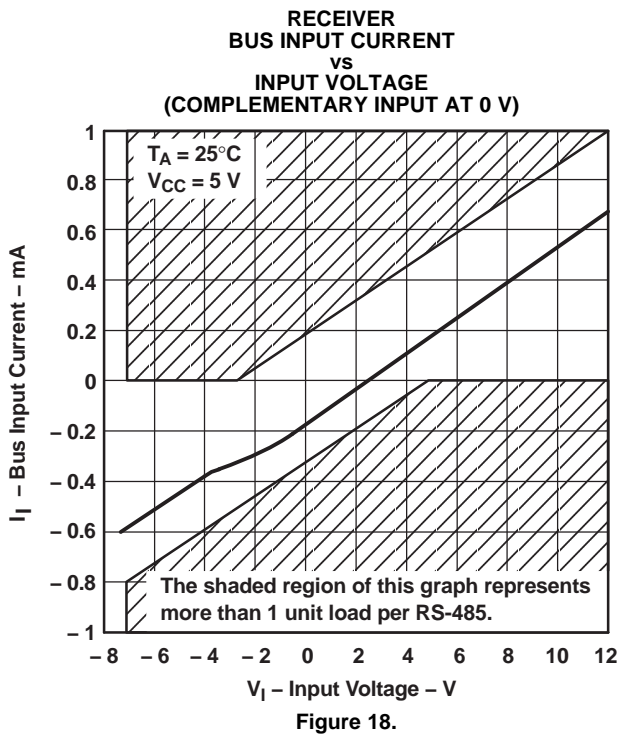
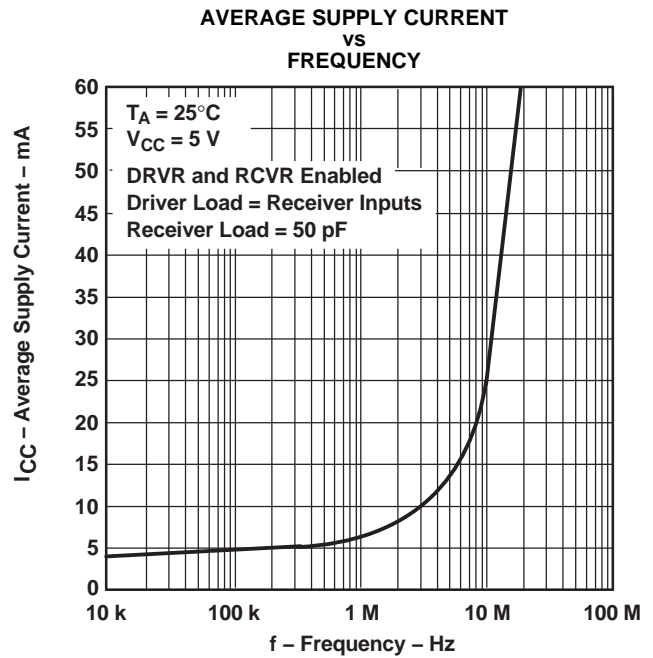
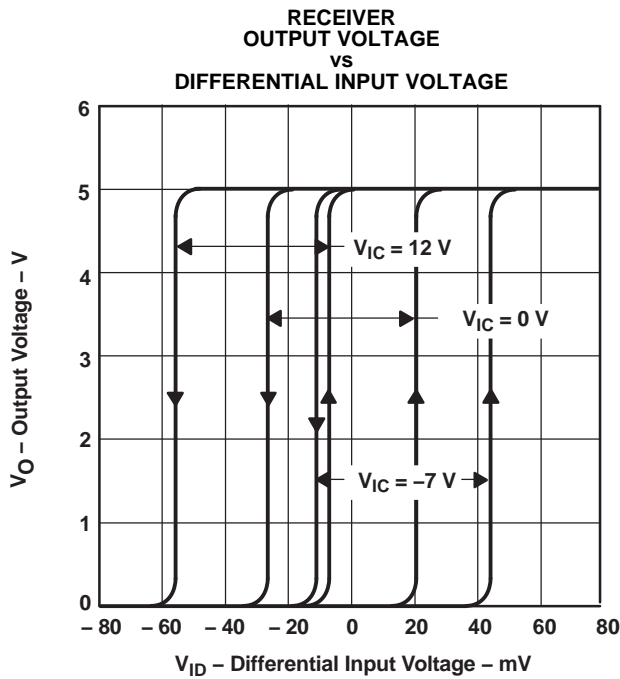


Figure 15.



APPLICATION INFORMATION

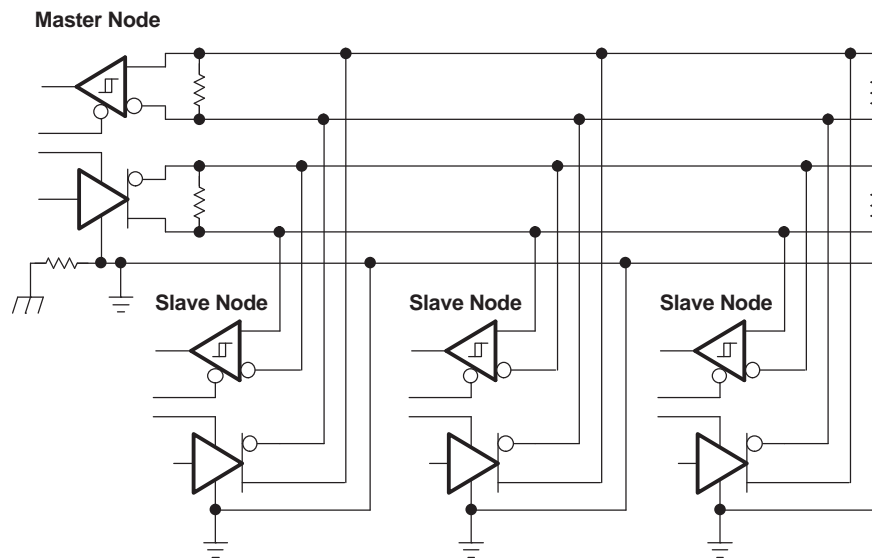


Figure 20. Full Duplex Application Circuit

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN55LBC180RSAR | ACTIVE | QFN | RSA | 16 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| SN55LBC180RSAT | ACTIVE | QFN | RSA | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| SN65LBC180D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LBC180DG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LBC180DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LBC180DRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LBC180N | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN65LBC180NE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN65LBC180RSAR | ACTIVE | QFN | RSA | 16 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| SN65LBC180RSARG4 | ACTIVE | QFN | RSA | 16 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| SN65LBC180RSAT | ACTIVE | QFN | RSA | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| SN65LBC180RSATG4 | ACTIVE | QFN | RSA | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| SN75LBC180D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75LBC180DG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75LBC180DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75LBC180DRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75LBC180N | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN75LBC180NE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN75LBC180RSAR | ACTIVE | QFN | RSA | 16 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| SN75LBC180RSARG4 | ACTIVE | QFN | RSA | 16 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| SN75LBC180RSAT | ACTIVE | QFN | RSA | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| SN75LBC180RSATG4 | ACTIVE | QFN | RSA | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN55LBC180, SN65LBC180, SN75LBC180 :

- Automotive: [SN65LBC180-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN55LBC180RSAR | QFN | RSA | 16 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| SN55LBC180RSAT | QFN | RSA | 16 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| SN65LBC180DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN65LBC180RSAR | QFN | RSA | 16 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| SN65LBC180RSAT | QFN | RSA | 16 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| SN75LBC180DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN75LBC180RSAR | QFN | RSA | 16 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| SN75LBC180RSAT | QFN | RSA | 16 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN55LBC180RSAR | QFN | RSA | 16 | 3000 | 367.0 | 367.0 | 35.0 |
| SN55LBC180RSAT | QFN | RSA | 16 | 250 | 210.0 | 185.0 | 35.0 |
| SN65LBC180DR | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| SN65LBC180RSAR | QFN | RSA | 16 | 3000 | 367.0 | 367.0 | 35.0 |
| SN65LBC180RSAT | QFN | RSA | 16 | 250 | 210.0 | 185.0 | 35.0 |
| SN75LBC180DR | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| SN75LBC180RSAR | QFN | RSA | 16 | 3000 | 367.0 | 367.0 | 35.0 |
| SN75LBC180RSAT | QFN | RSA | 16 | 250 | 210.0 | 185.0 | 35.0 |

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

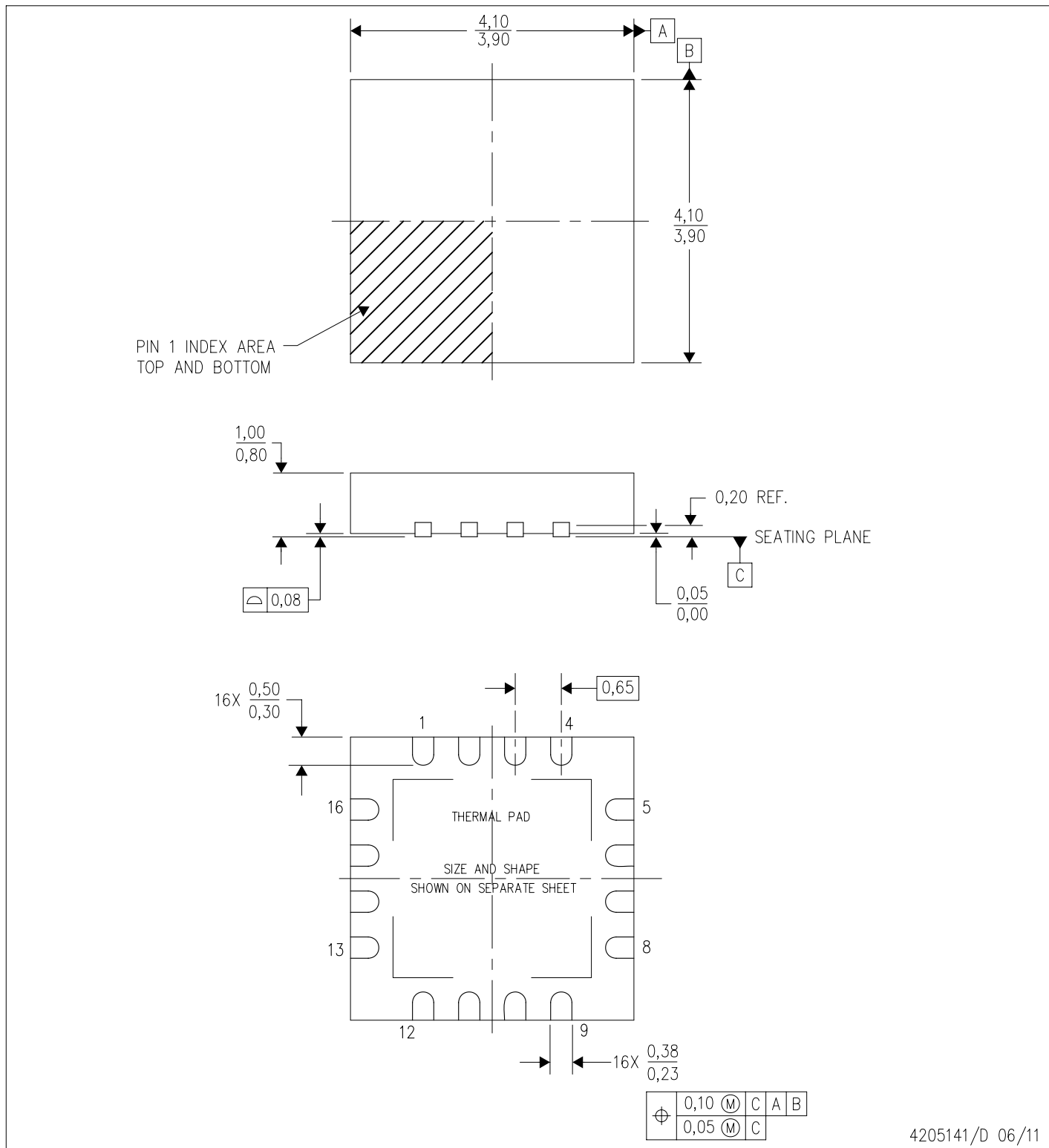
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RSA (S-PVQFN-N16)

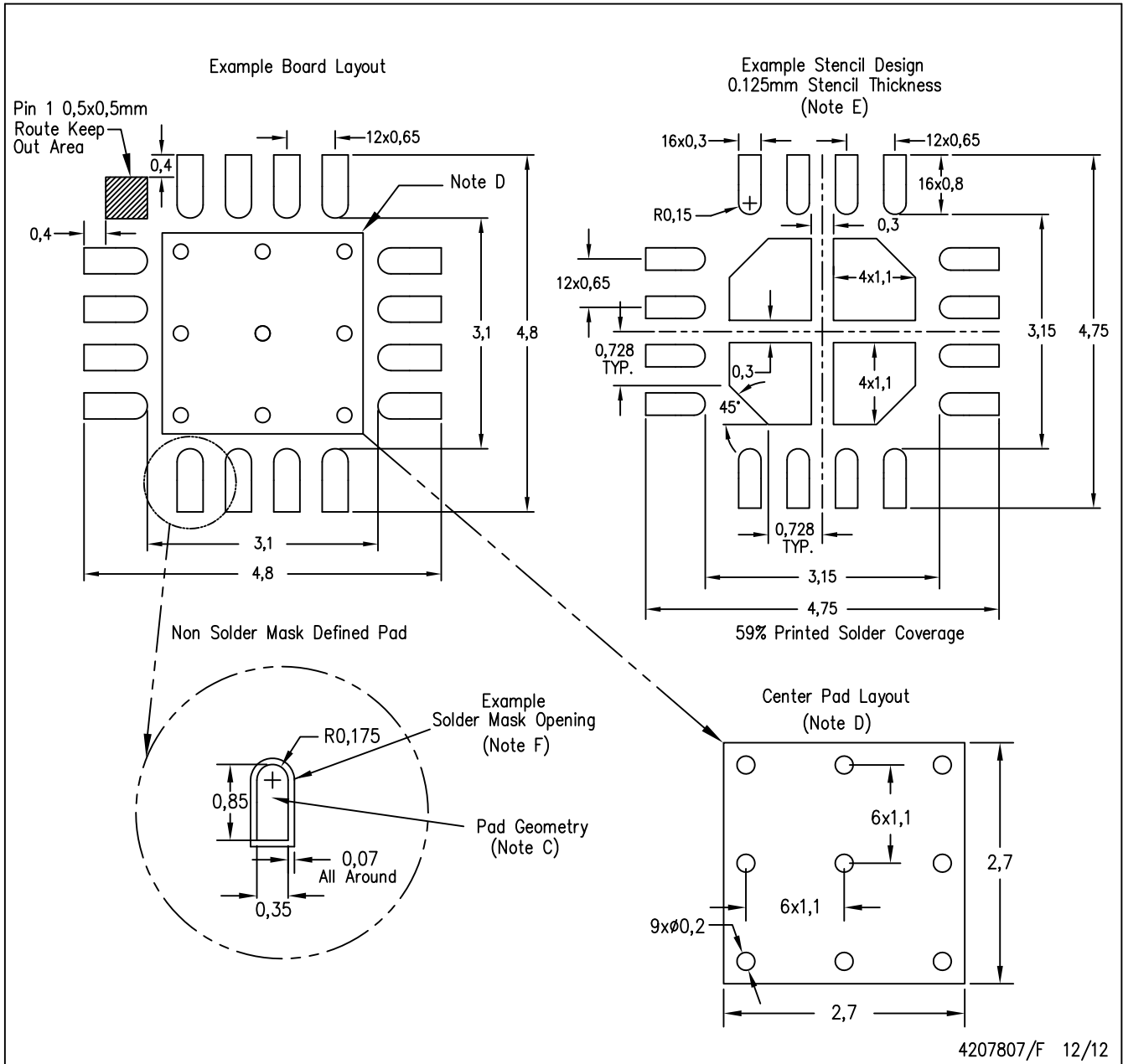
PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Quad Flatpack, No-leads (QFN) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-220.

RSA (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for solder mask tolerances.

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