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FDS6675

Single P-Channel, Logic Level, PowerTrench™ MOSFET

General Description

This P-Channel Logic Level MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

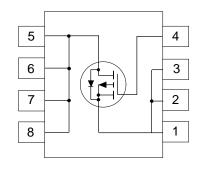
These devices are well suited for notebook computer applications: load switching and power management, battery charging circuits, and DC/DC conversion.

Features

- -11 A, -30 V. $R_{\rm DS(ON)}$ = 0.014 Ω @ $V_{\rm GS}$ = -10 V, $R_{\rm DS(ON)}$ = 0.020 Ω @ $V_{\rm GS}$ = -4.5 V.
- Low gate charge (30nC typical).
- \blacksquare High performance trench technology for extremely low $R_{\text{DS(ON)}}.$
- High power and current handling capability.







Absolute Maximum Ratings

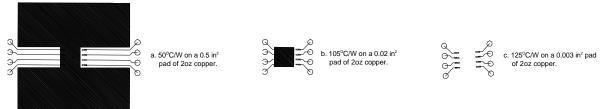
 $T_A = 25^{\circ}C$ unless otherwise noted

Symbol	Parameter		FDS6675	Units
V _{DSS}	Drain-Source Voltage		-30	V
/ _{GSS}	Gate-Source Voltage		±20	V
D	Drain Current - Continuous	(Note 1a)	-11	А
	- Pulsed		-50	
) D	Power Dissipation for Single Operation	(Note 1a)	2.5	W
		(Note 1b)	1.2	
		(Note 1c)	1	
J,T _{STG}	Operating and Storage Temperature Ran	nge	-55 to 150	°C
HERMA	L CHARACTERISTICS			•
R _{eJA}	Thermal Resistance, Junction-to-Ambier	nt (Note 1a)	50	°C/W
R _{euc}	Thermal Resistance, Junction-to-Case	(Note 1)	25	°C/W

Symbol	Parameter	Conditions	Min	Тур	Max	Units	
OFF CHAR	ACTERISTICS						
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = -250 \mu\text{A}$		-30			V
$\Delta BV_{DSS}/\Delta T_{J}$	Breakdown Voltage Temp. Coefficient	$I_D = -250 \mu\text{A}$, Referenced	to 25 °C		-22		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -24 \text{ V}, \ V_{GS} = 0 \text{ V}$				-1	μA
			$T_J = 55^{\circ}C$			-10	μA
I _{GSSF}	Gate - Body Leakage, Forward	$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$	•			100	nA
I _{GSSR}	Gate - Body Leakage, Reverse	$V_{GS} = -20 \text{ V}, V_{DS} = 0 \text{ V}$				-100	nA
ON CHARA	CTERISTICS (Note 2)			ı		l .	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -250 \mu\text{A}$		-1	-1.7	-3	V
$\Delta V_{GS(th)}/\Delta T_{J}$	Gate Threshold Voltage Temp. Coefficient	$I_D = 250 \mu\text{A}$, Referenced to	o 25 °C		4.3		mV/°C
R _{DS(ON)}	Static Drain-Source On-Resistance	$V_{GS} = -10 \text{ V}, I_D = -11 \text{ A}$			0.011	0.014	Ω
			T _J =125°C		0.016	0.023	
		$V_{GS} = -4.5 \text{ V}, I_{D} = -9 \text{ A}$			0.015	0.02	
I _{D(ON)}	On-State Drain Current	$V_{GS} = -10 \text{ V}, \ V_{DS} = -5 \text{ V}$		-50			Α
g _{FS}	Forward Transconductance	$V_{DS} = -10 \text{ V}, I_{D} = -11 \text{ A}$			32		S
DYNAMIC	CHARACTERISTICS	•					
C _{iss}	Input Capacitance	$V_{DS} = -15 \text{ V}, \ V_{GS} = 0 \text{ V},$			3000		pF
C _{oss}	Output Capacitance	f = 1.0 MHz			870		pF
C _{rss}	Reverse Transfer Capacitance			360		pF	
SWITCHING	CHARACTERISTICS (Note 2)						
t _{D(on)}	Turn - On Delay Time	$V_{DS} = -15 \text{ V}, I_{D} = -1 \text{ A}$			12	22	ns
t,	Turn - On Rise Time	$V_{GEN} = -10 \text{ V}, R_{GEN} = 6 \Omega$			16	27	ns
t _{D(off)}	Turn - Off Delay Time				50	80	ns
t,	Turn - Off Fall Time				100	140	ns
Q_g	Total Gate Charge	$V_{DS} = -15 \text{ V}, I_{D} = -11 \text{ A},$			30	42	nC
Q_{gs}	Gate-Source Charge	V _{GS} = -5 V			9		nC
Q_{gd}	Gate-Drain Charge				11		nC
DRAIN-SOL	JRCE DIODE CHARACTERISTICS AND MAX	(IMUM RATINGS					
I _s	Maximum Continuous Drain-Source Diode Fo	rward Current				-2.1	Α
V _{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = -2.1 \text{ A}$ (Not	e 2)		-0.72	-1.2	V

Notes

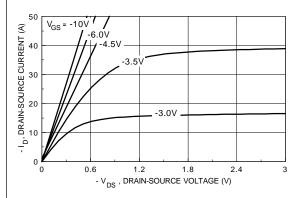
^{1.} $R_{g,u}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{g,c}$ is guaranteed by design while R_{gCA} is determined by the user's board design.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2.0%.

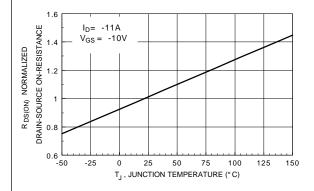
Typical Electrical Characteristics



2.5 D. DRAIN CURRENT (A)

Figure 1. On-Region Characteristics.

Figure 2. On-Resistance Variation with Dain Current and Gate Voltage.



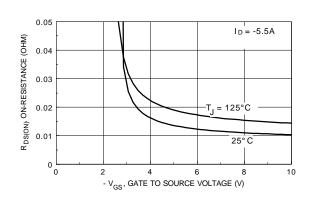
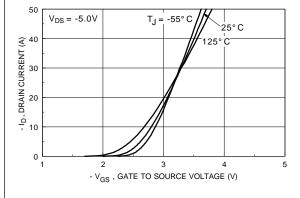


Figure 3. On-Resistance Variation with Temperature.

Figure 4. On-Resistance Variation with Gate-to-Source Voltage.



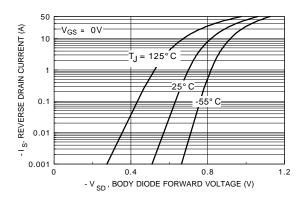
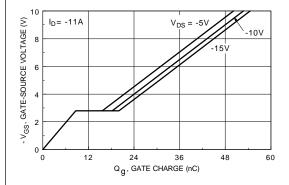


Figure 5. Transfer Characteristics.

Figure 6. Body Diode Forward Voltage
Variation with Source Current
and Temperature.

Typical Electrical Characteristics (continued)



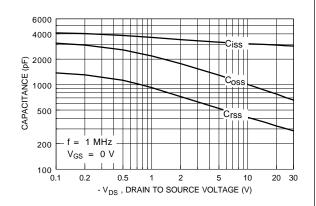
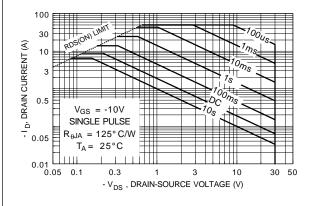


Figure 7. Gate Charge Characteristics.





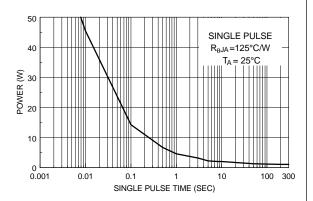


Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

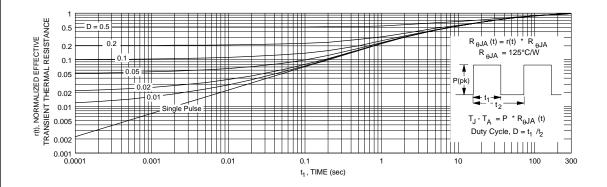
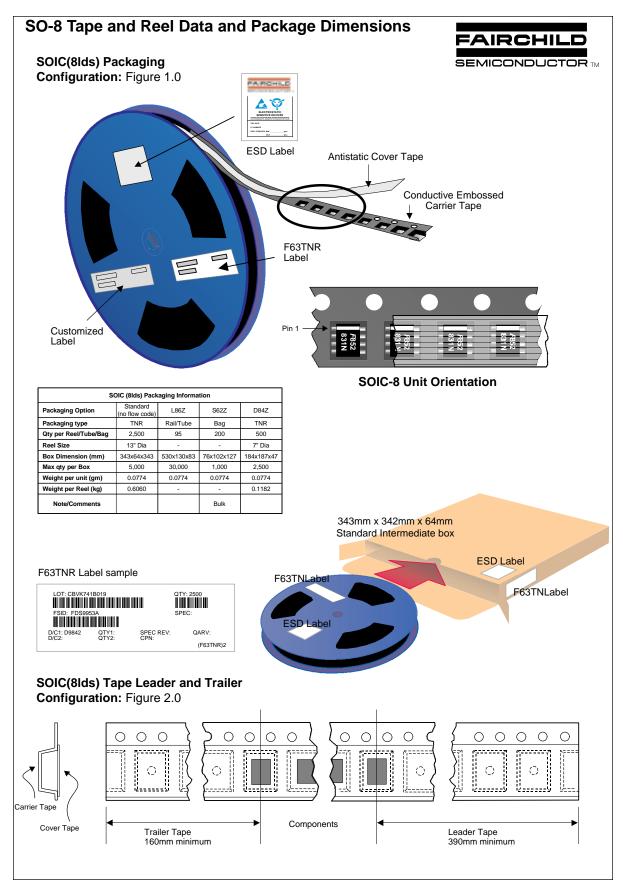
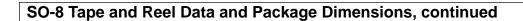


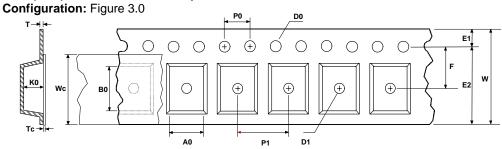
Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.





SOIC(8lds) Embossed Carrier Tape



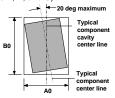
User Direction of Feed	
	_

	Dimensions are in millimeter													
Pkg type	Α0	В0	w	D0	D1	E1	E2	F	P1	P0	K0	т	Wc	Тс
SOIC(8lds) (12mm)	6.50 +/-0.10	5.30 +/-0.10	12.0 +/-0.3	1.55 +/-0.05	1.60 +/-0.10	1.75 +/-0.10	10.25 min	5.50 +/-0.05	8.0 +/-0.1	4.0 +/-0.1	2.1 +/-0.10	0.450 +/- 0.150	9.2 +/-0.3	0.06 +/-0.02

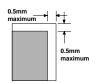
Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)
Component Rotation



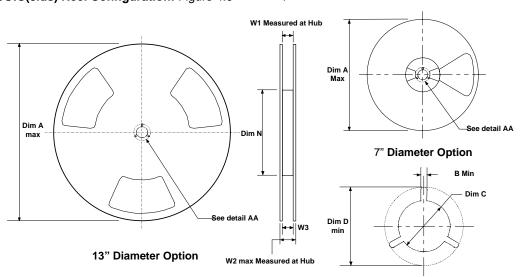
Sketch B (Top View)
Component Rotation



Sketch C (Top View)

Component lateral movement

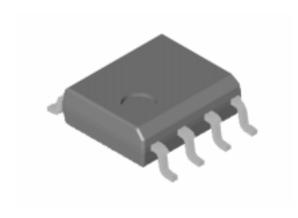
SOIC(8lds) Reel Configuration: Figure 4.0

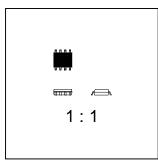


								DETAIL AA	L	
	Dimensions are in inches and millimeters									
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)	
12mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	5.906 150	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4	
12mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	7.00 178	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4	

SO-8 Tape and Reel Data and Package Dimensions, continued

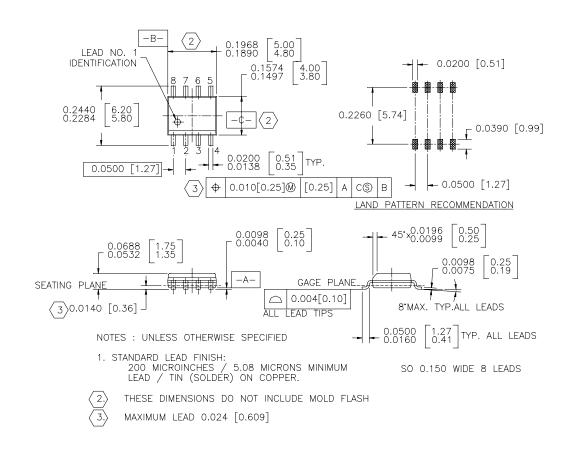
SOIC-8 (FS PKG Code S1)





Scale 1:1 on letter size paper
Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 0.0774



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CROSSVOLTTM POPTM

E²CMOS[™] PowerTrench[™]

FACTTM QSTM

 $\begin{array}{lll} \text{FACT Quiet Series}^{\text{TM}} & \text{Quite Series}^{\text{TM}} \\ \text{FAST}^{\text{\tiny{\$}}} & \text{SuperSOT}^{\text{TM}}\text{-3} \\ \text{FASTr}^{\text{TM}} & \text{SuperSOT}^{\text{TM}}\text{-6} \\ \text{GTO}^{\text{TM}} & \text{SuperSOT}^{\text{TM}}\text{-8} \\ \text{HiSeC}^{\text{TM}} & \text{TinyLogic}^{\text{TM}} \end{array}$

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