119- & 165-Bump BGA
Commercial Temp
Industrial Temp

8M x 18, 4M x 36
144Mb S/DCD Sync Burst SRAMs

400 MHz–200 MHz
2.5 V or 3.3 V V_{DD}
2.5 V or 3.3 V I/O

Features

- $\overline{FT}$ pin for user-configurable flow through or pipeline operation
- Single/Dual Cycle Deselect selectable
- IEEE 1149.1 JTAG-compatible Boundary Scan
- ZQ mode pin for user-selectable high/low output drive
- 2.5 V +10%/–10% core power supply
- 3.3 V +10%/–10% core power supply
- 2.5 V or 3.3 V I/O supply
- $\overline{LBO}$ pin for Linear or Interleaved Burst mode
- Internal input resistors on mode pins allow floating mode pins
- Default to SCD x18/x36 Interleaved Pipeline mode
- Byte Write ($\overline{BW}$) and/or Global Write ($\overline{GW}$) operation
- Internal self-timed write cycle
- ZZ pin for automatic power-down
- RoHS-compliant 119-bump and 165-bump BGA packages

Functional Description

Applications

The GS8128218/36 is a 150,994,944-bit high performance synchronous SRAM with a 2-bit burst address counter. Although of a type originally developed for Level 2 Cache applications supporting high performance CPUs, the device now finds application in synchronous SRAM applications, ranging from DSP main store to networking chip set support.

Controls

Addresses, data I/Os, chip enable ($\overline{E1}$), address burst control inputs ($\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$), and write control inputs ($\overline{Bx}$, $\overline{BW}$, $\overline{GW}$) are synchronous and are controlled by a positive-edge-triggered clock input (CK). Output enable ($\overline{G}$) and power down control (ZZ) are asynchronous inputs. Burst cycles can be initiated with either $\overline{ADSP}$ or $\overline{ADSC}$ inputs. In Burst mode, subsequent burst addresses are generated internally and are controlled by $\overline{ADV}$. The burst address counter may be configured to count in either linear or interleave order with the Linear Burst Order ($\overline{LBO}$) input. The Burst function need not be used. New addresses can be loaded on every cycle with no degradation of chip performance.

Flow Through/Pipeline Reads

The function of the Data Output register can be controlled by the user via the $\overline{FT}$ mode . Holding the $\overline{FT}$ mode pin low places the RAM in Flow Through mode, causing output data to bypass the Data Output Register. Holding $\overline{FT}$ high places the RAM in Pipeline mode, activating the rising-edge-triggered Data Output Register.

SCD and DCD Pipelined Reads

The GS8128218/36 is a SCD (Single Cycle Deselect) and DCD (Dual Cycle Deselect) pipelined synchronous SRAM. DCD SRAMs pipeline disable commands to the same degree as read commands. SCD SRAMs pipeline deselect commands one stage less than read commands. SCD RAMs begin turning off their outputs immediately after the deselect command has been captured in the input registers. DCD RAMs hold the deselect command for one full cycle and then begin turning off their outputs just after the second rising edge of clock. The user may configure this SRAM for either mode of operation using the SCD mode input.

Byte Write and Global Write

Byte write operation is performed by using Byte Write enable ($\overline{BW}$) input combined with one or more individual byte write signals ($\overline{Bx}$). In addition, Global Write ($\overline{GW}$) is available for writing all bytes at one time, regardless of the Byte Write control inputs.

FLXDrive™

The ZQ pin allows selection between high drive strength (ZQ low) for multi-drop bus applications and normal drive strength (ZQ floating or high) point-to-point applications. See the Output Driver Characteristics chart for details.

Core and Interface Voltages

The GS8128218/36 operates on a 2.5 V or 3.3 V power supply. All input are 3.3 V and 2.5 V compatible. Separate output power (V_{DDQ}) pins are used to decouple output noise from the internal circuits and are 3.3 V and 2.5 V compatible.

Parameter Synopsis

		-400	-333	-250	-200	Unit
Pipeline 3-1-1-1	t_{KQ}	2.5	2.5	2.5	3.0	ns
	tCycle	2.5	3.0	4.0	5.0	ns
	Curr (x18)	610	530	430	360	mA
	Curr (x32/x36)	690	600	470	400	mA
Flow Through 2-1-1-1	t_{KQ}	4.0	4.5	5.5	6.5	ns
	tCycle	4.0	4.5	5.5	6.5	ns
	Curr (x18)	430	400	360	295	mA
	Curr (x32/x36)	470	435	380	330	mA

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119-Bump BGA—x36 Common I/O—Top View

	1	2	3	4	5	6	7	
A	V_{DDQ}	A	A	$\overline{ADSP}$	A	A	V_{DDQ}	A
B	NC	A	A	$\overline{ADSC}$	A	A	NC	B
C	A	A	A	V_{DD}	A	A	NC	C
D	DQ_C	DQP_C	V_{SS}	ZQ	V_{SS}	DQP_B	DQ_B	D
E	DQ_C	DQ_C	V_{SS}	$\overline{E1}$	V_{SS}	DQ_B	DQ_B	E
F	V_{DDQ}	DQ_C	V_{SS}	$\overline{G}$	V_{SS}	DQ_B	V_{DDQ}	F
G	DQ_{C2}	DQ_C	$\overline{BC}$	$\overline{ADV}$	$\overline{BB}$	DQ_B	DQ_B	G
H	DQ_C	DQ_C	V_{SS}	$\overline{GW}$	V_{SS}	DQ_B	DQ_B	H
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}	J
K	DQ_D	DQ_D	V_{SS}	CK	V_{SS}	DQ_A	DQ_A	K
L	DQ_D	DQ_D	$\overline{BD}$	SCD	$\overline{BA}$	DQ_A	DQ_A	L
M	V_{DDQ}	DQ_D	V_{SS}	$\overline{BW}$	V_{SS}	DQ_A	V_{DDQ}	M
N	DQ_D	DQ_D	V_{SS}	A1	V_{SS}	DQ_A	DQ_A	N
P	DQ_D	DQP_D	V_{SS}	A0	V_{SS}	DQP_A	DQ_A	P
R	NC	A	$\overline{LBO}$	V_{DD}	$\overline{FT}$	A	NC	R
T	NC	A	A	A	A	A	ZZ	T
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}	U

7 x 17 Bump BGA—14 x 22 mm^2 Body—1.27 mm Bump Pitch

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119-Bump BGA—x18 Common I/O—Top View

	1	2	3	4	5	6	7	
A	V_{DDQ}	A	A	$\overline{ADSP}$	A	A	V_{DDQ}	A
B	NC	A	A	$\overline{ADSC}$	A	A	NC	B
C	A	A	A	V_{DD}	A	A	NC	C
D	DQ_B	NC	V_{SS}	ZQ	V_{SS}	DQP_A	NC	D
E	NC	DQ_B	V_{SS}	$\overline{E1}$	V_{SS}	NC	DQ_A	E
F	V_{DDQ}	NC	V_{SS}	$\overline{G}$	V_{SS}	DQ_A	V_{DDQ}	F
G	NC	DQ_B	$\overline{BB}$	$\overline{ADV}$	NC	NC	DQ_A	G
H	DQ_B	NC	V_{SS}	$\overline{GW}$	V_{SS}	DQ_A	NC	H
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}	J
K	NC	DQ_B	V_{SS}	CK	V_{SS}	NC	DQ_A	K
L	DQ_B	NC	NC	SCD	$\overline{BA}$	DQ_A	NC	L
M	V_{DDQ}	DQ_B	V_{SS}	$\overline{BW}$	V_{SS}	NC	V_{DDQ}	M
N	DQ_B	NC	V_{SS}	A1	V_{SS}	DQ_A	NC	N
P	NC	DQP_B	V_{SS}	A0	V_{SS}	NC	DQ_A	P
R	NC	A	$\overline{LBO}$	V_{DD}	$\overline{FT}$	A	NC	R
T	A	A	A	A	A	A	ZZ	T
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}	U

7 x 17 Bump BGA—14 x 22 mm^2 Body—1.27 mm Bump Pitch

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119-Bump BGA Pin Description

Symbol	Type	Description
A_0, A_1	I	Address field LSBs and Address Counter Preset Inputs
An	I	Address Inputs
DQ_A DQ_B DQ_C DQ_D	I/O	Data Input and Output pins
$\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D$	I	Byte Write Enable for DQ_A, DQ_B, DQ_C, DQ_D I/Os; active low
NC	—	No Connect
CK	I	Clock Input Signal; active high
$\overline{BW}$	I	Byte Write—Writes all enabled bytes; active low
$\overline{GW}$	I	Global Write Enable—Writes all bytes; active low
$\overline{E}_1$	I	Chip Enable; active low
$\overline{G}$	I	Output Enable; active low
$\overline{ADV}$	I	Burst address counter advance enable; active low
$\overline{ADSP}$, $\overline{ADSC}$	I	Address Strobe (Processor, Cache Controller); active low
ZZ	I	Sleep mode control; active high
$\overline{FT}$	I	Flow Through or Pipeline mode; active low
$\overline{LBO}$	I	Linear Burst Order mode; active low
ZQ	I	FLXDrive Output Impedance Control (Low = Low Impedance [High Drive], High = High Impedance [Low Drive])
SCD	I	Single Cycle Deselect/Dual Cyle Deselect Mode Control
TMS	I	Scan Test Mode Select
TDI	I	Scan Test Data In
TDO	O	Scan Test Data Out
TCK	I	Scan Test Clock
V_{DD}	I	Core power supply
V_{SS}	I	I/O and Core Ground
V_{SS}	I	I/O and Core Ground
V_{DDQ}	I	Output driver power supply
NC	—	No Connect

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165-Bump BGA—x18 Commom I/O—Top View

	1	2	3	4	5	6	7	8	9	10	11	
A	NC	A	$\overline{E1}$	$\overline{BB}$	NC	NC	$\overline{BW}$	$\overline{ADSC}$	$\overline{ADV}$	A	A	A
B	A	A	NC	NC	$\overline{BA}$	CK	$\overline{GW}$	$\overline{G}$	$\overline{ADSP}$	A	NC	B
C	NC	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	*DQPA*	C
D	NC	DQB	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQA	D
E	NC	DQB	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQA	E
F	NC	DQB	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQA	F
G	NC	DQB	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQA	G
H	$\overline{FT}$	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	ZQ	ZZ	H
J	DQB	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQA	NC	J
K	DQB	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQA	NC	K
L	DQB	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQA	NC	L
M	DQB	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQA	NC	M
N	*DQPB*	SCD	V_{DDQ}	V_{SS}	NC	A	NC	V_{SS}	V_{DDQ}	NC	NC	N
P	NC	A	A	A	TDI	A1	TDO	A	A	A	A	P
R	$\overline{LBO}$	A	A	A	TMS	A0	TCK	A	A	A	A	R

11 x 15 Bump BGA—13 mm x 15 mm Body—1.0 mm Bump Pitch

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165-Bump BGA—x36 Common I/O—Top View

	1	2	3	4	5	6	7	8	9	10	11	
A	NC	A	$\overline{E1}$	$\overline{BC}$	$\overline{BB}$	NC	$\overline{BW}$	$\overline{ADSC}$	$\overline{ADV}$	A	NC	A
B	A	A	NC	$\overline{BD}$	$\overline{BA}$	CK	$\overline{GW}$	$\overline{G}$	$\overline{ADSP}$	A	NC	B
C	*DQPC*	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	*DQPB*	C
D	DQC	DQC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQB	DQB	D
E	DQC	DQC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQB	DQB	E
F	DQC	DQC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQB	DQB	F
G	DQC	DQC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQB	DQB	G
H	$\overline{FT}$	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	ZQ	ZZ	H
J	DQD	DQD	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQA	DQA	J
K	DQD	DQD	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQA	DQA	K
L	DQD	DQD	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQA	DQA	L
M	DQD	DQD	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQA	DQA	M
N	*DQPD*	SCD	V_{DDQ}	V_{SS}	NC	A	NC	V_{SS}	V_{DDQ}	NC	*DQPA*	N
P	NC	A	A	A	TDI	A1	TDO	A	A	A	A	P
R	$\overline{LBO}$	A	A	A	TMS	A0	TCK	A	A	A	A	R

11 x 15 Bump BGA—13 mm x 15 mm Body—1.0 mm Bump Pitch

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165-Bump BGA Pin Description

Symbol	Type	Description
A_0, A_1	I	Address field LSBs and Address Counter Preset Inputs
A	I	Address Inputs
DQ_A DQ_B DQ_C DQ_D	I/O	Data Input and Output pins
$\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D$	I	Byte Write Enable for DQ_A, DQ_B, DQ_C, DQ_D I/Os; active low (x36 Version)
CK	I	Clock Input Signal; active high
$\overline{BW}$	I	Byte Write—Writes all enabled bytes; active low
$\overline{GW}$	I	Global Write Enable—Writes all bytes; active low
$\overline{E}_1$	I	Chip Enable; active low
$\overline{G}$	I	Output Enable; active low
$\overline{ADV}$	I	Burst address counter advance enable; active l0w
$\overline{ADSC}$, $\overline{ADSP}$	I	Address Strobe (Processor, Cache Controller); active low
ZZ	I	Sleep mode control; active high
$\overline{FT}$	I	Flow Through or Pipeline mode; active low
$\overline{LBO}$	I	Linear Burst Order mode; active low
ZQ	I	FLXDrive Output Impedance Control (Low = Low Impedance [High Drive], High = High Impedance [Low Drive])
TMS	I	Scan Test Mode Select
TDI	I	Scan Test Data In
TDO	O	Scan Test Data Out
TCK	I	Scan Test Clock
SCD	—	Single Cycle Deselect/Dual Cyle Deselect Mode Control
V_{DD}	I	Core power supply
V_{SS}	I	I/O and Core Ground
V_{DDQ}	I	Output driver power supply
NC	—	No Connect

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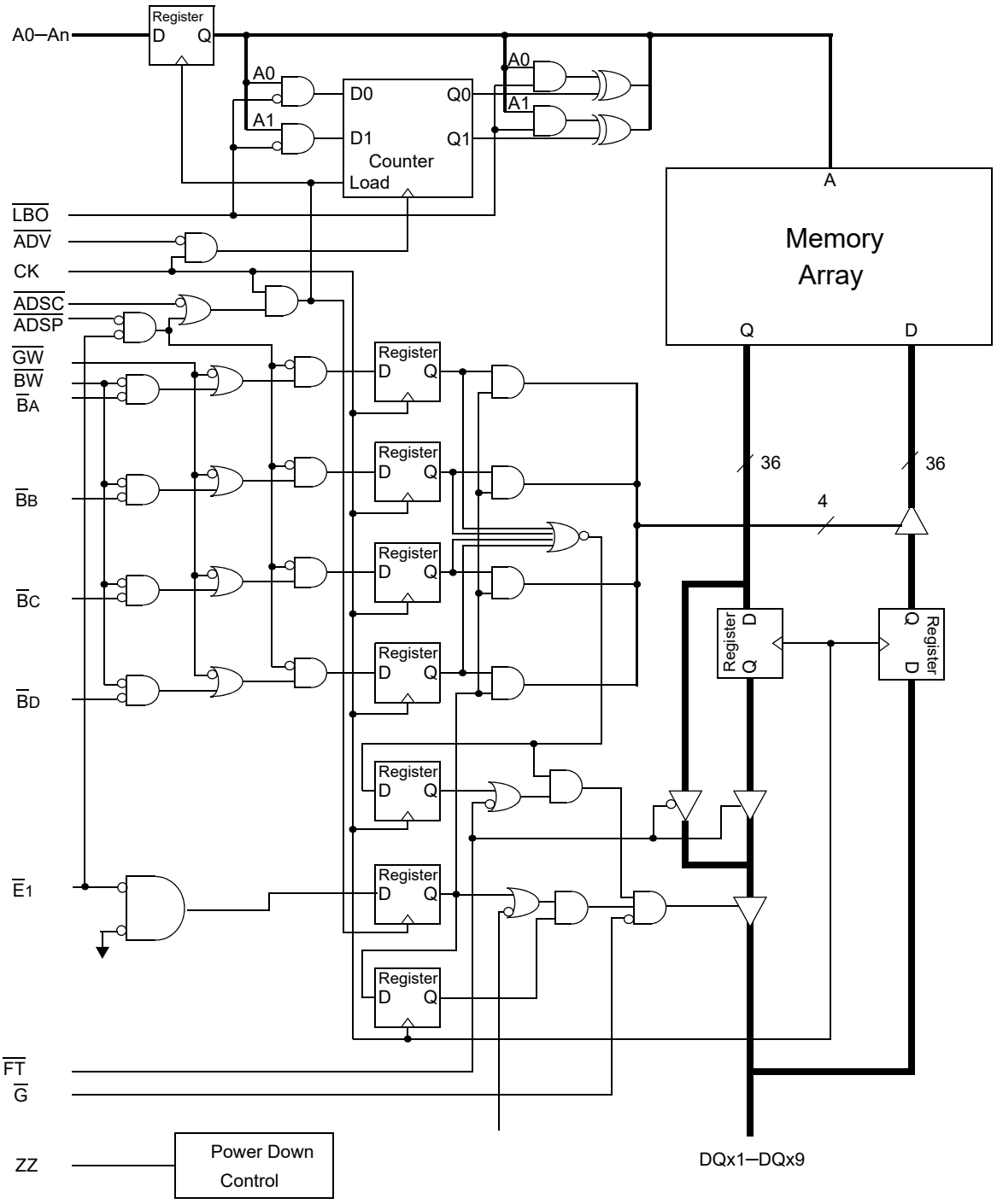
GS8128218/36 Block Diagram



Note: Only x36 version shown for simplicity.

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Mode Pin Functions

Mode Name	Pin Name	State	Function
Burst Order Control	$\overline{LBO}$	L	Linear Burst
		H	Interleaved Burst
Output Register Control	$\overline{FT}$	L	Flow Through
		H or NC	Pipeline
Power Down Control	ZZ	L or NC	Active
		H	Standby, $I_{DD} = I_{SB}$
Single/Dual Cycle Deselect Control	SCD	L	Dual Cycle Deselect
		H or NC	Single Cycle Deselect
FLXDrive Output Impedance Control	ZQ	L	High Drive (Low Impedance)
		H or NC	Low Drive (High Impedance)

Note:
There are pull-up devices on the ZQ, SCD, and $\overline{FT}$ pins and a pull-down device on the ZZ pin, so those input pins can be unconnected and the chip will operate in the default states as specified in the above tables.

Burst Counter Sequences

Linear Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	10	11	00
3rd address	10	11	00	01
4th address	11	00	01	10

Note:
The burst counter wraps to initial state on the 5th clock.

Interleaved Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	00	11	10
3rd address	10	11	00	01
4th address	11	10	01	00

Note:
The burst counter wraps to initial state on the 5th clock.

BPR 1999.05.18

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Byte Write Truth Table

Function	$\overline{GW}$	$\overline{BW}$	$\overline{B}_A$	$\overline{B}_B$	$\overline{B}_C$	$\overline{B}_D$	Notes
Read	H	H	X	X	X	X	1
Write No Bytes	H	L	H	H	H	H	1
Write byte a	H	L	L	H	H	H	2, 3
Write byte b	H	L	H	L	H	H	2, 3
Write byte c	H	L	H	H	L	H	2, 3, 4
Write byte d	H	L	H	H	H	L	2, 3, 4
Write all bytes	H	L	L	L	L	L	2, 3, 4
Write all bytes	L	X	X	X	X	X	

Notes:

1. All byte outputs are active in read cycles regardless of the state of Byte Write Enable inputs, $\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$ and/or $\overline{B}_D$.
2. Byte Write Enable inputs $\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$ and/or $\overline{B}_D$ may be used in any combination with $\overline{BW}$ to write single or multiple bytes.
3. All byte I/Os remain High-Z during all write operations regardless of the state of Byte Write Enable inputs.
4. Bytes "C" and "D" are only available on the x32 and x36 versions.

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Synchronous Truth Table

Operation	Address Used	State Diagram Key	$\overline{E}1$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{W}$	DQ[3]
Deselect Cycle, Power Down	None	X	H	X	L	X	X	High-Z
Read Cycle, Begin Burst	External	R	L	L	X	X	X	Q
Read Cycle, Begin Burst	External	R	L	H	L	X	F	Q
Write Cycle, Begin Burst	External	W	L	H	L	X	T	D
Read Cycle, Continue Burst	*Next*	*CR*	*X*	*H*	*H*	*L*	*F*	*Q*
Read Cycle, Continue Burst	Next	CR	H	X	H	L	F	Q
Write Cycle, Continue Burst	*Next*	*CW*	*X*	*H*	*H*	*L*	*T*	*D*
Write Cycle, Continue Burst	Next	CW	H	X	H	L	T	D
Read Cycle, Suspend Burst	Current		X	H	H	H	F	Q
Read Cycle, Suspend Burst	Current		H	X	H	H	F	Q
Write Cycle, Suspend Burst	Current		X	H	H	H	T	D
Write Cycle, Suspend Burst	Current		H	X	H	H	T	D

Notes:
1. X = Don't Care, H = High, L = Low
2. $\overline{W}$ = T (True) and F (False) is defined in the Byte Write Truth Table preceding.
3. $\overline{G}$ is an asynchronous input. $\overline{G}$ can be driven high at any time to disable active output drivers. $\overline{G}$ low can only enable active drivers (shown as "Q" in the Truth Table above).
4. All input combinations shown above are tested and supported. Input combinations shown in gray boxes need not be used to accomplish basic synchronous or synchronous burst operations and may be avoided for simplicity.
5. Tying $\overline{ADSP}$ high and $\overline{ADSC}$ low allows simple non-burst synchronous operations. See **BOLD** items above.
6. Tying $\overline{ADSP}$ high and $\overline{ADV}$ low while using $\overline{ADSC}$ to load new addresses allows simple burst operations. See *ITALIC* items above.

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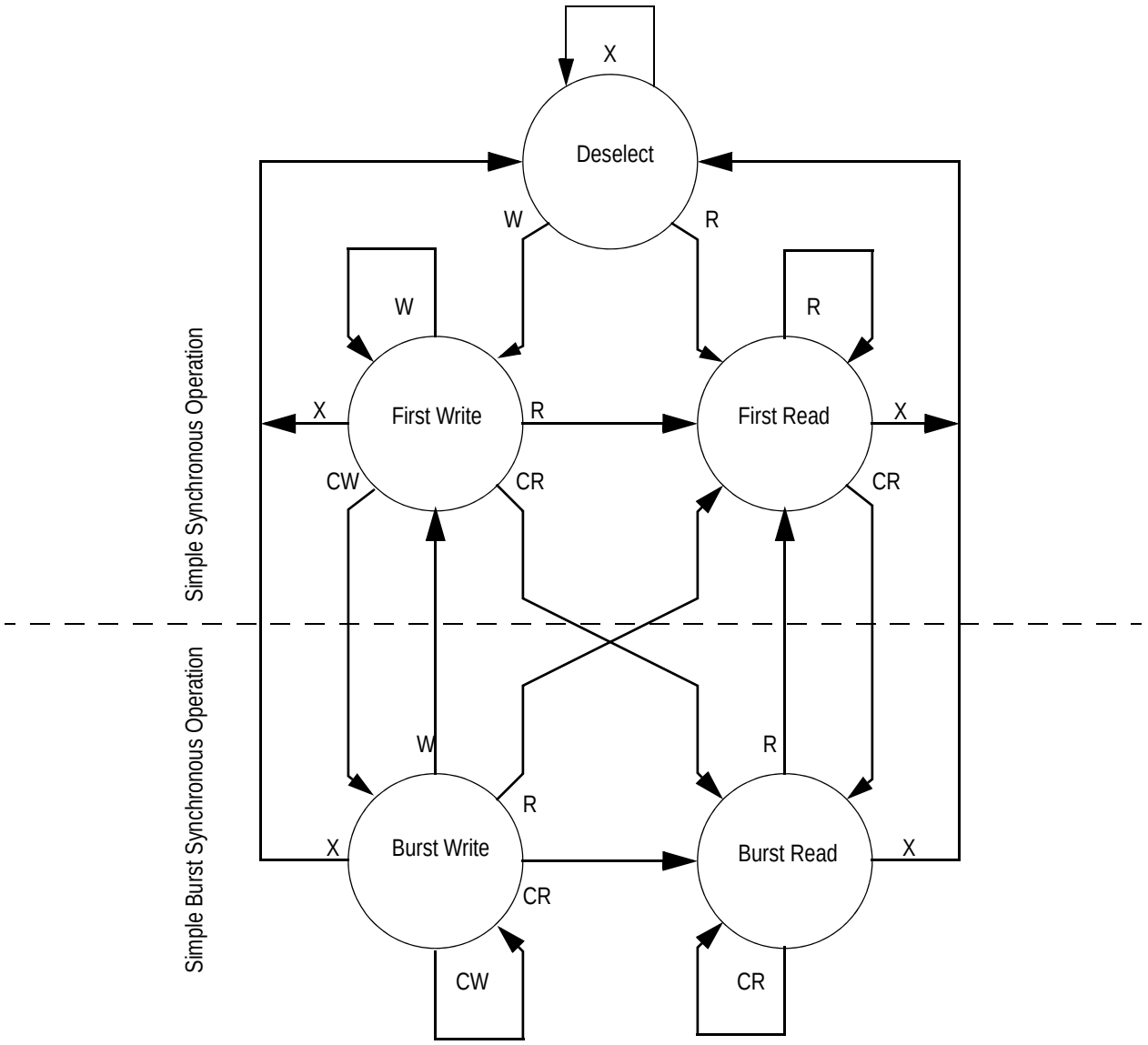
Simplified State Diagram



Notes:
1. The diagram shows only supported (tested) synchronous state transitions. The diagram presumes $\overline{G}$ is tied low.
2. The upper portion of the diagram assumes active use of only the Enable ($\overline{E1}$) and Write ($\overline{B_A}$, $\overline{B_B}$, $\overline{B_C}$, $\overline{B_D}$, $\overline{BW}$, and $\overline{GW}$) control inputs, and that $\overline{ADSP}$ is tied high and $\overline{ADSC}$ is tied low.
3. The upper and lower portions of the diagram together assume active use of only the Enable, Write, and $\overline{ADSC}$ control inputs and assumes $\overline{ADSP}$ is tied high and $\overline{ADV}$ is tied low.

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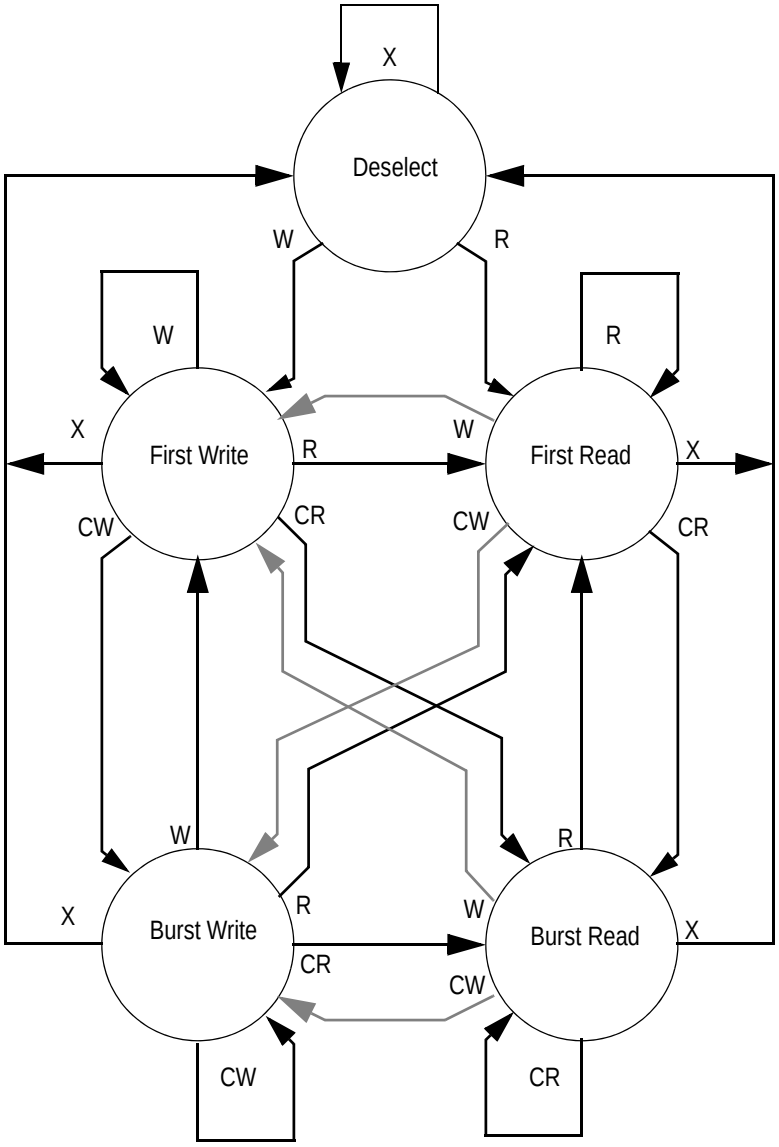
Simplified State Diagram with $\overline{G}$



Notes:

1. The diagram shows supported (tested) synchronous state transitions plus supported transitions that depend upon the use of $\overline{G}$.
2. Use of "Dummy Reads" (Read Cycles with $\overline{G}$ High) may be used to make the transition from read cycles to write cycles without passing through a Deselect cycle. Dummy Read cycles increment the address counter just like normal read cycles.
3. Transitions shown in grey tone assume $\overline{G}$ has been pulsed high long enough to turn the RAM's drivers off and for incoming data to meet Data Input Set Up Time.

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Absolute Maximum Ratings

(All voltages reference to V_{SS})

Symbol	Description	Value	Unit
V_{DD}	Voltage on V_{DD} Pins	–0.5 to 4.6	V
V_{DDQ}	Voltage in V_{DDQ} Pins	–0.5 to 4.6	V
$V_{I/O}$	Voltage on I/O Pins	–0.5 to V_{DDQ} +0.5 (≤ 4.6 V max.)	V
V_{IN}	Voltage on Other Input Pins	–0.5 to V_{DD} +0.5 (≤ 4.6 V max.)	V
I_{IN}	Input Current on Any Pin	+/–20	mA
I_{OUT}	Output Current on Any I/O Pin	+/–20	mA
P_D	Package Power Dissipation	1.5	W
T_{STG}	Storage Temperature	–55 to 125	°C
T_{BIAS}	Temperature Under Bias	–55 to 125	°C

Note:
Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Absolute Maximum Ratings, for an extended period of time, may affect reliability of this component.

Power Supply Voltage Ranges

Parameter	Symbol	Min.	Typ.	Max.	Unit
3.3 V Supply Voltage	V_{DD3}	3.0	3.3	3.6	V
2.5 V Supply Voltage	V_{DD2}	2.3	2.5	2.7	V
3.3 V V_{DDQ} I/O Supply Voltage	V_{DDQ3}	3.0	3.3	3.6	V
2.5 V V_{DDQ} I/O Supply Voltage	V_{DDQ2}	2.3	2.5	2.7	V

V_{DD3} Range Logic Levels

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}	2.0	—	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	–0.3	—	0.8	V

Note:
V_{IHQ} (max) is voltage on V_{DDQ} pins plus 0.3 V.

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V_{DD2} Range Logic Levels

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}	0.6*V_{DD}	—	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	–0.3	—	0.3*V_{DD}	V

Note:
V_{IHQ} (max) is voltage on V_{DDQ} pins plus 0.3 V.

Recommended Operating Temperatures

Parameter	Symbol	Min.	Typ.	Max.	Unit
Junction Temperature (Commercial Range Versions)	T_J	0	25	85	°C
Junction Temperature (Industrial Range Versions)*	T_J	–40	25	100	°C

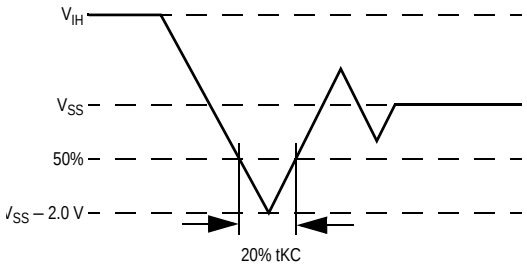
Note:
* The part numbers of Industrial Temperature Range versions end with the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.

Thermal Impedance

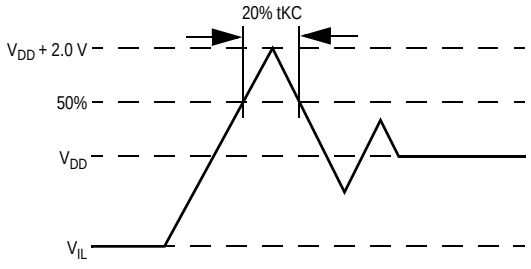
Package	Test PCB Substrate	θ JA (C°/W) Airflow = 0 m/s	θ JA (C°/W) Airflow = 1 m/s	θ JA (C°/W) Airflow = 2 m/s	θ JB (C°/W)	θ JC (C°/W)
119 BGA	4-layer	21.37	17.56	16.42	10.01	1.97
165 BGA	4-layer	20.70	17.51	16.44	9.14	2.96

Notes:
1. Thermal Impedance data is based on a number of samples from multiple lots and should be viewed as a typical number.
2. Please refer to JEDEC standard JESD51-6.
3. The characteristics of the test fixture PCB influence reported thermal characteristics of the device. Be advised that a good thermal path to the PCB can result in cooling or heating of the RAM depending on PCB temperature.

Undershoot Measurement and Timing



Overshoot Measurement and Timing



Note:
Input Under/overshoot voltage must be –2 V > Vi < V_{DDn}+2 V not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tKC.

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Capacitance

(T_A = 25°C, f = 1 MHz, V_{DD} = 2.5 V)

Parameter	Symbol	Test conditions	Typ.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V	4	5	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT} = 0 V	6	7	pF

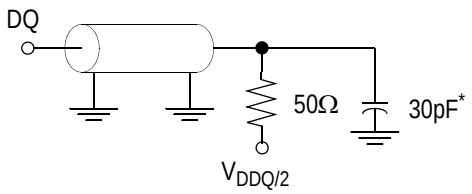
Note:
These parameters are sample tested.

AC Test Conditions

Parameter	Conditions
Input high level	V_{DD} – 0.2 V
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	V_{DD}/2
Output reference level	V_{DDQ}/2
Output load	Fig. 1

Notes:
1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in Fig. 1 unless otherwise noted.
3. Device is deselected as defined by the Truth Table.

Output Load 1



* Distributed Test Jig Capacitance

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DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current (except mode pins)	I_{IL}	V_{IN} = 0 to V_{DD}	–1 uA	1 uA
ZZ Input Current	I_{IN1}	$V_{DD} \geq V_{IN} \geq V_{IH}$ 0 V $\leq V_{IN} \leq V_{IH}$	–1 uA –1 uA	1 uA 100 uA
$\overline{FT}$, SCD, ZQ Input Current	I_{IN2}	$V_{DD} \geq V_{IN} \geq V_{IL}$ 0 V $\leq V_{IN} \leq V_{IL}$	–100 uA –1 uA	1 uA 1 uA
Output Leakage Current	I_{OL}	Output Disable, V_{OUT} = 0 to V_{DD}	–1 uA	1 uA
Output High Voltage	V_{OH2}	I_{OH} = –8 mA, V_{DDQ} = 2.375 V	1.7 V	—
Output High Voltage	V_{OH3}	I_{OH} = –8 mA, V_{DDQ} = 3.135 V	2.4 V	—
Output Low Voltage	V_{OL}	I_{OL} = 8 mA	—	0.4 V

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Operating Currents

Parameter	Test Conditions	Mode		Symbol	-400		-333		-250		-200		Unit
					0 to 85°C	–40 to 100°C	0 to 85°C	–40 to 100°C	0 to 85°C	–40 to 100°C	0 to 85°C	–40 to 100°C	
Operating Current	Device Selected; All other inputs ≥V_{IH} or ≤ V_{IL} Output open	(x32/ x36)	Pipeline	I_{DD}	690	710	600	620	470	490	400	420	mA
			Flow Through	I_{DD}	470	490	435	455	380	375	330	350	mA
		(x18)	Pipeline	I_{DD}	610	630	530	550	430	450	360	380	mA
			Flow Through	I_{DD}	430	450	400	420	360	380	295	315	mA
Standby Current	ZZ ≥ V_{DD} – 0.2 V	—	Pipeline	I_{SB}	100	120	100	120	100	120	100	120	mA
			Flow Through	I_{SB}	100	120	100	120	100	120	100	120	mA
Deselect Current	Device Deselected; All other inputs ≥ V_{IH} or ≤ V_{IL}	—	Pipeline	I_{DD}	130	150	120	140	120	140	120	140	mA
			Flow Through	I_{DD}	130	150	120	140	120	140	120	140	mA

Notes:

1. I_{DD} and I_{DDQ} apply to any combination of V_{DD3}, V_{DD2}, V_{DDQ3}, and V_{DDQ2} operation.
2. All parameters listed are worst case scenario.

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AC Electrical Characteristics

	Parameter	Symbol	-400		-333		-250		-200		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Pipeline	Clock Cycle Time	tKC	2.5	—	3.0	—	4.0	—	5.0	—	ns
	Clock to Output Valid	tKQ	—	2.5	—	2.5	—	2.5	—	3.0	ns
	Clock to Output Invalid	tKQX	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Clock to Output in Low-Z	tLZ[1]	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Setup time	tS	0.9	—	1.0	—	1.2	—	1.4	—	ns
	Hold time	tH	0.1	—	0.1	—	0.2	—	0.4	—	ns
Flow Through	Clock Cycle Time	tKC	4.0	—	4.5	—	5.5	—	6.5	—	ns
	Clock to Output Valid	tKQ	—	4.0	—	4.5	—	5.5	—	6.5	ns
	Clock to Output Invalid	tKQX	2.0	—	2.0	—	2.0	—	2.0	—	ns
	Clock to Output in Low-Z	tLZ[1]	2.0	—	2.0	—	2.0	—	2.0	—	ns
	Setup time	tS	1.2	—	1.3	—	1.5	—	1.5	—	ns
	Hold time	tH	0.2	—	0.3	—	0.5	—	0.5	—	ns
	Clock HIGH Time	tKH	0.9	—	1.0	—	1.3	—	1.3	—	ns
	Clock LOW Time	tKL	1.1	—	1.2	—	1.5	—	1.5	—	ns
	Clock to Output in High-Z	tHZ[1]	1.5	2.5	1.5	2.5	1.5	2.5	1.5	3.0	ns
	$\overline{G}$ to Output Valid	tOE	—	2.5	—	2.5	—	2.5	—	3.0	ns
	$\overline{G}$ to output in Low-Z	tOLZ[1]	0	—	0	—	0	—	0	—	ns
	$\overline{G}$ to output in High-Z	tOHZ[1]	—	2.5	—	2.5	—	2.5	—	3.0	ns
	ZZ setup time	tZZS[2]	5	—	5	—	5	—	5	—	ns
	ZZ hold time	tZZH[2]	1	—	1	—	1	—	1	—	ns
	ZZ recovery	tZZR	20	—	20	—	20	—	20	—	ns

Notes:

1. These parameters are sampled and are not 100% tested.

ZZ is an asynchronous signal. However, in order to be recognized on any given clock cycle, ZZ must meet the specified setup and hold times as specified above

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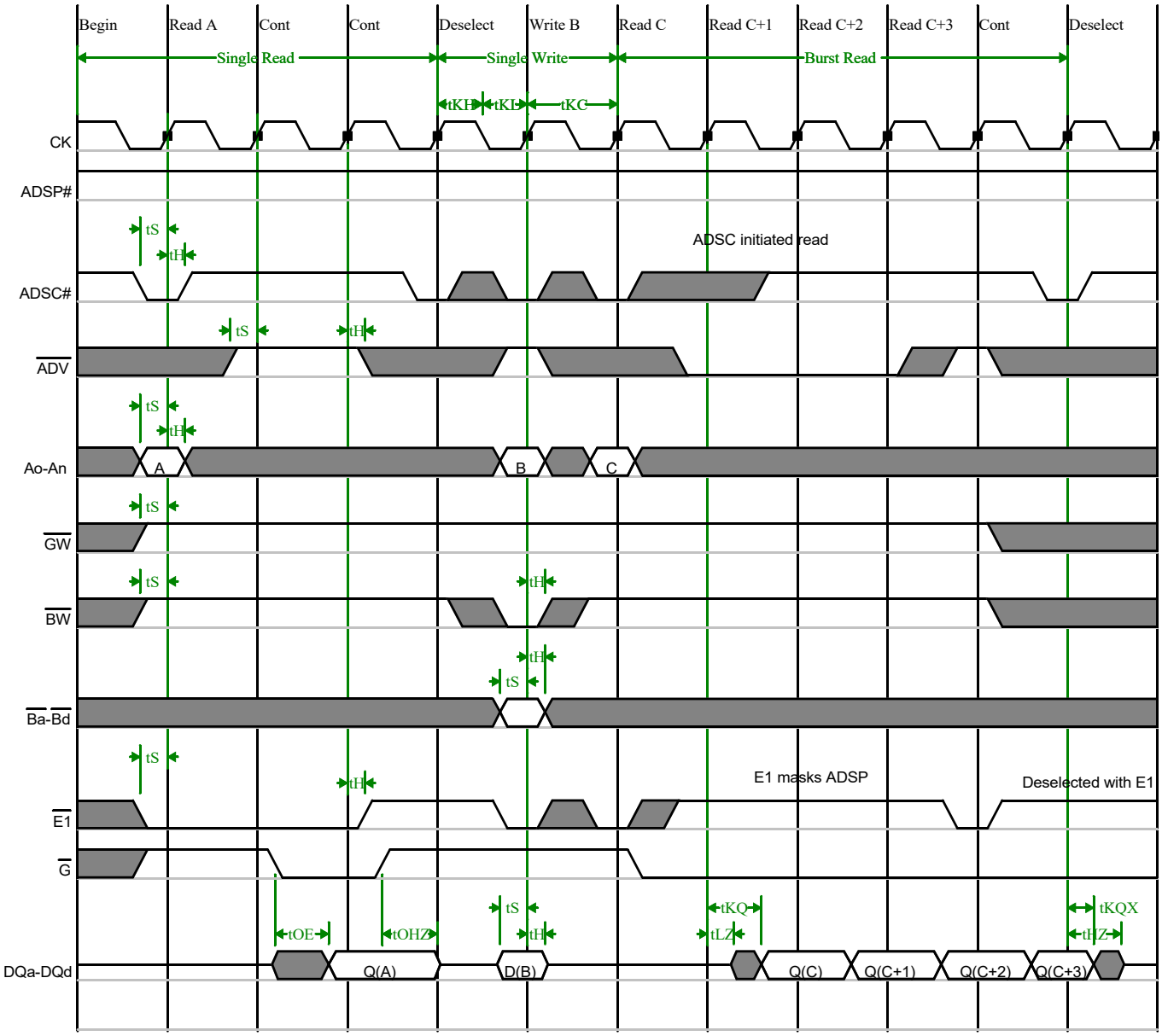
Pipeline Mode Timing (SCD)



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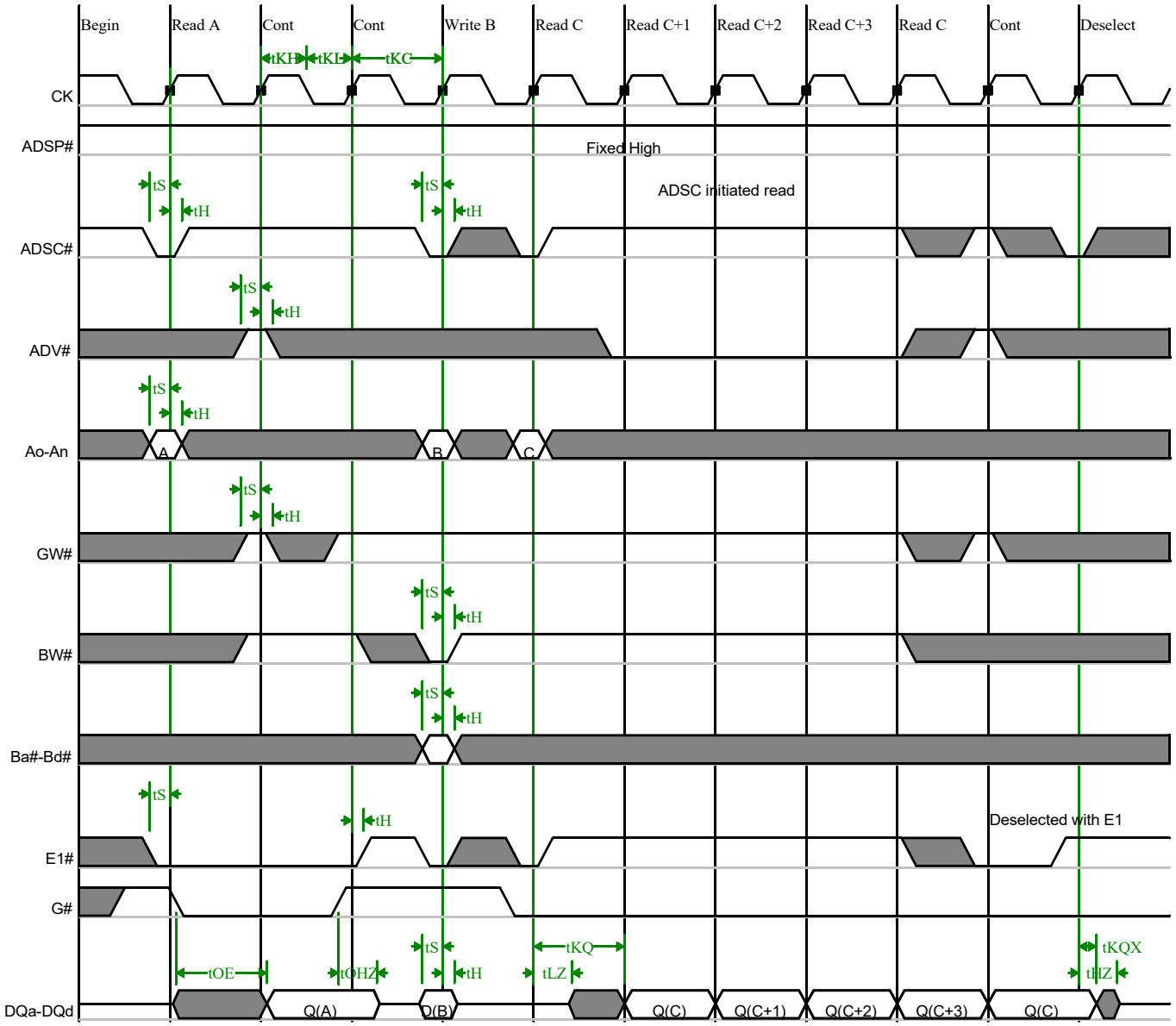
Flow Through Mode Timing (SCD)



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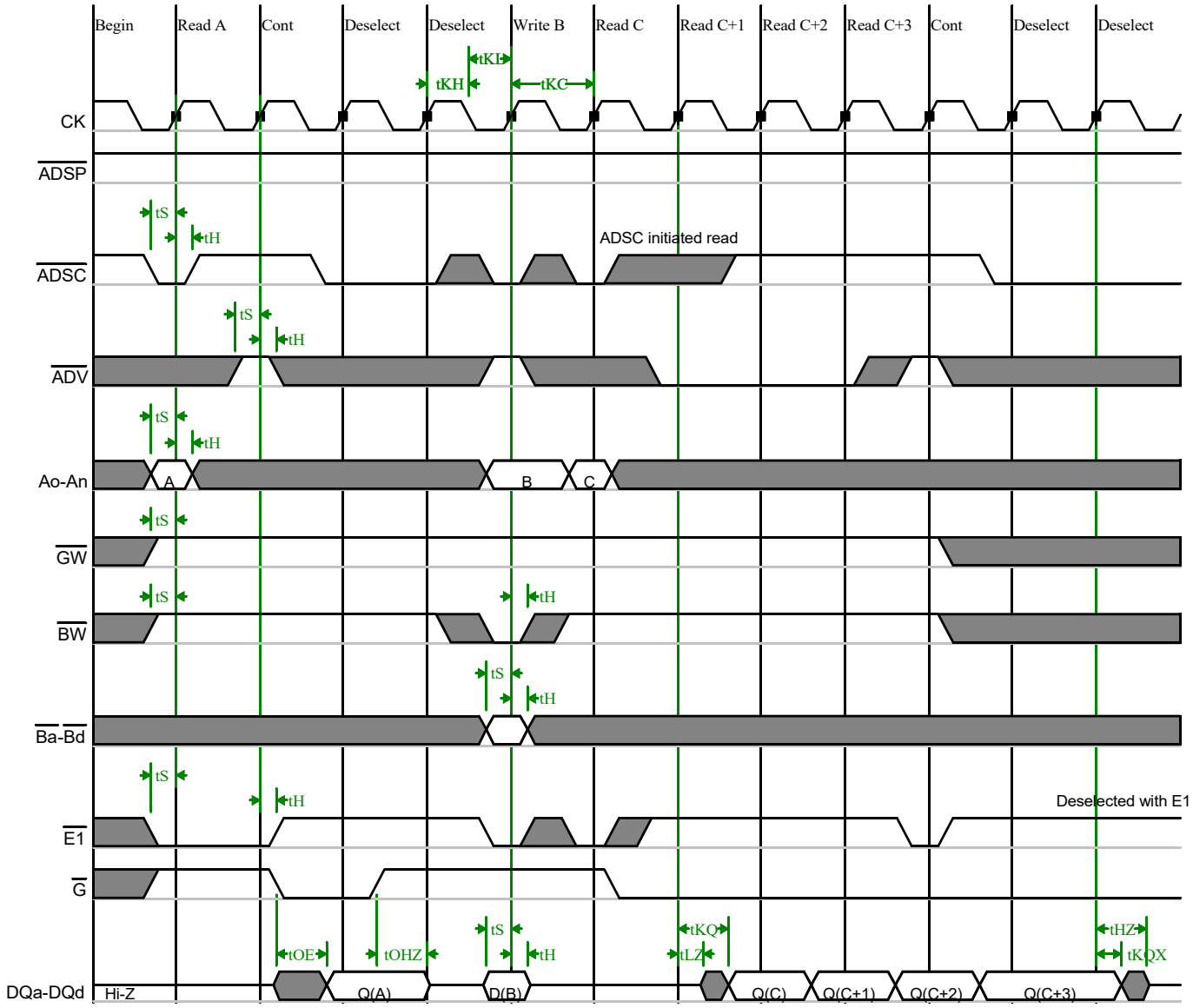
Pipeline Mode Timing (DCD)



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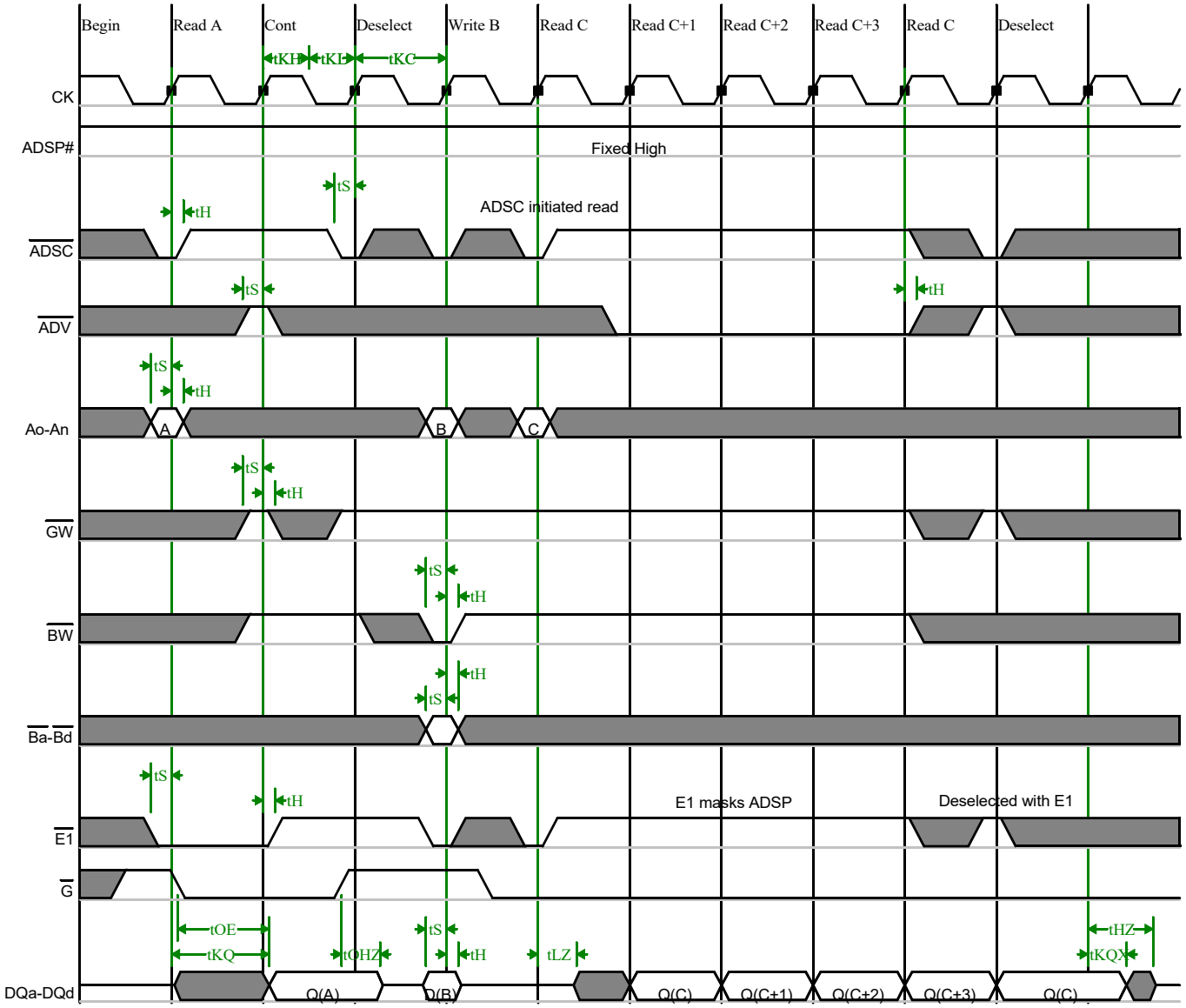
Flow Through Mode Timing (DCD)



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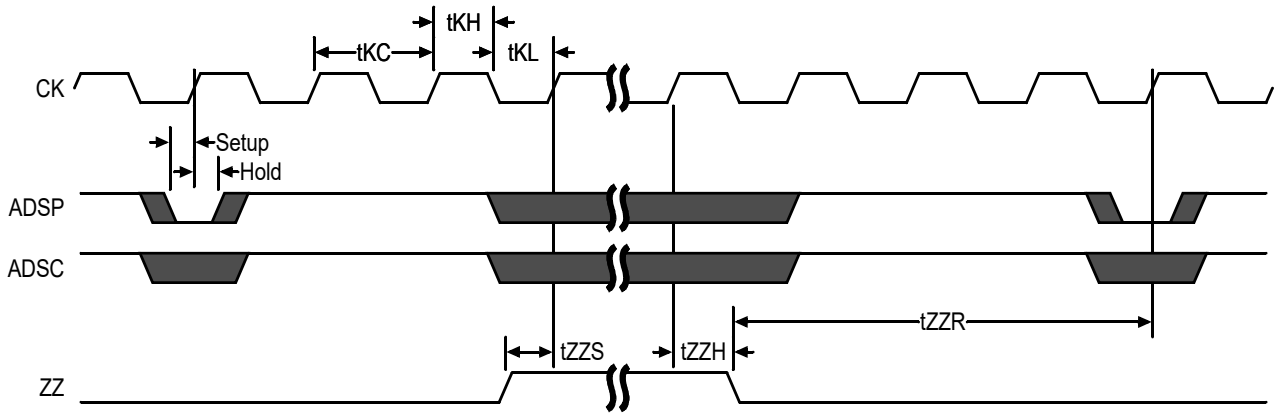
Sleep Mode

During normal operation, ZZ must be pulled low, either by the user or by its internal pull down resistor. When ZZ is pulled high, the SRAM will enter a Power Sleep mode after 2 cycles. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM operates normally after ZZ recovery time.

Sleep mode is a low current, power-down mode in which the device is deselected and current is reduced to $I_{SB}2$. The duration of Sleep mode is dictated by the length of time the ZZ is in a High state. After entering Sleep mode, all inputs except ZZ become disabled and all outputs go to High-Z The ZZ pin is an asynchronous, active high input that causes the device to enter Sleep mode. When the ZZ pin is driven high, $I_{SB}2$ is guaranteed after the time tZZI is met. Because ZZ is an asynchronous input, pending operations or operations in progress may not be properly completed if ZZ is asserted. Therefore, Sleep mode must not be initiated until valid pending operations are completed. Similarly, when exiting Sleep mode during tZZR, only a Deselect or Read commands may be applied while the SRAM is recovering from Sleep mode.

Sleep Mode Timing



Application Tips

Single and Dual Cycle Deselect

SCD devices (like this one) force the use of "dummy read cycles" (read cycles that are launched normally, but that are ended with the output drivers inactive) in a fully synchronous environment. Dummy read cycles waste performance, but their use usually assures there will be no bus contention in transitions from reads to writes or between banks of RAMs. DCD SRAMs do not waste bandwidth on dummy cycles and are logically simpler to manage in a multiple bank application (wait states need not be inserted at bank address boundary crossings), but greater care must be exercised to avoid excessive bus contention.

JTAG Port Operation

Overview

The JTAG Port on this RAM operates in a manner that is compliant with IEEE Standard 1149.1-1990, a serial boundary scan interface standard (commonly referred to as JTAG). The JTAG Port input interface levels scale with V_{DD}. The JTAG output drivers are powered by V_{DDQ}.

Disabling the JTAG Port

It is possible to use this device without utilizing the JTAG port. The port is reset at power-up and will remain inactive unless clocked. TCK, TDI, and TMS are designed with internal pull-up circuits.To assure normal operation of the RAM with the JTAG Port unused, TCK, TDI, and TMS may be left floating or tied to either V_{DD} or V_{SS}. TDO should be left unconnected.

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JTAG Pin Descriptions

Pin	Pin Name	I/O	Description
TCK	Test Clock	In	Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.
TMS	Test Mode Select	In	The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.
TDI	Test Data In	In	The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP Controller state machine and the instruction that is currently loaded in the TAP Instruction Register (refer to the TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.
TDO	Test Data Out	Out	Output that is active depending on the state of the TAP state machine. Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

Note:
This device does not have a TRST (TAP Reset) pin. TRST is optional in IEEE 1149.1. The Test-Logic-Reset state is entered while TMS is held high for five rising edges of TCK. The TAP Controller is also reset automaticly at power-up.

JTAG Port Registers

Overview

The various JTAG registers, refered to as Test Access Port orTAP Registers, are selected (one at a time) via the sequences of 1s and 0s applied to TMS as TCK is strobed. Each of the TAP Registers is a serial shift register that captures serial input data on the rising edge of TCK and pushes serial data out on the next falling edge of TCK. When a register is selected, it is placed between the TDI and TDO pins.

Instruction Register

The Instruction Register holds the instructions that are executed by the TAP controller when it is moved into the Run, Test/Idle, or the various data register states. Instructions are 3 bits long. The Instruction Register can be loaded when it is placed between the TDI and TDO pins. The Instruction Register is automatically preloaded with the IDCODE instruction at power-up or whenever the controller is placed in Test-Logic-Reset state.

Bypass Register

The Bypass Register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAM's JTAG Port to another device in the scan chain with as little delay as possible.

Boundary Scan Register

The Boundary Scan Register is a collection of flip flops that can be preset by the logic level found on the RAM's input or I/O pins. The flip flops are then daisy chained together so the levels found can be shifted serially out of the JTAG Port's TDO pin. The Boundary Scan Register also includes a number of place holder flip flops (always set to a logic 1). The relationship between the device pins and the bits in the Boundary Scan Register is described in the Scan Order Table following. The Boundary Scan Register, under the control of the TAP Controller, is loaded with the contents of the RAMs I/O ring when the controller is in Capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to Shift-DR state. SAMPLE-Z, SAMPLE/PRELOAD and EXTEST instructions can be used to activate the Boundary Scan Register.

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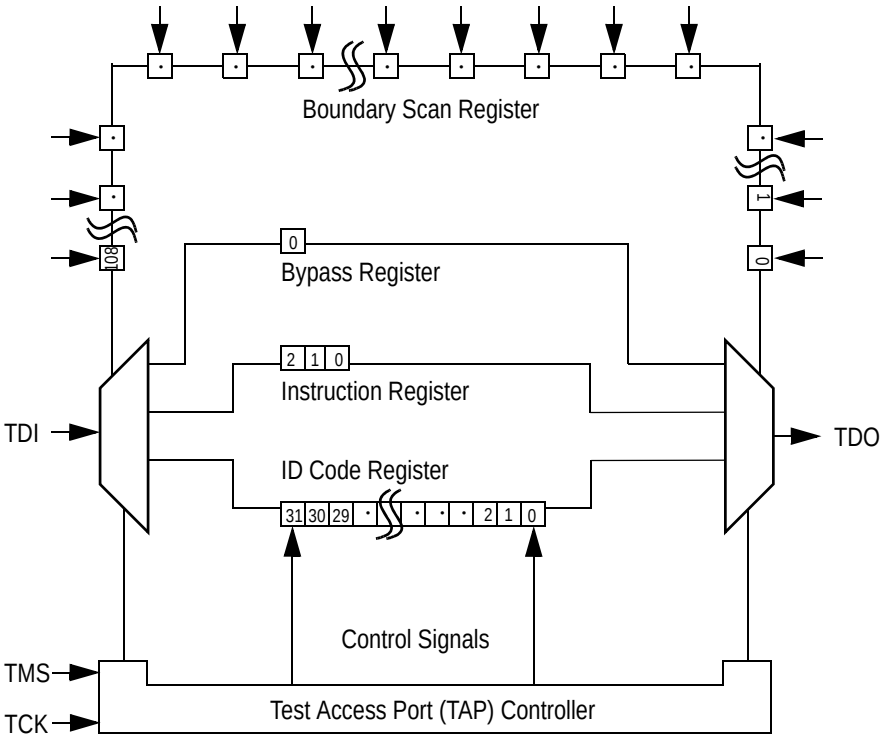
JTAG TAP Block Diagram



Identification (ID) Register

The ID Register is a 32-bit register that is loaded with a device and vendor specific 32-bit code when the controller is put in Capture-DR state with the IDCODE command loaded in the Instruction Register. The code is loaded from a 32-bit on-chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into Shift-DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID Register Contents

	Not Used																			GSI Technology JEDEC Vendor ID Code										Presence Register
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0	1	1	0	1	1	0	0	1	1

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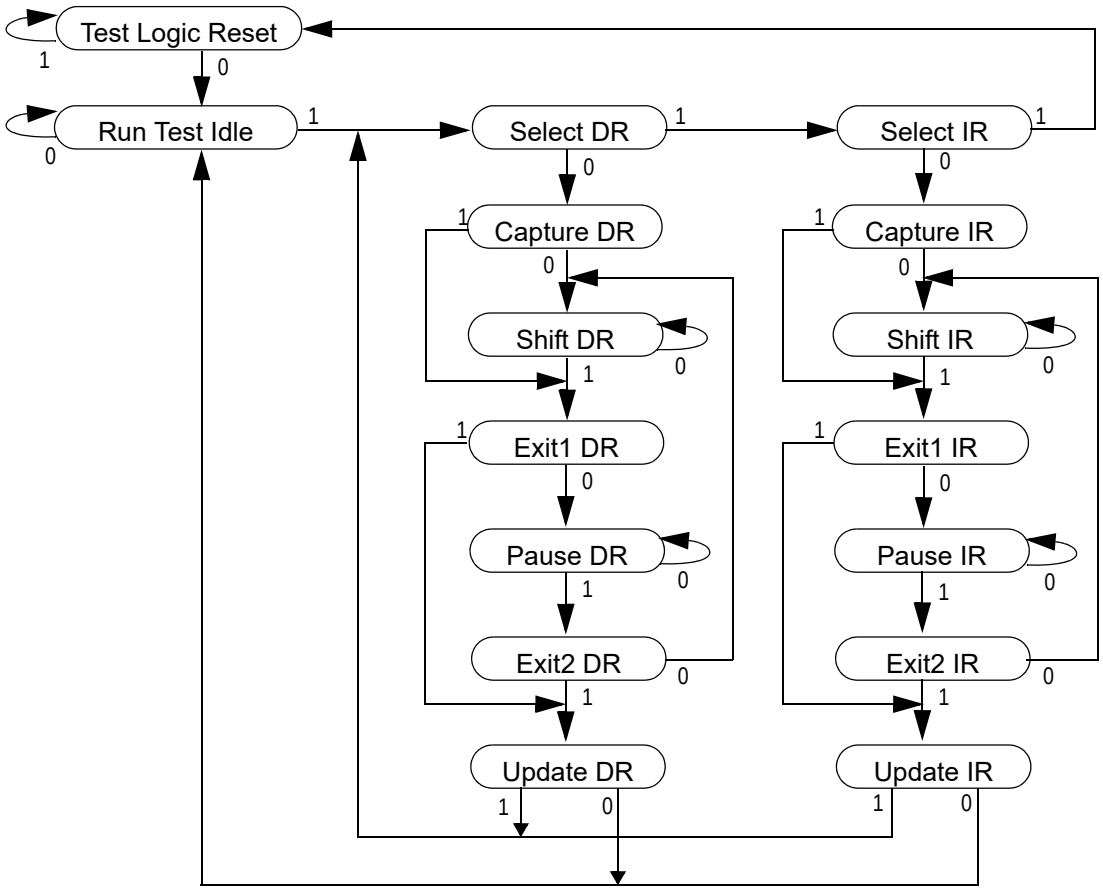
Tap Controller Instruction Set

Overview

There are two classes of instructions defined in the Standard 1149.1-1990; the standard (Public) instructions, and device specific (Private) instructions. Some Public instructions are mandatory for 1149.1 compliance. Optional Public instructions must be implemented in prescribed ways. The TAP on this device may be used to monitor all input and I/O pads, and can be used to load address, data or control signals into the RAM or to preload the I/O buffers.

When the TAP controller is placed in Capture-IR state the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the Shift-IR state the Instruction Register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to Update-IR state. The TAP instruction set for this device is listed in the following table.

JTAG Tap Controller State Diagram



Instruction Descriptions

BYPASS

When the BYPASS instruction is loaded in the Instruction Register the Bypass Register is placed between TDI and TDO. This occurs when the TAP controller is moved to the Shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a Standard 1149.1 mandatory public instruction. When the SAMPLE / PRELOAD instruction is

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loaded in the Instruction Register, moving the TAP controller into the Capture-DR state loads the data in the RAMs input and I/O buffers into the Boundary Scan Register. Boundary Scan Register locations are not associated with an input or I/O pin, and are loaded with the default state identified in the Boundary Scan Chain table at the end of this section of the datasheet. Because the RAM clock is independent from the TAP Clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture set-up plus hold time (tTS plus tTH). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the Boundary Scan Register. Moving the controller to Shift-DR state then places the boundary scan register between the TDI and TDO pins.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register is loaded with all logic 0s. The EXTEST command does not block or override the RAM's input pins; therefore, the RAM's internal state is still determined by its input pins.

Typically, the Boundary Scan Register is loaded with the desired pattern of data with the SAMPLE/PRELOAD command. Then the EXTEST command is used to output the Boundary Scan Register's contents, in parallel, on the RAM's data output drivers on the falling edge of TCK when the controller is in the Update-IR state.

Alternately, the Boundary Scan Register may be loaded in parallel using the EXTEST command. When the EXTEST instruction is selected, the sate of all the RAM's input and I/O pins, as well as the default values at Scan Register locations not associated with a pin, are transferred in parallel into the Boundary Scan Register on the rising edge of TCK in the Capture-DR state, the RAM's output pins drive out the value of the Boundary Scan Register location with which each output pin is associated.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in Capture-DR mode and places the ID register between the TDI and TDO pins in Shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the Test-Logic-Reset state.

SAMPLE-Z

If the SAMPLE-Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high-Z) and the Boundary Scan Register is connected between TDI and TDO when the TAP controller is moved to the Shift-DR state.

RFU

These instructions are Reserved for Future Use. In this device they replicate the BYPASS instruction.

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JTAG TAP Instruction Set Summary

Instruction	Code	Description	Notes
EXTEST	000	Places the Boundary Scan Register between TDI and TDO.	1
IDCODE	001	Preloads ID Register and places it between TDI and TDO.	1, 2
SAMPLE-Z	010	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO. Forces all RAM output drivers to High-Z.	1
RFU	011	Do not use this instruction; Reserved for Future Use. Replicates BYPASS instruction. Places Bypass Register between TDI and TDO.	1
SAMPLE/ PRELOAD	100	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO.	1
GSI	101	GSI private instruction.	1
RFU	110	Do not use this instruction; Reserved for Future Use. Replicates BYPASS instruction. Places Bypass Register between TDI and TDO.	1
BYPASS	111	Places Bypass Register between TDI and TDO.	1

Notes:
1. Instruction codes expressed in binary, MSB on left, LSB on right.
2. Default instruction automatically loaded at power-up and in test-logic-reset state.

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JTAG Port Recommended Operating Conditions and DC Characteristics

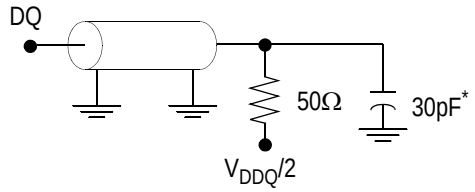
Parameter	Symbol	Min.	Max.	Unit	Notes
3.3 V Test Port Input High Voltage	V_{IHJ3}	2.0	V_{DD3} +0.3	V	1
3.3 V Test Port Input Low Voltage	V_{ILJ3}	–0.3	0.8	V	1
2.5 V Test Port Input High Voltage	V_{IHJ2}	0.6 * V_{DD2}	V_{DD2} +0.3	V	1
2.5 V Test Port Input Low Voltage	V_{ILJ2}	–0.3	0.3 * V_{DD2}	V	1
TMS, TCK and TDI Input Leakage Current	I_{INHJ}	–300	1	uA	2
TMS, TCK and TDI Input Leakage Current	I_{INLJ}	–1	100	uA	3
TDO Output Leakage Current	I_{OLJ}	–1	1	uA	4
Test Port Output High Voltage	V_{OHJ}	1.7	—	V	5, 6
Test Port Output Low Voltage	V_{OLJ}	—	0.4	V	5, 7
Test Port Output CMOS High	V_{OHJC}	V_{DDQ} – 100 mV	—	V	5, 8
Test Port Output CMOS Low	V_{OLJC}	—	100 mV	V	5, 9

Notes:
1. Input Under/overshoot voltage must be –2 V < Vi < V_{DDn} +2 V not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tTKC.
2. $V_{ILJ} \le V_{IN} \le V_{DDn}$
3. $0\ V \le V_{IN} \le V_{ILJn}$
4. Output Disable, V_{OUT} = 0 to V_{DDn}
5. The TDO output driver is served by the V_{DDQ} supply.
6. I_{OHJ} = –4 mA
7. I_{OLJ} = + 4 mA
8. I_{OHJC} = –100 uA
9. I_{OLJC} = +100 uA

JTAG Port AC Test Conditions

Parameter	Conditions
Input high level	V_{DD} – 0.2 V
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	$V_{DDQ}/2$
Output reference level	$V_{DDQ}/2$

JTAG Port AC Test Load



* Distributed Test Jig Capacitance

Notes:
1. Include scope and jig capacitance.
2. Test conditions as shown unless otherwise noted.

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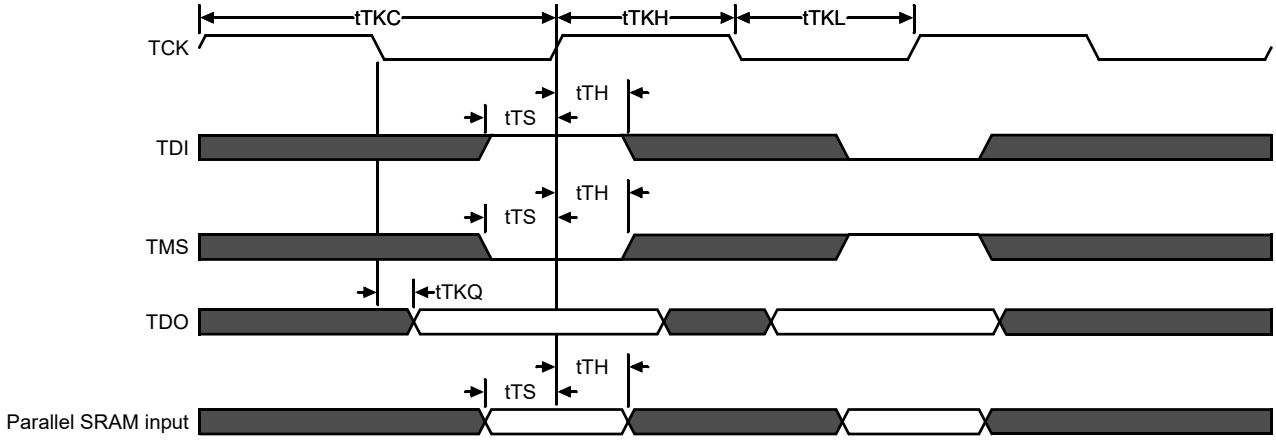
JTAG Port Timing Diagram



JTAG Port AC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
TCK Cycle Time	tTKC	50	—	ns
TCK Low to TDO Valid	tTKQ	—	20	ns
TCK High Pulse Width	tTKH	20	—	ns
TCK Low Pulse Width	tTKL	20	—	ns
TDI & TMS Set Up Time	tTS	10	—	ns
TDI & TMS Hold Time	tTH	10	—	ns

Boundary Scan (BSDL Files)

For information regarding the Boundary Scan Chain, or to obtain BSDL files for this part, please contact our Applications Engineering Department at: apps@gsitechnology.com.

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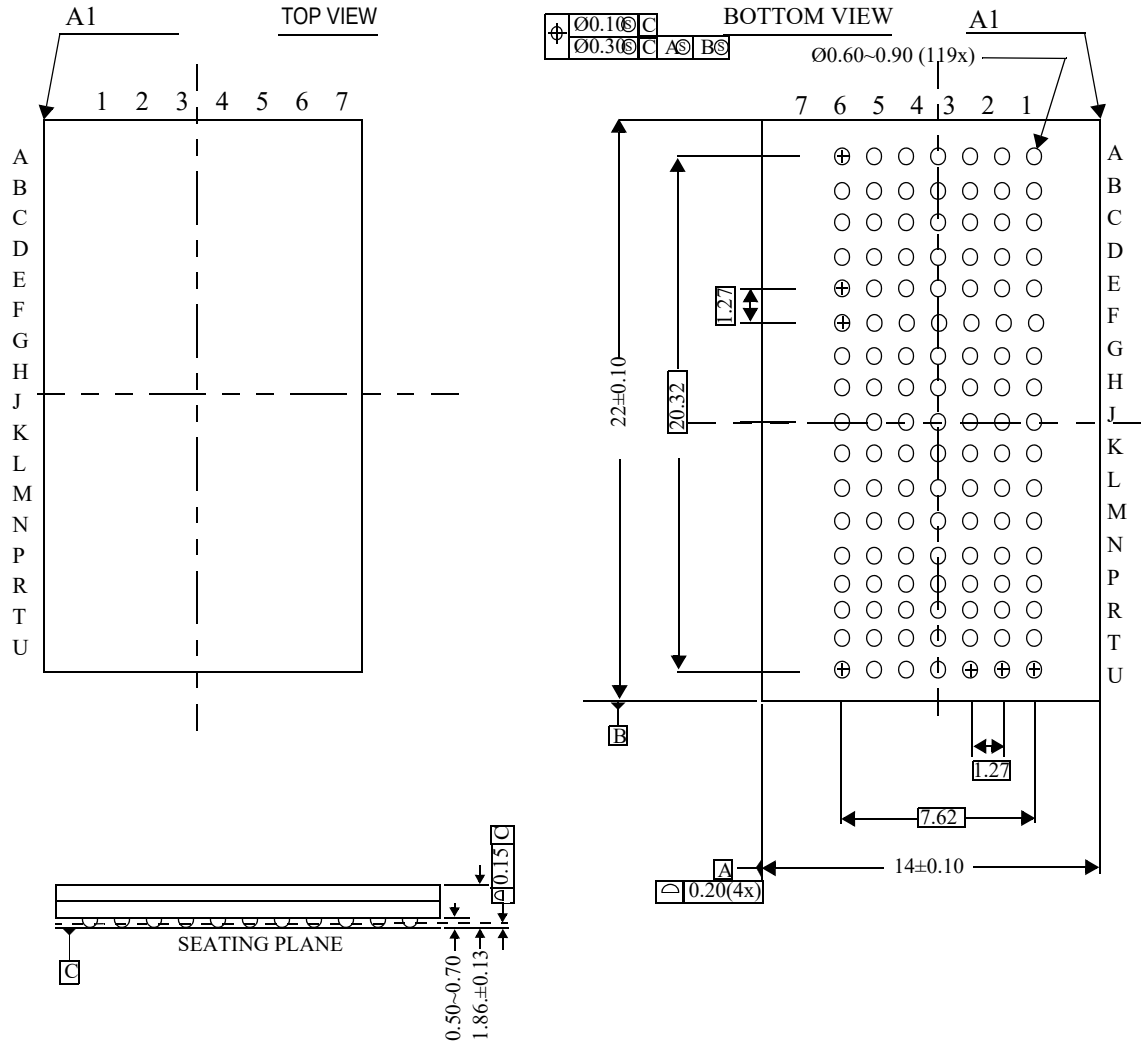
Package Dimensions—119-Bump FPBGA (Package B, Variation 2)



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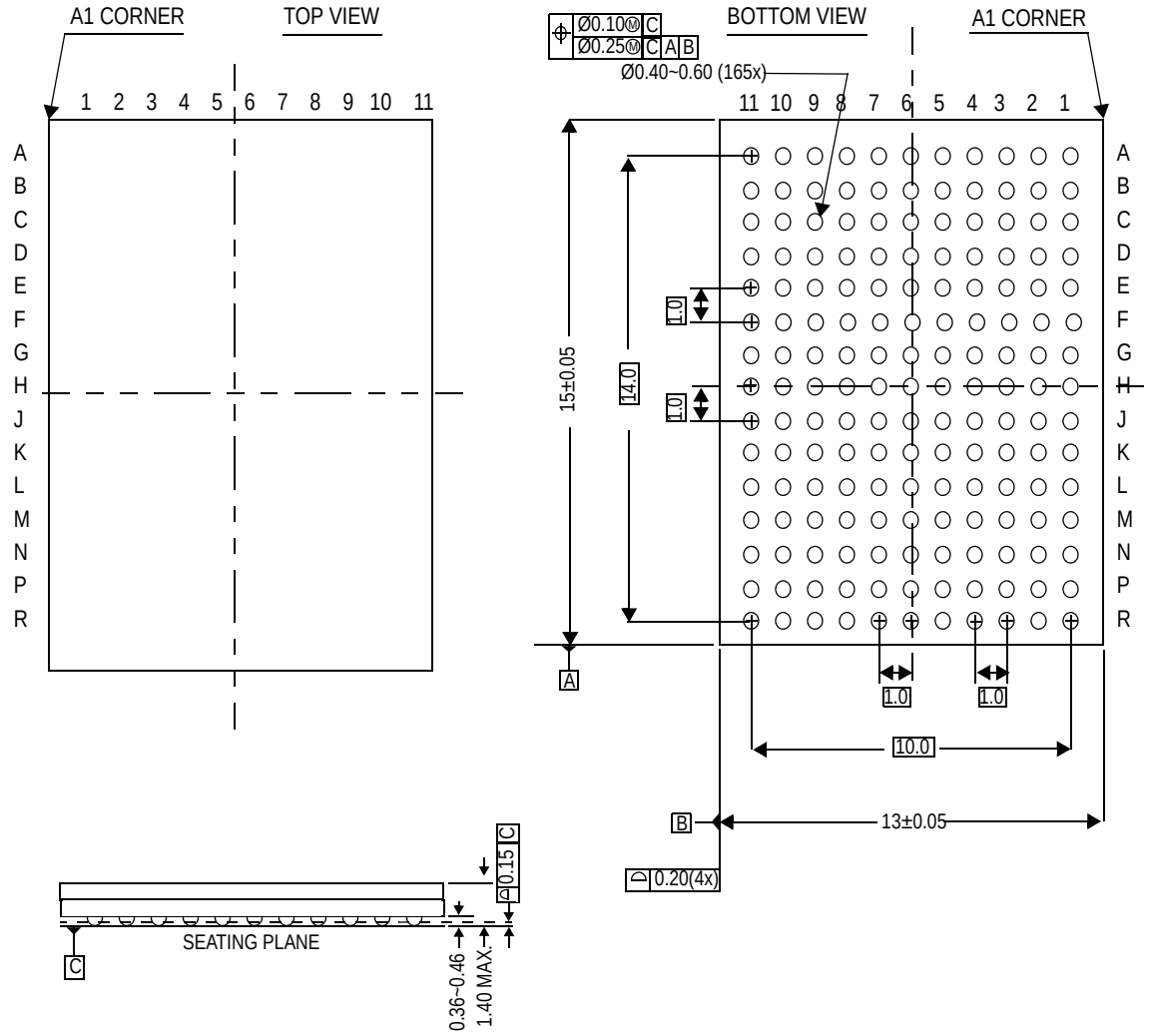
Package Dimensions—165-Bump FPBGA (Package D)



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Ordering Information for GSI Synchronous Burst RAMs

Org	Part Number[1]	Type	Package	Speed[2] (MHz/ns)	T_J[3]
8M x 18	GS8128218GB-400	SCD/DCD; PL/FT	RoHS-compliant 119 BGA (var.2)	400/4.0	C
8M x 18	GS8128218GB-333	SCD/DCD; PL/FT	RoHS-compliant 119 BGA (var.2)	333/4.5	C
8M x 18	GS8128218GB-250	SCD/DCD; PL/FT	RoHS-compliant 119 BGA (var.2)	250/5.5	C
8M x 18	GS8128218GB-200	SCD/DCD; PL/FT	RoHS-compliant 119 BGA (var.2)	200/6.5	C
4M x 36	GS8128236GB-400	SCD/DCD; PL/FT	RoHS-compliant 119 BGA (var.2)	400/4.0	C
4M x 36	GS8128236GB-333	SCD/DCD; PL/FT	RoHS-compliant 119 BGA (var.2)	333/4.5	C
4M x 36	GS8128236GB-250	SCD/DCD; PL/FT	RoHS-compliant 119 BGA (var.2)	250/5.5	C
4M x 36	GS8128236GB-200	SCD/DCD; PL/FT	RoHS-compliant 119 BGA (var.2)	200/6.5	C
8M x 18	GS8128218GB-400I	SCD/DCD; PL/FT	RoHS-compliant 119 BGA (var.2)	400/4.0	I
8M x 18	GS8128218GB-333I	SCD/DCD; PL/FT	RoHS-compliant 119 BGA (var.2)	333/4.5	I
8M x 18	GS1284218GB-250I	SCD/DCD; PL/FT	RoHS-compliant 119 BGA (var.2)	250/5.5	I
8M x 18	GS8128218GB-200I	SCD/DCD; PL/FT	RoHS-compliant 119 BGA (var.2)	200/6.5	I
4M x 36	GS8128236GB-400I	SCD/DCD; PL/FT	RoHS-compliant 119 BGA (var.2)	400/4.0	I
4M x 36	GS8128236GB-333I	SCD/DCD; PL/FT	RoHS-compliant 119 BGA (var.2)	333/4.5	I
4M x 36	GS8128236GB-250I	SCD/DCD; PL/FT	RoHS-compliant 119 BGA (var.2)	250/5.5	I
4M x 36	GS8128236GB-200I	SCD/DCD; PL/FT	RoHS-compliant 119 BGA (var.2)	200/6.5	I
8M x 18	GS8128218GD-400	SCD/DCD; PL/FT	RoHS-compliant 165 BGA	400/4.0	C
8M x 18	GS8128218GD-333	SCD/DCD; PL/FT	RoHS-compliant 165 BGA	333/4.5	C
8M x 18	GS8128218GD-250	SCD/DCD; PL/FT	RoHS-compliant 165 BGA	250/5.5	C
8M x 18	GS8128218GD-200	SCD/DCD; PL/FT	RoHS-compliant 165 BGA	200/6.5	C
4M x 36	GS8128236GD-400	SCD/DCD; PL/FT	RoHS-compliant 165 BGA	400/4.0	C
4M x 36	GS8128236GD-333	SCD/DCD; PL/FT	RoHS-compliant 165 BGA	333/4.5	C
4M x 36	GS8128236GD-250	SCD/DCD; PL/FT	RoHS-compliant 165 BGA	250/5.5	C
4M x 36	GS8128236GD-200	SCD/DCD; PL/FT	RoHS-compliant 165 BGA	200/6.5	C
8M x 18	GS8128218GD-400I	SCD/DCD; PL/FT	RoHS-compliant 165 BGA	400/4.0	I
8M x 18	GS8128218GD-333I	SCD/DCD; PL/FT	RoHS-compliant 165 BGA	333/4.5	I

Notes:

1. Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS8128218GB-200IT.
2. The speed column indicates the cycle frequency (MHz) of the device in Pipeline mode and the latency (ns) in Flow Through mode. Each device is Pipeline/ Flow Through mode-selectable by the user.
3. C = Commercial Temperature Range. I = Industrial Temperature Range.
4. GSI offers other versions this type of device in many different configurations and with a variety of different features, only some of which are covered in this data sheet. See the GSI Technology web site (www.gsitechnology.com) for a complete listing of current offerings.

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Ordering Information for GSI Synchronous Burst RAMs (Continued)

Org	Part Number[1]	Type	Package	Speed[2] (MHz/ns)	T_J[3]
8M x 18	GS1284218GD-250I	SCD/DCD; PL/FT	RoHS-compliant 165 BGA	250/5.5	I
8M x 18	GS8128218GD-200I	SCD/DCD; PL/FT	RoHS-compliant 165 BGA	200/6.5	I
4M x 36	GS8128236GD-400I	SCD/DCD; PL/FT	RoHS-compliant 165 BGA	400/4.0	I
4M x 36	GS8128236GD-333I	SCD/DCD; PL/FT	RoHS-compliant 165 BGA	333/4.5	I
4M x 36	GS8128236GD-250I	SCD/DCD; PL/FT	RoHS-compliant 165 BGA	250/5.5	I
4M x 36	GS8128236GD-200I	SCD/DCD; PL/FT	RoHS-compliant 165 BGA	200/6.5	I

Notes:

1. Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS8128218GB-200IT.
2. The speed column indicates the cycle frequency (MHz) of the device in Pipeline mode and the latency (ns) in Flow Through mode. Each device is Pipeline/ Flow Through mode-selectable by the user.
3. C = Commercial Temperature Range. I = Industrial Temperature Range.
4. GSI offers other versions this type of device in many different configurations and with a variety of different features, only some of which are covered in this data sheet. See the GSI Technology web site (www.gsitechnology.com) for a complete listing of current offerings.

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144Mb Sync SRAM Datasheet Revision History

DS/DateRev. Code: Old; New	Types of Changes Format or Content	Page;Revisions;Reason
81282xx_r1		• Creation of new datasheet
81282xx_r1_01	Content	• Updated for MP status • (Rev1.01a: Updated incorrect op current data for x36 FT @ 250 MHz)

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