Features

- **Compatible with the JPEG Baseline Standard as Defined by ISO IS 109 18-1**
- **Highly-integrated, Low-cost Single Chip Solution**
- **Up to 40 Mbytes/sec Sustained Compression Rate**
- **Maximum Processing Rate of 1.6 million pixels/sec**
- **Supports 8-bit Grayscale and YUV 4:2:2 Color Space Input and Output Formats**
- **Handles Images of Size up to 1024 x 1024 Pixels**
- **Fast DCT/IDCT Processor On-chip**
- **User-defined Quantization and Huffman Tables**
- **Support for Fast as well as Slow/Inexpensive Memories**
- **Provides Direct Interface for Microcontroller/Microprocessor Access**

Applications

The AT76C101 JPEG Processor is optimized for use in the following applications:

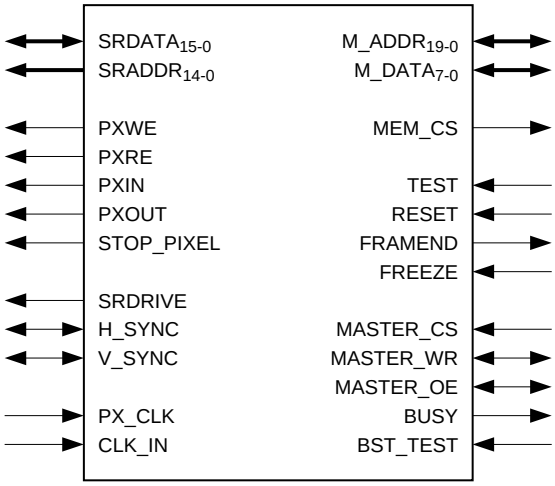
- Digital Cameras
- Color Printers and Plotters
- Low-cost Image Compression Systems
- Video Editing (3-4 frames/sec at CCIR 720 x 480 Image Resolution)

Hardware Resources

- On-chip Video Interface
- Custom Discrete Cosine Transform and Quantization Processor
- Variable Length and Huffman Encoder/Decoder
- Programmable Memory Interface (Supports Slow Memories)
- Microcontroller/Microprocessor Access Bus

Pin Configuration

100-Pin QFP



JPEG Image Compression Processor

AT76C101

Rev. 0751A–04/98

Description

The AT76C101 is an Image Compression/Decompression Processor that performs the JPEG Baseline Algorithm. The system is capable of high quality compression and decompression of continues-tone color or monochrome images. The AT76C101 performs the Discrete Cosine Transform, Quantization, and Entropy Encoding during the compression stage and carries out all inverse operations during the decompression phase. The AT76C101 uses an external SRAM as working memory, which is accessed by an on-chip video interface.

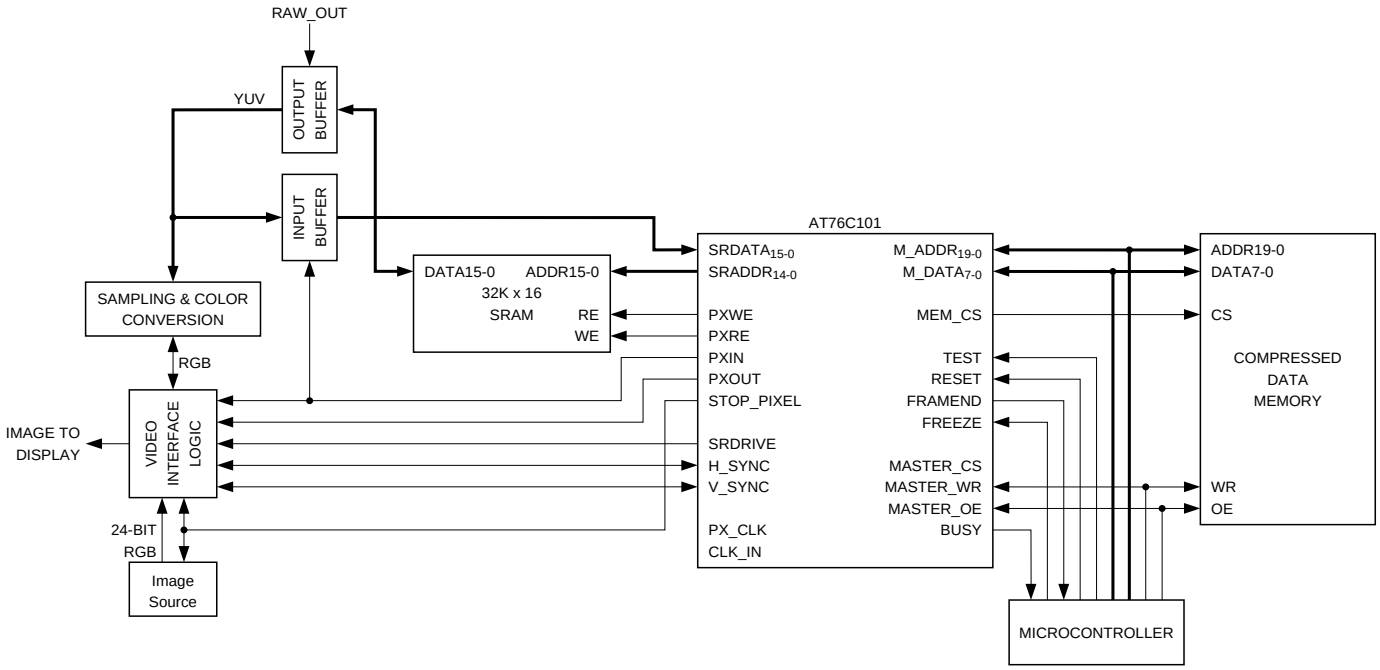
The AT76C101 is designed to operate with minimum host intervention. A host processor is required to program the chip in the required operating mode, and to extract the JPEG header from the compressed bit stream during the decompression phase. Based on this information, it then initializes the internal registers. Once the chip has been initialized, the AT76C101 operates continuously until it has completed compression/decompression of a image frame. The image compression ratio is controlled by the user supplied quantization tables, which are loaded before the compression/decompression operation. Compression ratios from 1:1 to 50:1 are possible depending on the quality and storage requirements of the application.

Basic System Configuration

An AT76C101-based image compression system is shown in Figure 1. The AT76C101 requires the following external devices:

- A microcontroller to program and initialize the chip in the required operating mode. This device is also used to strip the JPEG header during decompression and to provide the AT76C101 with the header information.
- An external working memory (SRAM) for handling uncompressed/decompressed images. The size of this memory depends on the size of the image being processed. The formula to assess the memory size is given in the Pixel Interface section of this manual.
- An external memory device to store the compressed data stream. This external memory can be either a fast memory or a slow inexpensive memory. The size of this memory depends on the needs of the specific application.

Figure 1. AT76C101-based Image Compression System



System Overview

Pixel Interface

The pixel interface is used to input uncompressed data during the compression mode, or to output decompressed data during the decompression mode. The AT76C101 expects uncompressed image data either in YUV 4:2:2 (for color images), or in grayscale format. During decompression, the AT76C101 generates images in the same format.

This interface requires an external buffer as working memory (Figure 2). During compression, the external buffer is used to store the incoming pixels. After 8 scan lines are read in, the AT76C101 performs a raster to 8x8 block conversion of the input data. During the inverse operation, the AT76C101 converts the outgoing pixels into the raster format and stores them in the external buffer. The uncompressed data is synchronized with the PX_CLK signal. This clock runs at twice the pixel rate so that two transfers can occur for each pixel, one to read pixel data from the external SRAM and one to write pixel data to the external SRAM.

Two signals synchronize video interface operation, HSync and VSync. These are active low, bi-directional signals and they are controlled from the Master bit of the Mode register of the chip. When Master is high, HSync and VSync are generated and driven by the chip. When Master is low, these two signals are read as inputs by the chip. In Master mode, the registers HPeriod, HSyncWidth, VPeriod, and VSyncWidth are used to generate HSync and VSync. HPeriod contains the total number of pixels per scan line, and HSyncWidth, the width of active HSync in number of pixels. VPeriod and VSyncWidth provide the same type of information for VSync in terms of scan lines, rather than pixels.

These registers and others are used to control the video interface of the chip. The other registers are HDelay, HActive, VDelay, and VActive. HDelay contains the number of pixels between falling HSync and the first active pixel of a line. HActive contains the number of active blocks in a line.

The size of the working memory depends on the size of the image being processed. The external buffer should be deep enough to store 16 scan lines of data at the highest horizontal resolution. The equations for determining the external buffer size are:

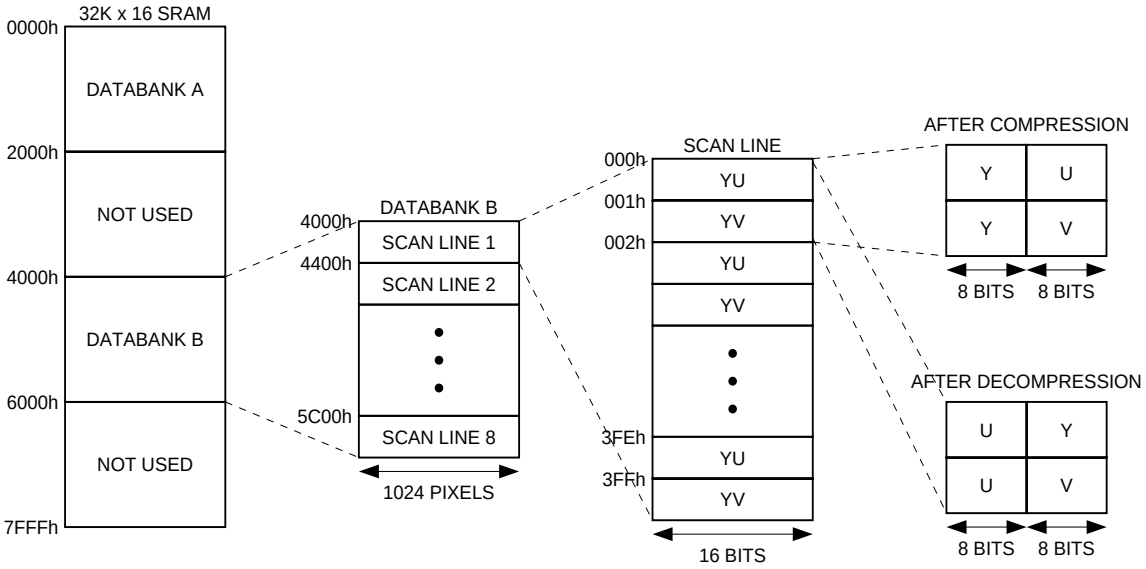
- Buffer bus width = 16 bits [For YUV data], 8 bits [For Grayscale data]
- Buffer size = 16 x (No. of pixels per line)

As an example, a system designed to process images of the maximum size of 1024 x 1024 pixels would have the following external buffer requirements:

- Buffer size = 16 x 1024 = 16,384 words

Thus, this system would require 16K x 16 working memory to process YUV images (color) and 16K x 8 working memory to process grayscale images. As the minimum size of available SRAM is 32K x 8, the SRAM requirements are as follows: YUV/grayscale images: two 32K x 8 SRAM's to form a 32K x 16 SRAM.

Figure 2. Memory Organization



SRAM ORGANIZATION FOR MAXIMUM SCAN LINE SIZE OF 1024 PIXELS.
EACH DATABANK STORES 8 SCAN LINES OF THE RAW IMAGE.

Host Interface

This is a 8-bit interface that allows the AT76C101 to transfer the compressed data to an external memory device. This interfaces also allows an external microcontroller/microprocessor (complexity of AT89C51) to access the internal memory (registers and tables) of the AT76C101. Two types of transfers can be carried out through this interface: the compressed data transfers and the microcontroller data accesses.

Compressed Data Mode

The host interface can work with a number of external memory devices. It has two programmable registers through which the user can specify up to eight wait states that allows the chip to interface with slow memory devices. Data transfers are 8 bit wide and are carried out through the Data Bus, Address Bus and the control signals MEM_CS, MASTER_OE and MASTER_WR. The AT76C101 is the bus master and controls all transfers to the external memory. Other devices cannot access the memory while the AT76C101 is in the operating mode.

The cycle time of the compressed data transfer varies from one to eight CLK cycles. This cycle time is controlled by two registers, the Read_Cnt_Reg which controls the read cycle time, and Write_Cnt_Reg which controls the write cycle time. These registers are programmed by the microcontroller during initialization. The address bus is also initialized from the Mem_Start_Addr register, which holds the start address of the compressed data memory.

Microcontroller Access Mode

In this mode, the main function of the host interface is to allow external devices, (i.e. microcontroller or a host processor) to access the internal memory of the JPEG chip. This is required to program the AT76C101 in the desired mode of operation, to load the internal quantization and Huffman tables during initialization, and to read the status of the chip for testing purposes.

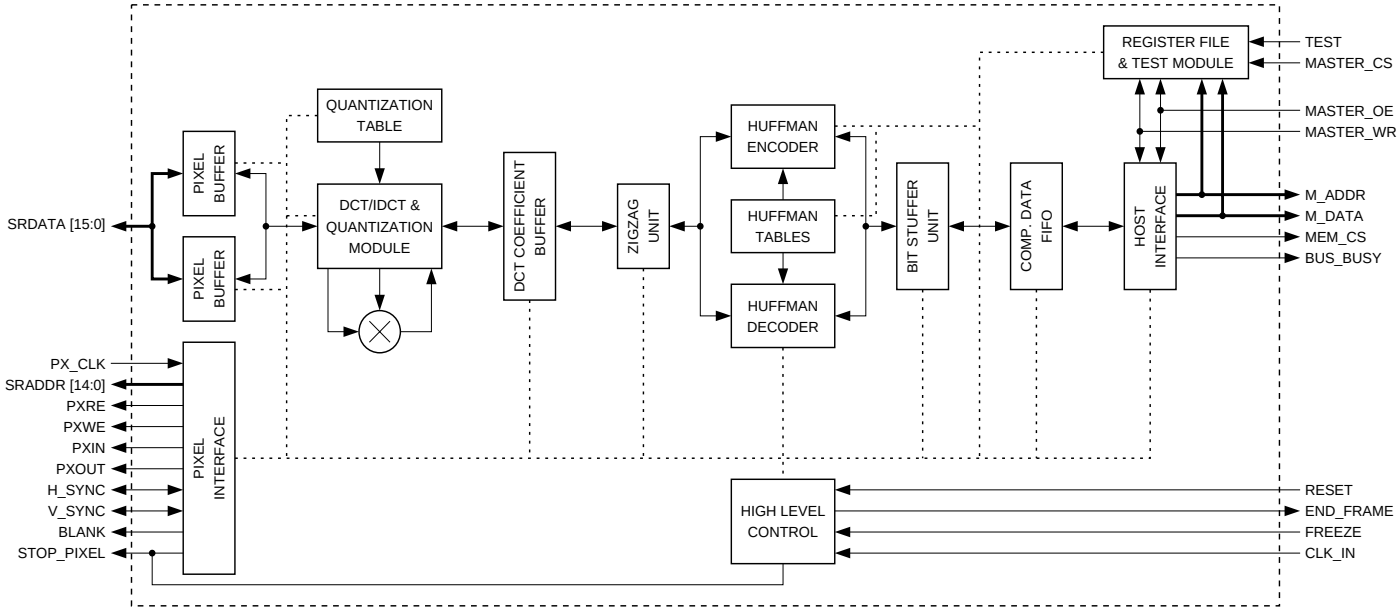
All transfers to the internal memory and tables of the JPEG codec are 8-bit wide. Data is transferred using the Data Bus, Address Bus, and the control signals MASTER_WR, MASTER_OE, MASTER_CS and BUS_BUSY. All transfers carried out in this mode are controlled by the microcontroller.

When the AT76C101 chip is operating in normal mode (i.e. either compression or decompression), it acts as a bus master on the external memory/microcontroller bus. Since the AT76C101 has higher priority over the microcontroller for these bus accesses, the microcontroller has to check the availability of the bus (by checking BUS_BUSY) before it can access it. Once all the internal registers of the AT76C101 are set up and the tables are loaded, the AT76C101 is activated by setting the Start_Reg register. Once the compression/decompression operation starts, the AT76C101 takes control of the bus, and gives it up only after the chip has processed the image.The microcontroller can access the internal memory of the AT76C101 only between frames and not during normal mode of operation.

Data Control

During compression, the AT76C101 monitors the internal image buffers and sends a stall signal (STOP) to prevent the external video interface logic from generating new pixels, in case the internal buffers are full. During decompression, the AT76C101 controls the transfer rate from the compressed data interface, based on the status of the compressed data FIFO (Figure 3).

Figure 3. Data Control



Compressed Data Memory Management

The AT76C101 starts reading/writing data from/to the compressed data memory starting from the address location specified by the Mem_Start_Addr register. Once a frame has been processed, the AT76C101 writes the address of the last compressed data into the Mem_End_Addr register. The microcontroller uses this information to keep track of the memory locations having valid images, and to specify the starting memory address of the next image

Initialization Sequence

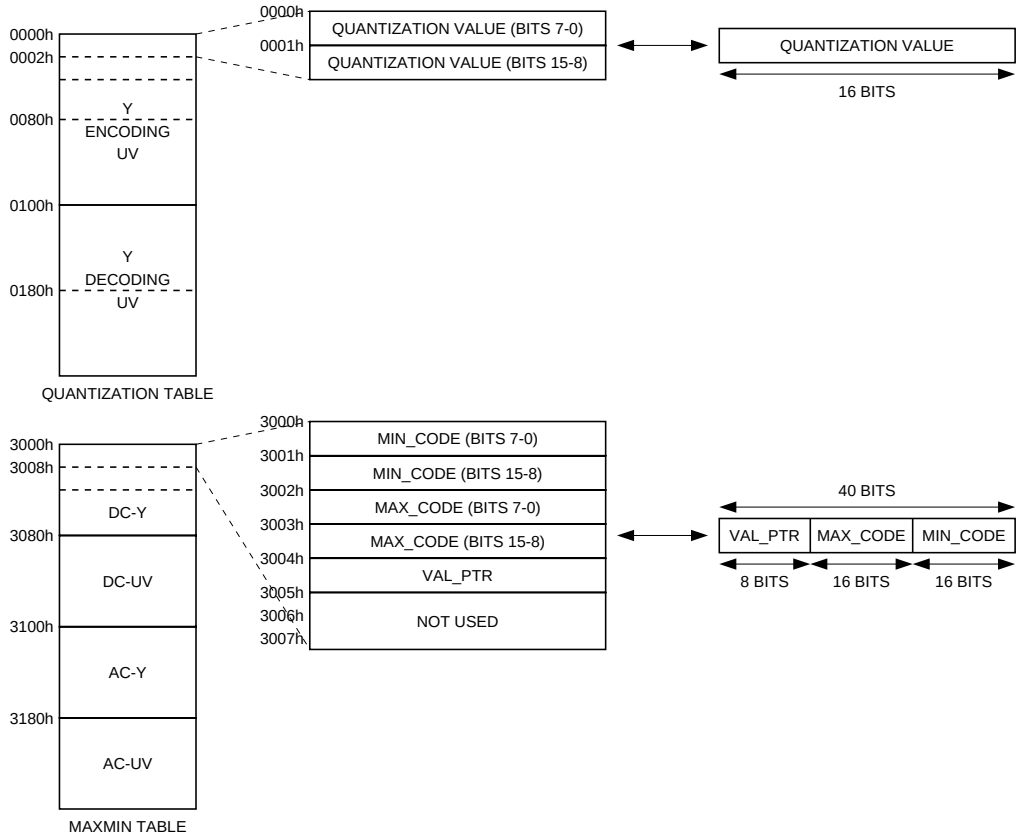
The active high RESET signal resets all the AT76C101 resources including the register file. Once the AT76C101 has been reset, the microcontroller can program the chip to the desired mode of operation. The microcontroller will also have to load the internal Huffman and Quantization Tables. Once the internal registers and tables have been initialized, the microcontroller can initiate a compression/decompression operation by asserting the Start_Reg register. The AT76C101 de-asserts this signal after the final image block is processed. When the AT76C101 completes the processing of an image, it asserts the FRAMEND signal, writes the address of the last compressed data into the Mem_End_Addr register and waits for a new Start_Reg request.

During decompression, the microcontroller has to do some additional processing of the JPEG data stream. The microcontroller extracts and process the JPEG header information from the compressed data stream. Based on this header information, the microcontroller then initializes the internal registers of the AT76C101 and writes the address of the memory location containing the first compressed image data (not the start of the JPEG header) into the Mem_Start_Addr register. It then follows the above mentioned initialization sequence.

Quantization Table Loading

The on-chip quantization tables must be loaded with the required values before the normal operation of the chip. The AT76C101's quantization table is a 256x16 RAM, and can store up to four 64-word quantization tables. The upper half of the RAM area is used to store the compression quantization tables and the lower half to store the decompression tables. The organization of the quantization RAM is shown in Figure 4. The Quantization Tables can be loaded only after the Quant_Table_Load_Enable register has been set. Once loaded, the quantization tables remain valid until the power is switched off or until they are reprogrammed (they are unaffected by RESET). The Quant_Table_Load_Enable register has to be reset after the tables are loaded and before normal operation of the chip can begin.

Figure 4. Internal Memory Organization (Quantization and MaxMin Tables)



Before loading, the quantization tables have to be converted from the JPEG interchange format (JPEG_Q_Table) to the AT76C101 specific format (AT76C101_Q_Table). This format varies, based on the mode of operation of the chip (compression or decompression). The steps to convert to the AT76C101 specific format are given below:

- The Quantization Tables are stored in the zigzag form in the JPEG interchange format. Convert these tables to the normal (un-zigzagged) form.
- Convert to AT76C101 format using the following algorithm where, M_Factor[i][j] = 16,384, if (i=1 and j=1) 32,768/sqrt(2), if (i=2.8) or (i=2.8 and j=1) 32,768 otherwise:

```
for (i = 1..8) begin
   for (j = 1..8) begin
      if (mode = COMPRESS)
         AT76C101_Q_Table[i][j] =
      (M_Factor[i][j]/
         JPEG_Q_Table[i][j]) + 0.5
      else if (mode = DECOMPRESS)
      AT76C101_Q_Table[i][j] =
   JPEG_Q_Table[i][j]
   end
end
```

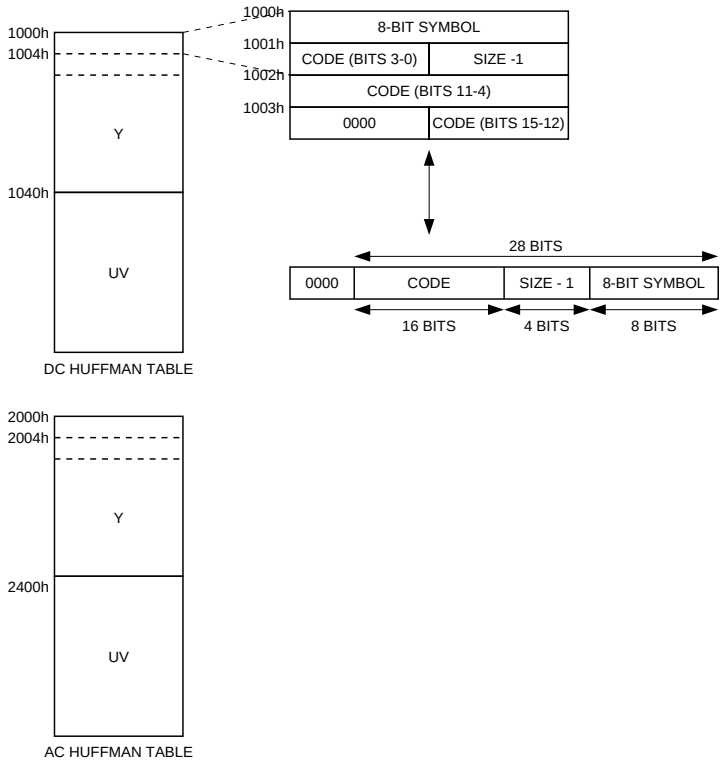
The Quantization tables are 16 bits wide and are loaded using the host bus. The host bus accesses the quantization table values in two 8-bit halves, with the lower address corresponding to the lower order byte and the higher address corresponding to the higher order byte (Figure 4).

Huffman Table Loading

Like the Quantization tables, the AT76C101 Huffman tables are specific to the chip. Before normal operation of the chip, the Huffman tables must be loaded in the AT76C101 specific format into the on-chip RAM. The INT_Table_Load_Enable register has to be set to load the Huffman tables. When the Huffman tables are loaded into the internal RAM, they remain valid until the power is switched off or until they are reprogrammed (they are not affected by RESET). The Huffman_Table_Load_Enable register has to be reset after the tables are loaded and before normal operation of the chip can begin.

The AT76C101 can store up to four Huffman tables: 2 Huffman AC tables and 2 Huffman DC tables. The memory organization and address mapping of the Huffman tables are given in Figure 5. The Huffman tables are 28 bits wide and consist of three fields, the size of the Huffman code (stored as 1 less than actual size), the Huffman code and the 8-bit symbol corresponding to the Huffman code. Each Huffman table value is accessed from the host bus in four 8-bit slices, with the lower order 8 bits corresponding to the lowest address (for e.g. 2000H) and the highest 8-bit slice (bit 24 through bit 31) corresponding to the highest address (2003H).

Figure 5. Internal Memory Organization (Huffman Tables)



The Huffman tables have the same format in both the compression and decompression mode, but the arrangement of the codes within the tables varies for the two modes. In the compression mode, the Huffman tables are indexed by the 8-bit symbol corresponding to the code. For example, the luminance AC Huffman table value corresponding to the 8-bit symbol value of 17 will be stored in the 17th location of the table, i.e. in the address locations 4068 to 4071. In the decompression mode, the Huffman tables are arranged in consecutive locations in increasing order of Huffman size. All codes of the same Huffman size are then arranged in terms of increasing Huffman code value. Appendix A, annex C of the JPEG International Standard gives the procedure for generating the Huffman codes and sizes from the Huffman table information extracted from the compressed JPEG header.

MaxMin Table Loading

The Maxmin tables are an extra set of tables which are required only for the decompression operation. Similar to the Huffman tables, these tables can be loaded only after the INT_Table_Load_Enable register has been set, and this register has to be reset before normal operation of the AT76C101 can commence. This table is required to keep track of the maximum and minimum Huffman code values for each Huffman code length. Since there is a maximum of 4 Huffman tables allowed and the longest Huffman code is 16 bits wide, the required maxmin table size is 64 words. The four maxmin tables are arranged in increasing order of size and each word of the maxmin table is 40 bits wide with three fields, a pointer to the position of the minimum code of that Huffman size, the minimum Huffman code and the maximum Huffman code corresponding to that Huffman code size. The maxmin tables are accessed by the host bus in terms of five 8-bit slices with the lowest address corresponding to bit 0-7 of the maxmin table value and the highest address corresponding to bit 32-39 (Figure 4).

These tables are generated from the AT76C101 specific decompression mode Huffman tables and the algorithm to develop them is given below:

```
for (i = 1..16) begin
   maxmin_min_code[i] = -1
   maxmin_max_code[i] = -1
end
for (i=1..total_num_of_huffman_codes)
   if (maxmin_min_code[size[i]] == -1)
begin
      maxmin_min_code[size[i]] = code[i]
      maxmin_val_ptr[size[i]] = i
   end
maxmin_max_code[size[i]] = code[i]
```

Signal Description

Figure 6. Symbol

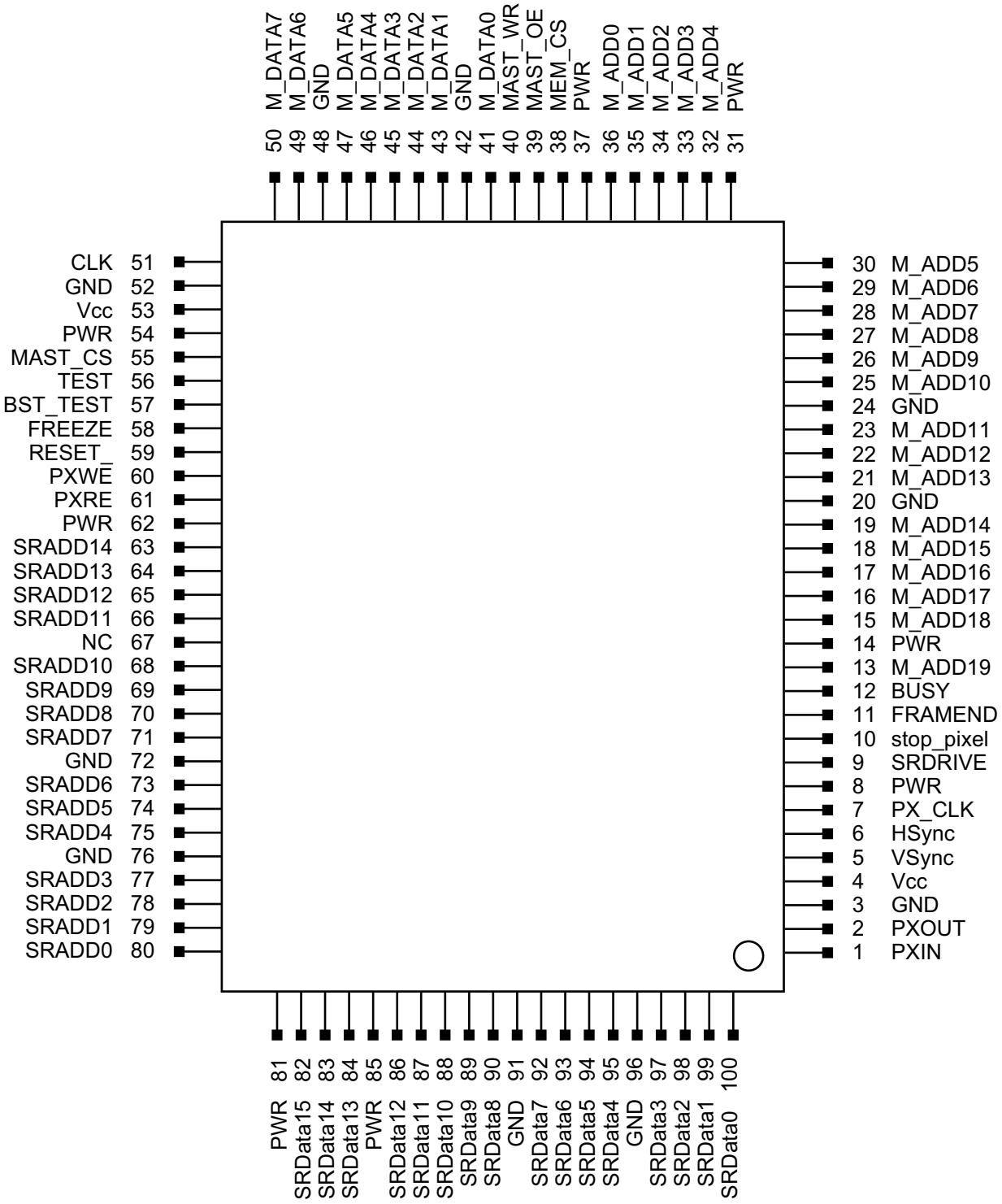


Table 1. Signal Description

Signal	Type	Description
BST_TEST	Input	BIST test pin (used only for testing), should be grounded.
CLK	Input	Master Clock.
FREEZE	Input	Stall Signal, active high. When this signal is asserted, the chip finishes processing the current block and then remains in that state until freeze is pulled low.
MAST_CS	Input	Master Chip Select Input. Used by microcontroller to access the JPEG chip. Active low.
PX_CLK	Input	Video Interface Clock (27 MHz fixed).
RESET_	Input	Global Reset Signal, active high, minimum pulse width is three CLK_IN 40 MHz cycles.
TEST	Input	Active high - Puts chip in test mode. User has access to all internal memory. Must be tied to gnd for normal operation.
HSync	Bidirectional	Indicates start of a horizontal line of the frame.
M_ADD[19:0]	Bidirectional	Memory/Microcontroller Address Bus. Used by JPEG chip to access the compressed data memory, and used by microcontroller to access the JPEG chip.
M_DATA[7:0]	Bidirectional	Memory/ Microcontroller Data Bus. Used to transfer compressed data to the external storage unit. Also used by microcontroller to program the JPEG chip.
MAST_OE	Bidirectional	Memory/ Microcontroller Read Select. Active low. Used by microcontroller to read from JPEG chip and used by JPEG chip to read compressed data from memory.
MAST_WR	Bidirectional	Memory/Microcontroller Write Select. Active low. Used by microcontroller to write to JPEG and used by JPEG to write to compressed data memory.
SRData[15:0]	Bidirectional	Pixel Data Bus for inputting uncompressed data in encoding mode, or for outputting decompressed image data in decoding mode.
VSync	Bidirectional	Indicates the start of a frame.
BUSY	Output	Microcontroller bus busy. Signals whether the JPEG chip (high) or microcontroller (low) controls the bus.
FRAMEND	Output	End of encoding/decoding operation. FRAMEND is active after chip is reset and it remains active until the Start Register is set by the host.
MEM_CS	Output	Compressed data memory select. Active low. Used by JPEG to select the external memory device used to store the compressed data stream.
PXIN	Output	Pixel Input Control. It is asserted low when pixels are being input from the active portion of the frame into the strip buffer.
PXOUT	Output	Pixel Output Control. It ia active only when the pixels from the active region of the field are being read from the strip buffer.
PXRE	Output	Active low. Controls reading data from external memory.
PXWE	Output	Active low. Controls writing to the external memory.
SRADD[14:0]	Output	Pixel Address Bus. This bus specifies the address location of the external memory device (strip buffer), from/ to which the pixel data is transferred. Supports external memory of up to 32K locations.
SRDRIVE	Output	Indicates that the AT76C101 is driving the SRDATA Bus.
stop_pixel	Output	When asserted, all operations in the video interface are stopped. Active when the DCT buffers are full, or when the ext. video logic is not ready.

Table 2. Register File Description

Register	Address	R/W	Description
HPeriod_Low	0F800	R/W	HPeriod-low byte (bit 0 to 7). For color pictures, in Master mode, HPeriod contains one less than the number of pixels between successive HSYNC pulses. In Slave Mode, it contains the time between the falling edge of one HSYNC pulse and the start of the next HSYNC pulse (in terms of pixels). For grayscale images: set this register to 1 less than half the number of pixels between successive Hsync pulses.
HPeriod_High	0F801	R/W	HPeriod - high byte (bit 8 to 15).
HSyncWidth_Low	0F802	R/W	HSyncWidth - low byte. Used only in Master mode. For color images: 1 less than the number of pixels that Hsync has to be held active low. For grayscale images: 1 less than half the number of pixels that Hsync has to be held active low.
HSyncWidth_High	0F803	R/W	HSyncWidth - high byte.
HDelay_Low	0F804	R/W	HDelay - low byte. Delay from falling edge of HSYNC to the first active pixel.
HDelay_High	0F805	R/W	HDelay - high byte.
HActive_Low	0F806	R/W	HActive - low byte. For color images: size of active horizontal line divided by 8. For grayscale images: size of active horizontal line in pixels divided by 16.
HActive_High	0F807	R/W	HActive - high byte.
VPeriod_Low	0F808	R/W	VPeriod - low byte. Used in Master mode - contains the number of lines in the frame_7.
VPeriod_High	0F809	R/W	VPeriod - high byte.
VSyncWidth_Low	0F80A	R/W	VSyncWidth - low byte. Used in Master mode - one less than the number of lines that Vsync has to be held active low.
VSyncWidth_High	0F80B	R/W	VSyncWidth - high byte.
VDelay_Low	0F80C	R/W	VDelay - low byte.
VDelay_High	0F80D	R/W	VDelay - high byte.
VActive_Low	0F80E	R/W	VActive - low byte. Number of active vertical lines.
VActive_High	0F80F	R/W	VActive - high byte.
Start_Reg	0F810	R/W	Bit 0 is used to initiate the compression/decompression pipeline.
Mode	0F812	R/W	Determine the device operating mode. The function of each bit is shown below. Bit 0: Encode(0)/Decode(1) operation. Bit 1: Color(0)/Grayscale(1) Image. Bit 2: Video Master(1)/Slave(0) Mode. Rest of bits are reserved and should be set to zero.
Int_Table_Load_Enable	0F813	R/W	Various bits of this register enable loading the different tables on chip. Bit 0: When set, enables programming the Quantization Tables. Bit 1: When set, enables loading the Huffman Tables, including the MAXMIN tables.
Decoder_Error	0F814	R	The chip sets this register to 1, if an error occurs while decoding.
Decoder_Error_Code_Low	0F815	R	Decoder_Error_Code - high byte.
Decoder_Error_Code_High	0F816	R	Decoder_Error_Code - high byte.

Table 2. Register File Description

Register	Address	R/W	Description
FIFO_Status	0F817	R	Shows the status of the internal FIFO. Bit 0 is the FIFO full indicator and bit 1 is the FIFO empty indicator.
Write_Cnt_Reg	0F818	R/W	The number of wait states required during a write to external memory is programmed into this register.
Read_Cnt_Reg	0F819	R/W	The number of wait states required during a read from external memory is programmed into this register.
Mem_Start_Addr_Low	0F81A	R/W	Mem_Start_Addr - low byte. The external memory start address is programmed here.
Mem_Start_Addr_Med	0F81B	R/W	Mem_Start_Adrr - middle byte (bit 16 to 31)
Mem_Start_Addr_High	0F81C	R/W	Mem_Start_Addr - high byte (bit 32 to 39)
Mem_End_Addr_Low	0F81D	R	Mem_End_Addr - low byte. AT76C101 writes the address of the last byte of the frame written into the external memory.
Mem_End_Addr_Med	0F81E	R	Mem_End_Addr - middle byte (bit 16 to 31).
Mem_End_Addr_High	0F81F	R	Mem_End_Addr - high byte (bit 32 to 39).

Table 3. Internal Memory Addressing

Module	Address Range
Quantization Tables (256 x 16 bits)	0x00000-0x001FF
DC Huffman Tables (32 x 28 bits)	0x01000-0x0107F
AC Huffman Tables (512 x 28 bits)	0x03000-0x031FF
Maxmin Tables - For Decoding only (64 x 40 bits)	0x04000-0x04200
Pixel Buffer (4 buffers of size 128 x 8 bits each)	0x04000-0x04200
DCT Coefficient Buffer (2 buffers of size 64 x 16 each)	0x05000-0x050FF
Compressed Data FIFO (64 x 8 bits)	Write Port 0x06000-0x06040 Read Port 0x07000-0x07040

Table 4. AC Characteristics

Symbol	Parameter	Min	Max	Units
t_{CSS}	Chip Select Setup Time	3		ns
t_{AS}	Address Setup Time	3		ns
t_{AH}	Address Hold Time	0		ns
t_{DS}	Data Setup Time	3		ns
t_{DH}	Data Hold Time	0		ns
t_{WPL}	Write Pulse Width	75		ns
t_{WREC}	Write Recovery Time	125		ns
t_{ACC}	Read Access Time		120	ns
t_{RPL}	Read Pulse Length	120		ns
t_{RREC}	Read Recovery Time	50		ns
t_{CYC}	Compressed Memory Read/Write Cycle Time	1	8	CLK_IN Cycles
t_{SWR}	Compressed Memory Write Set-up Time	0.5		
t_{SOE}	Compressed Memory Read Set-up Time	0.5		

Figure 7. Compressed Memory Write

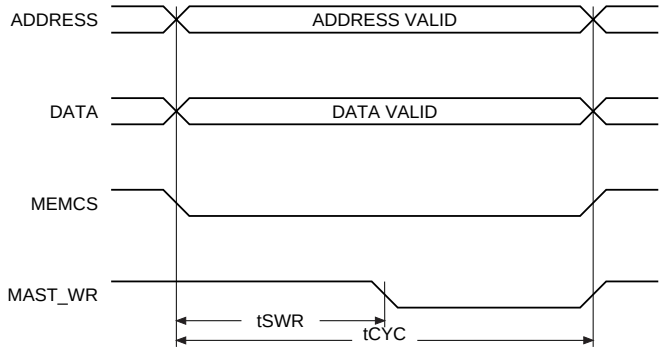


Figure 8. Compressed Memory Read

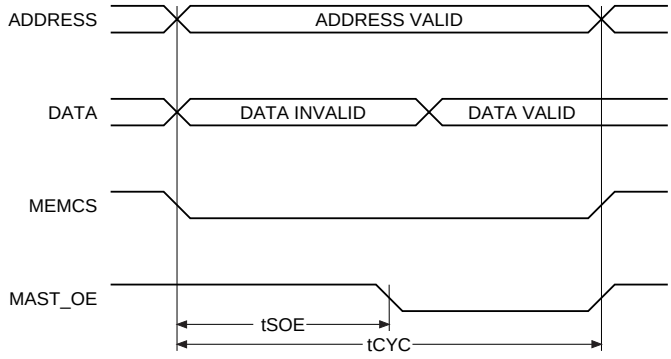


Figure 9. Microcontroller Write

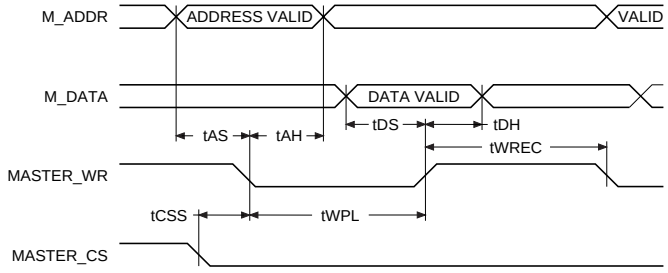
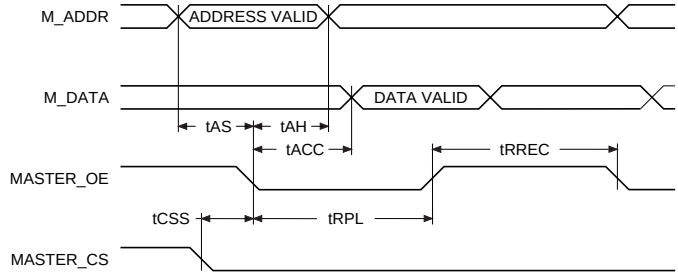


Figure 10. Microcontroller Read



Electrical Specifications

Table 5. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Conditions
V_{cc}	DC supply voltage	-0.3	4.6	V	Core and standard IOS
V_i	DC input voltage	-0.3	Vdd + 0.3V	V	or see +-IIk
V_o	DC output voltage		Vdd + 0.3V	V	or see +-IOk
$+-I_{Ik}$	DC input diode current		10	mA	Vi<-0.5V Vi>Vdd+0.5V
$+-I_{OK}$	DC output diode current		10	mA	V0<-0.5V V0>Vdd+0.5V
I_{olMAX}	Continuous output current		10	mA	Industrial
I_{ohMAX}	Continuous output current		10	mA	Industrial
t_{SH}	Time of outputs shorted		5	sec	
T_A	Temperature range	-40	+85	C	Industrial
T_{SG}	Storage Temperature	-65	+150	C	

Table 6. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{cc}	DC supply voltage	3	3.3	3.6	V	
V_i	DC input voltage	0		Vdd	V	
V_0	DC output voltage	0		Vdd	V	
T_A	Temperature range	-40		+85	C	Industrial
T_R	Input rise time			15	ns	10%-90% CMOS
T_F	Input fall time			15	ns	10%-90% CMOS

Table 7. DC Characteristics

Symbol	Parameter	Min	Max	Unit	Conditions
I_{ih} I_{il}	Input leakage, no pullup Input leakage, no pullup			µA µA	$V_{in} = V_{cc} = 5.5V$ $V_{in} = 0, V_{cc} = 5.5V$
I_{oz}	High-impedance output current bi-directional pins			µA	$V_{cc} = 5.5V$
V_{il} V_{ih}	Low level input voltage High level input voltage			V V	CMOS inputs and bi-dir. CMOS inputs and bi-dir.
V_{OL} V_{OH}	Low level input voltage High level input voltage			V V	$I_{OL} = 5.0mA$ $I_{OH} = 5.0mA$
C_{IN}	Input capacitance			pF	