VC7203 Virtex-7 FPGA GTX Transceiver Characterization Board

User Guide

UG957 (v1.0) October 10, 2012

XILINX®

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
10/10/12	1.0	Initial Xilinx release.

Table of Contents

Appendix E: Regulatory and Compliance Information

Chapter 1

VC7203 Board Features and Operation

This Chapter describes the components, features, and operation of the VC7203 Virtex™-7 FPGA GTX Transceiver Characterization Board. The VC7203 board provides the hardware environment for characterizing and evaluating the GTX transceivers available on the Virtex-7 XC7V485T-3 FFG1761E FPGA. The VC7203 board schematic, bill-of-material (BOM), layout files and reference designs are available online at http://www.xilinx.com/products/boards/vc7203

FPGA Compatibility

The VC7203 board is provided with Virtex-7 XC7V485T-3 FFG1761E FPGA. The board will also support all device densities (i.e., XC7VX330T, XC7V585T, XC7VX690T, XC7V1500T, and XC7V2000T devices) in the pin-compatible FFG1761, FLG1761, and FHG1761 packages. However, certain interfaces that are available in larger density devices may not be available in the XC7V485T device (for example: GTX QUAD_111, GTX QUAD_112, FMC 3, etc.). Unsupported interfaces are highlighted in this document.

VC7203 Board Features

- Virtex-7 XC7V485T-3 FFG1761E FPGA
- On-board power supplies for all necessary voltages
- Power jacks for optional use of external power supplies
- Digilent USB JTAG programming port
- System ACE™ SD controller
- Power module supporting Virtex-7 FPGA GTX transceiver power requirements
- A fixed, 200 MHz 2.5V LVDS oscillator wired to multi-region clock capable (MRCC) inputs
- Two pairs of differential MRCC inputs with SMA connectors
- SuperClock-2 module supporting multiple frequencies
- Nine Samtec BullsEye connector pads for the GTX transceivers and reference clocks
- Power status LEDs
- General purpose DIP switches, LEDs, push buttons, and test I/O
- Three VITA 57.1 FPGA mezzanine card (FMC) high pin count (HPC) connectors
- USB-to-UART bridge
- I^2C bus
- PMBus connectivity to on-board digital power supplies
- Active cooling for the FPGA

The VC7203 board block diagram is shown in Figure 1-1.

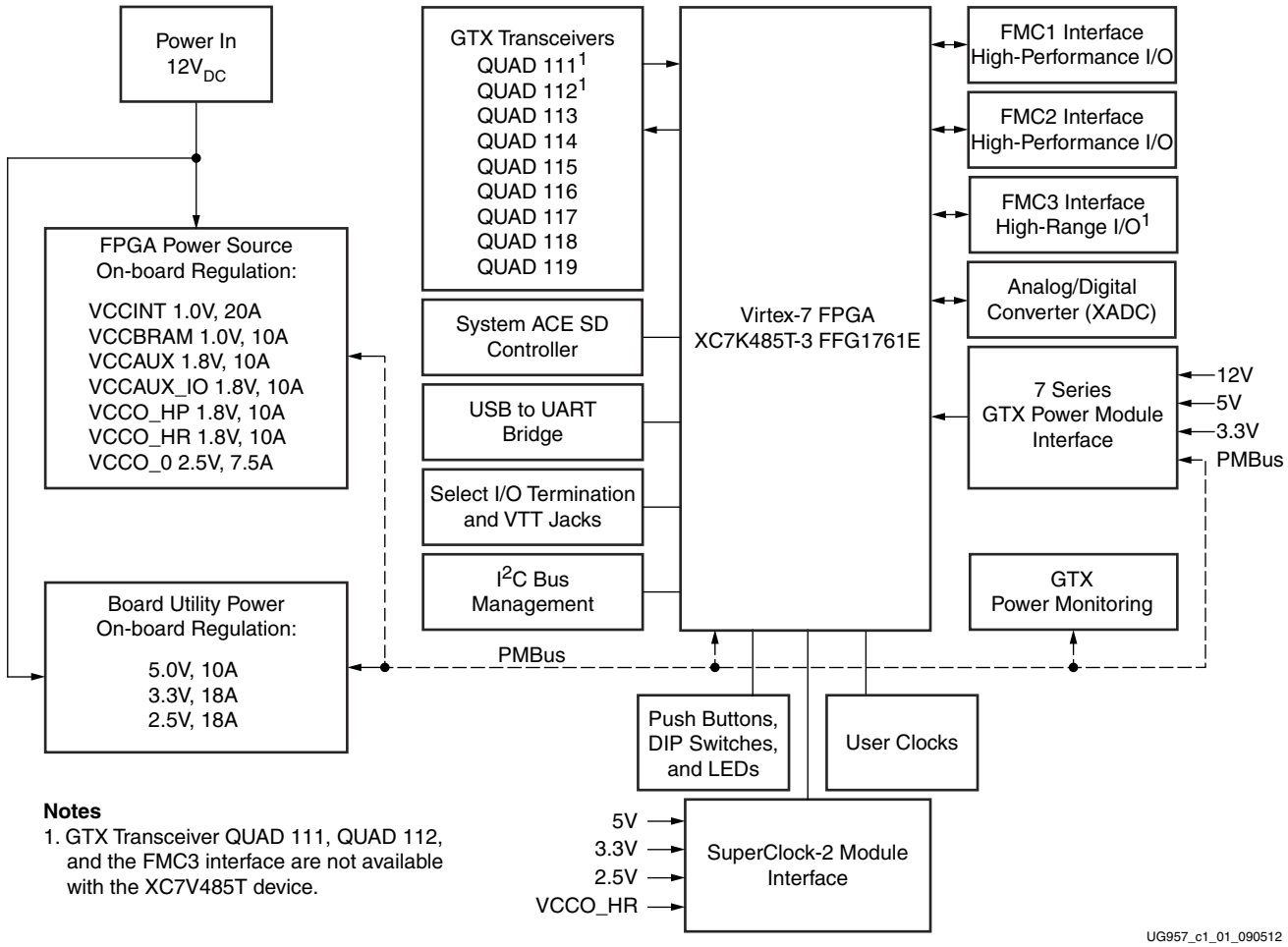

Figure 1-1: **VC7203 Board Block Diagram**

Detailed Description

Figure 1-2 shows the VC7203 board described in this user guide. Each numbered feature that is referenced in Figure 1-2 is described in the sections that follow.

Caution! The VC7203 board can be damaged by electrostatic discharge (ESD). Follow standard ESD prevention measures when handling the board.

Caution! Do not remove the rubber feet from the board. The feet provide clearance to prevent short circuits on the back side of the board.

Note: Figure 1-2 is for reference only and might not reflect the current revision of the board.

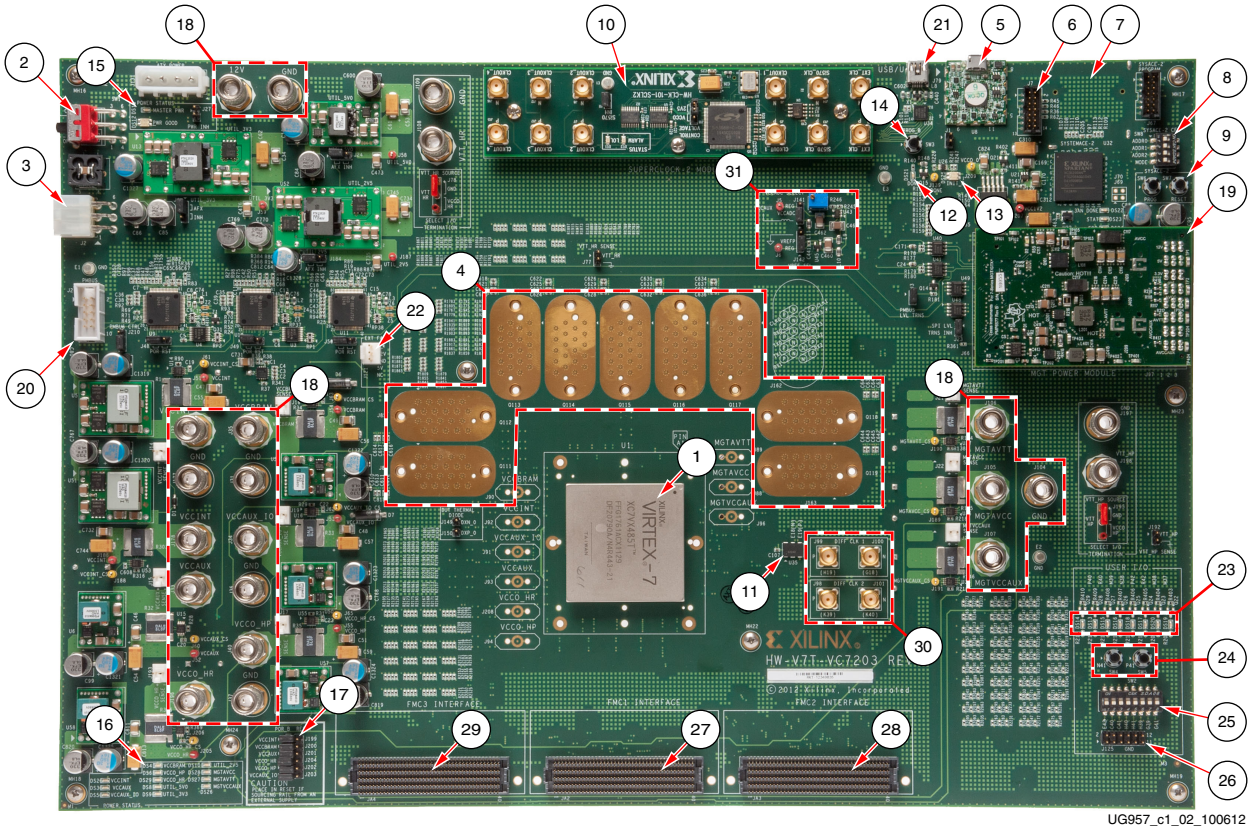

Figure 1-2: **VC7203 Board Features. Callouts Listed in Table 1-1**

Table 1-1: **VC7203 Board Feature Descriptions**

Figure 1-2 Callout	Reference Designator	Feature Description
1	U1	Virtex-7 XC7V485T-3 FFG1761E FPGA, page 15
2	SW1	Power switch, page 9
3	J2	12V Mini-Fit connector, page 8
4	J84, J85, J86, J158, J159, J160, J161, J162, J89	GTX transceiver connector pads Q111 , Q112, Q113, Q114, Q115, Q116, Q117, Q118 and Q119, page 22
5		USB JTAG connector (micro-B receptacle), page 15
6	J7	JTAG connector (alternate access for programming cables), page 15
7	J211	System ACE SD card connector (back-side of board), page 15
8	SW8	System ACE SD configuration address DIP switches, page 17
9	SW7	System ACE SD RESET button, page 17
10		SuperClock-2 module, page 18
11	U35	200 MHz 2.5V LVDS oscillator, page 18
12	DS21	FPGA DONE status LED, page 17

Table 1-1: **VC7203 Board Feature Descriptions *(Cont'd)***

Figure 1-2 Callout	Reference Designator	Feature Description
13	DS25	FPGA INIT_B status LED, page 17
14	SW3	FPGA PROG_B pushbutton, page 17
15	DS11	12V power status LED, page 9
16	DS2, DS3, DS4, DS5, DS6, DS8, DS9, DS10, DS26, DS27, DS28, DS29	Status LEDS for FPGA logic, transceiver and utility power,
17	J199, J200, J201 J202, J203 J204	Power regulation jumpers for onboard regulators
18	J28, J29, J31, J32, J33, J34, J35, J36, J37, J40, J104, J105, J106, J107, J177, J178, J196	External power supply jacks, page 11
19		GTX transceiver power supply module, page 12
20	J26	PMBUS connector, page 12
21	J79	Connector for USB to UART bridge (mini-B receptacle), page 26
22	J121	Power connector for active heatsink, page 13
23	DS13, DS14, DS15, DS16, DS17, DS18, DS19, DS20	User LEDs (active high), page 20
24	SW4, SW5	User push buttons (active high), page 21
25	SW2	User DIP switches (active high), page 20
26	J125	User I/O header, page 20
27	JA2	FMC1 connector, page 27
28	JA3	FMC2 connector page 27
29	JA4	FMC3 connector1 page 27
30	J98, J99, J100, J101	SMA connectors to differential MRCC pins on FPGA, page 18
31	J141, J142, R233	Jumpers and potentiometer for XADC reference and analog supply set-up, page 41

Power Management

Board 12V Input Power

VC7203 board receives 12V main power through J2 (callout 3, Figure 1-2) using the 12V AC adapter that ships with the board. J2 is a 6-pin (2 x 3), right angle, Mini-Fit connector.

Caution! When supplying 12V through J2, use only the power supply provided for use with this board (Xilinx part number 3800033).

Caution! Do **NOT** use a 6-pin, PC ATX power supply connector with J2. The pinout of the 6-pin, PC ATX connector is not compatible J2 and the board will be damaged if an attempt is made to power it from a PC ATX power supply connector.

12V power can also be provided through:

- Connector J131 which accepts an ATX hard drive, 4-pin, power plug
- Jacks J29 (12V) and J28 (ground) (callout 18, Figure 1-2)which can be connected to a bench-top power supply

Caution! Because jacks J29 and J28 provide no reverse polarity protection, use a power supply with a current limit set at 6A max.

Caution! Do **NOT** apply 12V power to more than a single input source. For example, do not apply power to J2 and J131 at the same time.

Power Switch

Main board power is turned on or off using switch SW1 (callout 2, Figure 1-2). When the switch is in the ON position, power is applied to the board and green LED DS11 illuminates (callout 15, Figure 1-2).

Onboard Power Regulation

Figure 1-3 shows the onboard power supply architecture.

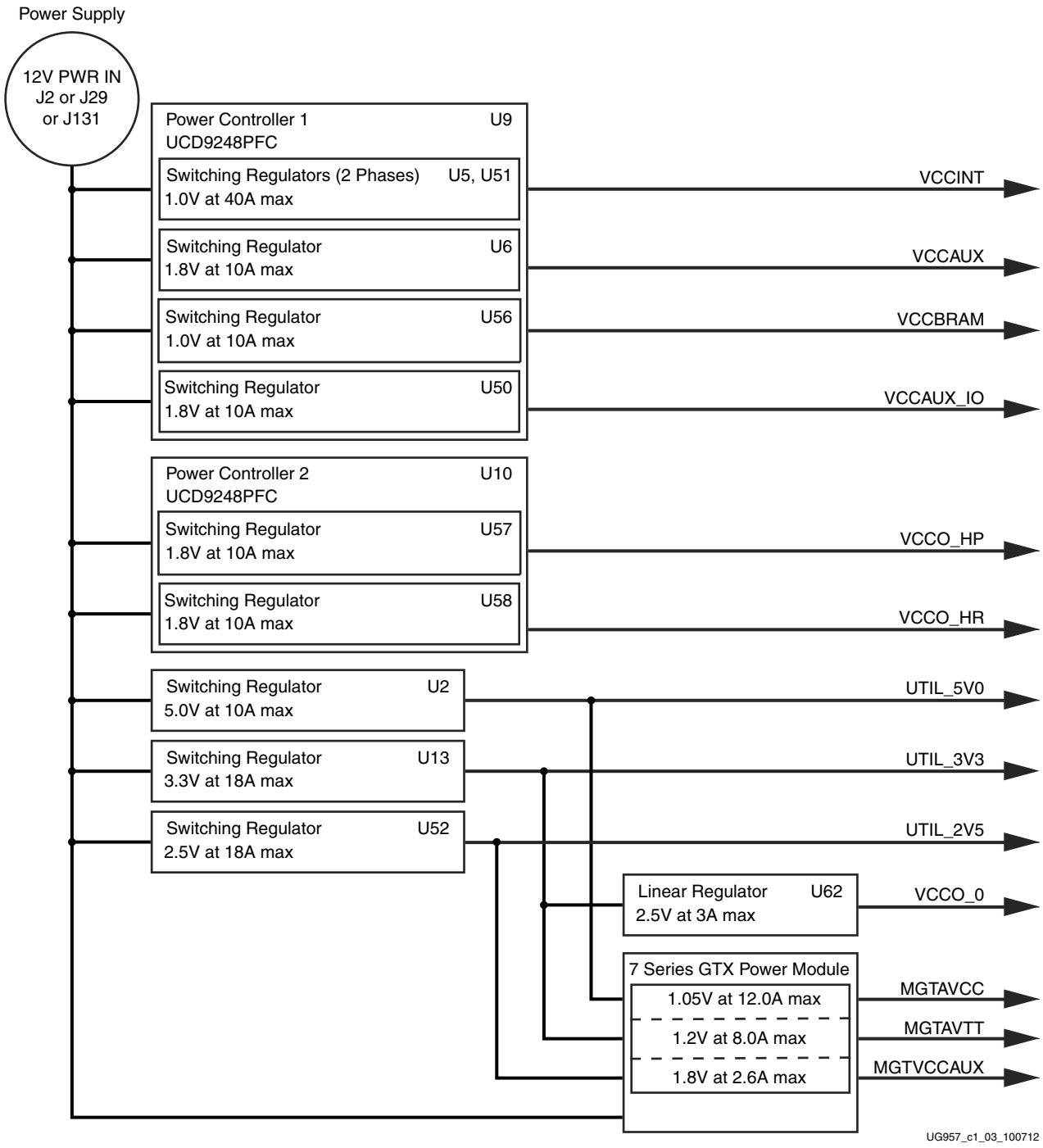

Figure 1-3: **VC7203 Board Power Supply Block Diagram**

The VC7203 board uses power regulators and PMBus compliant digital PWM system controllers from Texas Instruments to supply the FPGA logic and utility voltages listed in Table 1-2. The board can also be configured to use an external bench power supply for each voltage. See Using External Power Sources.

Table 1-2: **Onboard Power System Devices**

Device Part Number	Reference Designator(s)	Description	Power Rail Net Name	Voltage
FPGA Logic				
UCD9248PFC	U9	Digital PWM system controller, PMBUS address 52		
PTD08A020W	U5, U51	Adjustable(1) switching regulator, 40A (two phases at 20A/phase), 0.6V to 3.6V	VCCINT	1.0V
PTD08A010W	U6	Adjustable(1) switching regulator, 10A, 0.6V to 3.6V	VCCAUX	1.8V
PTD08A010W	U56	Adjustable(1) switching regulator 10A, 0.6V to 3.6V	VCCBRAM	1.0V
PTD08A020W	U50	Adjustable(1) switching regulator, 40A (two phases @ 20A/phase), 0.6V to 3.6V	VCCAUX_IO	1.8V (default)
UCD9248PFC	U10	Digital PWM system controller, PMBUS address 53		
PTD08A010W	U57	Adjustable switching regulator, 10A, 0.6V to 3.6V	VCCO_HP	1.8V
PTD08A010W	U58	Adjustable switching regulator, 10A, 0.6V to 3.6V	VCCO_HR	1.8V (default)
Utility				
PTH12060W	U2	Fixed switching regulator, 10A	UTIL_5V0	5.0V
PTH12020W	U13	Fixed switching regulator, 18A	UTIL_3V3	3.3V
PTH12020W	U52	Fixed switching regulator, 18A	UTIL_2V5	2.5V
TPS75925	U62	Fixed LDO regulator, 3A	VCCO_0	2.5V
GTX Transceivers (monitoring only)				
UCD9248PFC(2)	U11	Digital PWM system controller, PMBUS address 54		
XADC(3)				
ADP123	U43	Fixed LDO regulator	VCCADC_ADP	1.8V
REF3012	U45	Fixed LDO regulator	VREF_3012	1.25V
System ACE SD				
ADP123	U21	Fixed LDO regulator	VCC_1V2	1.2V

Notes:

1. The output voltages of regulators controlled by a UCD9248 can be reprogrammed using the Texas Instruments Fusion Digital Power Designer application (www.ti.com/tool/fusion_digital_power_designer). However, **extreme caution must be taken when attempting to modify of any of the onboard regulators. An incorrectly programmed regulator can damage onboard components**.
2. The UCD9248PFC (U11) at Address 54 monitors MGTAVCC, MGTAVTT, and MGTVCCAUX rail voltage and current levels which can be observed in real time using the Texas Instruments Fusion Digital Power Designer application (see Monitoring Voltage and Current, page 12). Transceiver supply voltages cannot be changed from this controller.
3. For information on XADC see UG480, *7 Series FPGAs XADC Dual 12-Bit 1MSPS Analog-to-Digital Converter User Guide*.

Using External Power Sources

Callout 18, Figure 1-2

Each voltage rail for the FPGA logic and GTX transceivers has an associated jack (or jacks) that can be used to provide power from an external source (Table 1-3). The jacks are binding posts that accept standard banana plugs.

Caution! Do **NOT** apply power to any of the FPGA logic power supply jacks without first disabling the associated regulator or regulators. Failing to disable the regulator can damage the board.

Each onboard FPGA Logic regulator can be disabled by using its respective Power Regulation jumper (callout 17, Figure 1-2) shown in Table 1-3. A regulator is disabled by moving its Power Regulation jumper from POR_B to RESET.

Table 1-3: **FPGA Logic and GTX Transceiver Rails**

	Power Rail Net Name	External Supply Jack(s)	Power Regulation Jumper
FPGA Logic	VCCINT	J32, J178	J199
	VCCAUX	J33	J201
	VCCBRAM	J35	J200
	VCCAUX_IO	J34	J203
	VCCO_HP	J40	J202
	VCCO_HR	J196	J204
GTX Transceiver	MGTAVCC	J105	None(1)
	MGTAVTT	J106	None(1)
	MGTVCCAUX	J107	None(1)

Notes:

1. 1.The GTX power module must be removed before providing external power to any of the transceiver rails (see 7 Series GTX Transceiver Power Module, page 12).

Default Jumper and Switch Positions

A list of jumpers and switches and their required positions for normal board operation is provided in Appendix A, Default Jumper Settings.

Monitoring Voltage and Current

Voltage and current monitoring and control are available for FPGA logic and transceiver power rails through Texas Instruments' Fusion Digital Power graphical user interface (GUI). The three onboard TI power controllers (U9 at PMBUS address 52, U10 at PMBUS address 53, and U11 at PMBUS address 54) are wired to the same PMBus. The PMBus connector, J26 (callout 20, Figure 1-2), is provided for use with the TI USB Interface Adapter PMBus pod and associated TI GUI.

References

More information about the power system components used by the VC7203 board are available from the Texas Instruments digital power website [Ref 1].

7 Series GTX Transceiver Power Module

The 7 Series GTX transceiver power module (callout 19, Figure 1-2) supplies MGTAVCC, MGTAVTT and MGTVCCAUX voltages to the FPGA GTX transceivers. Four 7 Series GTX power modules from four third-party vendors are provided with the VC7203 board for evaluation. Any one of the four modules can be plugged into connectors J66 and J97 in the outlined and labeled power module location shown in Figure 1-4.

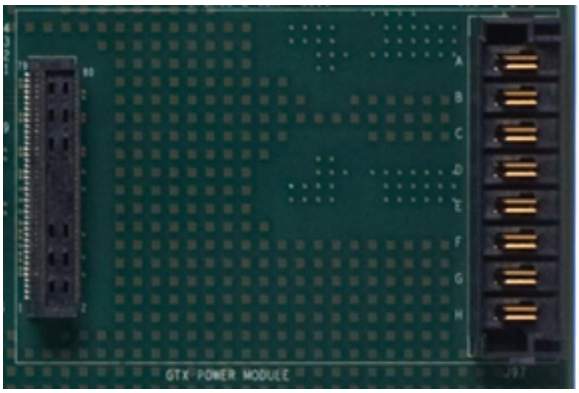

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Figure 1-4: **Mounting Location, 7 Series GTX Transceiver Power Module**

Table 1-4 lists the nominal voltage values for the MGTAVCC, MGTAVTT and MGTVCCAUX power rails. It also lists the maximum current rating for each rail supplied by 7 Series GTX modules included with the VC7203 board.

Table 1-4: **7 Series GTX Transceiver Power Module**

GTX Transceiver Rail Net Name	Nominal Voltage	Maximum Current Rating
MGTAVCC	1.05V	12A
MGTAVTT	1.2V	8A
MGTVCCAUX	1.8V	2.6A

Each GTX transceiver rail comes with an associated jack that can be used to provide external power. These external supply jacks are shown in Table 1-3.

Caution! The 7 Series GTX Module **MUST** be removed when providing external power to the GTX transceiver rails.

Information about the four 7 Series GTX power supply modules included with the KC724 kit is available from the vendor websites [Ref 2].

Active Heatsink Power Connector

Callout 22, Figure 1-2

An active heatsink (Figure 1-5) is provided for the FPGA. A 12V fan is affixed to the heatsink and is powered from the 3-pin friction lock header J121 (Figure 1-6).

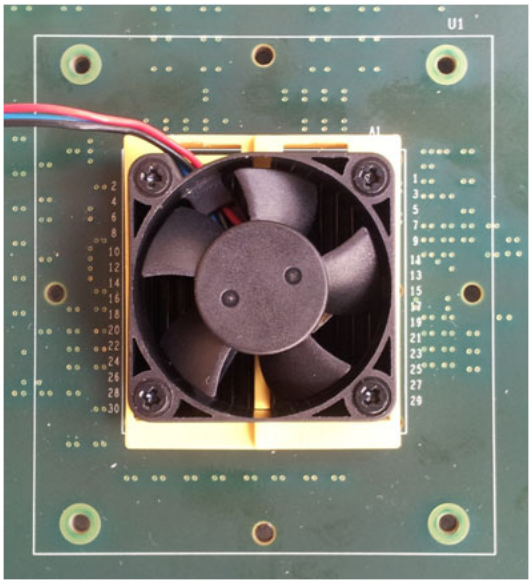

Figure 1-5: **Active FPGA Heatsink**

The fan power connections are detailed in Table 1-5:

Table 1-5: **Fan Power Connections**

Fan Wire	Header Pin
Black	J121.1 - GND
Red	J121.2 - 12V
Blue	J121.3 - NC

Figure 1-6 shows the heatsink fan power connector J121.

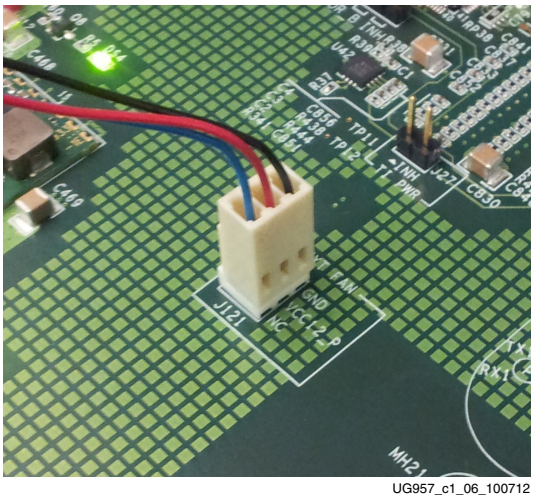

Figure 1-6: **Heatsink Fan Power Connector J121**

Virtex-7 FPGA

The VC7203 board is populated with the Virtex-7 XC7V485T-3 FFG1761E FPGA at U1 (callout 1, Figure 1-2). For further information on Virtex-7 FPGAs, see DS180, 7 Series *FPGAs Overview*.

FPGA Configuration

The FPGA is configured via JTAG using one of the following options:

- USB JTAG connector (callout 5, Figure 1-2)
- System ACE SD (callout 7, Figure 1-2)
- JTAG cable connector (callout 6, Figure 1-2)

The VC7203 board comes with an embedded USB-to-JTAG configuration module (U8) which allows a host computer to access the board JTAG chain using a Standard A to Micro-B USB cable. Alternately, the FPGA can be configured via System ACE from a Secure Digital (SD) memory card installed in J211 (see System ACE SD Configuration Address DIP Switches, page 17). Finally, a JTAG connector (J7) is available to provide access to the JTAG chain using one of Xilinx's configuration cables—Platform Cable USB, Platform Cable USB II or Parallel Cable IV (PCIV).

The JTAG chain of the board is illustrated in Figure 1-7. By default only the Virtex-7 FPGA and the System ACE SD controller are part of the chain (J1 jumper OFF). Installing the J1 jumper adds the FMC interfaces as well.

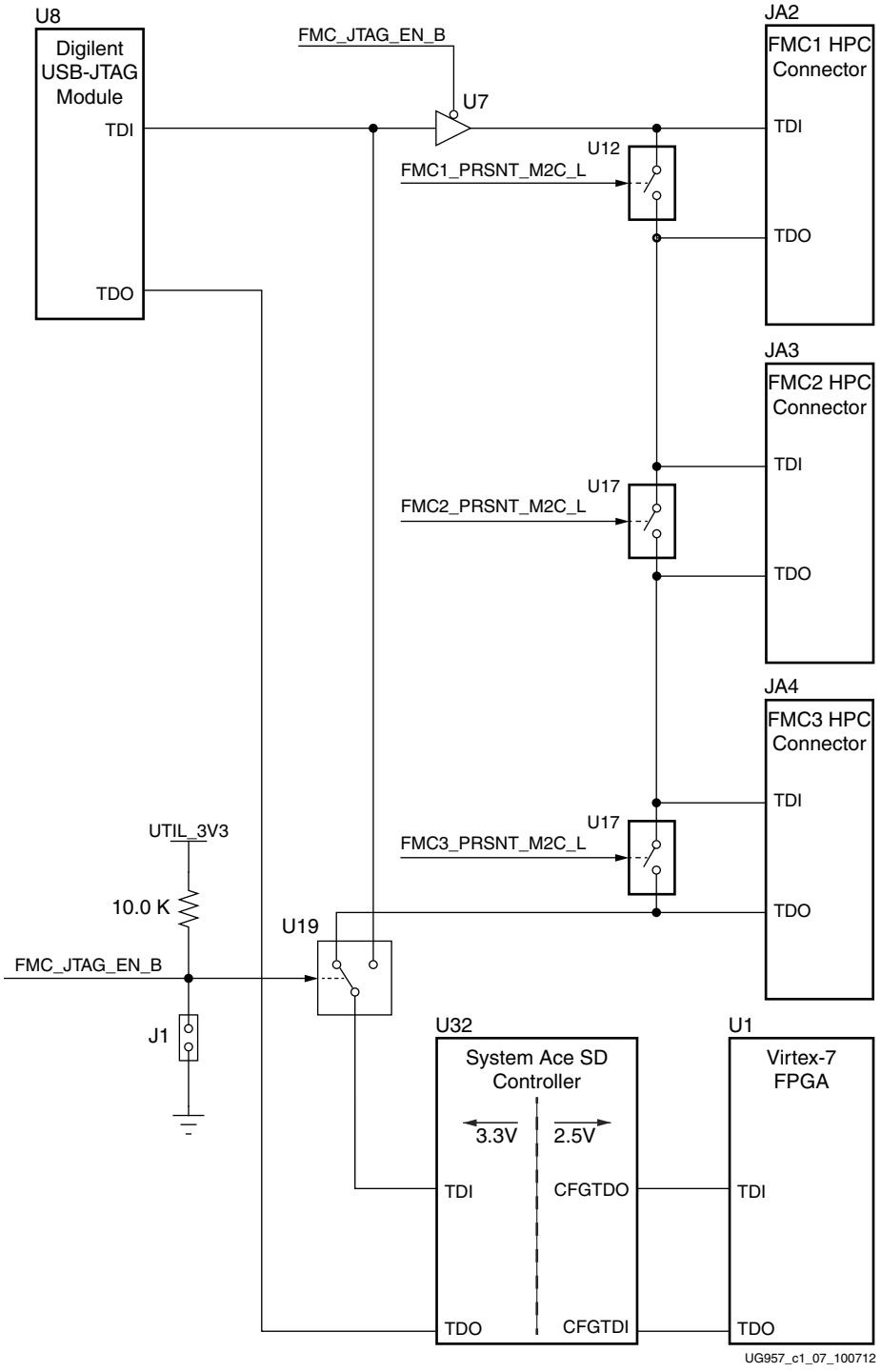

Figure 1-7: **JTAG Chain**

PROG_B Push Button

Pressing the PROG push button SW3 (callout 14, Figure 1-2) grounds the active-Low program pin of the FPGA.

DONE LED

The DONE LED DS21 (callout 12, Figure 1-2) indicates the state of the DONE pin of the FPGA. When the DONE pin is High, DS21 lights indicating the FPGA is successfully configured.

INIT LED

The dual-color INIT LED DS25 (callout 13, Figure 1-2) indicates the FPGA's initialization status. During FPGA initialization the INIT LED illuminates RED. When FPGA initialization has completed the LED illuminates GREEN.

System ACE SD Controller

The onboard System ACE SD controller U32 allows storage of multiple configuration files on a Secure Digital (SD) card. These configuration files can be used to program the FPGA. The SD card connects to the SD card connector J211 (callout 7, Figure 1-2) located directly below the System ACE SD controller on the back side of the board.

System ACE SD Controller Reset

Pressing the SASD RESET push button SW7 (callout 9, Figure 1-2) resets the System ACE SD controller. The reset pin is an active-Low input.

System ACE SD Configuration Address DIP Switches

DIP switch SW8 shown in Figure 1-8 selects one of the eight configuration bitstream addresses in the SD memory card. A switch is in the ON position if set to the far right and in the OFF position if set to the far left. The MODE bit (switch position 4) is not used and can be set either ON or OFF. SW8 is shown in Figure 1-2 as callout 8.

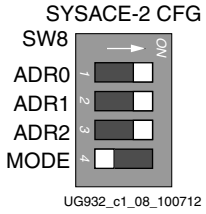

Figure 1-8: **Configuration Address DIP Switch (SW8)**

The switch settings for selecting each address are shown in Table 1-6.

Table 1-6: **SW8 DIP Switch Configuration**

Configuration Bitstream Address	ADR2	ADR1	ADR0
0	ON	ON	ON
1	ON	ON	OFF

Table 1-6: **SW8 DIP Switch Configuration *(Cont'd)***

Configuration Bitstream Address	ADR2	ADR1	ADR0
2	ON	OFF	ON
3	ON	OFF	OFF
4	OFF	ON	ON
5	OFF	ON	OFF
6	OFF	OFF	ON
7	OFF	OFF	OFF

200 MHz 2.5V LVDS Oscillator

U35 (callout 11, Figure 1-2).

The VC7203 board has one 200 MHz 2.5V LVDS oscillator (U35) connected to multi-region clock capable (MRCC) inputs on the FPGA. Table 1-7 lists the FPGA pin connections to the LVDS oscillator.

Table 1-7: **LVDS Oscillator MRCC Connections**

U1 FPGA Pin	Net Name	U35 Pin
E19	IO_LVDS_OSC_P	4
E18	IO_LVDS_OSC_N	5

Differential SMA MRCC Pin Inputs

Callout 30, Figure 1-2.

The VC7203 board provides two pairs of differential SMA transceiver clock inputs that can be used for connecting to an external function generator. The FPGA MRCC pins are connected to the SMA connectors as shown in Table 1-8.

Table 1-8: **Differential SMA Clock Connections**

U1 FPGA Pin	Net Name	SMA Connector
H19	CLK_DIFF_1_P	J99
G18	CLK_DIFF_1_N	J100
K39	CLK_DIFF_2_P	J98
K40	CLK_DIFF_2_N	J101

SuperClock-2 Module

Callout 10, Figure 1-2.

The SuperClock-2 module connects to the clock module interface connector (J82) and provides a programmable, low-noise and low-jitter clock source for the VC7203 board. The clock module maps to FPGA I/O by way of 24 control pins, 3 LVDS pairs, 1 regional clock pair, and 1 reset pin. Table 1-9 shows the FPGA I/O mapping for the SuperClock-2 module

interface. The VC7203 board also supplies UTIL_5V0, UTIL_3V3, UTIL_2V5 and VCCO_HR input power to the clock module interface.

Table 1-9: **SuperClock-2 FPGA I/O Mapping**

U1 FPGA Pin	Net Name	J82 Pin
E12	CM_LVDS1_P	1
D12	CM_LVDS1_N	3
L12	CM_LVDS2_P	9
L11	CM_LVDS2_N	11
BA12	CM_LVDS3_P	17
BB12	CM_LVDS3_N	19
K19	CM_GCLK_P	25
J18	CM_GCLK_N	27
C19	CM_CTRL_0	61
B19	CM_CTRL_1	63
A16	CM_CTRL_2	65
A15	CM_CTRL_3	67
A20	CM_CTRL_4	69
A19	CM_CTRL_5	71
B17	CM_CTRL_6	73
A17	CM_CTRL_7	75
B21	CM_CTRL_8	77
A21	CM_CTRL_9	79
C18	CM_CTRL_10	81
B18	CM_CTRL_11	83
D20	CM_CTRL_12	85
C20	CM_CTRL_13	87
F17	CM_CTRL_14	89
E17	CM_CTRL_15	91
D21	CM_CTRL_16	93
C21	CM_CTRL_17	95
D18	CM_CTRL_18	97
D17	CM_CTRL_19	99
F20	CM_CTRL_20	101
E20	CM_CTRL_21	103
K17	CM_CTRL_22	105

Table 1-9: **SuperClock-2 FPGA I/O Mapping *(Cont'd)***

U1 FPGA Pin	Net Name	J82 Pin
J17	CM_CTRL_23	107
J20	CM_RST	66

User LEDs (Active High)

Callout 23, Figure 1-2.

DS13 through DS20 are eight active-High LEDs that are connected to user I/O pins on the FPGA as shown in Table 1-11 These LEDs can be used to indicate status or any other purpose determined by the user.

Table 1-10: **User LEDs**

U1 FPGA Pin	Net Name	Reference Designator
M37	APP_LED1	DS19
M38	APP_LED2	DS20
R42	APP_LED3	DS17
P42	APP_LED4	DS18
N38	APP_LED5	DS16
M39	APP_LED6	DS15
R40	APP_LED7	DS13
P40	APP_LED8	DS14

User DIP Switches (Active High) and I/O Header

Callout 25, Figure 1-2.

The DIP switch SW2 provides a set of eight active-High switches that are connected to user I/O pins on the FPGA as shown in Table 1-11. These pins can be used to set control pins or any other purpose determined by the user. Six of the eight I/Os also map to 2 x 6 test header J125 providing external access for these pins (callout 26, Figure 1-2.).

Table 1-11: **User DIP Switches**

U1 FPGA Pin	Net Name	DIP Switch Reference Designator	J125 Test Header Pin
E42	USER_SW1	SW2	2
C40	USER_SW2		4
C41	USER_SW3		6
H40	USER_SW4		8
H41	USER_SW5		10
H39	USER_SW6		12
G39	USER_SW7		
G41	USER_SW8		

Figure 1-9 Shows the user test I/O connector J125 (Callout 26, Figure 1-2).

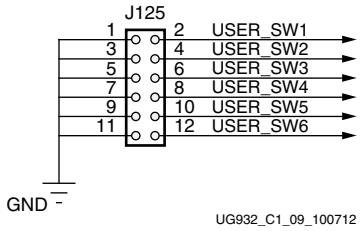

Figure 1-9: **User Test I/O**

User Push Buttons (Active High)

Callout 24, Figure 1-2.

SW4 and SW5 are active-High user push buttons that are connected to user I/O pins on the FPGA as shown in Table 1-12. These switches can be used for any purpose determined by the user.

Table 1-12: **User Push Buttons**

U1 FPGA Pin	Net Name	Reference Designator
P41	USER_PB1	SW5
N41	USER_PB2	SW4

GTX Transceivers and Reference Clocks

Callout 4, Figure 1-2.

The VC7203 board provides access to all GTX transceiver and reference clock pins on the FPGA as shown in Figure 1-10. The GTX transceivers are grouped into nine sets of four RX-TX *lanes*. Four lanes are referred to as a *Quad*.

Note: QUAD 111 and QUAD 112 do not connect to pins on the XCV485T.

Note: Figure 1-10 is for reference only and might not reflect the current revision of the board.

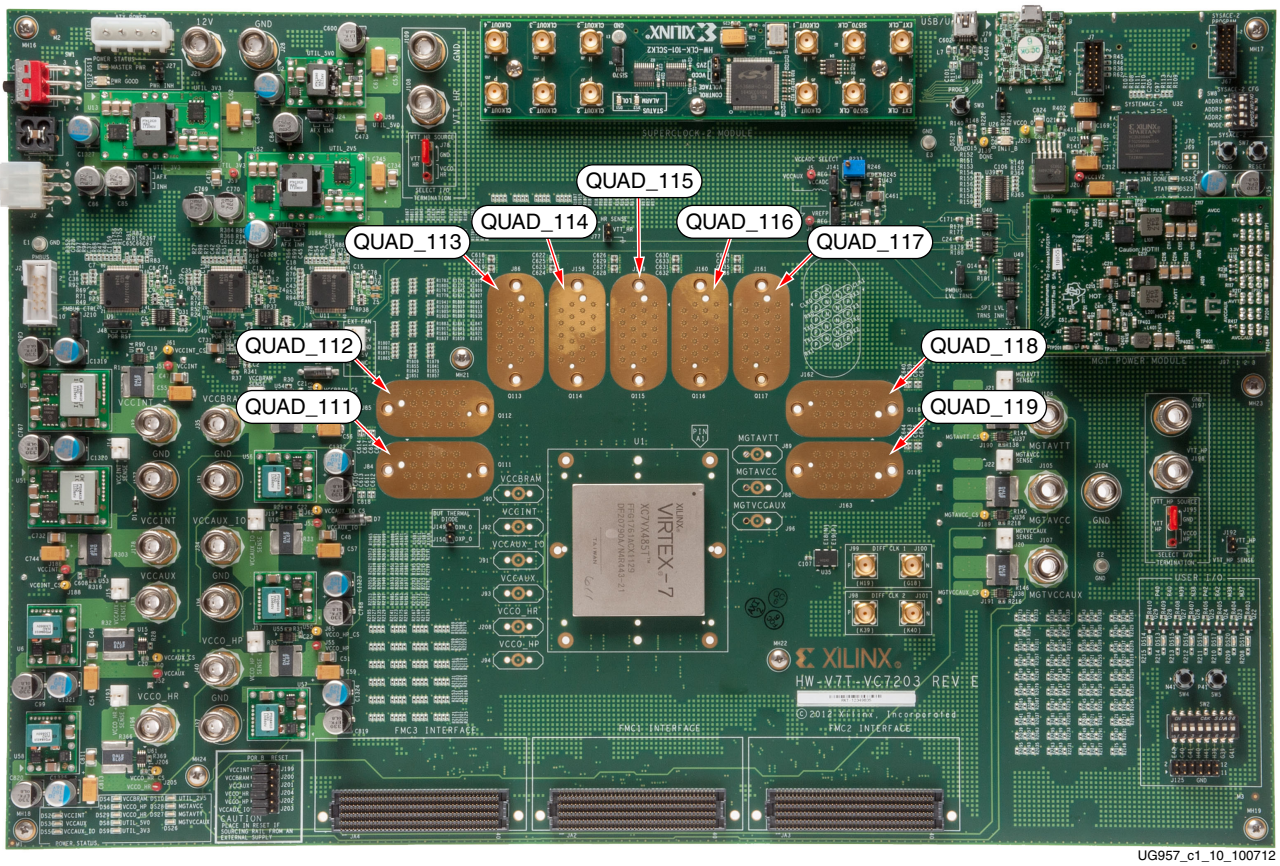

Figure 1-10: **GTX Quad Locations**

Each GTX Quad and its associated reference clocks (CLK0 and CLK1) are brought out to a connector pad which interfaces with Samtec BullsEye connectors used with the Samtec HDR-155805-01-BEYE cable assembly. Contact Samtec, Inc. for information about this or other cable assemblies. Figure 1-11 *A* shows the connector pad. Figure 1-11 *B* shows the connector pinout.

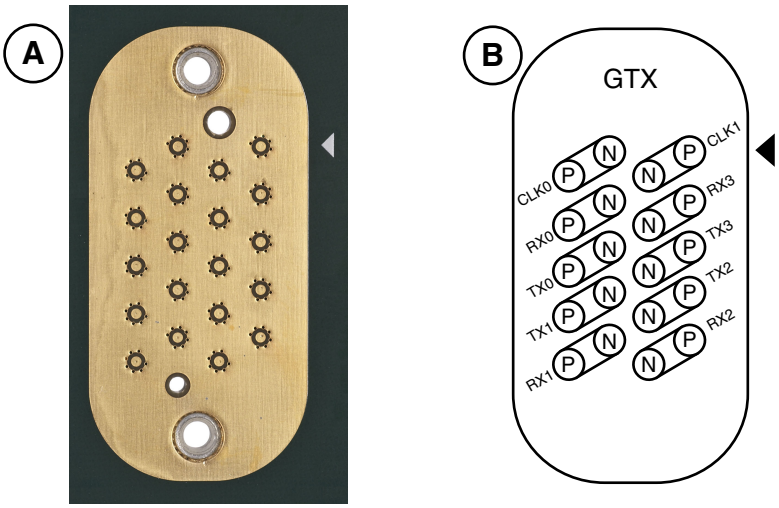

Figure 1-11: **A – GTX Connector Pad. B – GTX Connector Pinout**

Information for each GTX transceiver pin is shown in Table 1-13.

Table 1-13: **GTX Transceiver Pins**

U1 FPGA Pin	Net Name	Quad	Connector	Trace Length (mils)
Y2	115_TX0_P	115	J83	2,805
Y1	115_TX0_N	115	J83	2,806
AA4	115_RX0_P	115	J83	2,898
AA3	115_RX0_N	115	J83	2,898
V2	115_TX1_P	115	J83	2,525
V1	115_TX1_N	115	J83	2,523
Y6	115_RX1_P	115	J83	2,489
Y5	115_RX1_N	115	J83	2,489
U4	115_TX2_P	115	J83	2,549
U3	115_TX2_N	115	J83	2,549
W4	115_RX2_P	115	J83	2,308
W3	115_RX2_N	115	J83	2,309
T2	115_TX3_P	115	J83	2,840
T1	115_TX3_N	115	J83	2,840
V6	115_RX3_P	115	J83	2,933
V5	115_RX3_N	115	J83	2,933
P2	116_TX0_P	116	J84	2,677
P1	116_TX0_N	116	J84	2,677

Table 1-13: **GTX Transceiver Pins *(Cont'd)***

U1 FPGA Pin	Net Name	Quad	Connector	Trace Length (mils)
T6	116_RX0_P	116	J84	2,667
T5	116_RX0_N	116	J84	2,668
N4	116_TX1_P	116	J84	2,469
N3	116_TX1_N	116	J84	2,469
R4	116_RX1_P	116	J84	2,207
R3	116_RX1_N	116	J84	2,207
M2	116_TX2_P	116	J84	2,359
M1	116_TX2_N	116	J84	2,357
P6	116_RX2_P	116	J84	2,218
P5	116_RX2_N	116	J84	2,218
L4	116_TX3_P	116	J84	2,555
L3	116_TX3_N	116	J84	2,555
M6	116_RX3_P	116	J84	2,821
M5	116_RX3_N	116	J84	2,821
K2	117_TX0_P	117	J85	2,617
K1	117_TX0_N	117	J85	2,616
K6	117_RX0_P	117	J85	2,886
K5	117_RX0_N	117	J85	2,886
J4	117_TX1_P	117	J85	2,400
J3	117_TX1_N	117	J85	2,401
H6	117_RX1_P	117	J85	2,337
H5	117_RX1_N	117	J85	2,337
H2	117_TX2_P	117	J85	2,635
H1	117_TX2_N	117	J85	2,634
G4	117_RX2_P	117	J85	2,349
G3	117_RX2_N	117	J85	2,349
F2	117_TX3_P	117	J85	2,823
F1	117_TX3_N	117	J85	2,823
F6	117_RX3_P	117	J85	2,873
F5	117_RX3_N	117	J85	2,872
D2	118_TX0_P	118	J86	2,842
D1	118_TX0_N	118	J86	2,844

Table 1-13: **GTX Transceiver Pins *(Cont'd)***

U1 FPGA Pin	Net Name	Quad	Connector	Trace Length (mils)
E4	118_RX0_P	118	J86	3,048
E3	118_RX0_N	118	J86	3,049
C4	118_TX1_P	118	J86	2,629
C3	118_TX1_N	118	J86	2,628
D6	118_RX1_P	118	J86	2,597
D5	118_RX1_N	118	J86	2,597
B2	118_TX2_P	118	J86	2,787
B1	118_TX2_N	118	J86	2,789
B6	118_RX2_P	118	J86	2,681
B5	118_RX2_N	118	J86	2,680
A4	118_TX3_P	118	J86	3,044
A3	118_TX3_N	118	J86	3,044
A8	118_RX3_P	118	J86	3,515
A7	118_RX3_N	118	J86	3,515

Information for each GTX transceiver clock input is shown in Table 1-14.

Table 1-14: **GTX Transceiver Reference Clock Inputs**

U1 FPGA Pin	Net Name	Quad	Connector
R8	115_REFCLK0_P	115	J83
R7	115_REFCLK0_N	115	J83
U8	115_REFCLK1_P	115	J83
U7	115_REFCLK1_N	115	J83
L8	116_REFCLK0_P	116	J84
L7	116_REFCLK0_N	116	J84
N8	116_REFCLK1_P	116	J84
N7	116_REFCLK1_N	116	J84
G8	117_REFCLK0_P	117	J85
G7	117_REFCLK0_N	117	J85
J8	117_REFCLK1_P	117	J85
J7	117_REFCLK1_N	117	J85
C8	118_REFCLK0_P	118	J86
C7	118_REFCLK0_N	118	J86

Table 1-14: **GTX Transceiver Reference Clock Inputs *(Cont'd)***

U1 FPGA Pin	Net Name	Quad	Connector
E8	118_REFCLK1_P	118	J86
E7	118_REFCLK1_N	118	J86

USB-to-UART Bridge

Callout 21, Figure 1-2.

A USB-to-UART bridge (U34, Silicon Laboratories CP2103) is provided for serial communication between a host computer and the FPGA over a USB cable. The USB connector on the board is a mini-B receptacle (J79) and its pinout is shown in Table 1-15.

Table 1-15: **USB Mini-B Receptacle Pin Assignments and Signals**

J79 Pin	Signal Name	Description
1	VBUS	+5V into the CP2103 USB-to-UART bridge at U34. Used to sense USB network connection.
2	USB_DATA_N	Bidirectional differential serial data (N-side).
3	USB_DATA_P	Bidirectional differential serial data (P-side).
4	GROUND	Signal ground.

The CP2103 supports an IO voltage range of 1.8V to 3.3V. Xilinx UART IP is expected to be implemented in the FPGA fabric. The FPGA supports the USB-to-UART bridge using four signal pins:

- Transmit (TX)
- Receive (RX)
- Request to Send (RTS)
- Clear to Send (CTS)

Connections of these signals between the FPGA and the CP2103 are listed in Table 1-16.

Table 1-16: **FPGA to UART Connections**

U1 FPGA Pin	FPGA Function	Net Name	U34 Pin	U34 Function
B31	RTS, output	USB_CTS_I_B	22	CTS, input
C31	CTS, input	USB_RTS_0_B	23	RTS, output
A30	TX, data out	USB_RXD_I	24	RXD, data in
A29	RX, data in	USB_TXD_0	25	TXD, data out

The bridge device also provides as many as 4 GPIO signals that can be defined by the user for status and control information (Table 1-17).

Table 1-17: **CP2103 USB-to-UART Bridge User GPIO**

U1 FPGA Pin	Net Name	U26 Pin
B28	USB_GPIO_0	19
B29	USB_GPIO_1	18
A31	USB_GPIO_2	17
A32	USB_GPIO_3	16

A royalty-free software driver named Virtual COM Port (VCP) is available from Silicon Laboratories. This driver permits the CP2103 USB-to-UART bridge to appear as a COM port to the host computer communications application software (for example, HyperTerminal or TeraTerm). The VCP driver must be installed on the host computer prior to establishing communications with the VC7203 board.

FPGA Mezzanine Card HPC Interface

Callout 27, 28, and 29, Figure 1-2.

The VC7203 board features three high pin count (HPC) connectors as defined by the VITA 57.1 FPGA Mezzanine card (FMC) specification. The FMC HPC connector is a 10 x 40 position socket. See Appendix B, VITA 57.1 FMC Connector Pinouts for a cross-reference of signal names to pin coordinates.

FMC1 HPC connector JA2 provides connectivity for:

- 69 differential user defined pairs:
  - 34 LA pairs
  - 18 HA pairs
  - 17 HB pairs
- 2 differential clocks

FMC2 HPC connector JA3 provides connectivity for:

- 80 differential user defined pairs:
  - 34 LA pairs
  - 24 HA pairs
  - 22 HB pairs
- 4 differential clocks

FMC3 HPC connector JA4 provides connectivity for:

- 65 differential user defined pairs:
  - 34 LA pairs
  - 16 HA pairs
  - 15 HB pairs
- 4 differential clocks

Note: FMC3 is not supported by the XC7V485T device. The IO banks that connect to FMC3 are not available in this density.

Note: The V_{ADJ} voltage on the three FMC HPC connectors tracks VCCO_HP.

The FMC HPC connectors on the VC7203 board are identified as FMC1 at JA2, FMC2 at JA3 and FMC3 at JA4. The connections for each of these connectors are listed in Table 1-18 and Table 1-19, page 32 respectively.

Table 1-18: **VITA 57.1 FMC1 HPC Connections at JA2**

U1 FPGA Pin	Net Name	FMC Pin
AJ32	FMC1_CLK0_M2C_P	H4
AK32	FMC1_CLK0_M2C_N	H5
AL31	FMC1_CLK1_M2C_P	G2
AL32	FMC1_CLK1_M2C_N	G3
AD32	FMC1_CLK2_BIDIR_P	K4
AD33	FMC1_CLK2_BIDIR_N	K5
AC34	FMC1_CLK3_BIDIR_P	J2
AD35	FMC1_CLK3_BIDIR_N	J3
AV40	FMC1_HA00_CC_P	F4
AW40	FMC1_HA00_CC_N	F5
AY39	FMC1_HA01_CC_P	E2
AY40	FMC1_HA01_CC_N	E3
AT41	FMC1_HA02_P	K7
AU42	FMC1_HA02_N	K8
AY42	FMC1_HA03_P	J6
BA42	FMC1_HA03_N	J7
AU41	FMC1_HA04_P	F7
AV41	FMC1_HA04_N	F8
BA41	FMC1_HA05_P	E6
BB41	FMC1_HA05_N	E7
AW41	FMC1_HA06_P	K10
AW42	FMC1_HA06_N	K11
AJ30	FMC1_HA07_P	J9
AK30	FMC1_HA07_N	J10
AF29	FMC1_HA08_P	F10
AG29	FMC1_HA08_N	F11
AK28	FMC1_HA09_P	E9
AK29	FMC1_HA09_N	E10
AF30	FMC1_HA10_P	K13
AG31	FMC1_HA10_N	K14

Table 1-18: **VITA 57.1 FMC1 HPC Connections at JA2 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
AH28	FMC1_HA11_P	J12
AJ28	FMC1_HA11_N	J13
AC31	FMC1_HA12_P	F13
AD31	FMC1_HA12_N	F14
AA31	FMC1_HA13_P	E12
AA32	FMC1_HA13_N	E13
AC30	FMC1_HA14_P	J15
AD30	FMC1_HA14_N	J16
AA29	FMC1_HA15_P	F16
AA30	FMC1_HA15_N	F17
AB29	FMC1_HA16_P	E15
AC29	FMC1_HA16_N	E16
AB33	FMC1_HB00_CC_P	K25
AC33	FMC1_HB00_CC_N	K26
AF35	FMC1_HB01_P	J24
AF36	FMC1_HB01_N	J25
AE37	FMC1_HB02_P	F22
AF37	FMC1_HB02_N	F23
AF34	FMC1_HB03_P	E21
AG34	FMC1_HB03_N	E22
AD36	FMC1_HB04_P	F25
AD37	FMC1_HB04_N	F26
AC35	FMC1_HB05_P	E24
AC36	FMC1_HB05_N	E25
AB31	FMC1_HB06_CC_P	K28
AB32	FMC1_HB06_CC_N	K29
AG36	FMC1_HB07_P	J27
AH36	FMC1_HB07_N	J28
Y37	FMC1_HB08_P	F28
AA37	FMC1_HB08_N	F29
Y35	FMC1_HB09_P	E27
AA36	FMC1_HB09_N	E28
AB36	FMC1_HB10_P	K31

Table 1-18: **VITA 57.1 FMC1 HPC Connections at JA2 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
AB37	FMC1_HB10_N	K32
AA34	FMC1_HB11_P	J30
AA35	FMC1_HB11_N	J31
AE32	FMC1_HB12_P	F31
AE33	FMC1_HB12_N	F32
AF31	FMC1_HB13_P	E30
AF32	FMC1_HB13_N	E31
AE34	FMC1_HB14_P	K34
AE35	FMC1_HB14_N	K35
AE29	FMC1_HB15_P	J33
AE30	FMC1_HB15_N	J34
Y32	FMC1_HB16_P	F34
Y33	FMC1_HB16_N	F35
AU38	FMC1_LA00_CC_P	G6
AV38	FMC1_LA00_CC_N	G7
AU39	FMC1_LA01_CC_P	D8
AV39	FMC1_LA01_CC_N	D9
AN38	FMC1_LA02_P	H7
AP38	FMC1_LA02_N	H8
AM41	FMC1_LA03_P	G9
AM42	FMC1_LA03_N	G10
AR38	FMC1_LA04_P	H10
AR39	FMC1_LA04_N	H11
AN40	FMC1_LA05_P	D11
AN41	FMC1_LA05_N	D12
AR37	FMC1_LA06_P	C10
AT37	FMC1_LA06_N	C11
AM39	FMC1_LA07_P	H13
AN39	FMC1_LA07_N	H14
AP40	FMC1_LA08_P	G12
AR40	FMC1_LA08_N	G13
AP41	FMC1_LA09_P	D14
AP42	FMC1_LA09_N	D15

Table 1-18: **VITA 57.1 FMC1 HPC Connections at JA2 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
AT39	FMC1_LA10_P	C14
AT40	FMC1_LA10_N	C15
AR42	FMC1_LA11_P	H16
AT42	FMC1_LA11_N	H17
AW37	FMC1_LA12_P	G15
AY37	FMC1_LA12_N	G16
BA37	FMC1_LA13_P	D17
BB37	FMC1_LA13_N	D18
AW38	FMC1_LA14_P	C18
AY38	FMC1_LA14_N	C19
BB38	FMC1_LA15_P	H19
BB39	FMC1_LA15_N	H20
BA39	FMC1_LA16_P	G18
BA40	FMC1_LA16_N	G19
AK34	FMC1_LA17_CC_P	D20
AL34	FMC1_LA17_CC_N	D21
AJ33	FMC1_LA18_CC_P	C22
AK33	FMC1_LA18_CC_N	C23
AM36	FMC1_LA19_P	H22
AN36	FMC1_LA19_N	H23
AJ36	FMC1_LA20_P	G21
AJ37	FMC1_LA20_N	G22
AP36	FMC1_LA21_P	H25
AP37	FMC1_LA21_N	H26
AK37	FMC1_LA22_P	G24
AL37	FMC1_LA22_N	G25
AN35	FMC1_LA23_P	D23
AP35	FMC1_LA23_N	D24
AL36	FMC1_LA24_P	H28
AM37	FMC1_LA24_N	H29
AG33	FMC1_LA25_P	G27
AH33	FMC1_LA25_N	G28
AK35	FMC1_LA26_P	D26

Table 1-18: **VITA 57.1 FMC1 HPC Connections at JA2 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
AL35	FMC1_LA26_N	D27
AH31	FMC1_LA27_P	C26
AJ31	FMC1_LA27_N	C27
AH34	FMC1_LA28_P	H31
AJ35	FMC1_LA28_N	H32
AM34	FMC1_LA29_P	G30
AN34	FMC1_LA29_N	G31
AM31	FMC1_LA30_P	H34
AM32	FMC1_LA30_N	H35
AM33	FMC1_LA31_P	G33
AN33	FMC1_LA31_N	G34
AL29	FMC1_LA32_P	H37
AL30	FMC1_LA32_N	H38
AH29	FMC1_LA33_P	G36
AH30	FMC1_LA33_N	G37
AM38	FMC1_PRSNT_M2C_L	H2

Table 1-19: **VITA 57.1 FMC1 HPC Connections at JA3**

U1 FPGA Pin	Net Name	FMC Pin
E34	FMC2_CLK0_M2C_P	H4
E35	FMC2_CLK0_M2C_N	H5
D37	FMC2_CLK1_M2C_P	G2
D38	FMC2_CLK1_M2C_N	G3
M24	FMC2_CLK2_BIDIR_P	K4
L24	FMC2_CLK2_BIDIR_N	K5
K23	FMC2_CLK3_BIDIR_P	J2
J23	FMC2_CLK3_BIDIR_N	J3
N30	FMC2_HA00_CC_P	F4
M31	FMC2_HA00_CC_N	F5
P30	FMC2_HA01_CC_P	E2
N31	FMC2_HA01_CC_N	E3
V30	FMC2_HA02_P	K7

Table 1-19: **VITA 57.1 FMC1 HPC Connections at JA3 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
V31	FMC2_HA02_N	K8
T29	FMC2_HA03_P	J6
T30	FMC2_HA03_N	J7
W30	FMC2_HA04_P	F7
W31	FMC2_HA04_N	F8
V29	FMC2_HA05_P	E6
U29	FMC2_HA05_N	E7
Y29	FMC2_HA06_P	K10
Y30	FMC2_HA06_N	K11
G36	FMC2_HA07_P	J9
G37	FMC2_HA07_N	J10
F39	FMC2_HA08_P	F10
E39	FMC2_HA08_N	F11
J37	FMC2_HA09_P	E9
J38	FMC2_HA09_N	E10
H38	FMC2_HA10_P	K13
G38	FMC2_HA10_N	K14
J36	FMC2_HA11_P	J12
H36	FMC2_HA11_N	J13
P25	FMC2_HA12_P	F13
P26	FMC2_HA12_N	F14
P22	FMC2_HA13_P	E12
P23	FMC2_HA13_N	E13
N25	FMC2_HA14_P	J15
N26	FMC2_HA14_N	J16
N23	FMC2_HA15_P	F16
N24	FMC2_HA15_N	F17
M27	FMC2_HA16_P	E15
L27	FMC2_HA16_N	E16
J25	FMC2_HB00_CC_P	K25
J26	FMC2_HB00_CC_N	K26
H24	FMC2_HB01_P	J24
G24	FMC2_HB01_N	J25

Table 1-19: **VITA 57.1 FMC1 HPC Connections at JA3 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
J21	FMC2_HB02_P	F22
H21	FMC2_HB02_N	F23
H25	FMC2_HB03_P	E21
H26	FMC2_HB03_N	E22
G21	FMC2_HB04_P	F25
G22	FMC2_HB04_N	F26
G26	FMC2_HB05_P	E24
G27	FMC2_HB05_N	E25
K24	FMC2_HB06_CC_P	K28
K25	FMC2_HB06_CC_N	K29
H23	FMC2_HB07_P	J27
G23	FMC2_HB07_N	J28
G28	FMC2_HB08_P	F28
G29	FMC2_HB08_N	F29
K28	FMC2_HB09_P	E27
J28	FMC2_HB09_N	E28
H28	FMC2_HB10_P	K31
H29	FMC2_HB10_N	K32
K27	FMC2_HB11_P	J30
J27	FMC2_HB11_N	J31
M22	FMC2_HB12_P	F31
L22	FMC2_HB12_N	F32
L25	FMC2_HB13_P	E30
L26	FMC2_HB13_N	E31
K22	FMC2_HB14_P	K34
J22	FMC2_HB14_N	K35
M21	FMC2_HB15_P	J33
L21	FMC2_HB15_N	J34
P21	FMC2_HB16_P	F34
N21	FMC2_HB16_N	F35
L31	FMC2_LA00_CC_P	G6
K32	FMC2_LA00_CC_N	G7
M32	FMC2_LA01_CC_P	D8

Table 1-19: **VITA 57.1 FMC1 HPC Connections at JA3 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
L32	FMC2_LA01_CC_N	D9
K35	FMC2_LA02_P	H7
J35	FMC2_LA02_N	H8
J32	FMC2_LA03_P	G9
J33	FMC2_LA03_N	G10
K33	FMC2_LA04_P	H10
K34	FMC2_LA04_N	H11
L34	FMC2_LA05_P	D11
L35	FMC2_LA05_N	D12
M33	FMC2_LA06_P	C10
M34	FMC2_LA06_N	C11
H34	FMC2_LA07_P	H13
H35	FMC2_LA07_N	H14
K29	FMC2_LA08_P	G12
K30	FMC2_LA08_N	G13
J30	FMC2_LA09_P	D14
H30	FMC2_LA09_N	D15
L29	FMC2_LA10_P	C14
L30	FMC2_LA10_N	C15
J31	FMC2_LA11_P	H16
H31	FMC2_LA11_N	H17
M28	FMC2_LA12_P	G15
M29	FMC2_LA12_N	G16
R28	FMC2_LA13_P	D17
P28	FMC2_LA13_N	D18
N28	FMC2_LA14_P	C18
N29	FMC2_LA14_N	C19
R30	FMC2_LA15_P	H19
P31	FMC2_LA15_N	H20
U31	FMC2_LA16_P	G18
T31	FMC2_LA16_N	G19
C35	FMC2_LA17_CC_P	D20
C36	FMC2_LA17_CC_N	D21

Table 1-19: **VITA 57.1 FMC1 HPC Connections at JA3 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
D35	FMC2_LA18_CC_P	C22
D36	FMC2_LA18_CC_N	C23
B36	FMC2_LA19_P	H22
A37	FMC2_LA19_N	H23
B34	FMC2_LA20_P	G21
A34	FMC2_LA20_N	G22
B39	FMC2_LA21_P	H25
A39	FMC2_LA21_N	H26
A35	FMC2_LA22_P	G24
A36	FMC2_LA22_N	G25
C38	FMC2_LA23_P	D23
C39	FMC2_LA23_N	D24
B37	FMC2_LA24_P	H28
B38	FMC2_LA24_N	H29
E32	FMC2_LA25_P	G27
D32	FMC2_LA25_N	G28
B32	FMC2_LA26_P	D26
B33	FMC2_LA26_N	D27
E33	FMC2_LA27_P	C26
D33	FMC2_LA27_N	C27
C33	FMC2_LA28_P	H31
C34	FMC2_LA28_N	H32
G32	FMC2_LA29_P	G30
F32	FMC2_LA29_N	G31
F36	FMC2_LA30_P	H34
F37	FMC2_LA30_N	H35
F34	FMC2_LA31_P	G33
F35	FMC2_LA31_N	G34
H33	FMC2_LA32_P	H37
G33	FMC2_LA32_N	H38
E37	FMC2_LA33_P	G36
E38	FMC2_LA33_N	G37
G31	FMC2_PRSNT_M2C_L	H2

Table 1-20: **VITA 57.1 FMC1 HPC Connections at JA4**

U1 FPGA Pin	Net Name	FMC Pin
AY18	FMC3_CLK0_M2C_P	H4
AY17	FMC3_CLK0_M2C_N	H5
AW18	FMC3_CLK1_M2C_P	G2
AW17	FMC3_CLK1_M2C_N	G3
H15	FMC3_CLK2_BIDIR_P	K4
H14	FMC3_CLK2_BIDIR_N	K5
J13	FMC3_CLK3_BIDIR_P	J2
H13	FMC3_CLK3_BIDIR_N	J3
AU14	FMC3_HA00_CC_P	F4
AU13	FMC3_HA00_CC_N	F5
AV13	FMC3_HA01_CC_P	E2
AW13	FMC3_HA01_CC_N	E3
AW12	FMC3_HA02_P	K7
AY12	FMC3_HA02_N	K8
BA15	FMC3_HA03_P	J6
BA14	FMC3_HA03_N	J7
AY14	FMC3_HA04_P	F7
AY13	FMC3_HA04_N	F8
BB14	FMC3_HA05_P	E6
BB13	FMC3_HA05_N	E7
AV20	FMC3_HA06_P	K10
AW20	FMC3_HA06_N	K11
BA17	FMC3_HA07_P	J9
BB17	FMC3_HA07_N	J10
AY20	FMC3_HA08_P	F10
BA20	FMC3_HA08_N	F11
BA16	FMC3_HA09_P	E9
BB16	FMC3_HA09_N	E10
AY19	FMC3_HA10_P	K13
BA19	FMC3_HA10_N	K14
C16	FMC3_HA11_P	J12
B16	FMC3_HA11_N	J13

Table 1-20: **VITA 57.1 FMC1 HPC Connections at JA4 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
B14	FMC3_HA12_P	F13
A14	FMC3_HA12_N	F14
C15	FMC3_HA13_P	E12
C14	FMC3_HA13_N	E13
D13	FMC3_HA14_P	J15
C13	FMC3_HA14_N	J16
D16	FMC3_HA15_P	F16
D15	FMC3_HA15_N	F17
G14	FMC3_HB00_CC_P	K25
G13	FMC3_HB00_CC_N	K26
F16	FMC3_HB01_P	J24
E15	FMC3_HB01_N	J25
E14	FMC3_HB02_P	F22
E13	FMC3_HB02_N	F23
H16	FMC3_HB03_P	E21
G16	FMC3_HB03_N	E22
G12	FMC3_HB04_P	F25
F12	FMC3_HB04_N	F26
K12	FMC3_HB05_P	E24
J12	FMC3_HB05_N	E25
F15	FMC3_HB06_CC_P	K28
F14	FMC3_HB06_CC_N	K29
K15	FMC3_HB07_P	J27
J15	FMC3_HB07_N	J28
K14	FMC3_HB08_P	F28
K13	FMC3_HB08_N	F29
L16	FMC3_HB09_P	E27
L15	FMC3_HB09_N	E28
M14	FMC3_HB10_P	K31
L14	FMC3_HB10_N	K32
N16	FMC3_HB11_P	J30
M16	FMC3_HB11_N	J31
N13	FMC3_HB12_P	F31

Table 1-20: **VITA 57.1 FMC1 HPC Connections at JA4 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
M13	FMC3_HB12_N	F32
N15	FMC3_HB13_P	E30
N14	FMC3_HB13_N	E31
M12	FMC3_HB14_P	K34
M11	FMC3_HB14_N	K35
AP13	FMC3_LA00_CC_P	G6
AR13	FMC3_LA00_CC_N	G7
AR14	FMC3_LA01_CC_P	D8
AT14	FMC3_LA01_CC_N	D9
AJ16	FMC3_LA02_P	H7
AJ15	FMC3_LA02_N	H8
AK14	FMC3_LA03_P	G9
AK13	FMC3_LA03_N	G10
AK15	FMC3_LA04_P	H10
AL14	FMC3_LA04_N	H11
AJ13	FMC3_LA05_P	D11
AJ12	FMC3_LA05_N	D12
AL16	FMC3_LA06_P	C10
AL15	FMC3_LA06_N	C11
AK12	FMC3_LA07_P	H13
AL12	FMC3_LA07_N	H14
AM13	FMC3_LA08_P	G12
AN13	FMC3_LA08_N	G13
AM12	FMC3_LA09_P	D14
AM11	FMC3_LA09_N	D15
AN15	FMC3_LA10_P	C14
AN14	FMC3_LA10_N	C15
AN11	FMC3_LA11_P	H16
AP11	FMC3_LA11_N	H17
AP12	FMC3_LA12_P	G15
AR12	FMC3_LA12_N	G16
AR15	FMC3_LA13_P	D17
AT15	FMC3_LA13_N	D18

Table 1-20: **VITA 57.1 FMC1 HPC Connections at JA4 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
AT12	FMC3_LA14_P	C18
AU12	FMC3_LA14_N	C19
AV15	FMC3_LA15_P	H19
AV14	FMC3_LA15_N	H20
AW15	FMC3_LA16_P	G18
AY15	FMC3_LA16_N	G19
AT17	FMC3_LA17_CC_P	D20
AU17	FMC3_LA17_CC_N	D21
AU18	FMC3_LA18_CC_P	C22
AV18	FMC3_LA18_CC_N	C23
AL19	FMC3_LA19_P	H22
AM19	FMC3_LA19_N	H23
AK17	FMC3_LA20_P	G21
AL17	FMC3_LA20_N	G22
AM18	FMC3_LA21_P	H25
AM17	FMC3_LA21_N	H26
AK19	FMC3_LA22_P	G24
AK18	FMC3_LA22_N	G25
AM16	FMC3_LA23_P	D23
AN16	FMC3_LA23_N	D24
AJ18	FMC3_LA24_P	H28
AJ17	FMC3_LA24_N	H29
AP18	FMC3_LA25_P	G27
AP17	FMC3_LA25_N	G28
AP20	FMC3_LA26_P	D26
AR19	FMC3_LA26_N	D27
AN19	FMC3_LA27_P	C26
AN18	FMC3_LA27_N	C27
AR18	FMC3_LA28_P	H31
AR17	FMC3_LA28_N	H32
AU19	FMC3_LA29_P	G30
AV19	FMC3_LA29_N	G31
AT20	FMC3_LA30_P	H34

Table 1-20: **VITA 57.1 FMC1 HPC Connections at JA4 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
AT19	FMC3_LA30_N	H35
AV16	FMC3_LA31_P	G33
AW16	FMC3_LA31_N	G34
AT16	FMC3_LA32_P	H37
AU16	FMC3_LA32_N	H38
BB19	FMC3_LA33_P	G36
BB18	FMC3_LA33_N	G37
AR20	FMC3_PRSNT_M2C_L	H2

XADC

Callout 31, Figure 1-2.

7 Series FPGAs provide an Analog Front End (XADC) block. The XADC block includes a dual 12-bit, 1 MSPS Analog-to-Digital Convertor (ADC) and on-chip sensors.See UG480, 7 Series *FPGAs XADC User Guide* for details on the capabilities of the analog front end.

The VC7203 board provides two options for providing power (VCCADC) to the analog circuitry in the XADC. Either option can be selected by placing a shunt in one of two positions on the 3-pin VCCADC SELECT header, J141 (callout 31, Figure 1-2):

- **Pins 1-2 (VCCAUX):** In this configuration VCCADC is provided from VCCAUX through a low pass filter network.
- **Pin 2-3 (REG):** In this configuration VCCADC is provided by an on-board regulator, U43 (Analog Devices P/N ADP123AUJZ-R7). The output voltage of the regulator VCCADC can be adjusted using the potentiometer R233.

In addition, the VC7203 board provides two options for providing the reference voltage for the analog-to-digital converter. Either option can be selected by placing a shunt in one of two positions on the 3-pin VREF SEL header J142 (callout 31, Figure 1-2):

- **Pins 1-2 (REG):** In this configuration the ADC reference voltage is provided by an on-board, low-temperature coefficient 1.25V reference, U45 (Texas Instruments P/N REF3012AIDBZT)
- **Pin 2-3 (AGND):** In this configuration the VREFP on XADC is connected to analog ground and the ADC uses an on-chip reference.

I^{2}C Bus Management

The I^{2}C bus is controlled through U39, an 8-channel I^{2}C-bus multiplexer (NXP Semiconductor PCA9547). The FPGA communicates with the multiplexer through I^{2}C data and clock signals mapped to FPGA pins E21 and F21, respectively. The I^{2}C idcode for the PCA9547 device is `0x70`. The bus hosts four components:

- SuperClock-2 module
- 7 Series GTX transceiver power supply module

- FMC1
- FMC2
- FMC3

An I2C component can be accessed by selecting the appropriate channel through the control register of the MUX as shown in Table 1-21.

Table 1-21: **I2C Channel Assignments**

U39 Channel	I2C Component
0	SuperClock-2 module
1	7 Series GTX transceiver power supply module
2	FMC1
3	FMC2
7	FMC3

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Appendix A

Default Jumper Settings

Table A-1 lists the jumpers that must be installed on the VC7203 board for proper operation. These jumpers must be installed except where specifically noted in this user guide.

Note: Any jumper not listed in Table A-1 should be left open for normal operation.

Table A-1: **Default Jumper Settings**

Reference Designator	Name	Board Location	Jumper	Comments
J4	UTIL_3V3	Upper Left	AFX (1-2)	
J184	UTIL_2V5	Upper Left	AFX (1-2)	
J24	UTIL_5V0	Upper Left	AFX (1-2)	
J78	VTT_HR SOURCE	Upper Left	GND (1-2)	Red 20A jumper
J210	PMBUS CTRL	Upper Left	GND (2-3)	
J48		Upper Left	POR (1-2)	
J49		Upper Left	POR (1-2)	
J50		Upper Left	POR (1-2)	
J199	VCCINT	Lower Left	POR_B (1-2)	
J200	VCCBRAM	Lower Left	POR_B (1-2)	
J201	VCCAUX	Lower Left	POR_B (1-2)	
J204	VCCO_HR	Lower Left	POR_B (1-2)	
J202	VCCO_HP	Lower Left	POR_B (1-2)	
J203	VCCAUX_IO	Lower Left	POR_B (1-2)	
J141	VCCADC SELECT	Upper Center	VCCAUX (1-2)	
J142	VREF SEL	Upper Center	REG (1-2)	
J23	SPI LVL TRNS INH	Upper Right	Installed	
J195	VTT_HP SOURCE	Center Right	GND (1-2)	Red 20A jumper

VITA 57.1 FMC Connector Pinouts

Figure B-1 provides a cross-reference of signal names to pin coordinates for the VITA 57.1 FMC HPC connector.

	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	RES1	GND
2	GND	CLK3_M2C_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK3_M2C_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK2_M2C_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
5	CLK2_M2C_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND

UG957_ac_01_100712

Figure B-1: **FMC HPC Connector Pinout**

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Appendix C

Master UCF Listing

The VC7203 board master user constraints file (UCF) template provides for designs targeting the VC7203 Virtex-7 FPGA GTX Transceiver Characterization Board. Net names in the constraints listed below correlate with net names on the VC7203 board schematic. Users must identify the appropriate pins and replace the net names below with net names in the user RTL. See UG625, *Constraints Guide* for more information.

VC7203 Board UCF Listing

```
NET  IO_0_VRN_12                LOC = AN29 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L1P_T0_AD0P_12          LOC = AY27 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L1N_T0_AD0N_12          LOC = AY28 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L2P_T0_AD8P_12          LOC = AU29 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L2N_T0_AD8N_12          LOC = AV29 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L3P_T0_DQS_AD1P_12      LOC = BA26 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L3N_T0_DQS_AD1N_12      LOC = BA27 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L4P_T0_12               LOC = BB28 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L4N_T0_12               LOC = BB29 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L5P_T0_AD9P_12          LOC = BB26 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L5N_T0_AD9N_12          LOC = BB27 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L6P_T0_12               LOC = AY29 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L6N_T0_VREF_12          LOC = BA29 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L7P_T1_AD2P_12          LOC = AW25 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L7N_T1_AD2N_12          LOC = AW26 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L8P_T1_AD10P_12         LOC = AR29 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L8N_T1_AD10N_12         LOC = AT29 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L9P_T1_DQS_AD3P_12      LOC = AV25 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L9N_T1_DQS_AD3N_12      LOC = AV26 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L10P_T1_AD11P_12        LOC = AW27 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L10N_T1_AD11N_12        LOC = AW28 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L11P_T1_SRCC_12         LOC = AU28 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L11N_T1_SRCC_12         LOC = AV28 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L12P_T1_MRCC_12         LOC = AU26 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L12N_T1_MRCC_12         LOC = AU27 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L13P_T2_MRCC_12         LOC = AR27 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L13N_T2_MRCC_12         LOC = AT27 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L14P_T2_SRCC_12         LOC = AP27 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L14N_T2_SRCC_12         LOC = AR28 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L15P_T2_DQS_12          LOC = AN28 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L15N_T2_DQS_ADV_B_12    LOC = AP28 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L16P_T2_A28_12          LOC = AT25 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L16N_T2_A27_12          LOC = AT26 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L17P_T2_A26_12          LOC = AP25 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L17N_T2_A25_12          LOC = AR25 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L18P_T2_A24_12          LOC = AN25 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L18N_T2_A23_12          LOC = AN26 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L19P_T3_A22_12          LOC = AM28 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L19N_T3_A21_VREF_12     LOC = AM29 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L20P_T3_A20_12          LOC = AK27 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L20N_T3_A19_12          LOC = AL27 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L21P_T3_DQS_12          LOC = AM26 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L21N_T3_DQS_A18_12      LOC = AM27 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L22P_T3_A17_12          LOC = AK24 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L22N_T3_A16_12          LOC = AK25 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L23P_T3_FOE_B_12        LOC = AL25 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L23N_T3_FWE_B_12        LOC = AL26 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L24P_T3_RS1_12          LOC = AJ25 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_L24N_T3_RS0_12          LOC = AJ26 | IOSTANDARD=LVCMOS18; # Bank  12
NET  IO_25_VRP_12               LOC = AP26 | IOSTANDARD=LVCMOS18; # Bank  12
```

```
NET  IO_0_VRN_13              LOC = AR35 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L1P_T0_13             LOC = AY34 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L1N_T0_13             LOC = BA35 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L2P_T0_13             LOC = AV36 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L2N_T0_13             LOC = AW36 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L3P_T0_DQS_13         LOC = BA34 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L3N_T0_DQS_13         LOC = BB34 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L4P_T0_13             LOC = BA36 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L4N_T0_13             LOC = BB36 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L5P_T0_13             LOC = BB32 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L5N_T0_13             LOC = BB33 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L6P_T0_13             LOC = AW35 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L6N_T0_VREF_13        LOC = AY35 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L7P_T1_13             LOC = AT34 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L7N_T1_13             LOC = AU34 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L8P_T1_13             LOC = AT36 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L8N_T1_13             LOC = AU36 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L9P_T1_DQS_13         LOC = AT32 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L9N_T1_DQS_13         LOC = AU33 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L10P_T1_13            LOC = AR34 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L10N_T1_13            LOC = AT35 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L11P_T1_SRCC_13       LOC = AU32 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L11N_T1_SRCC_13       LOC = AV33 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L12P_T1_MRCC_13       LOC = AW32 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L12N_T1_MRCC_13       LOC = AW33 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L13P_T2_MRCC_13       LOC = AV34 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L13N_T2_MRCC_13       LOC = AV35 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L14P_T2_SRCC_13       LOC = AY32 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L14N_T2_SRCC_13       LOC = AY33 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L15P_T2_DQS_13        LOC = BA31 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L15N_T2_DQS_13        LOC = BA32 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L16P_T2_13            LOC = AW30 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L16N_T2_13            LOC = AY30 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L17P_T2_13            LOC = BA30 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L17N_T2_13            LOC = BB31 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L18P_T2_13            LOC = AV30 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L18N_T2_13            LOC = AW31 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L19P_T3_13            LOC = AR30 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L19N_T3_VREF_13       LOC = AT30 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L20P_T3_13            LOC = AU31 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L20N_T3_13            LOC = AV31 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L21P_T3_DQS_13        LOC = AN30 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L21N_T3_DQS_13        LOC = AP30 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L22P_T3_13            LOC = AP32 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L22N_T3_13            LOC = AR32 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L23P_T3_13            LOC = AN31 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L23N_T3_13            LOC = AP31 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L24P_T3_13            LOC = AP33 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_L24N_T3_13            LOC = AR33 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_25_VRP_13             LOC = AT31 | IOSTANDARD=LVCMOS18; # Bank  13
NET  IO_0_VRN_14              LOC = AH35 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_LA19_P              LOC = AM36 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_LA19_N              LOC = AN36 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_LA20_P              LOC = AJ36 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_LA20_N              LOC = AJ37 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_LA21_P              LOC = AP36 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_LA21_N              LOC = AP37 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_LA22_P              LOC = AK37 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_LA22_N              LOC = AL37 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_LA23_P              LOC = AN35 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_LA23_N              LOC = AP35 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_LA24_P              LOC = AL36 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_LA24_N              LOC = AM37 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_LA25_P              LOC = AG33 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_LA25_N              LOC = AH33 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_LA26_P              LOC = AK35 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_LA26_N              LOC = AL35 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_LA27_P              LOC = AH31 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_LA27_N              LOC = AJ31 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_LA28_P              LOC = AH34 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_LA28_N              LOC = AJ35 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_LA18_CC_P           LOC = AJ33 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_LA18_CC_N           LOC = AK33 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_LA17_CC_P           LOC = AK34 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_LA17_CC_N           LOC = AL34 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_CLK0_M2C_P          LOC = AJ32 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_CLK0_M2C_N          LOC = AK32 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_CLK1_M2C_P          LOC = AL31 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_CLK1_M2C_N          LOC = AL32 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_LA29_P              LOC = AM34 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_LA29_N              LOC = AN34 | IOSTANDARD=LVCMOS18; # Bank  14
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NET  FMC1_LA30_P              LOC = AM31 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_LA30_N              LOC = AM32 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_LA31_P              LOC = AM33 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_LA31_N              LOC = AN33 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_LA32_P              LOC = AL29 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_LA32_N              LOC = AL30 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_LA33_P              LOC = AH29 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_LA33_N              LOC = AH30 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_HA07_P              LOC = AJ30 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_HA07_N              LOC = AK30 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_HA08_P              LOC = AF29 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_HA08_N              LOC = AG29 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_HA09_P              LOC = AK28 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_HA09_N              LOC = AK29 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_HA10_P              LOC = AF30 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_HA10_N              LOC = AG31 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_HA11_P              LOC = AH28 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_HA11_N              LOC = AJ28 | IOSTANDARD=LVCMOS18; # Bank  14
NET  IO_25_VRP_14             LOC = AG32 | IOSTANDARD=LVCMOS18; # Bank  14
NET  FMC1_PRSNT_M2C_L         LOC = AM38 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_LA02_P              LOC = AN38 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_LA02_N              LOC = AP38 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_LA03_P              LOC = AM41 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_LA03_N              LOC = AM42 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_LA04_P              LOC = AR38 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_LA04_N              LOC = AR39 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_LA05_P              LOC = AN40 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_LA05_N              LOC = AN41 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_LA06_P              LOC = AR37 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_LA06_N              LOC = AT37 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_LA07_P              LOC = AM39 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_LA07_N              LOC = AN39 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_LA08_P              LOC = AP40 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_LA08_N              LOC = AR40 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_LA09_P              LOC = AP41 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_LA09_N              LOC = AP42 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_LA10_P              LOC = AT39 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_LA10_N              LOC = AT40 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_LA11_P              LOC = AR42 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_LA11_N              LOC = AT42 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_LA01_CC_P           LOC = AU39 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_LA01_CC_N           LOC = AV39 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_LA00_CC_P           LOC = AU38 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_LA00_CC_N           LOC = AV38 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_HA00_CC_P           LOC = AV40 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_HA00_CC_N           LOC = AW40 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_HA01_CC_P           LOC = AY39 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_HA01_CC_N           LOC = AY40 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_LA12_P              LOC = AW37 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_LA12_N              LOC = AY37 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_LA13_P              LOC = BA37 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_LA13_N              LOC = BB37 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_LA14_P              LOC = AW38 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_LA14_N              LOC = AY38 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_LA15_P              LOC = BB38 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_LA15_N              LOC = BB39 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_LA16_P              LOC = BA39 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_LA16_N              LOC = BA40 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_HA02_P              LOC = AT41 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_HA02_N              LOC = AU42 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_HA03_P              LOC = AY42 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_HA03_N              LOC = BA42 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_HA04_P              LOC = AU41 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_HA04_N              LOC = AV41 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_HA05_P              LOC = BA41 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_HA05_N              LOC = BB41 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_HA06_P              LOC = AW41 | IOSTANDARD=LVCMOS18; # Bank  15
NET  FMC1_HA06_N              LOC = AW42 | IOSTANDARD=LVCMOS18; # Bank  15
NET  IO_25_VRP_15             LOC = AU37 | IOSTANDARD=LVCMOS18; # Bank  15
NET  IO_0_VRN_16              LOC = Y34  | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HB01_P              LOC = AF35 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HB01_N              LOC = AF36 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HB02_P              LOC = AE37 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HB02_N              LOC = AF37 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HB03_P              LOC = AF34 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HB03_N              LOC = AG34 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HB04_P              LOC = AD36 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HB04_N              LOC = AD37 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HB05_P              LOC = AC35 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HB05_N              LOC = AC36 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HB07_P              LOC = AG36 | IOSTANDARD=LVCMOS18; # Bank  16
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NET  FMC1_HB07_N              LOC = AH36 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HB08_P              LOC = Y37  | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HB08_N              LOC = AA37 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HB09_P              LOC = Y35  | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HB09_N              LOC = AA36 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HB10_P              LOC = AB36 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HB10_N              LOC = AB37 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HB11_P              LOC = AA34 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HB11_N              LOC = AA35 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HB06_CC_P           LOC = AB31 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HB06_CC_N           LOC = AB32 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HB00_CC_P           LOC = AB33 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HB00_CC_N           LOC = AC33 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_CLK2_BIDIR_P        LOC = AD32 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_CLK2_BIDIR_N        LOC = AD33 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_CLK3_BIDIR_P        LOC = AC34 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_CLK3_BIDIR_N        LOC = AD35 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HB12_P              LOC = AE32 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HB12_N              LOC = AE33 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HB13_P              LOC = AF31 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HB13_N              LOC = AF32 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HB14_P              LOC = AE34 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HB14_N              LOC = AE35 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HB15_P              LOC = AE29 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HB15_N              LOC = AE30 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HB16_P              LOC = Y32  | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HB16_N              LOC = Y33  | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HA12_P              LOC = AC31 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HA12_N              LOC = AD31 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HA13_P              LOC = AA31 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HA13_N              LOC = AA32 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HA14_P              LOC = AC30 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HA14_N              LOC = AD30 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HA15_P              LOC = AA29 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HA15_N              LOC = AA30 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HA16_P              LOC = AB29 | IOSTANDARD=LVCMOS18; # Bank  16
NET  FMC1_HA16_N              LOC = AC29 | IOSTANDARD=LVCMOS18; # Bank  16
NET  IO_25_VRP_16             LOC = AB34 | IOSTANDARD=LVCMOS18; # Bank  16
NET  IO_0_VRN_17              LOC = Y38  | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L1P_T0_17             LOC = AB41 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L1N_T0_17             LOC = AB42 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L2P_T0_17             LOC = W40  | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L2N_T0_17             LOC = Y40  | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L3P_T0_DQS_17         LOC = Y39  | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L3N_T0_DQS_17         LOC = AA39 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L4P_T0_17             LOC = Y42  | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L4N_T0_17             LOC = AA42 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L5P_T0_17             LOC = AB38 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L5N_T0_17             LOC = AB39 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L6P_T0_17             LOC = AA40 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L6N_T0_VREF_17        LOC = AA41 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L7P_T1_17             LOC = AC38 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L7N_T1_17             LOC = AC39 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L8P_T1_17             LOC = AD42 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L8N_T1_17             LOC = AE42 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L9P_T1_DQS_17         LOC = AD38 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L9N_T1_DQS_17         LOC = AE38 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L10P_T1_17            LOC = AC40 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L10N_T1_17            LOC = AC41 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L11P_T1_SRCC_17       LOC = AE39 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L11N_T1_SRCC_17       LOC = AE40 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L12P_T1_MRCC_17       LOC = AD40 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L12N_T1_MRCC_17       LOC = AD41 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L13P_T2_MRCC_17       LOC = AF39 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L13N_T2_MRCC_17       LOC = AF40 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L14P_T2_SRCC_17       LOC = AF41 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L14N_T2_SRCC_17       LOC = AG41 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L15P_T2_DQS_17        LOC = AG39 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L15N_T2_DQS_17        LOC = AH39 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L16P_T2_17            LOC = AF42 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L16N_T2_17            LOC = AG42 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L17P_T2_17            LOC = AG38 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L17N_T2_17            LOC = AH38 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L18P_T2_17            LOC = AJ38 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L18N_T2_17            LOC = AK38 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L19P_T3_17            LOC = AK40 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L19N_T3_VREF_17       LOC = AL40 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L20P_T3_17            LOC = AH40 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L20N_T3_17            LOC = AH41 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L21P_T3_DQS_17        LOC = AL41 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L21N_T3_DQS_17        LOC = AL42 | IOSTANDARD=LVCMOS18; # Bank  17
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NET  IO_L22P_T3_17             LOC = AJ40 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L22N_T3_17             LOC = AJ41 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L23P_T3_17             LOC = AK39 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L23N_T3_17             LOC = AL39 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L24P_T3_17             LOC = AJ42 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_L24N_T3_17             LOC = AK42 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_25_VRP_17              LOC = AG37 | IOSTANDARD=LVCMOS18; # Bank  17
NET  IO_0_VRN_18               LOC = N35  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L1P_T0_AD0P_18         LOC = T34  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L1N_T0_AD0N_18         LOC = R35  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L2P_T0_AD8P_18         LOC = N33  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L2N_T0_AD8N_18         LOC = N34  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L3P_T0_DQS_AD1P_18     LOC = R33  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L3N_T0_DQS_AD1N_18     LOC = R34  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L4P_T0_18              LOC = P35  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L4N_T0_18              LOC = P36  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L5P_T0_AD9P_18         LOC = T32  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L5N_T0_AD9N_18         LOC = R32  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L6P_T0_18              LOC = P32  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L6N_T0_VREF_18         LOC = P33  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L7P_T1_AD2P_18         LOC = T36  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L7N_T1_AD2N_18         LOC = R37  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L8P_T1_AD10P_18        LOC = P37  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L8N_T1_AD10N_18        LOC = P38  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L9P_T1_DQS_AD3P_18     LOC = U34  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L9N_T1_DQS_AD3N_18     LOC = T35  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L10P_T1_AD11P_18       LOC = R38  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L10N_T1_AD11N_18       LOC = R39  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L11P_T1_SRCC_18        LOC = U37  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L11N_T1_SRCC_18        LOC = U38  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L12P_T1_MRCC_18        LOC = U39  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L12N_T1_MRCC_18        LOC = T39  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L13P_T2_MRCC_18        LOC = U36  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L13N_T2_MRCC_18        LOC = T37  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L14P_T2_SRCC_18        LOC = V35  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L14N_T2_SRCC_18        LOC = V36  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L15P_T2_DQS_18         LOC = V33  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L15N_T2_DQS_ADV_B_18   LOC = V34  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L16P_T2_A28_18         LOC = W36  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L16N_T2_A27_18         LOC = W37  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L17P_T2_A26_18         LOC = U32  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L17N_T2_A25_18         LOC = U33  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L18P_T2_A24_18         LOC = W32  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L18N_T2_A23_18         LOC = W33  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L19P_T3_A22_18         LOC = V39  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L19N_T3_A21_VREF_18    LOC = V40  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L20P_T3_A20_18         LOC = T40  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L20N_T3_A19_18         LOC = T41  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L21P_T3_DQS_18         LOC = W41  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L21N_T3_DQS_A18_18     LOC = W42  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L22P_T3_A17_18         LOC = U41  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L22N_T3_A16_18         LOC = T42  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L23P_T3_FOE_B_18       LOC = W38  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L23N_T3_FWE_B_18       LOC = V38  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L24P_T3_RS1_18         LOC = V41  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_L24N_T3_RS0_18         LOC = U42  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_25_VRP_18              LOC = W35  | IOSTANDARD=LVCMOS18; # Bank  18
NET  IO_0_VRN_19               LOC = L36  | IOSTANDARD=LVCMOS18; # Bank  19
NET  DUT_PMB_ALERT             LOC = E40  | IOSTANDARD=LVCMOS18; # Bank  19
NET  DUT_PMB_CTRL              LOC = D40  | IOSTANDARD=LVCMOS18; # Bank  19
NET  DUT_PMB_CLK               LOC = A40  | IOSTANDARD=LVCMOS18; # Bank  19
NET  DUT_PMB_DATA              LOC = A41  | IOSTANDARD=LVCMOS18; # Bank  19
NET  IO_L3P_T0_DQS_19          LOC = D41  | IOSTANDARD=LVCMOS18; # Bank  19
NET  IO_L3N_T0_DQS_19          LOC = D42  | IOSTANDARD=LVCMOS18; # Bank  19
NET  IO_L4P_T0_19              LOC = B41  | IOSTANDARD=LVCMOS18; # Bank  19
NET  IO_L4N_T0_19              LOC = B42  | IOSTANDARD=LVCMOS18; # Bank  19
NET  IO_L5P_T0_19              LOC = F42  | IOSTANDARD=LVCMOS18; # Bank  19
NET  USER_SW1                  LOC = E42  | IOSTANDARD=LVCMOS18; # Bank  19
NET  USER_SW2                  LOC = C40  | IOSTANDARD=LVCMOS18; # Bank  19
NET  USER_SW3                  LOC = C41  | IOSTANDARD=LVCMOS18; # Bank  19
NET  USER_SW4                  LOC = H40  | IOSTANDARD=LVCMOS18; # Bank  19
NET  USER_SW5                  LOC = H41  | IOSTANDARD=LVCMOS18; # Bank  19
NET  USER_SW6                  LOC = H39  | IOSTANDARD=LVCMOS18; # Bank  19
NET  USER_SW7                  LOC = G39  | IOSTANDARD=LVCMOS18; # Bank  19
NET  USER_SW8                  LOC = G41  | IOSTANDARD=LVCMOS18; # Bank  19
NET  IO_L9N_T1_DQS_19          LOC = G42  | IOSTANDARD=LVCMOS18; # Bank  19
NET  IO_L10P_T1_19             LOC = F40  | IOSTANDARD=LVCMOS18; # Bank  19
NET  IO_L10N_T1_19             LOC = F41  | IOSTANDARD=LVCMOS18; # Bank  19
NET  IO_L11P_T1_SRCC_19        LOC = J40  | IOSTANDARD=LVCMOS18; # Bank  19
NET  IO_L11N_T1_SRCC_19        LOC = J41  | IOSTANDARD=LVCMOS18; # Bank  19
NET  CLK_DIFF_2_P              LOC = K39  | IOSTANDARD=LVCMOS18; # Bank  19
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NET  CLK_DIFF_2_N             LOC = K40  | IOSTANDARD=LVCMOS18; # Bank  19
NET  IO_L13P_T2_MRCC_19       LOC = L39  | IOSTANDARD=LVCMOS18; # Bank  19
NET  IO_L13N_T2_MRCC_19       LOC = L40  | IOSTANDARD=LVCMOS18; # Bank  19
NET  DUT_I2C_SCL              LOC = M41  | IOSTANDARD=LVCMOS18; # Bank  19
NET  DUT_I2C_SDA              LOC = L41  | IOSTANDARD=LVCMOS18; # Bank  19
NET  IO_L15P_T2_DQS_19        LOC = K42  | IOSTANDARD=LVCMOS18; # Bank  19
NET  IO_L15N_T2_DQS_19        LOC = J42  | IOSTANDARD=LVCMOS18; # Bank  19
NET  IO_L16P_T2_19            LOC = M42  | IOSTANDARD=LVCMOS18; # Bank  19
NET  IO_L16N_T2_19            LOC = L42  | IOSTANDARD=LVCMOS18; # Bank  19
NET  IO_L17P_T2_19            LOC = K37  | IOSTANDARD=LVCMOS18; # Bank  19
NET  IO_L17N_T2_19            LOC = K38  | IOSTANDARD=LVCMOS18; # Bank  19
NET  IO_L18P_T2_19            LOC = M36  | IOSTANDARD=LVCMOS18; # Bank  19
NET  IO_L18N_T2_19            LOC = L37  | IOSTANDARD=LVCMOS18; # Bank  19
NET  USER_PB1                 LOC = P41  | IOSTANDARD=LVCMOS18; # Bank  19
NET  USER_PB2                 LOC = N41  | IOSTANDARD=LVCMOS18; # Bank  19
NET  APP_LED1                 LOC = M37  | IOSTANDARD=LVCMOS18; # Bank  19
NET  APP_LED2                 LOC = M38  | IOSTANDARD=LVCMOS18; # Bank  19
NET  APP_LED3                 LOC = R42  | IOSTANDARD=LVCMOS18; # Bank  19
NET  APP_LED4                 LOC = P42  | IOSTANDARD=LVCMOS18; # Bank  19
NET  APP_LED5                 LOC = N38  | IOSTANDARD=LVCMOS18; # Bank  19
NET  APP_LED6                 LOC = M39  | IOSTANDARD=LVCMOS18; # Bank  19
NET  APP_LED7                 LOC = R40  | IOSTANDARD=LVCMOS18; # Bank  19
NET  APP_LED8                 LOC = P40  | IOSTANDARD=LVCMOS18; # Bank  19
NET  IO_L24P_T3_19            LOC = N39  | IOSTANDARD=LVCMOS18; # Bank  19
NET  IO_L24N_T3_19            LOC = N40  | IOSTANDARD=LVCMOS18; # Bank  19
NET  IO_25_VRP_19             LOC = N36  | IOSTANDARD=LVCMOS18; # Bank  19
NET  IO_0_VRN_31              LOC = AM14 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_LA02_P              LOC = AJ16 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_LA02_N              LOC = AJ15 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_LA03_P              LOC = AK14 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_LA03_N              LOC = AK13 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_LA04_P              LOC = AK15 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_LA04_N              LOC = AL14 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_LA05_P              LOC = AJ13 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_LA05_N              LOC = AJ12 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_LA06_P              LOC = AL16 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_LA06_N              LOC = AL15 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_LA07_P              LOC = AK12 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_LA07_N              LOC = AL12 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_LA08_P              LOC = AM13 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_LA08_N              LOC = AN13 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_LA09_P              LOC = AM12 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_LA09_N              LOC = AM11 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_LA10_P              LOC = AN15 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_LA10_N              LOC = AN14 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_LA11_P              LOC = AN11 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_LA11_N              LOC = AP11 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_LA01_CC_P           LOC = AR14 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_LA01_CC_N           LOC = AT14 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_LA00_CC_P           LOC = AP13 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_LA00_CC_N           LOC = AR13 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_HA00_CC_P           LOC = AU14 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_HA00_CC_N           LOC = AU13 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_HA01_CC_P           LOC = AV13 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_HA01_CC_N           LOC = AW13 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_LA12_P              LOC = AP12 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_LA12_N              LOC = AR12 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_LA13_P              LOC = AR15 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_LA13_N              LOC = AT15 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_LA14_P              LOC = AT12 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_LA14_N              LOC = AU12 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_LA15_P              LOC = AV15 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_LA15_N              LOC = AV14 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_LA16_P              LOC = AW15 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_LA16_N              LOC = AY15 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_HA02_P              LOC = AW12 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_HA02_N              LOC = AY12 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_HA03_P              LOC = BA15 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_HA03_N              LOC = BA14 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_HA04_P              LOC = AY14 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_HA04_N              LOC = AY13 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_HA05_P              LOC = BB14 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_HA05_N              LOC = BB13 | IOSTANDARD=LVCMOS18; # Bank  31
NET  CM_LVDS3_P               LOC = BA12 | IOSTANDARD=LVDS;     # Bank  31
NET  CM_LVDS3_N               LOC = BB12 | IOSTANDARD=LVDS;     # Bank  31
NET  IO_25_VRP_31             LOC = AP15 | IOSTANDARD=LVCMOS18; # Bank  31
NET  FMC3_PRSNT_M2C_L         LOC = AR20 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_LA19_P              LOC = AL19 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_LA19_N              LOC = AM19 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_LA20_P              LOC = AK17 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_LA20_N              LOC = AL17 | IOSTANDARD=LVCMOS18; # Bank  32
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NET  FMC3_LA21_P              LOC = AM18 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_LA21_N              LOC = AM17 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_LA22_P              LOC = AK19 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_LA22_N              LOC = AK18 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_LA23_P              LOC = AM16 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_LA23_N              LOC = AN16 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_LA24_P              LOC = AJ18 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_LA24_N              LOC = AJ17 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_LA25_P              LOC = AP18 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_LA25_N              LOC = AP17 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_LA26_P              LOC = AP20 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_LA26_N              LOC = AR19 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_LA27_P              LOC = AN19 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_LA27_N              LOC = AN18 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_LA28_P              LOC = AR18 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_LA28_N              LOC = AR17 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_LA18_CC_P           LOC = AU18 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_LA18_CC_N           LOC = AV18 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_LA17_CC_P           LOC = AT17 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_LA17_CC_N           LOC = AU17 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_CLK0_M2C_P          LOC = AY18 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_CLK0_M2C_N          LOC = AY17 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_CLK1_M2C_P          LOC = AW18 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_CLK1_M2C_N          LOC = AW17 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_LA29_P              LOC = AU19 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_LA29_N              LOC = AV19 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_LA30_P              LOC = AT20 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_LA30_N              LOC = AT19 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_LA31_P              LOC = AV16 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_LA31_N              LOC = AW16 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_LA32_P              LOC = AT16 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_LA32_N              LOC = AU16 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_LA33_P              LOC = BB19 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_LA33_N              LOC = BB18 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_HA06_P              LOC = AV20 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_HA06_N              LOC = AW20 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_HA07_P              LOC = BA17 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_HA07_N              LOC = BB17 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_HA08_P              LOC = AY20 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_HA08_N              LOC = BA20 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_HA09_P              LOC = BA16 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_HA09_N              LOC = BB16 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_HA10_P              LOC = AY19 | IOSTANDARD=LVCMOS18; # Bank  32
NET  FMC3_HA10_N              LOC = BA19 | IOSTANDARD=LVCMOS18; # Bank  32
NET  IO_25_VRP_32             LOC = AP16 | IOSTANDARD=LVCMOS18; # Bank  32
NET  IO_0_VRN_33              LOC = AL24 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L1P_T0_33             LOC = AJ23 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L1N_T0_33             LOC = AK23 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L2P_T0_33             LOC = AK20 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L2N_T0_33             LOC = AL20 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L3P_T0_DQS_33         LOC = AJ22 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L3N_T0_DQS_33         LOC = AK22 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L4P_T0_33             LOC = AL21 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L4N_T0_33             LOC = AM21 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L5P_T0_33             LOC = AJ21 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L5N_T0_33             LOC = AJ20 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L6P_T0_33             LOC = AL22 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L6N_T0_VREF_33        LOC = AM22 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L7P_T1_33             LOC = AM24 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L7N_T1_33             LOC = AN24 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L8P_T1_33             LOC = AM23 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L8N_T1_33             LOC = AN23 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L9P_T1_DQS_33         LOC = AP23 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L9N_T1_DQS_33         LOC = AP22 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L10P_T1_33            LOC = AN21 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L10N_T1_33            LOC = AP21 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L11P_T1_SRCC_33       LOC = AR23 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L11N_T1_SRCC_33       LOC = AR22 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L12P_T1_MRCC_33       LOC = AT22 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L12N_T1_MRCC_33       LOC = AU22 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L13P_T2_MRCC_33       LOC = AU23 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L13N_T2_MRCC_33       LOC = AV23 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L14P_T2_SRCC_33       LOC = AW23 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L14N_T2_SRCC_33       LOC = AW22 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L15P_T2_DQS_33        LOC = AT21 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L15N_T2_DQS_33        LOC = AU21 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L16P_T2_33            LOC = AR24 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L16N_T2_33            LOC = AT24 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L17P_T2_33            LOC = AV21 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L17N_T2_33            LOC = AW21 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L18P_T2_33            LOC = AU24 | IOSTANDARD=LVCMOS18; # Bank  33
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NET  IO_L18N_T2_33             LOC = AV24 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L19P_T3_33             LOC = AY23 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L19N_T3_VREF_33        LOC = AY22 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L20P_T3_33             LOC = AY25 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L20N_T3_33             LOC = BA25 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L21P_T3_DQS_33         LOC = BA22 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L21N_T3_DQS_33         LOC = BB22 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L22P_T3_33             LOC = AY24 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L22N_T3_33             LOC = BA24 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L23P_T3_33             LOC = BA21 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L23N_T3_33             LOC = BB21 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L24P_T3_33             LOC = BB24 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_L24N_T3_33             LOC = BB23 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_25_VRP_33              LOC = AN20 | IOSTANDARD=LVCMOS18; # Bank  33
NET  IO_0_VRN_34               LOC = R29  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_LA02_P               LOC = K35  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_LA02_N               LOC = J35  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_LA03_P               LOC = J32  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_LA03_N               LOC = J33  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_LA04_P               LOC = K33  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_LA04_N               LOC = K34  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_LA05_P               LOC = L34  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_LA05_N               LOC = L35  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_LA06_P               LOC = M33  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_LA06_N               LOC = M34  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_LA07_P               LOC = H34  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_LA07_N               LOC = H35  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_LA08_P               LOC = K29  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_LA08_N               LOC = K30  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_LA09_P               LOC = J30  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_LA09_N               LOC = H30  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_LA10_P               LOC = L29  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_LA10_N               LOC = L30  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_LA11_P               LOC = J31  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_LA11_N               LOC = H31  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_LA01_CC_P            LOC = M32  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_LA01_CC_N            LOC = L32  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_LA00_CC_P            LOC = L31  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_LA00_CC_N            LOC = K32  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_HA00_CC_P            LOC = N30  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_HA00_CC_N            LOC = M31  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_HA01_CC_P            LOC = P30  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_HA01_CC_N            LOC = N31  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_LA12_P               LOC = M28  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_LA12_N               LOC = M29  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_LA13_P               LOC = R28  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_LA13_N               LOC = P28  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_LA14_P               LOC = N28  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_LA14_N               LOC = N29  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_LA15_P               LOC = R30  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_LA15_N               LOC = P31  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_LA16_P               LOC = U31  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_LA16_N               LOC = T31  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_HA02_P               LOC = V30  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_HA02_N               LOC = V31  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_HA03_P               LOC = T29  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_HA03_N               LOC = T30  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_HA04_P               LOC = W30  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_HA04_N               LOC = W31  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_HA05_P               LOC = V29  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_HA05_N               LOC = U29  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_HA06_P               LOC = Y29  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_HA06_N               LOC = Y30  | IOSTANDARD=LVCMOS18; # Bank  34
NET  IO_25_VRP_34              LOC = U28  | IOSTANDARD=LVCMOS18; # Bank  34
NET  FMC2_PRSNT_M2C_L          LOC = G31  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_LA19_P               LOC = B36  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_LA19_N               LOC = A37  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_LA20_P               LOC = B34  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_LA20_N               LOC = A34  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_LA21_P               LOC = B39  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_LA21_N               LOC = A39  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_LA22_P               LOC = A35  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_LA22_N               LOC = A36  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_LA23_P               LOC = C38  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_LA23_N               LOC = C39  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_LA24_P               LOC = B37  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_LA24_N               LOC = B38  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_LA25_P               LOC = E32  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_LA25_N               LOC = D32  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_LA26_P               LOC = B32  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_LA26_N               LOC = B33  | IOSTANDARD=LVCMOS18; # Bank  35
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NET  FMC2_LA27_P              LOC = E33  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_LA27_N              LOC = D33  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_LA28_P              LOC = C33  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_LA28_N              LOC = C34  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_LA18_CC_P           LOC = D35  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_LA18_CC_N           LOC = D36  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_LA17_CC_P           LOC = C35  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_LA17_CC_N           LOC = C36  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_CLK0_M2C_P          LOC = E34  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_CLK0_M2C_N          LOC = E35  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_CLK1_M2C_P          LOC = D37  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_CLK1_M2C_N          LOC = D38  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_LA29_P              LOC = G32  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_LA29_N              LOC = F32  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_LA30_P              LOC = F36  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_LA30_N              LOC = F37  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_LA31_P              LOC = F34  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_LA31_N              LOC = F35  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_LA32_P              LOC = H33  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_LA32_N              LOC = G33  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_LA33_P              LOC = E37  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_LA33_N              LOC = E38  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_HA07_P              LOC = G36  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_HA07_N              LOC = G37  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_HA08_P              LOC = F39  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_HA08_N              LOC = E39  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_HA09_P              LOC = J37  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_HA09_N              LOC = J38  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_HA10_P              LOC = H38  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_HA10_N              LOC = G38  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_HA11_P              LOC = J36  | IOSTANDARD=LVCMOS18; # Bank  35
NET  FMC2_HA11_N              LOC = H36  | IOSTANDARD=LVCMOS18; # Bank  35
NET  IO_25_VRP_35             LOC = G34  | IOSTANDARD=LVCMOS18; # Bank  35
NET  IO_0_VRN_36              LOC = M23  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HB01_P              LOC = H24  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HB01_N              LOC = G24  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HB02_P              LOC = J21  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HB02_N              LOC = H21  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HB03_P              LOC = H25  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HB03_N              LOC = H26  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HB04_P              LOC = G21  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HB04_N              LOC = G22  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HB05_P              LOC = G26  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HB05_N              LOC = G27  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HB07_P              LOC = H23  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HB07_N              LOC = G23  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HB08_P              LOC = G28  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HB08_N              LOC = G29  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HB09_P              LOC = K28  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HB09_N              LOC = J28  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HB10_P              LOC = H28  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HB10_N              LOC = H29  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HB11_P              LOC = K27  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HB11_N              LOC = J27  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HB06_CC_P           LOC = K24  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HB06_CC_N           LOC = K25  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HB00_CC_P           LOC = J25  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HB00_CC_N           LOC = J26  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_CLK2_BIDIR_P        LOC = M24  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_CLK2_BIDIR_N        LOC = L24  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_CLK3_BIDIR_P        LOC = K23  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_CLK3_BIDIR_N        LOC = J23  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HB12_P              LOC = M22  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HB12_N              LOC = L22  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HB13_P              LOC = L25  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HB13_N              LOC = L26  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HB14_P              LOC = K22  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HB14_N              LOC = J22  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HB15_P              LOC = M21  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HB15_N              LOC = L21  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HB16_P              LOC = P21  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HB16_N              LOC = N21  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HA12_P              LOC = P25  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HA12_N              LOC = P26  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HA13_P              LOC = P22  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HA13_N              LOC = P23  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HA14_P              LOC = N25  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HA14_N              LOC = N26  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HA15_P              LOC = N23  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HA15_N              LOC = N24  | IOSTANDARD=LVCMOS18; # Bank  36
NET  FMC2_HA16_P              LOC = M27  | IOSTANDARD=LVCMOS18; # Bank  36
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NET  FMC2_HA16_N              LOC = L27  | IOSTANDARD=LVCMOS18; # Bank  36
NET  IO_25_VRP_36             LOC = M26  | IOSTANDARD=LVCMOS18; # Bank  36
NET  IO_0_VRN_37              LOC = F21  | IOSTANDARD=LVCMOS18; # Bank  37
NET  MGT_MOD_SPI_SCK          LOC = A24  | IOSTANDARD=LVCMOS18; # Bank  37
NET  MGT_MOD_SPI_D            LOC = A25  | IOSTANDARD=LVCMOS18; # Bank  37
NET  MGT_MOD_SPI_Q            LOC = B22  | IOSTANDARD=LVCMOS18; # Bank  37
NET  GTX_MOD_SPI_CS           LOC = A22  | IOSTANDARD=LVCMOS18; # Bank  37
NET  IO_L3P_T0_DQS_37         LOC = A26  | IOSTANDARD=LVCMOS18; # Bank  37
NET  IO_L3N_T0_DQS_37         LOC = A27  | IOSTANDARD=LVCMOS18; # Bank  37
NET  SA2_SDHOST_CMD           LOC = C23  | IOSTANDARD=LVCMOS18; # Bank  37
NET  SA2_SDHOST_D0            LOC = B23  | IOSTANDARD=LVCMOS18; # Bank  37
NET  SA2_SDHOST_D1            LOC = B26  | IOSTANDARD=LVCMOS18; # Bank  37
NET  SA2_SDHOST_D3            LOC = B27  | IOSTANDARD=LVCMOS18; # Bank  37
NET  SA2_SDHOST_D2            LOC = C24  | IOSTANDARD=LVCMOS18; # Bank  37
NET  SA2_SDHOST_CLK           LOC = B24  | IOSTANDARD=LVCMOS18; # Bank  37
NET  IO_L7P_T1_37             LOC = E23  | IOSTANDARD=LVCMOS18; # Bank  37
NET  IO_L7N_T1_37             LOC = E24  | IOSTANDARD=LVCMOS18; # Bank  37
NET  IO_L8P_T1_37             LOC = F22  | IOSTANDARD=LVCMOS18; # Bank  37
NET  IO_L8N_T1_37             LOC = E22  | IOSTANDARD=LVCMOS18; # Bank  37
NET  IO_L9P_T1_DQS_37         LOC = F25  | IOSTANDARD=LVCMOS18; # Bank  37
NET  IO_L9N_T1_DQS_37         LOC = E25  | IOSTANDARD=LVCMOS18; # Bank  37
NET  IO_L10P_T1_37            LOC = D22  | IOSTANDARD=LVCMOS18; # Bank  37
NET  IO_L10N_T1_37            LOC = D23  | IOSTANDARD=LVCMOS18; # Bank  37
NET  IO_L11P_T1_SRCC_37       LOC = D25  | IOSTANDARD=LVCMOS18; # Bank  37
NET  IO_L11N_T1_SRCC_37       LOC = D26  | IOSTANDARD=LVCMOS18; # Bank  37
NET  IO_L12P_T1_MRCC_37       LOC = C25  | IOSTANDARD=LVCMOS18; # Bank  37
NET  IO_L12N_T1_MRCC_37       LOC = C26  | IOSTANDARD=LVCMOS18; # Bank  37
NET  IO_L13P_T2_MRCC_37       LOC = D27  | IOSTANDARD=LVCMOS18; # Bank  37
NET  IO_L13N_T2_MRCC_37       LOC = D28  | IOSTANDARD=LVCMOS18; # Bank  37
NET  IO_L14P_T2_SRCC_37       LOC = C28  | IOSTANDARD=LVCMOS18; # Bank  37
NET  IO_L14N_T2_SRCC_37       LOC = C29  | IOSTANDARD=LVCMOS18; # Bank  37
NET  USB_GPIO_0               LOC = B28  | IOSTANDARD=LVCMOS18; # Bank  37
NET  USB_GPIO_1               LOC = B29  | IOSTANDARD=LVCMOS18; # Bank  37
NET  USB_GPIO_2               LOC = A31  | IOSTANDARD=LVCMOS18; # Bank  37
NET  USB_GPIO_3               LOC = A32  | IOSTANDARD=LVCMOS18; # Bank  37
NET  USB_TXD_0                LOC = A29  | IOSTANDARD=LVCMOS18; # Bank  37
NET  USB_RXD_I                LOC = A30  | IOSTANDARD=LVCMOS18; # Bank  37
NET  USB_RTS_0_B              LOC = C31  | IOSTANDARD=LVCMOS18; # Bank  37
NET  USB_CTS_I_B              LOC = B31  | IOSTANDARD=LVCMOS18; # Bank  37
NET  IO_L19P_T3_37            LOC = E30  | IOSTANDARD=LVCMOS18; # Bank  37
NET  IO_L19N_T3_VREF_37       LOC = D31  | IOSTANDARD=LVCMOS18; # Bank  37
NET  IO_L20P_T3_37            LOC = D30  | IOSTANDARD=LVCMOS18; # Bank  37
NET  IO_L20N_T3_37            LOC = C30  | IOSTANDARD=LVCMOS18; # Bank  37
NET  IO_L21P_T3_DQS_37        LOC = E27  | IOSTANDARD=LVCMOS18; # Bank  37
NET  IO_L21N_T3_DQS_37        LOC = E28  | IOSTANDARD=LVCMOS18; # Bank  37
NET  IO_L22P_T3_37            LOC = F29  | IOSTANDARD=LVCMOS18; # Bank  37
NET  IO_L22N_T3_37            LOC = E29  | IOSTANDARD=LVCMOS18; # Bank  37
NET  IO_L23P_T3_37            LOC = F26  | IOSTANDARD=LVCMOS18; # Bank  37
NET  IO_L23N_T3_37            LOC = F27  | IOSTANDARD=LVCMOS18; # Bank  37
NET  IO_L24P_T3_37            LOC = F30  | IOSTANDARD=LVCMOS18; # Bank  37
NET  IO_L24N_T3_37            LOC = F31  | IOSTANDARD=LVCMOS18; # Bank  37
NET  IO_25_VRP_37             LOC = F24  | IOSTANDARD=LVCMOS18; # Bank  37
NET  IO_0_VRN_38              LOC = K18  | IOSTANDARD=LVCMOS18; # Bank  38
NET  CM_CTRL_0                LOC = C19  | IOSTANDARD=LVCMOS18; # Bank  38
NET  CM_CTRL_1                LOC = B19  | IOSTANDARD=LVCMOS18; # Bank  38
NET  CM_CTRL_2                LOC = A16  | IOSTANDARD=LVCMOS18; # Bank  38
NET  CM_CTRL_3                LOC = A15  | IOSTANDARD=LVCMOS18; # Bank  38
NET  CM_CTRL_4                LOC = A20  | IOSTANDARD=LVCMOS18; # Bank  38
NET  CM_CTRL_5                LOC = A19  | IOSTANDARD=LVCMOS18; # Bank  38
NET  CM_CTRL_6                LOC = B17  | IOSTANDARD=LVCMOS18; # Bank  38
NET  CM_CTRL_7                LOC = A17  | IOSTANDARD=LVCMOS18; # Bank  38
NET  CM_CTRL_8                LOC = B21  | IOSTANDARD=LVCMOS18; # Bank  38
NET  CM_CTRL_9                LOC = A21  | IOSTANDARD=LVCMOS18; # Bank  38
NET  CM_CTRL_10               LOC = C18  | IOSTANDARD=LVCMOS18; # Bank  38
NET  CM_CTRL_11               LOC = B18  | IOSTANDARD=LVCMOS18; # Bank  38
NET  CM_CTRL_12               LOC = D20  | IOSTANDARD=LVCMOS18; # Bank  38
NET  CM_CTRL_13               LOC = C20  | IOSTANDARD=LVCMOS18; # Bank  38
NET  CM_CTRL_14               LOC = F17  | IOSTANDARD=LVCMOS18; # Bank  38
NET  CM_CTRL_15               LOC = E17  | IOSTANDARD=LVCMOS18; # Bank  38
NET  CM_CTRL_16               LOC = D21  | IOSTANDARD=LVCMOS18; # Bank  38
NET  CM_CTRL_17               LOC = C21  | IOSTANDARD=LVCMOS18; # Bank  38
NET  CM_CTRL_18               LOC = D18  | IOSTANDARD=LVCMOS18; # Bank  38
NET  CM_CTRL_19               LOC = D17  | IOSTANDARD=LVCMOS18; # Bank  38
NET  IO_L11P_T1_SRCC_38       LOC = G19  | IOSTANDARD=LVCMOS18; # Bank  38
NET  IO_L11N_T1_SRCC_38       LOC = F19  | IOSTANDARD=LVCMOS18; # Bank  38
NET  LVDS_OSC_P               LOC = E19  | IOSTANDARD=LVDS;     # Bank  38
NET  LVDS_OSC_N               LOC = E18  | IOSTANDARD=LVDS;     # Bank  38
NET  CLK_DIFF_1_P             LOC = H19  | IOSTANDARD=LVCMOS18; # Bank  38
NET  CLK_DIFF_1_N             LOC = G18  | IOSTANDARD=LVCMOS18; # Bank  38
NET  CM_GCLK_P                LOC = K19  | IOSTANDARD=LVCMOS18; # Bank  38
NET  CM_GCLK_N                LOC = J18  | IOSTANDARD=LVCMOS18; # Bank  38
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NET  CM_CTRL_20              LOC = F20  | IOSTANDARD=LVCMOS18; # Bank  38
NET  CM_CTRL_21              LOC = E20  | IOSTANDARD=LVCMOS18; # Bank  38
NET  CM_CTRL_22              LOC = K17  | IOSTANDARD=LVCMOS18; # Bank  38
NET  CM_CTRL_23              LOC = J17  | IOSTANDARD=LVCMOS18; # Bank  38
NET  CM_RST                  LOC = J20  | IOSTANDARD=LVCMOS18; # Bank  38
NET  IO_L17N_T2_38           LOC = H20  | IOSTANDARD=LVCMOS18; # Bank  38
NET  IO_L18P_T2_38           LOC = H18  | IOSTANDARD=LVCMOS18; # Bank  38
NET  IO_L18N_T2_38           LOC = G17  | IOSTANDARD=LVCMOS18; # Bank  38
NET  IO_L19P_T3_38           LOC = P18  | IOSTANDARD=LVCMOS18; # Bank  38
NET  IO_L19N_T3_VREF_38      LOC = P17  | IOSTANDARD=LVCMOS18; # Bank  38
NET  IO_L20P_T3_38           LOC = M17  | IOSTANDARD=LVCMOS18; # Bank  38
NET  IO_L20N_T3_38           LOC = L17  | IOSTANDARD=LVCMOS18; # Bank  38
NET  IO_L21P_T3_DQS_38       LOC = N19  | IOSTANDARD=LVCMOS18; # Bank  38
NET  IO_L21N_T3_DQS_38       LOC = N18  | IOSTANDARD=LVCMOS18; # Bank  38
NET  IO_L22P_T3_38           LOC = M19  | IOSTANDARD=LVCMOS18; # Bank  38
NET  IO_L22N_T3_38           LOC = M18  | IOSTANDARD=LVCMOS18; # Bank  38
NET  IO_L23P_T3_38           LOC = P20  | IOSTANDARD=LVCMOS18; # Bank  38
NET  IO_L23N_T3_38           LOC = N20  | IOSTANDARD=LVCMOS18; # Bank  38
NET  IO_L24P_T3_38           LOC = L20  | IOSTANDARD=LVCMOS18; # Bank  38
NET  IO_L24N_T3_38           LOC = L19  | IOSTANDARD=LVCMOS18; # Bank  38
NET  IO_25_VRP_38            LOC = K20  | IOSTANDARD=LVCMOS18; # Bank  38
NET  IO_0_VRN_39             LOC = J16  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_HA11_P             LOC = C16  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_HA11_N             LOC = B16  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_HA12_P             LOC = B14  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_HA12_N             LOC = A14  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_HA13_P             LOC = C15  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_HA13_N             LOC = C14  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_HA14_P             LOC = D13  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_HA14_N             LOC = C13  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_HA15_P             LOC = D16  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_HA15_N             LOC = D15  | IOSTANDARD=LVCMOS18; # Bank  39
NET  CM_LVDS1_P              LOC = E12  | IOSTANDARD=LVDS;     # Bank  39
NET  CM_LVDS1_N              LOC = D12  | IOSTANDARD=LVDS;     # Bank  39
NET  FMC3_HB01_P             LOC = F16  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_HB01_N             LOC = E15  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_HB02_P             LOC = E14  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_HB02_N             LOC = E13  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_HB03_P             LOC = H16  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_HB03_N             LOC = G16  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_HB04_P             LOC = G12  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_HB04_N             LOC = F12  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_HB06_CC_P          LOC = F15  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_HB06_CC_N          LOC = F14  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_HB00_CC_P          LOC = G14  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_HB00_CC_N          LOC = G13  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_CLK2_BIDIR_P       LOC = H15  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_CLK2_BIDIR_N       LOC = H14  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_CLK3_BIDIR_P       LOC = J13  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_CLK3_BIDIR_N       LOC = H13  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_HB05_P             LOC = K12  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_HB05_N             LOC = J12  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_HB07_P             LOC = K15  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_HB07_N             LOC = J15  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_HB08_P             LOC = K14  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_HB08_N             LOC = K13  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_HB09_P             LOC = L16  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_HB09_N             LOC = L15  | IOSTANDARD=LVCMOS18; # Bank  39
NET  CM_LVDS2_P              LOC = L12  | IOSTANDARD=LVDS;     # Bank  39
NET  CM_LVDS2_N              LOC = L11  | IOSTANDARD=LVDS;     # Bank  39
NET  FMC3_HB10_P             LOC = M14  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_HB10_N             LOC = L14  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_HB11_P             LOC = N16  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_HB11_N             LOC = M16  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_HB12_P             LOC = N13  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_HB12_N             LOC = M13  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_HB13_P             LOC = N15  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_HB13_N             LOC = N14  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_HB14_P             LOC = M12  | IOSTANDARD=LVCMOS18; # Bank  39
NET  FMC3_HB14_N             LOC = M11  | IOSTANDARD=LVCMOS18; # Bank  39
NET  IO_25_VRP_39            LOC = J11  | IOSTANDARD=LVCMOS18; # Bank  39
NET  111_TX3_P               LOC = AW2                       ; # Bank 111
NET  111_RX3_P               LOC = AW6                       ; # Bank 111
NET  111_TX3_N               LOC = AW1                       ; # Bank 111
NET  111_RX3_N               LOC = AW5                       ; # Bank 111
NET  111_TX2_P               LOC = AY4                       ; # Bank 111
NET  111_RX2_P               LOC = AY8                       ; # Bank 111
NET  111_TX2_N               LOC = AY3                       ; # Bank 111
NET  111_REFCLK0_P           LOC = AW10                      ; # Bank 111
NET  111_RX2_N               LOC = AY7                       ; # Bank 111
NET  111_REFCLK0_N           LOC = AW9                       ; # Bank 111
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NET  111_REFCLK1_N            LOC = BA9                 ; # Bank 111
NET  111_REFCLK1_P            LOC = BA10                ; # Bank 111
NET  111_TX1_P                LOC = BA2                 ; # Bank 111
NET  111_RX1_P                LOC = BA6                 ; # Bank 111
NET  111_TX1_N                LOC = BA1                 ; # Bank 111
NET  111_RX1_N                LOC = BA5                 ; # Bank 111
NET  111_TX0_P                LOC = BB4                 ; # Bank 111
NET  111_RX0_P                LOC = BB8                 ; # Bank 111
NET  111_TX0_N                LOC = BB3                 ; # Bank 111
NET  111_RX0_N                LOC = BB7                 ; # Bank 111
NET  112_TX3_P                LOC = AR2                 ; # Bank 112
NET  112_RX3_P                LOC = AP8                 ; # Bank 112
NET  112_TX3_N                LOC = AR1                 ; # Bank 112
NET  112_RX3_N                LOC = AP7                 ; # Bank 112
NET  112_TX2_P                LOC = AT4                 ; # Bank 112
NET  112_RX2_P                LOC = AR6                 ; # Bank 112
NET  112_TX2_N                LOC = AT3                 ; # Bank 112
NET  112_REFCLK0_P            LOC = AT8                 ; # Bank 112
NET  112_RX2_N                LOC = AR5                 ; # Bank 112
NET  112_REFCLK0_N            LOC = AT7                 ; # Bank 112
NET  112_MGTRREF              LOC = W9                  ; # Bank 112
NET  112_REFCLK1_N            LOC = AU9                 ; # Bank 112
NET  112_REFCLK1_P            LOC = AU10                ; # Bank 112
NET  112_TX1_P                LOC = AU2                 ; # Bank 112
NET  112_RX1_P                LOC = AU6                 ; # Bank 112
NET  112_TX1_N                LOC = AU1                 ; # Bank 112
NET  112_RX1_N                LOC = AU5                 ; # Bank 112
NET  112_TX0_P                LOC = AV4                 ; # Bank 112
NET  112_RX0_P                LOC = AV8                 ; # Bank 112
NET  112_TX0_N                LOC = AV3                 ; # Bank 112
NET  112_RX0_N                LOC = AV7                 ; # Bank 112
NET  113_TX3_P                LOC = AL2                 ; # Bank 113
NET  113_RX3_P                LOC = AJ6                 ; # Bank 113
NET  113_TX3_N                LOC = AL1                 ; # Bank 113
NET  113_RX3_N                LOC = AJ5                 ; # Bank 113
NET  113_TX2_P                LOC = AM4                 ; # Bank 113
NET  113_RX2_P                LOC = AL6                 ; # Bank 113
NET  113_TX2_N                LOC = AM3                 ; # Bank 113
NET  113_REFCLK0_P            LOC = AH8                 ; # Bank 113
NET  113_RX2_N                LOC = AL5                 ; # Bank 113
NET  113_REFCLK0_N            LOC = AH7                 ; # Bank 113
NET  113_REFCLK1_N            LOC = AK7                 ; # Bank 113
NET  113_REFCLK1_P            LOC = AK8                 ; # Bank 113
NET  113_TX1_P                LOC = AN2                 ; # Bank 113
NET  113_RX1_P                LOC = AM8                 ; # Bank 113
NET  113_TX1_N                LOC = AN1                 ; # Bank 113
NET  113_RX1_N                LOC = AM7                 ; # Bank 113
NET  113_TX0_P                LOC = AP4                 ; # Bank 113
NET  113_RX0_P                LOC = AN6                 ; # Bank 113
NET  113_TX0_N                LOC = AP3                 ; # Bank 113
NET  113_RX0_N                LOC = AN5                 ; # Bank 113
NET  114_TX3_P                LOC = AG2                 ; # Bank 114
NET  114_RX3_P                LOC = AD4                 ; # Bank 114
NET  114_TX3_N                LOC = AG1                 ; # Bank 114
NET  114_RX3_N                LOC = AD3                 ; # Bank 114
NET  114_TX2_P                LOC = AH4                 ; # Bank 114
NET  114_RX2_P                LOC = AE6                 ; # Bank 114
NET  114_TX2_N                LOC = AH3                 ; # Bank 114
NET  114_REFCLK0_P            LOC = AD8                 ; # Bank 114
NET  114_RX2_N                LOC = AE5                 ; # Bank 114
NET  114_REFCLK0_N            LOC = AD7                 ; # Bank 114
NET  114_REFCLK1_N            LOC = AF7                 ; # Bank 114
NET  114_REFCLK1_P            LOC = AF8                 ; # Bank 114
NET  114_TX1_P                LOC = AJ2                 ; # Bank 114
NET  114_RX1_P                LOC = AF4                 ; # Bank 114
NET  114_TX1_N                LOC = AJ1                 ; # Bank 114
NET  114_RX1_N                LOC = AF3                 ; # Bank 114
NET  114_TX0_P                LOC = AK4                 ; # Bank 114
NET  114_RX0_P                LOC = AG6                 ; # Bank 114
NET  114_TX0_N                LOC = AK3                 ; # Bank 114
NET  114_RX0_N                LOC = AG5                 ; # Bank 114
NET  115_TX3_P                LOC = W2                  ; # Bank 115
NET  115_RX3_P                LOC = Y4                  ; # Bank 115
NET  115_TX3_N                LOC = W1                  ; # Bank 115
NET  115_RX3_N                LOC = Y3                  ; # Bank 115
NET  115_TX2_P                LOC = AA2                 ; # Bank 115
NET  115_RX2_P                LOC = AA6                 ; # Bank 115
NET  115_TX2_N                LOC = AA1                 ; # Bank 115
NET  115_REFCLK0_P            LOC = Y8                  ; # Bank 115
NET  115_RX2_N                LOC = AA5                 ; # Bank 115
NET  115_REFCLK0_N            LOC = Y7                  ; # Bank 115
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NET  115_MGTRREF             LOC = B11                ; # Bank 115
NET  115_REFCLK1_N           LOC = AB7                ; # Bank 115
NET  115_REFCLK1_P           LOC = AB8                ; # Bank 115
NET  115_TX1_P               LOC = AC2                ; # Bank 115
NET  115_RX1_P               LOC = AB4                ; # Bank 115
NET  115_TX1_N               LOC = AC1                ; # Bank 115
NET  115_RX1_N               LOC = AB3                ; # Bank 115
NET  115_TX0_P               LOC = AE2                ; # Bank 115
NET  115_RX0_P               LOC = AC6                ; # Bank 115
NET  115_TX0_N               LOC = AE1                ; # Bank 115
NET  115_RX0_N               LOC = AC5                ; # Bank 115
NET  116_TX3_P               LOC = P4                 ; # Bank 116
NET  116_RX3_P               LOC = R6                 ; # Bank 116
NET  116_TX3_N               LOC = P3                 ; # Bank 116
NET  116_RX3_N               LOC = R5                 ; # Bank 116
NET  116_TX2_P               LOC = R2                 ; # Bank 116
NET  116_RX2_P               LOC = U6                 ; # Bank 116
NET  116_TX2_N               LOC = R1                 ; # Bank 116
NET  116_REFCLK0_P           LOC = T8                 ; # Bank 116
NET  116_RX2_N               LOC = U5                 ; # Bank 116
NET  116_REFCLK0_N           LOC = T7                 ; # Bank 116
NET  116_REFCLK1_N           LOC = V7                 ; # Bank 116
NET  116_REFCLK1_P           LOC = V8                 ; # Bank 116
NET  116_TX1_P               LOC = T4                 ; # Bank 116
NET  116_RX1_P               LOC = V4                 ; # Bank 116
NET  116_TX1_N               LOC = T3                 ; # Bank 116
NET  116_RX1_N               LOC = V3                 ; # Bank 116
NET  116_TX0_P               LOC = U2                 ; # Bank 116
NET  116_RX0_P               LOC = W6                 ; # Bank 116
NET  116_TX0_N               LOC = U1                 ; # Bank 116
NET  116_RX0_N               LOC = W5                 ; # Bank 116
NET  117_TX3_P               LOC = K4                 ; # Bank 117
NET  117_RX3_P               LOC = J6                 ; # Bank 117
NET  117_TX3_N               LOC = K3                 ; # Bank 117
NET  117_RX3_N               LOC = J5                 ; # Bank 117
NET  117_TX2_P               LOC = L2                 ; # Bank 117
NET  117_RX2_P               LOC = L6                 ; # Bank 117
NET  117_TX2_N               LOC = L1                 ; # Bank 117
NET  117_REFCLK0_P           LOC = K8                 ; # Bank 117
NET  117_RX2_N               LOC = L5                 ; # Bank 117
NET  117_REFCLK0_N           LOC = K7                 ; # Bank 117
NET  117_REFCLK1_N           LOC = M7                 ; # Bank 117
NET  117_REFCLK1_P           LOC = M8                 ; # Bank 117
NET  117_TX1_P               LOC = M4                 ; # Bank 117
NET  117_RX1_P               LOC = N6                 ; # Bank 117
NET  117_TX1_N               LOC = M3                 ; # Bank 117
NET  117_RX1_N               LOC = N5                 ; # Bank 117
NET  117_TX0_P               LOC = N2                 ; # Bank 117
NET  117_RX0_P               LOC = P8                 ; # Bank 117
NET  117_TX0_N               LOC = N1                 ; # Bank 117
NET  117_RX0_N               LOC = P7                 ; # Bank 117
NET  118_TX3_P               LOC = F4                 ; # Bank 118
NET  118_RX3_P               LOC = E6                 ; # Bank 118
NET  118_TX3_N               LOC = F3                 ; # Bank 118
NET  118_RX3_N               LOC = E5                 ; # Bank 118
NET  118_TX2_P               LOC = G2                 ; # Bank 118
NET  118_RX2_P               LOC = F8                 ; # Bank 118
NET  118_TX2_N               LOC = G1                 ; # Bank 118
NET  118_REFCLK0_P           LOC = E10                ; # Bank 118
NET  118_RX2_N               LOC = F7                 ; # Bank 118
NET  118_REFCLK0_N           LOC = E9                 ; # Bank 118
NET  118_MGTRREF             LOC = AC9                ; # Bank 118
NET  118_REFCLK1_N           LOC = G9                 ; # Bank 118
NET  118_REFCLK1_P           LOC = G10                ; # Bank 118
NET  118_TX1_P               LOC = H4                 ; # Bank 118
NET  118_RX1_P               LOC = G6                 ; # Bank 118
NET  118_TX1_N               LOC = H3                 ; # Bank 118
NET  118_RX1_N               LOC = G5                 ; # Bank 118
NET  118_TX0_P               LOC = J2                 ; # Bank 118
NET  118_RX0_P               LOC = H8                 ; # Bank 118
NET  118_TX0_N               LOC = J1                 ; # Bank 118
NET  118_RX0_N               LOC = H7                 ; # Bank 118
NET  119_TX3_P               LOC = B4                 ; # Bank 119
NET  119_RX3_P               LOC = A6                 ; # Bank 119
NET  119_TX3_N               LOC = B3                 ; # Bank 119
NET  119_RX3_N               LOC = A5                 ; # Bank 119
NET  119_TX2_P               LOC = C2                 ; # Bank 119
NET  119_RX2_P               LOC = B8                 ; # Bank 119
NET  119_TX2_N               LOC = C1                 ; # Bank 119
NET  119_REFCLK0_P           LOC = A10                ; # Bank 119
NET  119_RX2_N               LOC = B7                 ; # Bank 119
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NET  119_REFCLK0_N            LOC = A9                  ; # Bank 119
NET  119_REFCLK1_N            LOC = C9                  ; # Bank 119
NET  119_REFCLK1_P            LOC = C10                 ; # Bank 119
NET  119_TX1_P                LOC = D4                  ; # Bank 119
NET  119_RX1_P                LOC = C6                  ; # Bank 119
NET  119_TX1_N                LOC = D3                  ; # Bank 119
NET  119_RX1_N                LOC = C5                  ; # Bank 119
NET  119_TX0_P                LOC = E2                  ; # Bank 119
NET  119_RX0_P                LOC = D8                  ; # Bank 119
NET  119_TX0_N                LOC = E1                  ; # Bank 119
NET  119_RX0_N                LOC = D7                  ; # Bank 119
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Appendix D

Additional Resources

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website at:

http://www.xilinx.com/support.

Create a Xilinx user account and sign up to receive automatic e-mail notification whenever this document is updated:

http://www.xilinx.com/support/myalerts.

For a glossary of technical terms used in Xilinx documentation, see:

www.xilinx.com/company/terms.htm.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips:

http://www.xilinx.com/support/solcenters.htm

Further Resources

The most up to date information related to the VC7203 board and its documentation is available on the following websites.

The VC7203 Characterization Kit product page:

http://www.xilinx.com/products/boards/VC7203

These Xilinx documents provide supplemental material useful with this guide:

UG846, *VC7203 IBERT Getting Started Guide (ISE Design Suite)*

UG847, *VC7203 IBERT Getting Started Guide (Vivado Design Suite)*

DS180, *7 Series FPGAs Overview*

DS182, *Kintex-7 FPGAs Data Sheet: DC and Switching Characteristics*

UG470, *7 Series FPGAs Configuration User Guide*

UG471, *7 Series FPGAs SelectIO Resources User Guide*

UG472, *7 Series FPGAs Clocking Resources User Guide*

UG474, *7 Series FPGAs Configurable Logic Block User Guide*

UG475, *7 Series FPGAs Packaging and Pinout User Guide*

UG476, *7 Series FPGAs GTX Transceivers User Guide*

UG477 *7 Series FPGAs Integrated Block for PCI Express User Guide*

UG480, *7 Series FPGAs XADC Dual 12-Bit 1MSPS Analog-to-Digital Converter User Guide*

UG770, *HW-CLK-101-SCLK2 SuperClock-2 Module User Guide*

To find additional documentation, see the Xilinx website at:

http://www.xilinx.com/support/documentation/index.htm

References

The following websites provide supplemental material useful with this guide:

1. Information about the power system components used by the VC7203 board is available from the Texas Instruments digital power website at:

   http://www.ti.com/ww/en/analog/digital-power/index.html

2. Information about the four 7 Series GTX power supply modules included with the VC7203 Characterization Kit is available from the following vendors:

   Intersil: http://www.intersil.com/en/applications/computing/xilinx.html

   Texas Instruments: http://www.ti.com/ww/en/xilinx/

   Bellnix: http://www.bellnix.com/fpga/xilinxfpga.html

   Lineage: http://www.lineagepower.com/oem/xilinx.html

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Appendix E

Regulatory and Compliance Information

This product is designed and tested to conform to the European Union directives and standards described in this section.

Declaration of Conformity

To view the declaration of conformity online, visit:

http://www.xilinx.com/support/documentation/boards_and_kits/ce-declarations-of-conformity-xtp251.zip

Directives

2006/95/EC, *Low Voltage Directive (LVD)*

2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*

Standards

EN standards are maintained by the European Committee for Electrotechnical Standardization (CENELEC). IEC standards are maintained by the International Electrotechnical Commission (IEC).

Electromagnetic Compatibility

EN 55022:2010, *Information Technology Equipment Radio Disturbance Characteristics – Limits and Methods of Measurement*

EN 55024:2010, *Information Technology Equipment Immunity Characteristics – Limits and Methods of Measurement*

This is a Class A product and can cause radio interference. In a domestic environment, the user might be required to take adequate corrective measures.

Safety

IEC 60950-1:2005, *Information technology equipment – Safety, Part 1: General requirements*

EN 60950-1:2006, *Information technology equipment – Safety, Part 1: General requirements*

Markings

This product complies with Directive 2002/96/EC on waste electrical and electronic equipment (WEEE). The affixed product label indicates that the user must not discard this electrical or electronic product in domestic household waste.

This product complies with Directive 2002/95/EC on the restriction of hazardous substances (RoHS) in electrical and electronic equipment.

This product complies with CE Directives 2006/95/EC, *Low Voltage Directive (LVD)* and 2004/108/EC, *Electromagnetic Compatibility (EMC) Directive.*