ACTT8B-800CTN

Enhanced and high temperature ACTT power switch

14 May 2015 **Product data sheet**

1. General description

AC Thyristor Triac power switch in a SOT404 (D2PAK) surface mountable plastic package with self-protective clamping capabilities against low and high energy transients. This "series CTN" triac will commutate the full RMS current at the maximum rated junction temperature ($T_{j(max)}$ = 150 °C) without the aid of a snubber. It is used in applications where "high junction operating temperature capability" is required.

2. Features and benefits

- Clamping structure ensuring safe high over-voltage withstand capability
- High junction operating temperature capability ($T_{j(max)}$ = 150 °C)
- High minimum I_{GT} for guaranteed immunity to gate noise
- Full cycle AC conduction
- Over-voltage withstand capability to IEC 61000-4-5
- Pin compatible with standard triacs
- Planar passivated for voltage ruggedness and reliability
- Protective self turn-on capability for high energy transients
- Safe clamping capability for low energy over-voltage transients
- Less sensitive gate for high noise immunity
- Surface mountable package
- Triggering in three quadrants only
- Very high immunity to false turn-on by dV/dt and IEC 61000-4-4 fast transient
- Package meets UL94V0 flammability requirement
- Package is RoHS compliant

3. Applications

- AC fan, pump and compressor controls
- Highly inductive, resistive and safety loads
- Large and small appliances (White Goods)
- Reversing induction motor controls
- Applications subject to high temperature ($T_{j(max)}$ = 150 °C)

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	-	800	V

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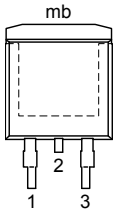
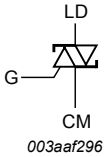
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)}$ = 25 °C; t_p = 20 ms; Fig. 4; Fig. 5		-	-	80	A
T_j	junction temperature			-	-	150	°C
$I_{T(RMS)}$	RMS on-state current	full sine wave; T_{mb} ≤ 131 °C; Fig. 1; Fig. 2; Fig. 3		-	-	8	A
V_{PP}	peak pulse voltage	T_j = 25 °C; non-repetitive, off-state; Fig. 6		-	-	2	kV
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 100 mA; LD+ G+; T_j = 25 °C; Fig. 8		5	-	35	mA
		V_D = 12 V; I_T = 100 mA; LD+ G-; T_j = 25 °C; Fig. 8		5	-	35	mA
		V_D = 12 V; I_T = 100 mA; LD- G-; T_j = 25 °C; Fig. 8		5	-	35	mA
V_{CL}	clamping voltage	I_{CL} = 0.1 mA; t_p = 1 ms; T_j = 25 °C		850	-	-	V
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit		4000	-	-	V/µs
		V_{DM} = 536 V; T_j = 150 °C; exponnetial waveform; gate open circuit		2000	-	-	V/µs
dI_{com}/dt	rate of change of commutating current	V_D = 400 V; T_j = 150 °C; $I_{T(RMS)}$ = 8 A; dV_{com}/dt = 20 V/µs; gate open circuit; snubberless condition		12	-	-	A/ms

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	CM	common	 **D2PAK (SOT404A)**	 *003aaf296*
2	LD	load		
3	G	gate		
mb	LD	mounting base; load		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
ACTT8B-800CTN	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404A

7. Marking

Table 4. Marking codes

Type number	Marking code
ACTT8B-800CTN	ACTT8B-800CTN

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 131$ °C; Fig. 1; Fig. 2; Fig. 3		-	8	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25$ °C; $t_p = 20$ ms; Fig. 4; Fig. 5		-	80	A
		full sine wave; $T_{j(init)} = 25$ °C; $t_p = 16.7$ ms		-	88	A
I^2t	I^2t for fusing	$t_p = 10$ ms; sine-wave pulse		-	32	A^2s
dI_T/dt	rate of rise of on-state current	$I_G = 70$ mA		-	100	A/µs
I_{GM}	peak gate current	t = 20 µs		-	2	A
P_{GM}	peak gate power			-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.5	W
T_{stg}	storage temperature			-40	150	°C
T_j	junction temperature			-	150	°C
V_{PP}	peak pulse voltage	$T_j = 25$ °C; non-repetitive, off-state; Fig. 6		-	2	kV

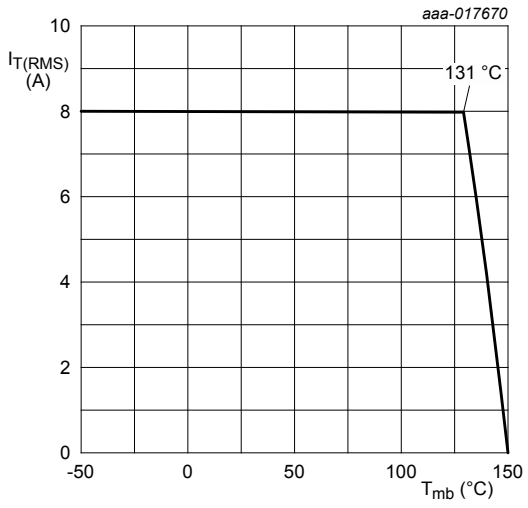
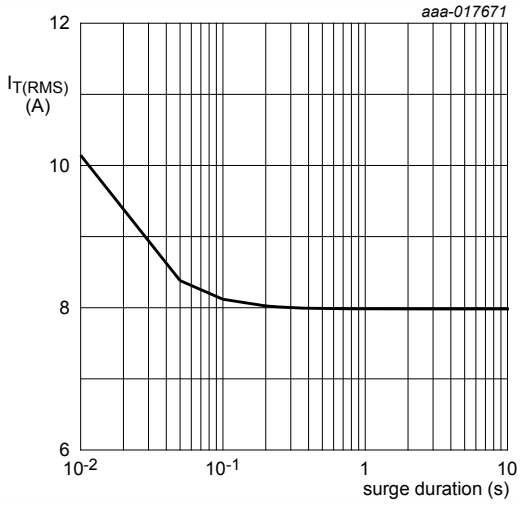
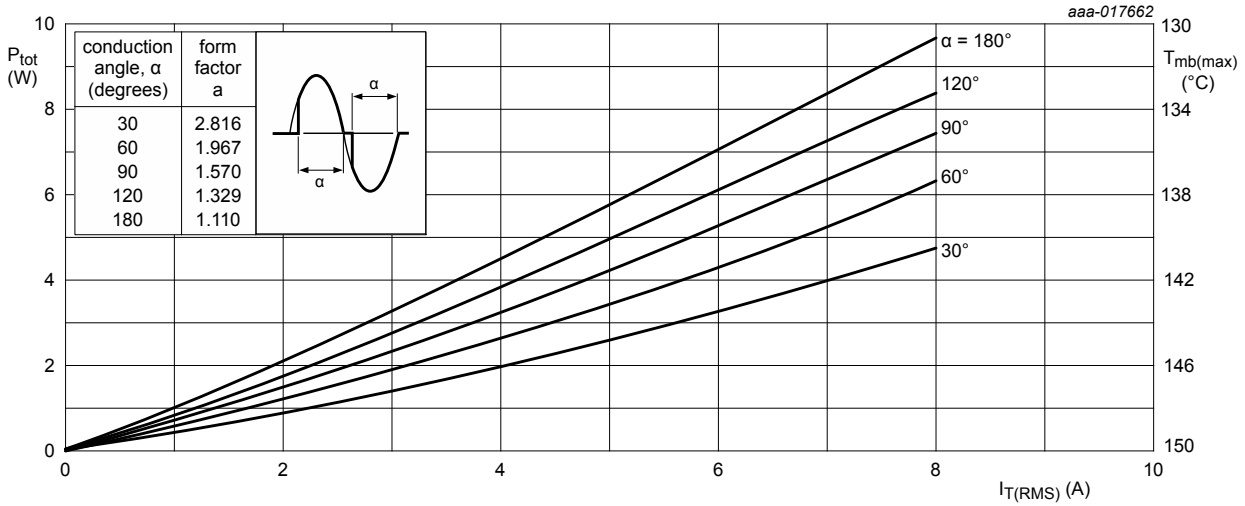


Fig. 1. RMS on-state current as a function of mounting base temperature; maximum values



f = 50 Hz; T_{mb} = 131 °C

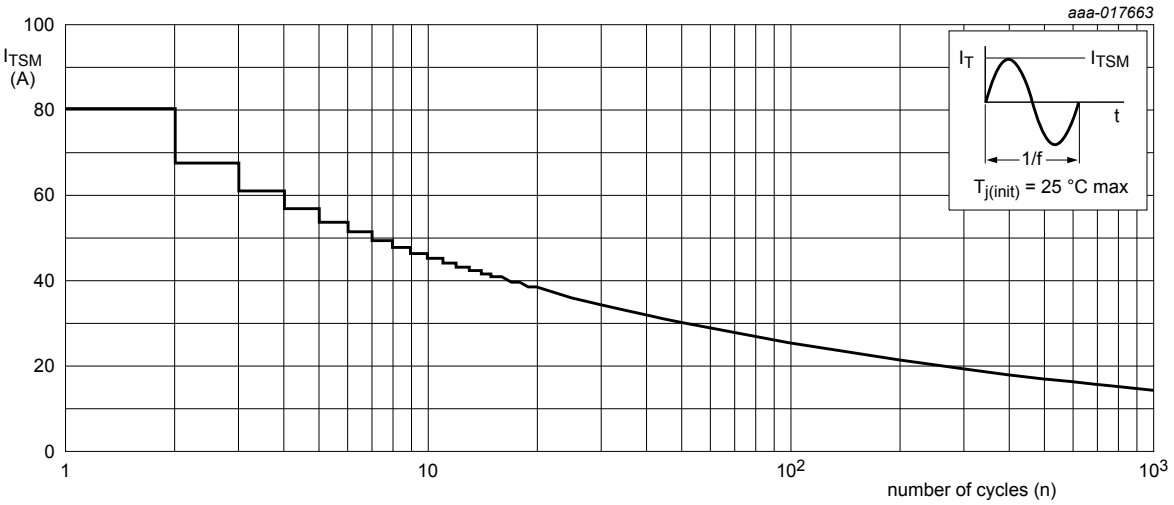
Fig. 2. RMS on-state current as a function of surge duration; maximum values



α = conduction angle

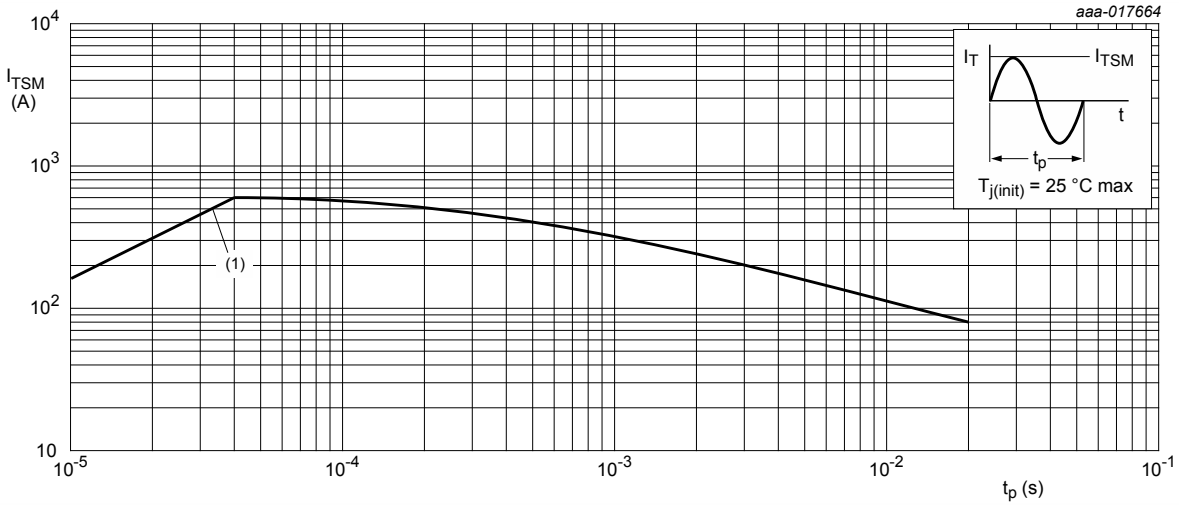
a = form factor = $I_{T(RMS)}$ / $I_{T(AV)}$

Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values



f = 50 Hz

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



$t_p \leq 20$ ms

(1) dI_T/dt limit

Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

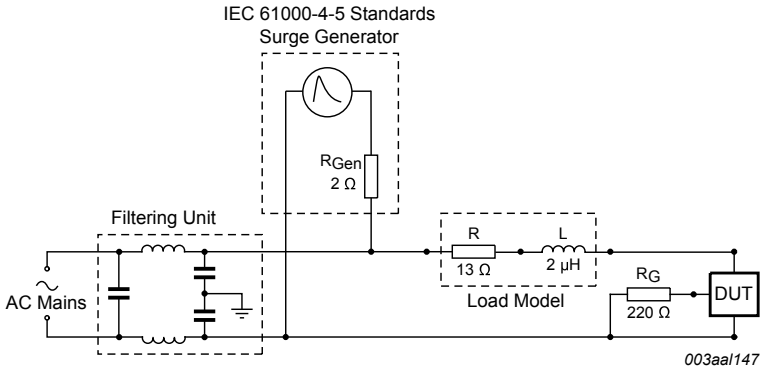


Fig. 6. Test circuit for inductive and resistive loads with conditions equivalent to IEC 61000-4-5

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	full cycle; Fig. 7		-	-	2	K/W
		half cycle		-	-	2.4	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; printed circuit board (FR4) mounted		-	55	-	K/W

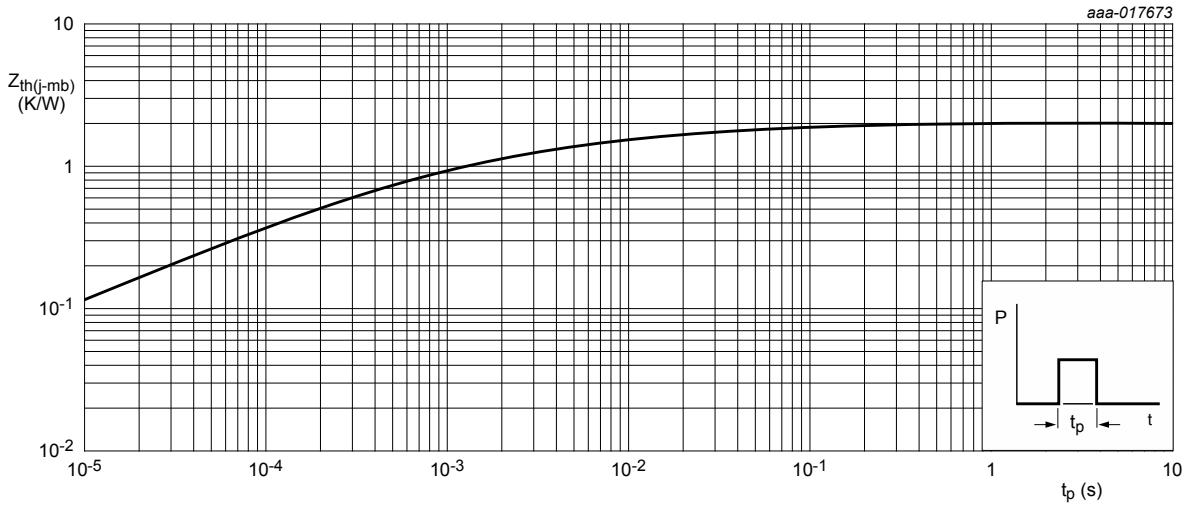
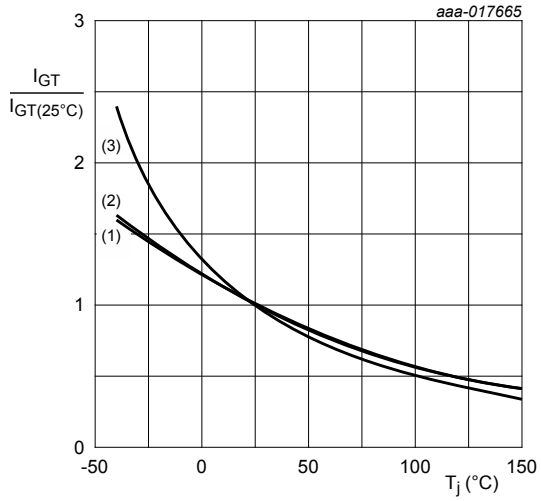


Fig. 7. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 100 mA; LD+ G+; T_j = 25 °C; Fig. 8		5	-	35	mA
		V_D = 12 V; I_T = 100 mA; LD+ G-; T_j = 25 °C; Fig. 8		5	-	35	mA
		V_D = 12 V; I_T = 100 mA; LD- G-; T_j = 25 °C; Fig. 8		5	-	35	mA
I_L	latching current	V_D = 12 V; I_G = 100 mA; LD+ G+; T_j = 25 °C; Fig. 9		-	-	50	mA
		V_D = 12 V; I_G = 100 mA; LD+ G-; T_j = 25 °C; Fig. 9		-	-	60	mA
		V_D = 12 V; I_G = 100 mA; LD- G-; T_j = 25 °C; Fig. 9		-	-	50	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 10		-	-	40	mA
V_T	on-state voltage	I_T = 10 A; T_j = 25 °C; Fig. 11		-	-	1.5	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 100 mA; T_j = 25 °C; Fig. 12		-	0.8	1	V
		V_D = 400 V; I_T = 100 mA; T_j = 150 °C; Fig. 12		0.2	0.45	-	V
I_D	off-state current	V_D = 800 V; T_j = 25 °C		-	-	10	µA
		V_D = 800 V; T_j = 150 °C		-	-	2	mA
V_{CL}	clamping voltage	I_{CL} = 0.1 mA; t_p = 1 ms; T_j = 25 °C		850	-	-	V
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit		4000	-	-	V/µs
		V_{DM} = 536 V; T_j = 150 °C; exponnetial waveform; gate open circuit		2000	-	-	V/µs
dI_{com}/dt	rate of change of commutating current	V_D = 400 V; T_j = 150 °C; $I_{T(RMS)}$ = 8 A; dV_{com}/dt = 20 V/µs; gate open circuit; snubberless condition		12	-	-	A/ms
		V_D = 400 V; T_j = 150 °C; $I_{T(RMS)}$ = 8 A; dV_{com}/dt = 10 V/µs; gate open circuit		15	-	-	A/ms
		V_D = 400 V; T_j = 150 °C; $I_{T(RMS)}$ = 8 A; dV_{com}/dt = 1 V/µs; gate open circuit		20	-	-	A/ms



(1) T2+ G+
(2) T2+ G-
(3) T2- G-

Fig. 8. Normalized gate trigger current as a function of junction temperature

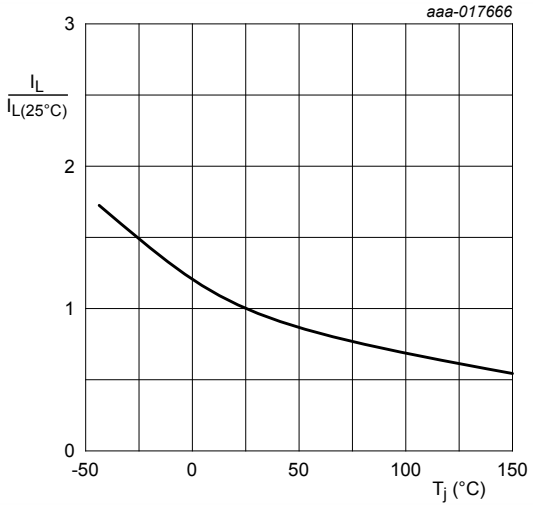


Fig. 9. Normalized latching current as a function of junction temperature

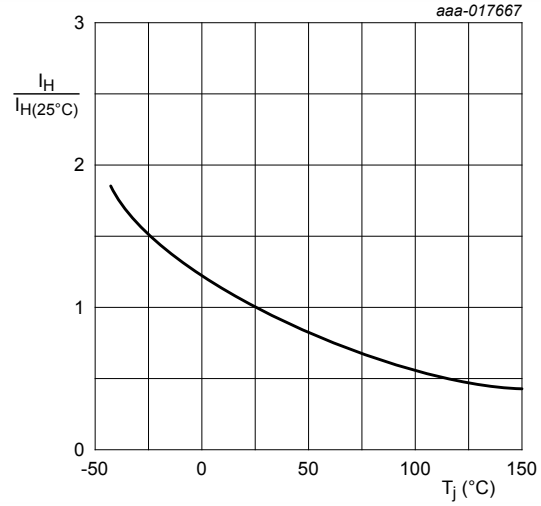
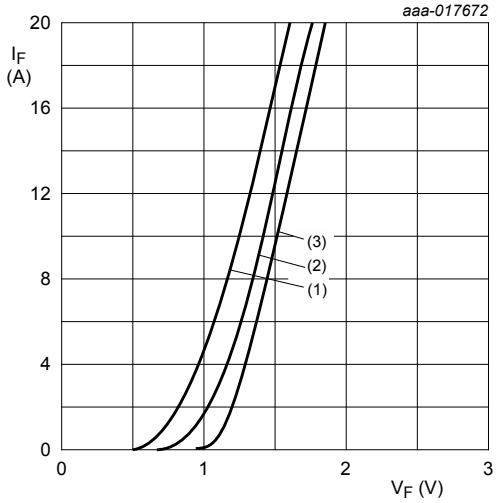


Fig. 10. Normalized holding current as a function of junction temperature



V_o = 1.089 V; R_s = 0.028 Ω
(1) T_j = 150 °C; typical values
(2) T_j = 150 °C; maximum values
(3) T_j = 25 °C; maximum values

Fig. 11. On-state current as a function of on-state voltage

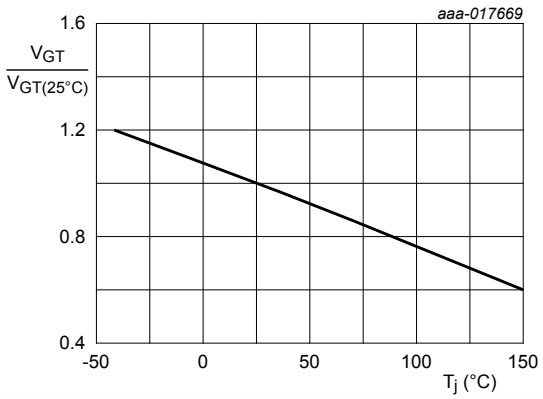
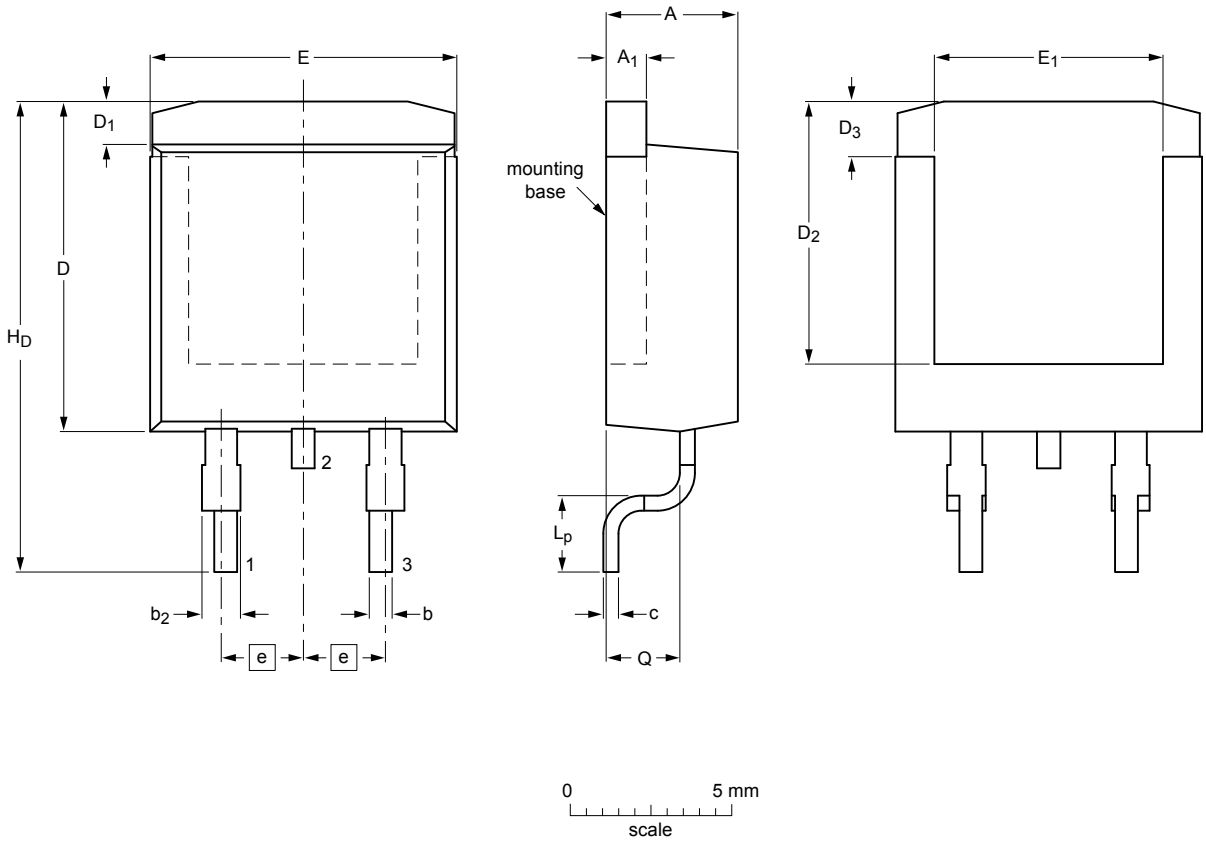


Fig. 12. Normalized gate trigger voltage as a function of junction temperature

11. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) **SOT404A**



Dimensions (mm are the original dimensions)

Unit		A	A_1	b	b_2	c	D_{max}	D_1	D_2	D_3	E	E_1	e	H_D	L_p	Q
mm	max	4.5	1.40	0.85	1.45	0.64	11	1.6	8.6	1.85	10.3	8.1		15.8	2.9	2.6
	nom												2.54			
	min	4.1	1.27	0.60	1.05	0.46		1.2	8.0	1.40	9.7	7.6		14.8	2.1	2.2

sot404a_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT404A						~~13-02-28~~ 13-03-12

Fig. 13. Package outline D2PAK (SOT404A)

12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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