

Double channel high-side driver with analog current sense for automotive applications

Datasheet - production data



Features

| | | |
|-----------------------------------|------------|--------------------------|
| Max transient supply voltage | V_{CC} | 41V |
| Operating voltage range | V_{CC} | 4.5 to 28V |
| Max on-state resistance (per ch.) | R_{ON} | 12 m Ω |
| Current limitation (typ) | I_{LIMH} | 74 A |
| Off-state supply current | I_S | 2 μ A ⁽¹⁾ |

1. Typical value with all loads connected

- General:
 - Inrush current active management by power limitation
 - Very low standby current
 - 3.0 V CMOS compatible input
 - Optimized electromagnetic emission
 - Very low electromagnetic susceptibility
 - In compliance with the 2002/95/EC european directive
 - Proportional load current sense
 - High current sense precision for wide range current
 - Very low current sense leakage
- Diagnostic functions:
 - Off-state open-load detection
 - Current sense disable
 - Thermal shutdown indication
 - Output short to V_{CC} detection
 - Overload and short to ground (power limitation) indication
- Protection:

- Undervoltage shutdown
- Overvoltage clamp
- Load current limitation
- Self limiting of fast thermal transients
- Protection against loss of ground and loss of V_{CC}
- Thermal shutdown
- Reverse battery protection with self switch of the Power MOS
- Electrostatic discharge protection

Applications

- All types of resistive, inductive and capacitive loads
- Suitable as LED driver

Description

The VND5E012AY-E is a device made using STMicroelectronics® VIPower® M0-5 technology. It is intended for driving resistive or inductive loads with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes.

This device integrates an analog current sense which delivers a current proportional to the load current when CS_DIS high leads the current sense pin in high impedance.

Fault conditions such as overload, overtemperature or openload are reported via the current sense pin.

Output current limitation protects the device in overload condition. In case of long overload duration, the device limits the dissipated power to safe level up to thermal shutdown intervention. Thermal shutdown with automatic restart allows the device to recover normal operation as soon as fault condition disappears.

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1 Block diagram and pin description

Figure 1. Block diagram

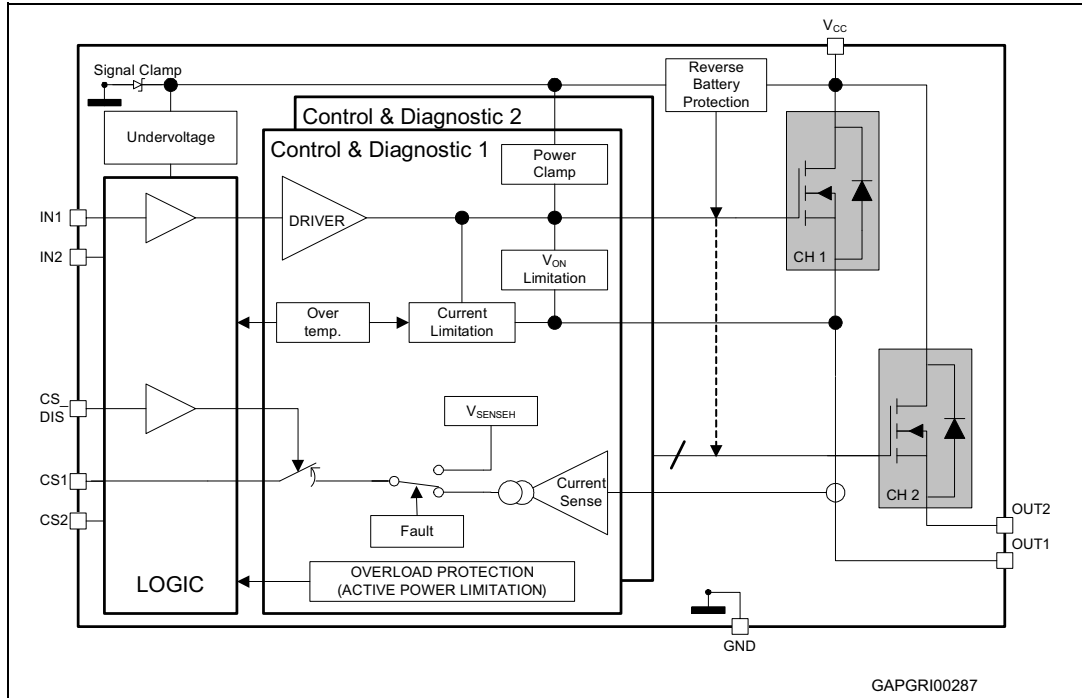


Table 1. Pin function

| Name | Function |
|--------------------|---|
| V _{CC} | Battery connection |
| OUT _{1,2} | Power output |
| GND | Ground connection |
| IN _{1,2} | Voltage controlled input pin with hysteresis, CMOS compatible; controls output switch state |
| CS _{1,2} | Analog current sense pin delivers a current proportional to the load current |
| CS_DIS | Active high CMOS compatible pin, to disable the current sense pin |

Figure 2. Configuration diagram (top view)

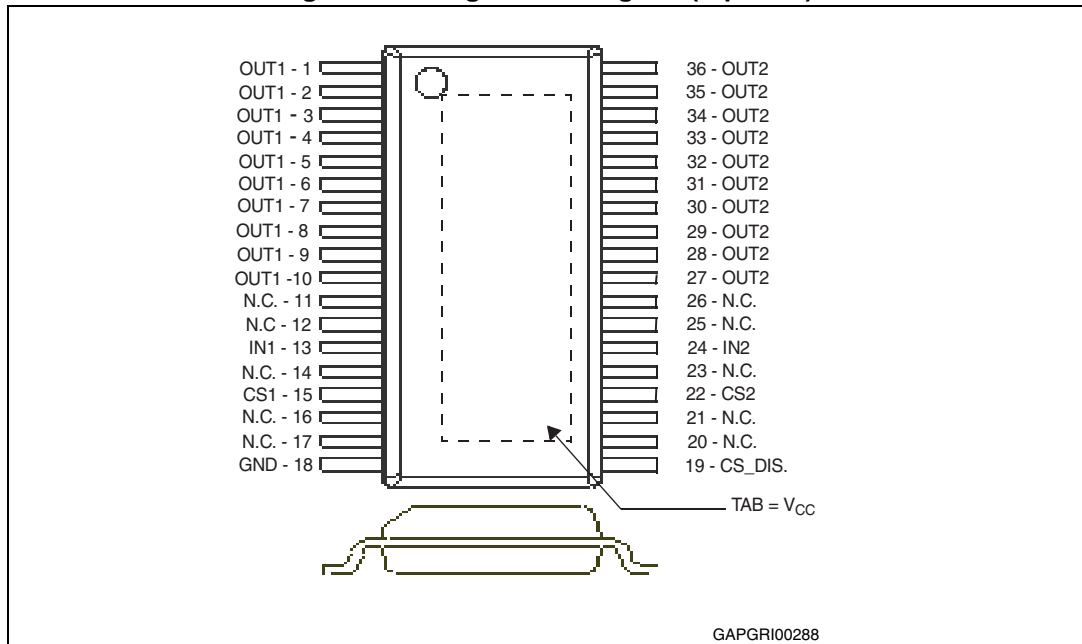
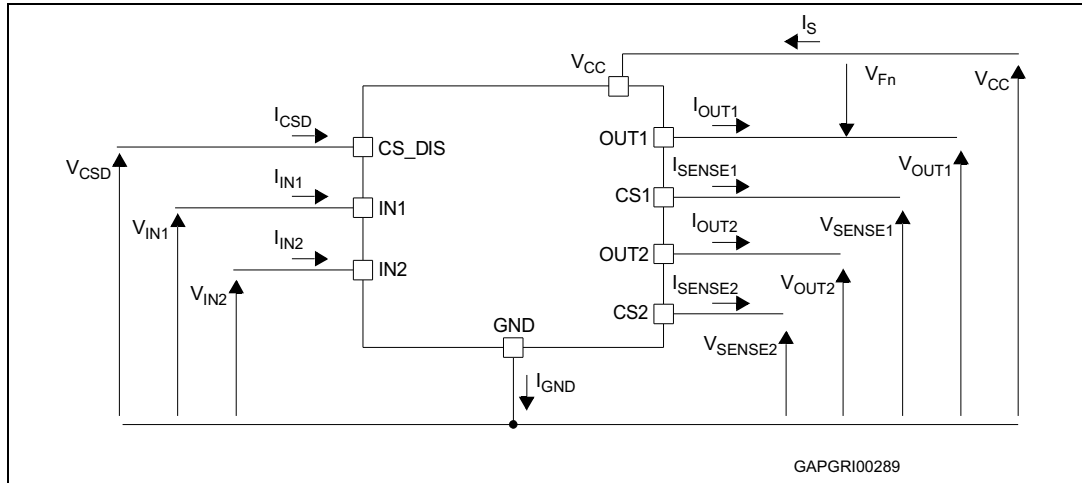


Table 2. Suggested connections for unused and not connected pins

| Connection / pin | Current sense | Not connected | Output | Input | CS_DIS |
|------------------|-----------------------|---------------|-------------|------------------------|------------------------|
| Floating | Not allowed | X | X | X | X |
| To ground | Through 1 KΩ resistor | X | Not allowed | Through 10 KΩ resistor | Through 10 KΩ resistor |

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Applying stress which exceeds the ratings listed in the [Table 3](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in this section for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|---------------|---|--------------------------|--------|
| V_{CC} | DC supply voltage | 28 | V |
| V_{CCPK} | Transient supply voltage ($T < 400$ ms, $R_{LOAD} > 0.5 \Omega$) | 41 | V |
| $-V_{CC}$ | Reverse DC supply voltage | 16 | V |
| V_{CC_LSC} | Maximum supply voltage for full protection to short-circuit (acc. AEC-Q100-012) | 18 | V |
| $-I_{GND}$ | DC reverse ground pin current | 200 | mA |
| I_{OUT} | DC output current | Internally limited | A |
| $-I_{OUT}$ | Reverse DC output current | 50 | A |
| I_{IN} | DC input current | -1 to 10 | mA |
| I_{CSD} | DC current sense disable input current | -1 to 10 | mA |
| $-I_{CSENSE}$ | DC Reverse CS pin current | 200 | mA |
| V_{CSENSE} | Current sense maximum voltage | $V_{CC}-41$ $+V_{CC}$ | V V |

Table 3. Absolute maximum ratings (continued)

| Symbol | Parameter | Value | Unit |
|-----------|--|----------------------|------------------|
| E_{MAX} | Maximum switching energy (single pulse) ($L = 0.47 \text{ mH}$; $R_L = 0 \text{ }\Omega$; $V_{bat} = 13.5 \text{ V}$; $T_{jstart} = 150 \text{ }^\circ\text{C}$; $I_{OUT} = I_{limL}(Typ.)$) | 110 | mJ |
| V_{ESD} | Electrostatic Discharge (Human Body Model: $R=1.5K\Omega$; $C=100\text{pF}$) – V_{CC} , OUTPUT – INPUT, CS_DIS – CURRENT SENSE | 5000 4000 2000 | V |
| V_{ESD} | Charge device model (CDM-AEC-Q100-011) | 750 | V |
| T_j | Junction operating temperature | -40 to 150 | $^\circ\text{C}$ |
| T_{stg} | Storage temperature | -55 to 150 | $^\circ\text{C}$ |

2.2 Thermal data

Table 4. Thermal data

| Symbol | Parameter | Maximum value | Unit |
|----------------|---|--|--------------------|
| $R_{thj-case}$ | Thermal resistance junction-case (With one channel ON) | 2 | $^\circ\text{C/W}$ |
| $R_{thj-amb}$ | Thermal resistance junction-ambient | See Figure 36 in the thermal section | $^\circ\text{C/W}$ |

2.3 Electrical characteristics

$8V < V_{CC} < 28V$; $-40^{\circ}C < T_j < 150^{\circ}C$, unless otherwise specified

Table 5. Power section

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|-------------------------------------|---|------|-------|-------|------------|
| V_{CC} | Operating supply voltage | | 4.5 | 13 | 28 | V |
| V_{USD} | Undervoltage shutdown | | | 3.5 | 4.5 | V |
| $V_{USDhyst}$ | Undervoltage shutdown hysteresis | | | 0.5 | | V |
| R_{ON} | On-state resistance | $I_{OUT}=5A$; $T_j=25^{\circ}C$ | | 11 | 16 | |
| | | $I_{OUT}=5A$; $T_j=150^{\circ}C$ | | | 24 | m Ω |
| | | $I_{OUT}=5A$; $V_{CC}=5V$; $T_j=25^{\circ}C$ | | | 16 | m Ω |
| $R_{ON REV}$ | Reverse battery on-state resistance | $V_{CC}=-13V$; $I_{OUT}=-5A$; $T_j=25^{\circ}C$ | | | 12 | m Ω |
| V_{clamp} | Clamp voltage | $I_S=20$ mA | 41 | 46 | 52 | V |
| I_S | Supply current | Off-state; $V_{CC}=13V$; $T_j=25^{\circ}C$; | | | | |
| | | $V_{IN}=V_{OUT}=V_{SENSE}=V_{CSD}=0$ V | | 2 (1) | 5 (1) | μ A |
| | | On-state; $V_{CC}=13V$; $V_{IN}=5V$; $I_{OUT}=0A$ | | 3.5 | 6.5 | mA |
| $I_{L(off)}$ | Off-state output current (2) | $V_{IN}=V_{OUT}=0V$; $V_{CC}=13V$; $T_j=25^{\circ}C$ | 0 | 0.01 | 3 | |
| | | $V_{IN}=V_{OUT}=0V$; $V_{CC}=13V$; $T_j=125^{\circ}C$ | 0 | | 5 | μ A |

1. PowerMOS leakage included

2. For each channel

Table 6. Switching ($V_{CC} = 13V$; $T_j = 25^{\circ}C$)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------------|---|---|------|-------------------------------|------|------------|
| $t_{d(on)}$ | Turn-on delay time | $R_L=2.6\Omega$ (see Figure 8) | - | 30 | - | μ s |
| $t_{d(off)}$ | Turn-off delay time | $R_L=2.6\Omega$ (see Figure 8) | - | 20 | - | μ s |
| $(dV_{OUT}/dt)_{on}$ | Turn-on voltage slope | $R_L=2.6\Omega$ | - | See Figure 28 | - | V/ μ s |
| $(dV_{OUT}/dt)_{off}$ | Turn-off voltage slope | $R_L=2.6\Omega$ | - | See Figure 29 | - | V/ μ s |
| W_{ON} | Switching energy losses during t_{WON} | $R_L=2.6\Omega$ (see Figure 8) | - | 1 | - | mJ |
| W_{OFF} | Switching energy losses during t_{WOFF} | $R_L=2.6\Omega$ (see Figure 8) | - | 0.5 | - | mJ |

Table 7. Current sense (8V<V_{CC}<18V)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--|--|--|--------------|--------------|--------------|----------------|
| K ₀ | I _{OUT} /I _{SENSE} | I _{OUT} =0.25A; V _{SENSE} =0.5V T _J = -40°C...150°C | 2615 | 5130 | 7770 | |
| K ₁ | I _{OUT} /I _{SENSE} | I _{OUT} =5A; V _{SENSE} =0.5V T _J =-40°C...150°C T _J =25°C...150°C | 4155 4530 | 5330 5330 | 6650 6130 | |
| dK ₁ /K ₁ ⁽¹⁾ | Current sense ratio drift | I _{OUT} =5A; V _{SENSE} = 0.5V; V _{CSD} =0V; T _J = -40 °C to 150 °C | -8 | | 8 | % |
| K ₂ | I _{OUT} /I _{SENSE} | I _{OUT} =10A; V _{SENSE} =4V T _J =-40°C...150°C T _J =25°C...150°C | 4705 4865 | 5290 5290 | 5950 5715 | |
| dK ₂ /K ₂ ⁽¹⁾ | Current sense ratio drift | I _{OUT} = 10 A; V _{SENSE} = 4 V; V _{CSD} =0V; T _J = -40 °C to 150 °C | -5 | | 5 | % |
| K ₃ | I _{OUT} /I _{SENSE} | I _{OUT} =25A; V _{SENSE} =4V T _J =-40°C...150°C T _J =25°C...150°C | 4935 4985 | 5250 5250 | 5565 5515 | |
| dK ₃ /K ₃ ⁽¹⁾ | Current sense ratio drift | I _{OUT} = 25 A; V _{SENSE} = 4 V; V _{CSD} = 0V; T _J = -40 °C to 150 °C | -4 | | 4 | % |
| I _{SENSE0} | Analog sense leakage current | I _{OUT} =0A; V _{SENSE} =0V; V _{CSD} =5V; V _{IN} =0V; T _J =-40°C...150°C V _{CSD} =0V; V _{IN} =5V; T _J =-40°C...150°C I _{OUT} =5A; V _{SENSE} =0V; V _{CSD} =V _{IN} =5V; | 0 0 0 | | 1 2 1 | μA μA μA |
| V _{SENSE} | Max analog sense output voltage | I _{OUT} =15A; V _{CSD} =0V | 5 | | | V |
| V _{SENSEH} | Analog sense output voltage in overtemperature condition | V _{CC} =13V; R _{SENSE} =10KΩ | | 8 | | V |
| I _{SENSEH} | Analog sense output current in overtemperature condition | V _{CC} =13V; V _{SENSE} =5V | | 9 | | mA |
| t _{DSSENSE1H} | Delay response time from falling edge of CS_DIS pin | V _{SENSE} <4V, 1.5A<I _{OUT} <25A I _{SENSE} =90% of I _{SENSE} max (see fig Figure 4) | | 50 | 100 | μs |

Table 7. Current sense (8V<V_{CC}<18V) (continued)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|------------------------|--|--|------|------|------|------|
| t _{DSENSE1L} | Delay Response time from rising edge of CS_DIS pin | V _{SENSE} <4V, 1.5A<I _{out} <25A I _{SENSE} =10% of I _{SENSE max} (see fig Figure 4) | | 5 | 20 | μs |
| t _{DSENSE2H} | Delay Response time from rising edge of INPUT pin | V _{SENSE} <4V, 1.5A<I _{out} <25A I _{SENSE} =90% of I _{SENSE max} (see fig Figure 4) | | 70 | 300 | μs |
| Δt _{DSENSE2H} | Delay response time between rising edge of output current and rising edge of current sense | V _{SENSE} < 4V, I _{SENSE} = 90% of I _{SENSEMAX} , I _{OUT} = 90% of I _{OUTMAX} I _{OUTMAX} = 5A (see Figure 9) | | | 300 | μs |
| t _{DSENSE2L} | Delay Response time from falling edge of INPUT pin | V _{SENSE} <4V, 1.5A<I _{out} <25A I _{SENSE} =10% of I _{SENSE max} (see fig Figure 4) | | 100 | 250 | μs |

1. Parameter guaranteed by design; it is not tested.

Table 8. Open-load detection (8V<V_{CC}<18V)

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|-----------------------|---|---|------|-----|------|------|
| V _{OL} | Openload off-state voltage detection threshold | V _{IN} = 0V | 2 | - | 4 | V |
| t _{DSTKON} | Output short circuit to V _{CC} detection delay at turn-off | see Figure 5 | 180 | - | 1200 | μs |
| I _{L(off2)r} | Off-state output current at V _{OUT} = 4 V | V _{IN} = 0 V; V _{SENSE} = 0 V V _{OUT} rising from 0 V to 4 V | -120 | - | 90 | μA |
| I _{L(off2)f} | Off-state output current at V _{OUT} = 2V | V _{IN} = 0 V; V _{SENSE} = V _{SENSEH} V _{OUT} falling to V _{CC} to 2 V | -50 | - | 90 | μA |

Table 9. Protections ⁽¹⁾

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-------------------|--|--|---------------------|---------------------|------------|--------|
| I _{limH} | DC Short circuit current | V _{CC} =13V 5V<V _{CC} <18V | 52 | 74 | 104 104 | A A |
| I _{limL} | Short circuit current during thermal cycling | V _{CC} =13V; T _R <T _j <T _{TSD} | | 18.5 | | A |
| T _{TSD} | Shutdown temperature | | 150 | 175 | 200 | °C |
| T _R | Reset temperature | | T _{RS} + 1 | T _{RS} + 5 | | °C |
| T _{RS} | Thermal reset of STATUS | | 135 | | | °C |

Table 9. Protections ⁽¹⁾ (continued)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------------|--|---|---------------------|---------------------|---------------------|------|
| T _{HYST} | Thermal hysteresis (T _{TSD} -T _R) | | | 7 | | °C |
| V _{DEMAG} | Turn-off output voltage clamp | I _{OUT} =2A; V _{IN} =0; L=6mH | V _{CC} -28 | V _{CC} -31 | V _{CC} -35 | V |
| V _{ON} | Output voltage drop limitation | I _{OUT} =0.4A; T _j =-40°C...150°C (see fig. Figure 10) | | 25 | | mV |

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles

Table 10. Logic input

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|------------------------|---------------------------|---|------|------|------|--------|
| V _{IL} | Input low level voltage | | | | 0.9 | V |
| I _{IL} | Low level input current | V _{IN} =0.9V | 1 | | | μA |
| V _{IH} | Input high level voltage | | 2.1 | | | V |
| I _{IH} | High level input current | V _{IN} =2.1V | | | 10 | μA |
| V _{I(hyst)} | Input hysteresis voltage | | 0.25 | | | V |
| V _{ICL} | Input clamp voltage | I _{IN} =1mA I _{IN} =-1mA | 5.5 | -0.7 | 7 | V V |
| V _{CSDL} | CS_DIS low level voltage | | | | 0.9 | V |
| I _{CSDL} | Low level CS_DIS current | V _{CSD} =0.9V | 1 | | | μA |
| V _{CSDH} | CS_DIS high level voltage | | 2.1 | | | V |
| I _{CSDH} | High level CS_DIS current | V _{CSD} =2.1V | | | 10 | μA |
| V _{CSD(hyst)} | CS_DIS hysteresis voltage | | 0.25 | | | V |
| V _{CACL} | CS_DIS clamp voltage | I _{CSD} =1mA I _{CSD} =-1mA | 5.5 | -0.7 | 7 | V V |

Figure 4. Current sense delay characteristics

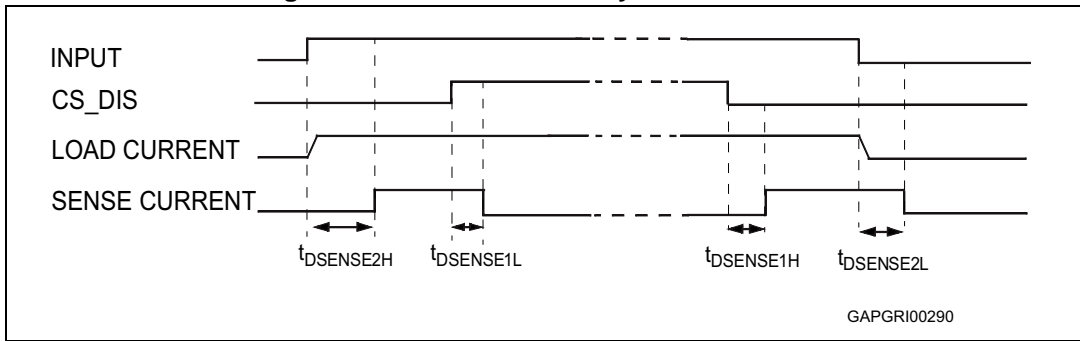


Figure 5. Open-load off-state delay timing

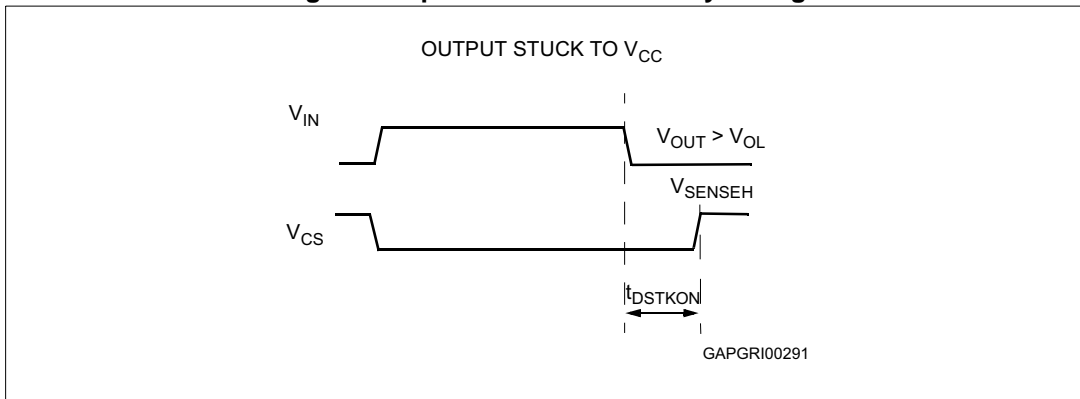


Figure 6. I_{OUT}/I_{SENSE} vs I_{OUT}

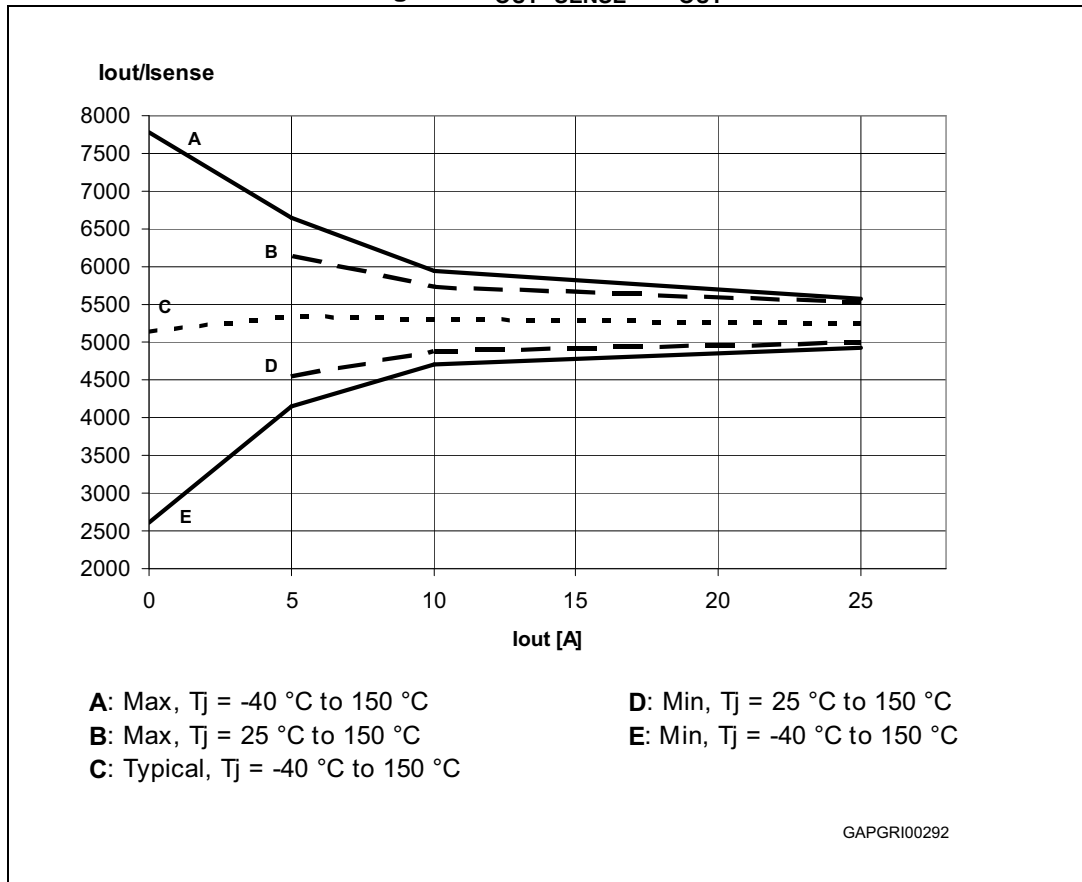


Figure 7. Maximum current sense ratio drift vs load current

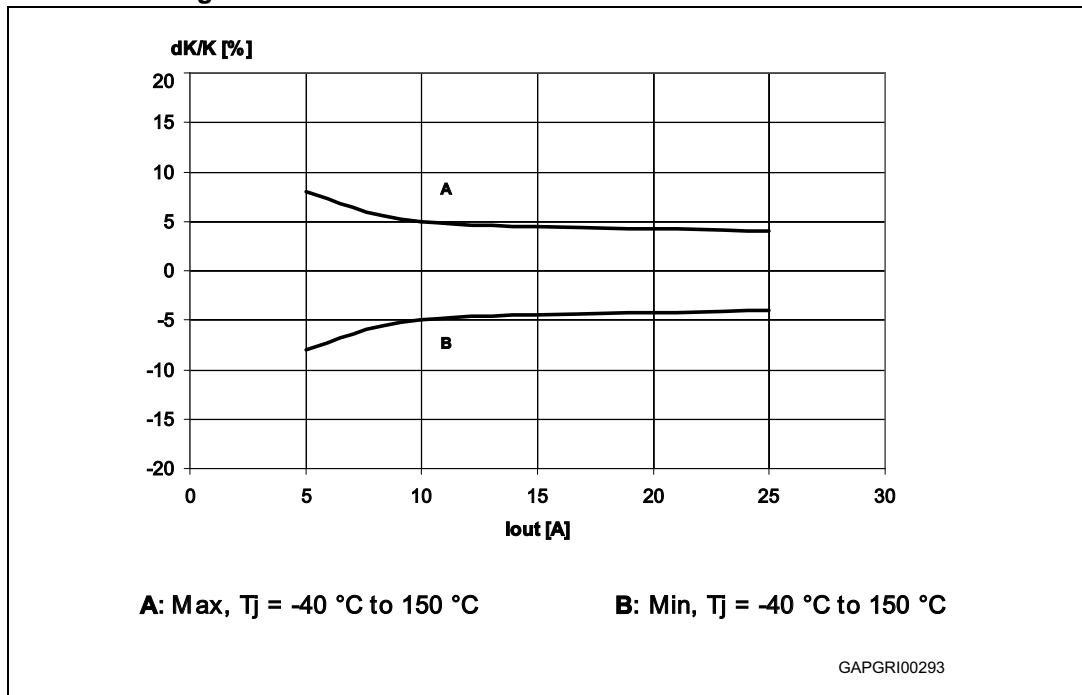


Table 11. Truth table

| Conditions | Input | Output | Sense($V_{CSD}=0V$) ⁽¹⁾ |
|--|-------|-------------------------------|--------------------------------------|
| Normal operation | L | L | 0 |
| | H | H | Nominal |
| Overtemperature | L | L | 0 |
| | H | L | V_{SENSEH} |
| Undervoltage | L | L | 0 |
| | H | L | 0 |
| Overload | H | X (no power limitation) | Nominal |
| | H | Cycling (power limitation) | V_{SENSEH} |
| Short circuit to GND (Power limitation) | L | L | 0 |
| | H | L | V_{SENSEH} |
| Open load off-state (with external pull up) | L | H | V_{SENSEH} |
| Short circuit to V_{CC} (external pull up disconnected) | L | H | V_{SENSEH} |
| | H | H | < Nominal |
| Negative output voltage clamp | L | L | 0 |

1. If the V_{CSD} is high, the SENSE output is at a high impedance; its potential depends on leakage currents and external circuit

Figure 8. Switching characteristics

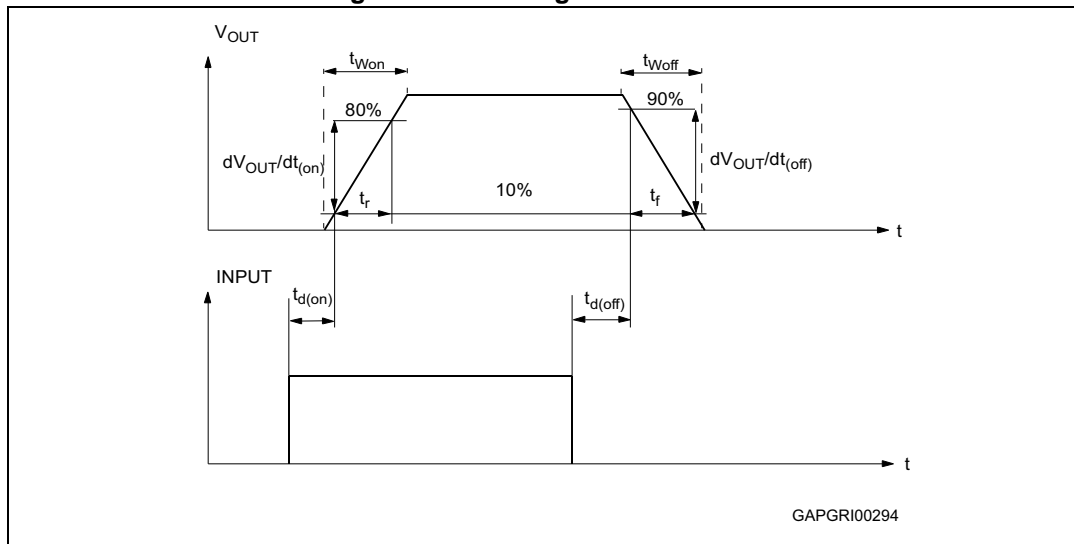


Figure 9. Delay response time between rising edge of ouput current and rising edge of current sense (CS enabled)

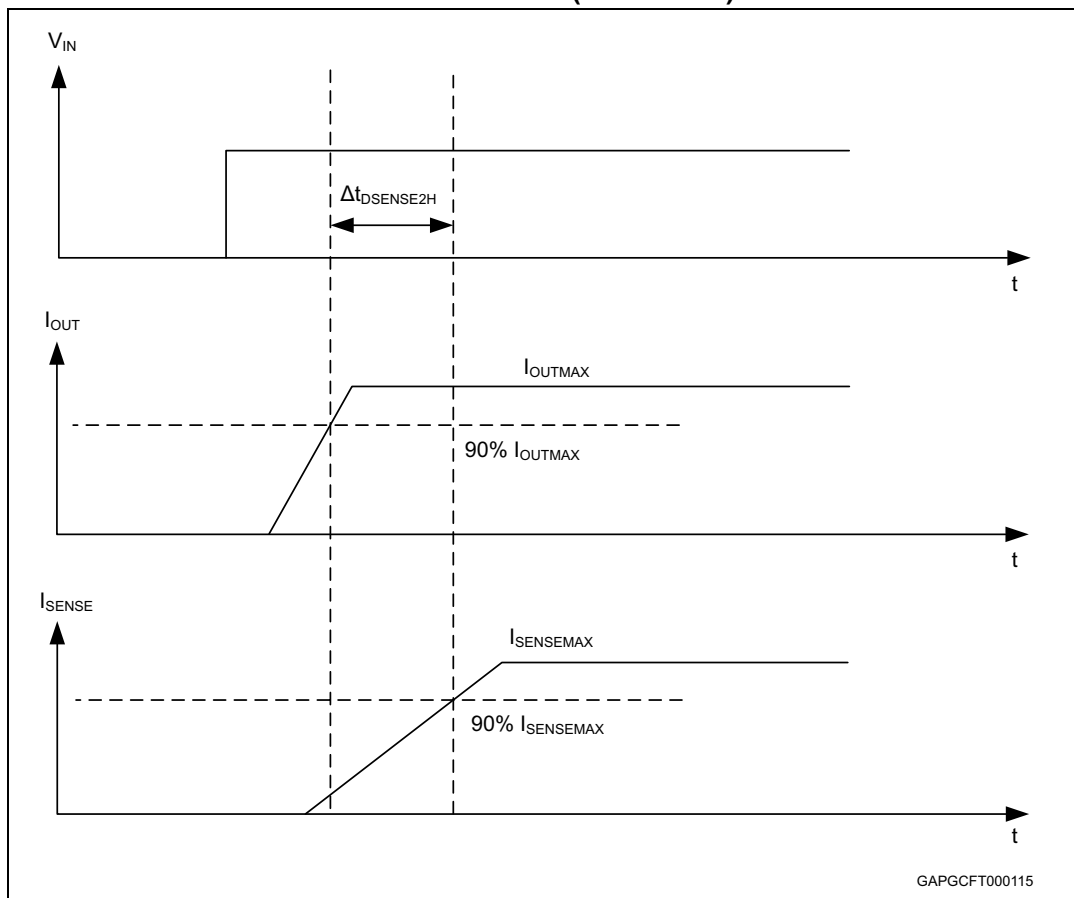


Figure 10. Output voltage drop limitation

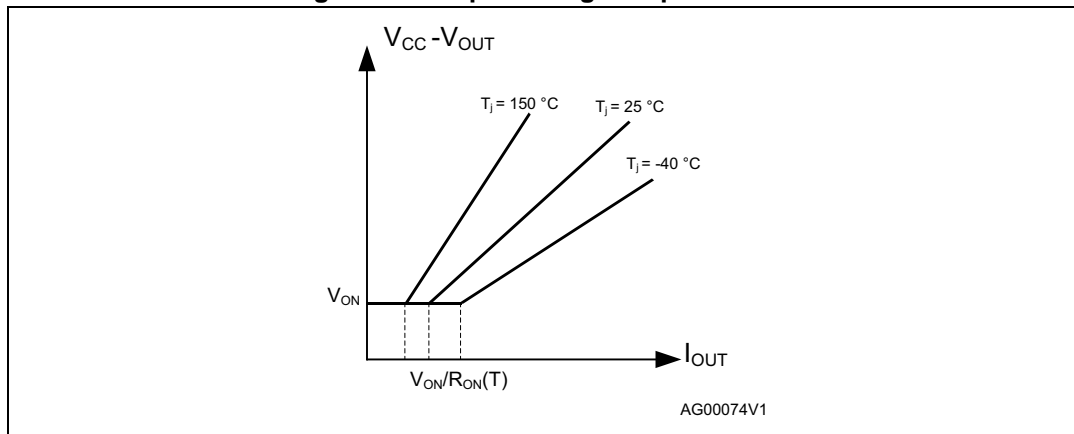


Table 12. Electrical transient requirements (part 1)

| ISO 7637-2: 2004(E) Test Pulse | Test levels ⁽¹⁾ | | Number of pulses or test times | Burst cycle/pulse repetition time | | Delays and impedance |
|--------------------------------------|----------------------------|--------|--------------------------------------|--------------------------------------|--------|--------------------------|
| | III | IV | | | | |
| 1 | -75 V | -100 V | 5000 pulses | 0.5 s | 5 s | 2 ms, 10 Ω |
| 2a | +37 V | +50 V | 5000 pulses | 0.2 s | 5 s | 50 μ s, 2 Ω |
| 3a | -100 V | -150 V | 1h | 90 ms | 100 ms | 0.1 μ s, 50 Ω |
| 3b | +75 V | +100 V | 1h | 90 ms | 100 ms | 0.1 μ s, 50 Ω |
| 4 | -6 V | -7 V | 1 pulse | | | 100 ms, 0.01 Ω |
| 5b ⁽²⁾ | +65 V | +87 V | 1 pulse | | | 400 ms, 2 Ω |

1. The above test levels must be considered referred to $V_{CC} = 13.5$ V except for pulse 5b
2. Valid in case of external load dump clamp: 40V maximum referred to ground. The protection strategy allows PowerMOS to be cyclically switched on during load dump, so distributing the load dump energy along the time and to transfer a part of it to the load.

Table 13. Electrical transient requirements (part 2)

| ISO 7637-2: 2004(E) Test pulse | Test level results ⁽¹⁾ | |
|--------------------------------------|-----------------------------------|----|
| | III | IV |
| 1 | C | C |
| 2a | C | C |
| 3a | C | C |
| 3b | C | C |
| 4 | C | C |
| 5b ⁽²⁾ (3) | C | C |

1. The above test levels must be considered referred to $V_{CC} = 13.5$ V except for pulse 5b
2. Valid in case of external load dump clamp: 40V maximum referred to ground. The protection strategy allows PowerMOS to be cyclically switched on during load dump, so distributing the load dump energy along the time and to transfer a part of it to the load.
3. Suppressed load dump (pulse 5b) is withstood with a minimum load connected as specified in [Table 3: Absolute maximum ratings](#)

Table 14. Electrical transient requirements (part 3)

| Class | Contents |
|-------|--|
| C | All functions of the device are performed as designed after exposure to disturbance. |
| E | One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device. |

2.4 Waveforms

Figure 11. Normal operation

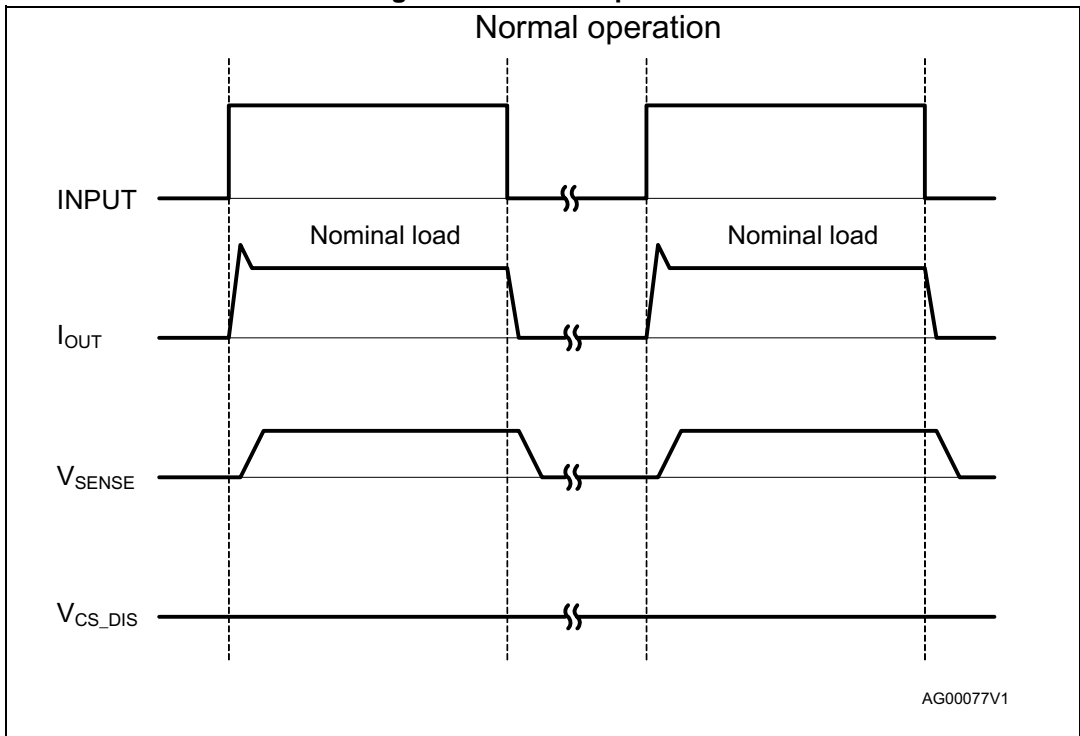


Figure 12. Overload or short to GND

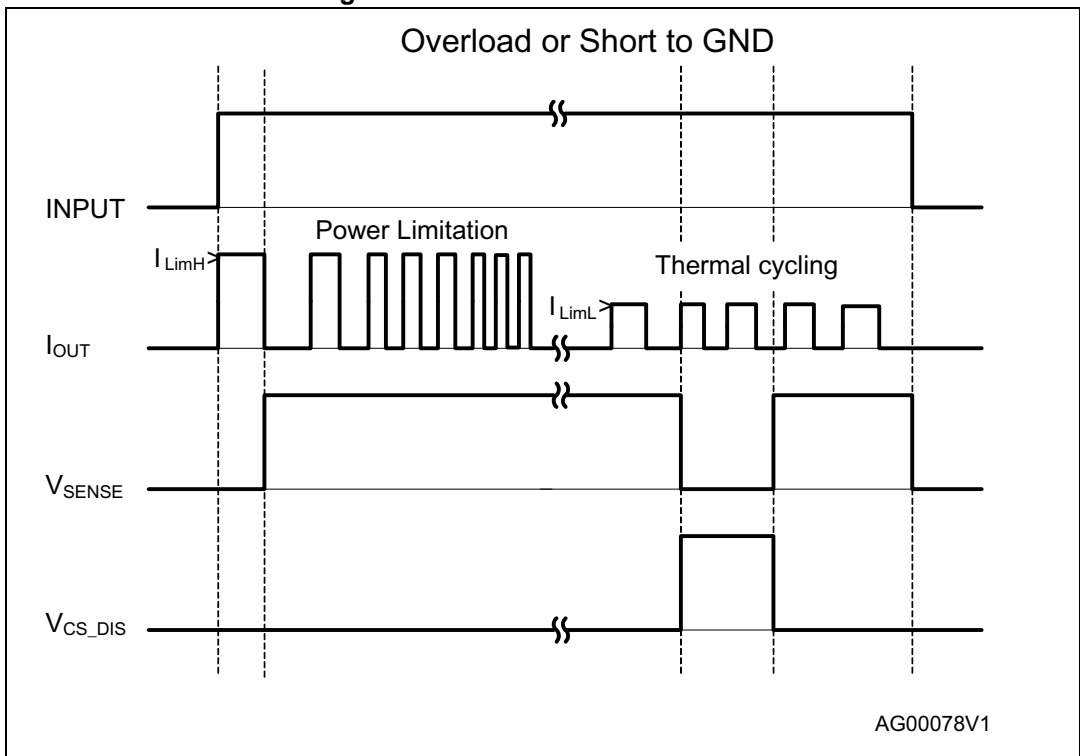


Figure 13. Intermittent overload

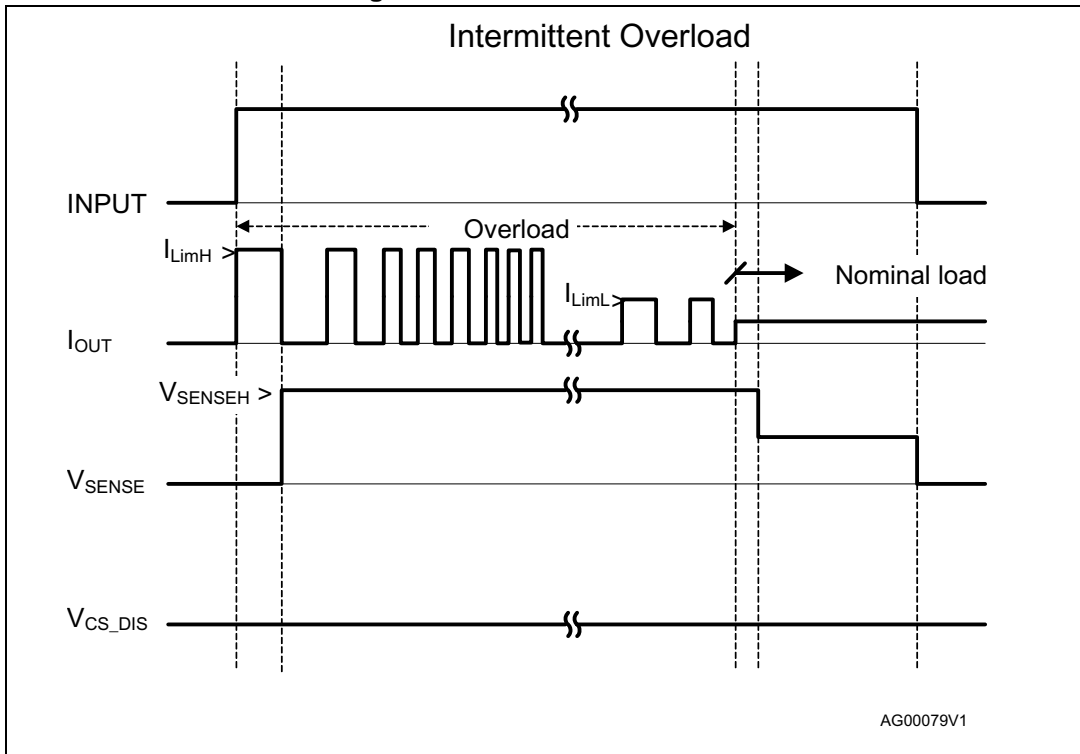
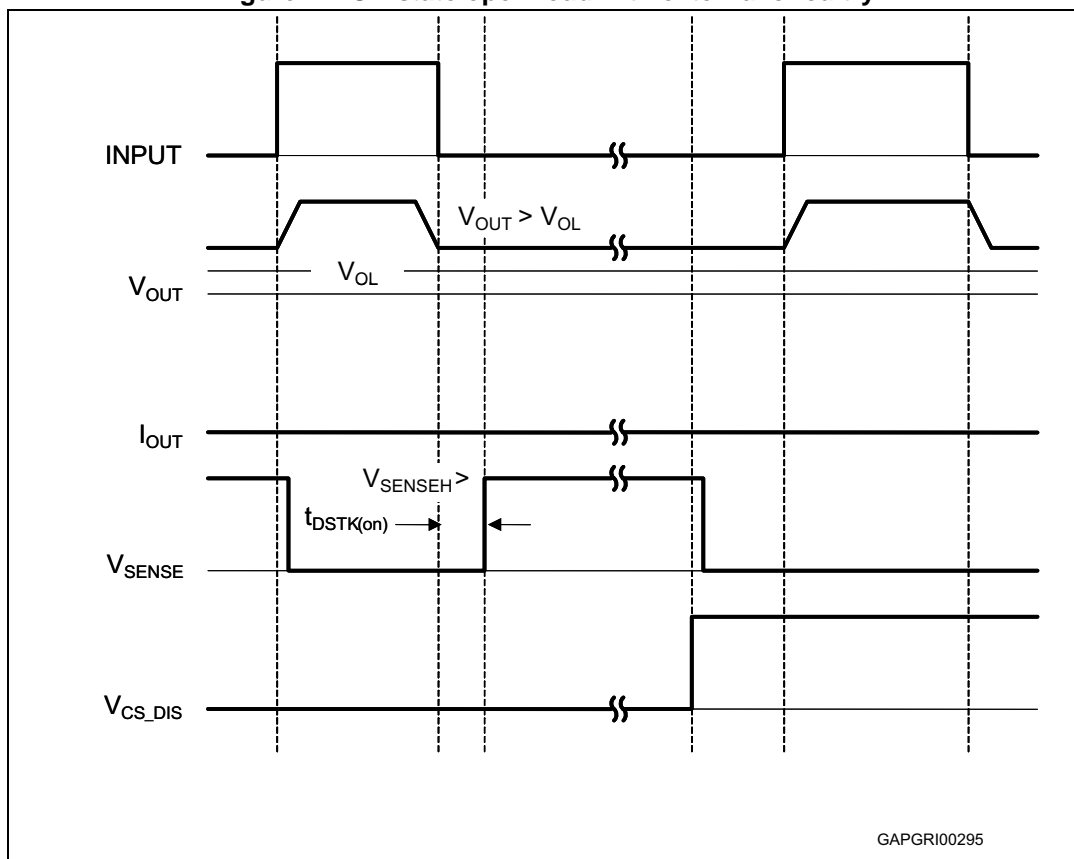


Figure 14. Off-state open-load with external circuitry



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Figure 15. Short to V_{CC}

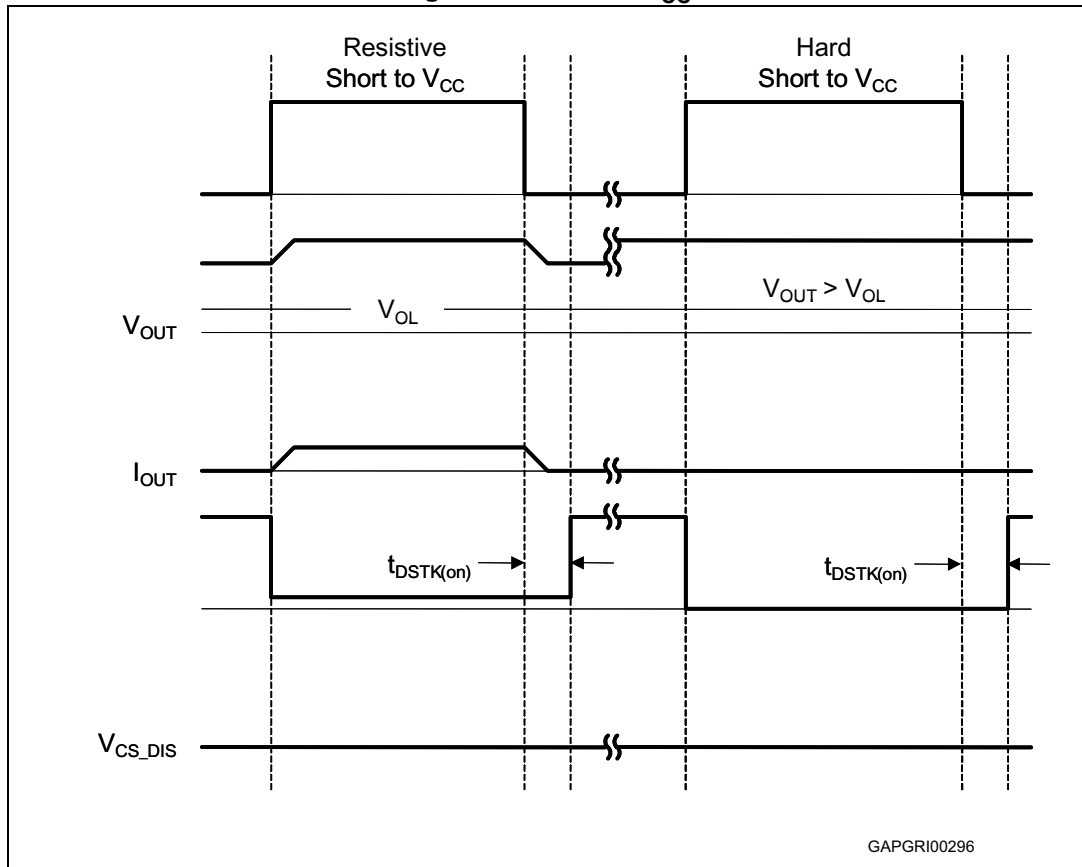
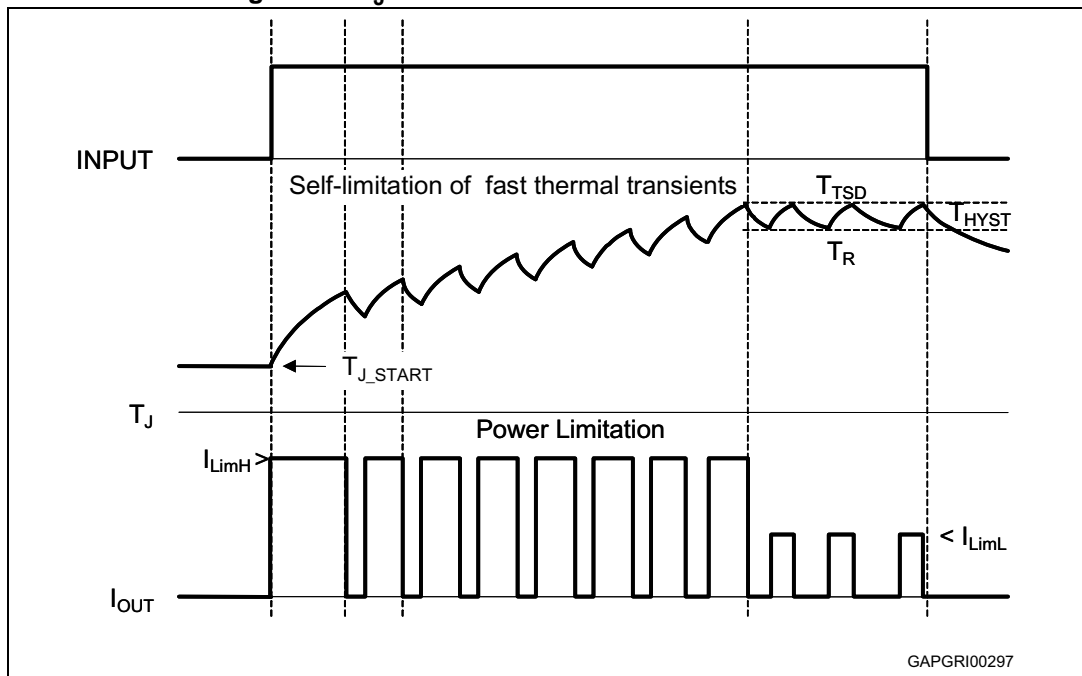


Figure 16. T_J evolution in overload or short to GND



2.5 Electrical characteristics curves

Figure 17. Off-state output current

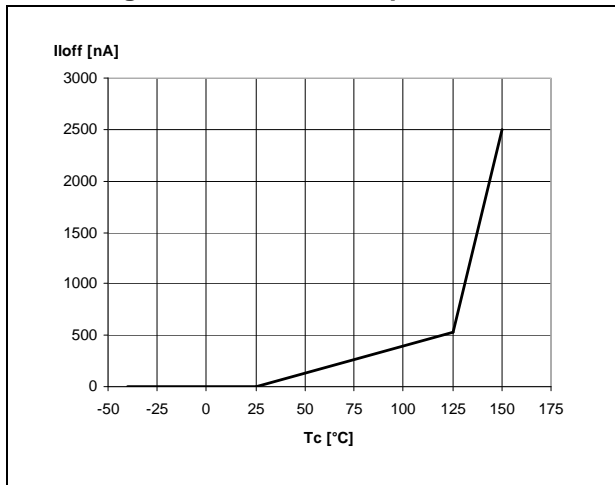


Figure 18. High level input current

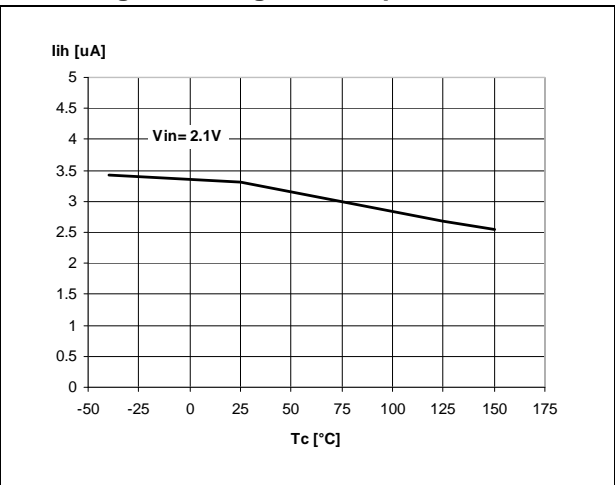


Figure 19. Input clamp voltage

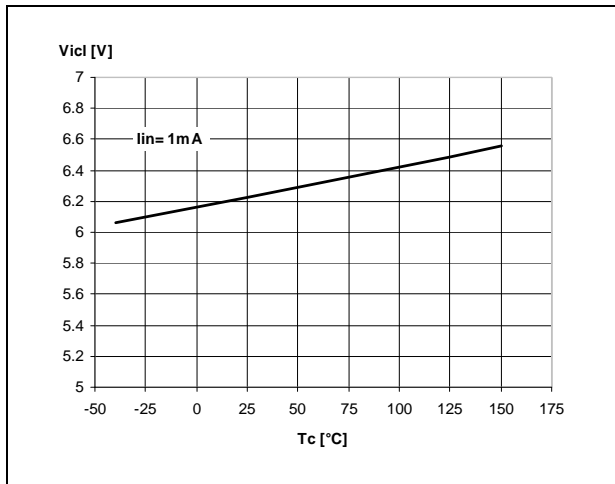


Figure 20. Input high level voltage

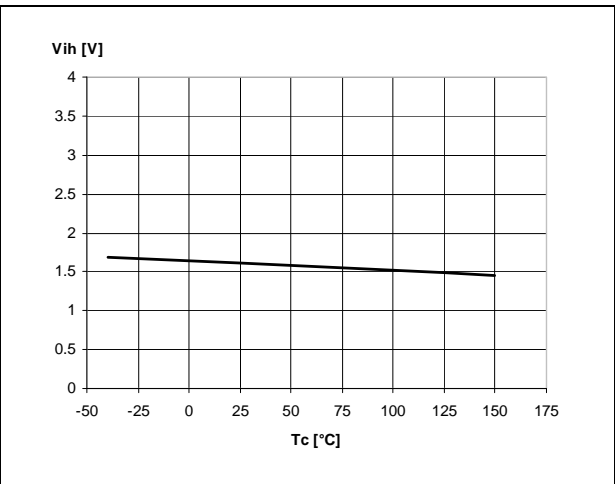


Figure 21. Input low level voltage

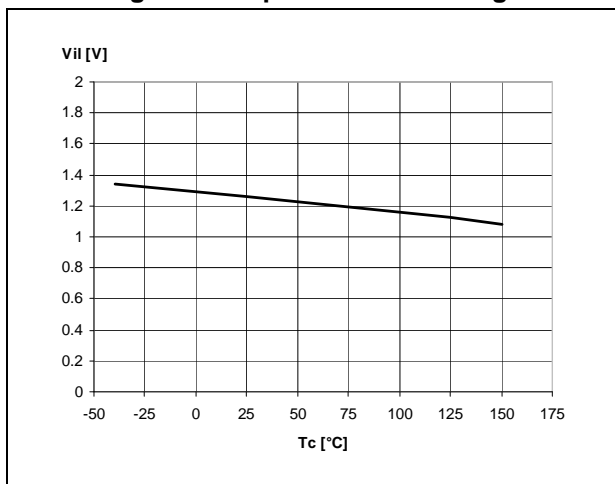


Figure 22. Input hysteresis voltage

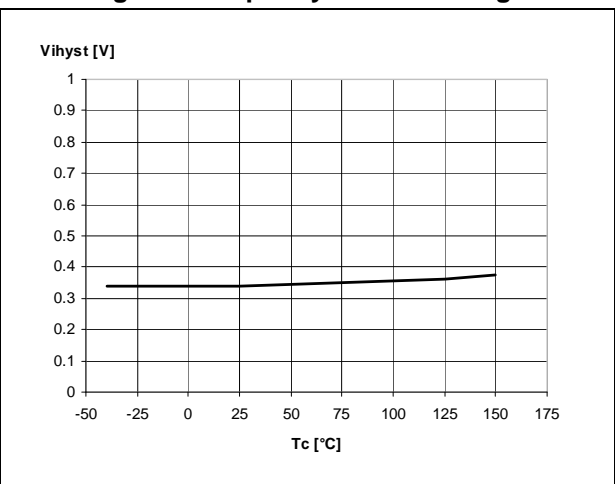


Figure 23. On-state resistance vs T_{case}

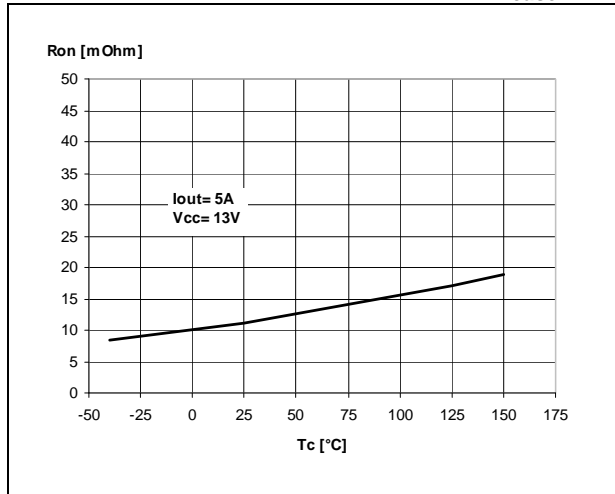


Figure 24. On-state resistance vs V_{CC}

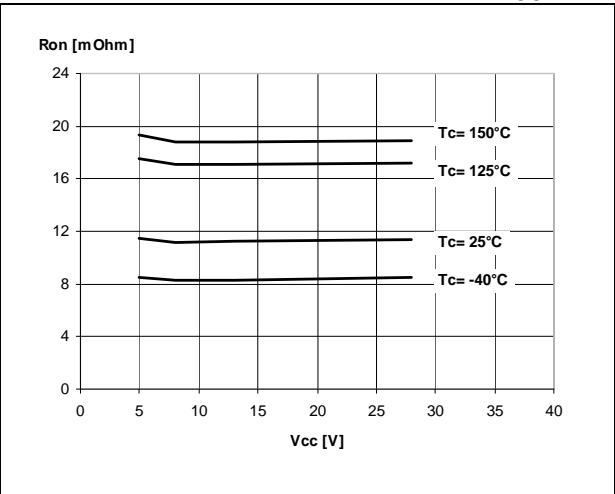


Figure 25. Undervoltage shutdown

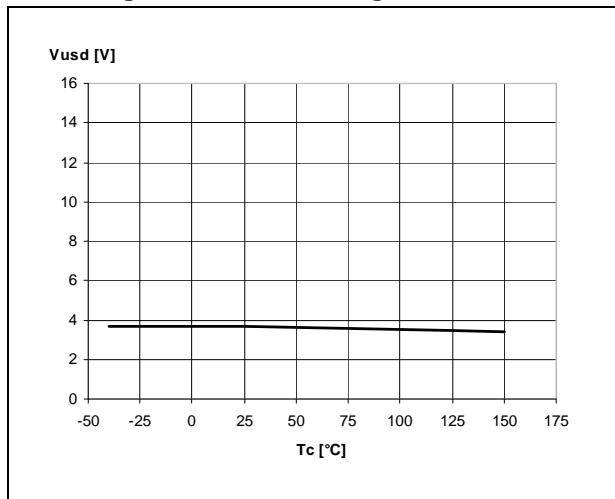


Figure 26. I_{LIMH} vs T_{case}

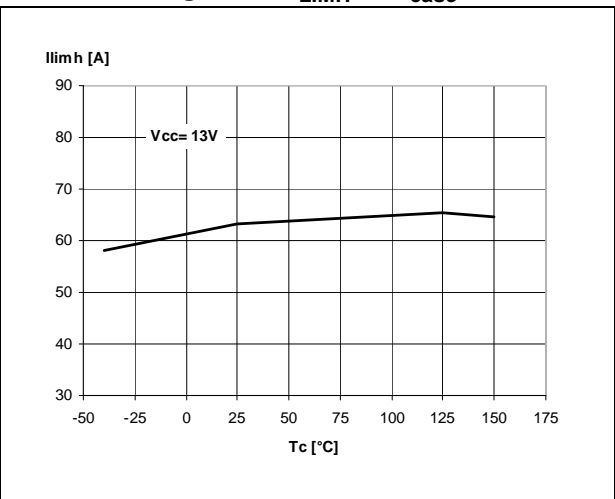


Figure 27. Turn-on voltage slope

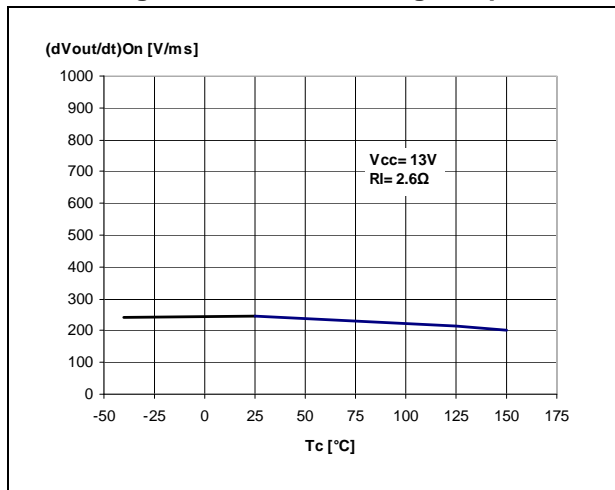


Figure 28. Turn-off voltage slope

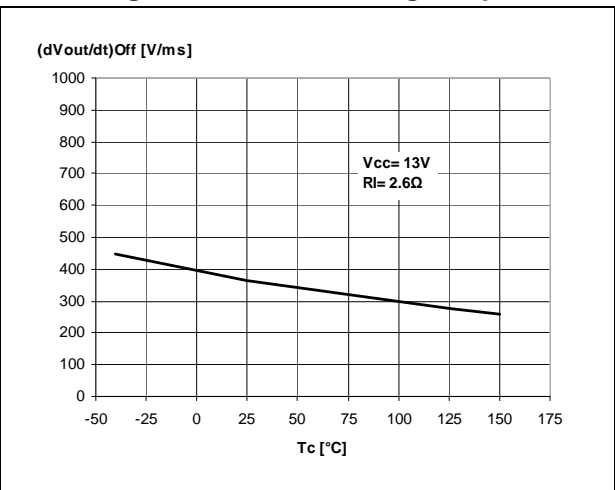


Figure 29. CS_DIS clamp voltage

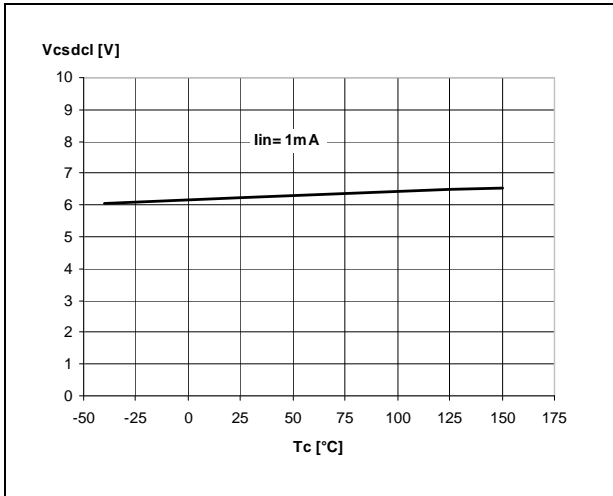


Figure 30. Low level CS_DIS voltage

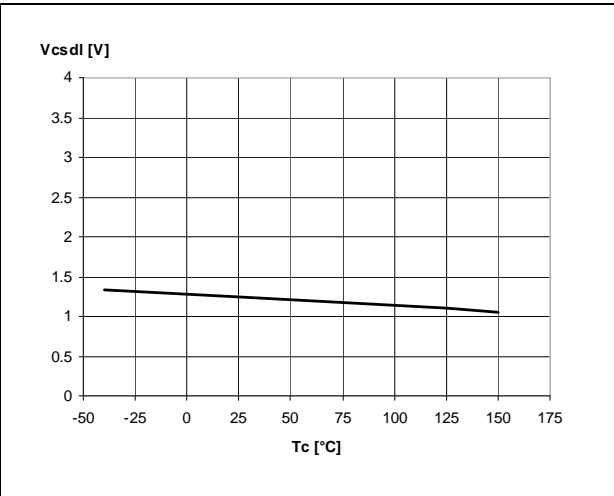
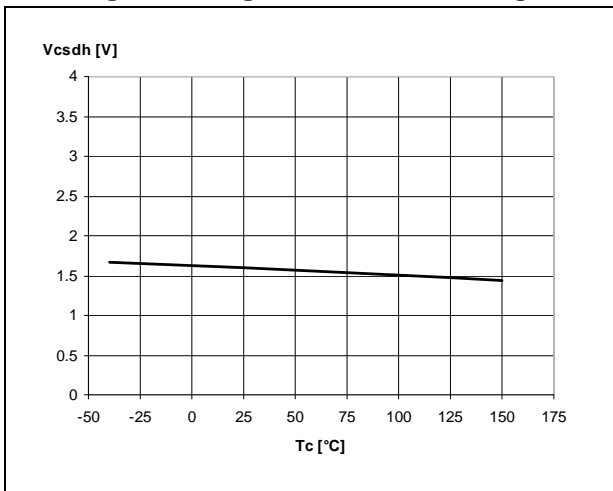
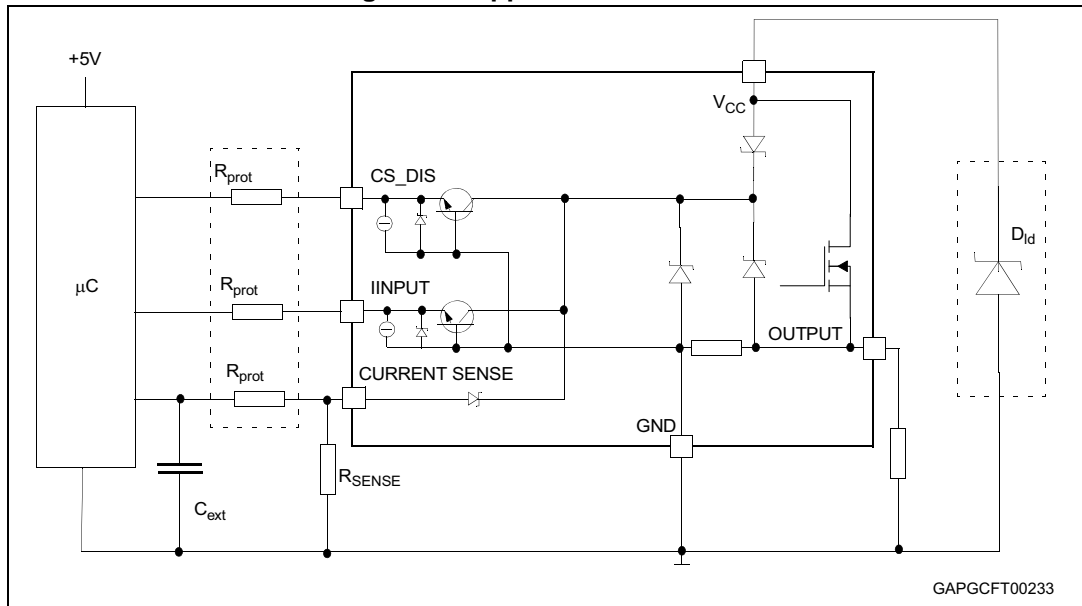


Figure 31. High level CS_DIS voltage



3 Application information

Figure 32. Application schematic



Note: Channel 2 has the same internal circuit as channel 1.

3.1 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the V_{CCPK} max rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

3.2 MCU I/Os protection

When negative transients are present on the V_{CC} line, the control pin is pulled negative to approximately -1.5 V. ST suggests to insert a resistor (R_{prot}) in line to prevent the microcontroller I/Os pins from latching-up.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (input levels compatibility) with the latch-up limit of microcontroller I/Os.

Equation 1

$$V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH}) / I_{IHmax}$$

Calculation example:

For V_{CCpeak} = - 1.5 V; I_{latchup} ≥ 20 mA; V_{OHμC} ≥ 4.5 V

$$75 \Omega \leq R_{prot} \leq 240 \text{ k}\Omega.$$

Recommended values: $R_{\text{prot}} = 10 \text{ k}\Omega$, $C_{\text{EXT}} = 10 \text{ nF}$.

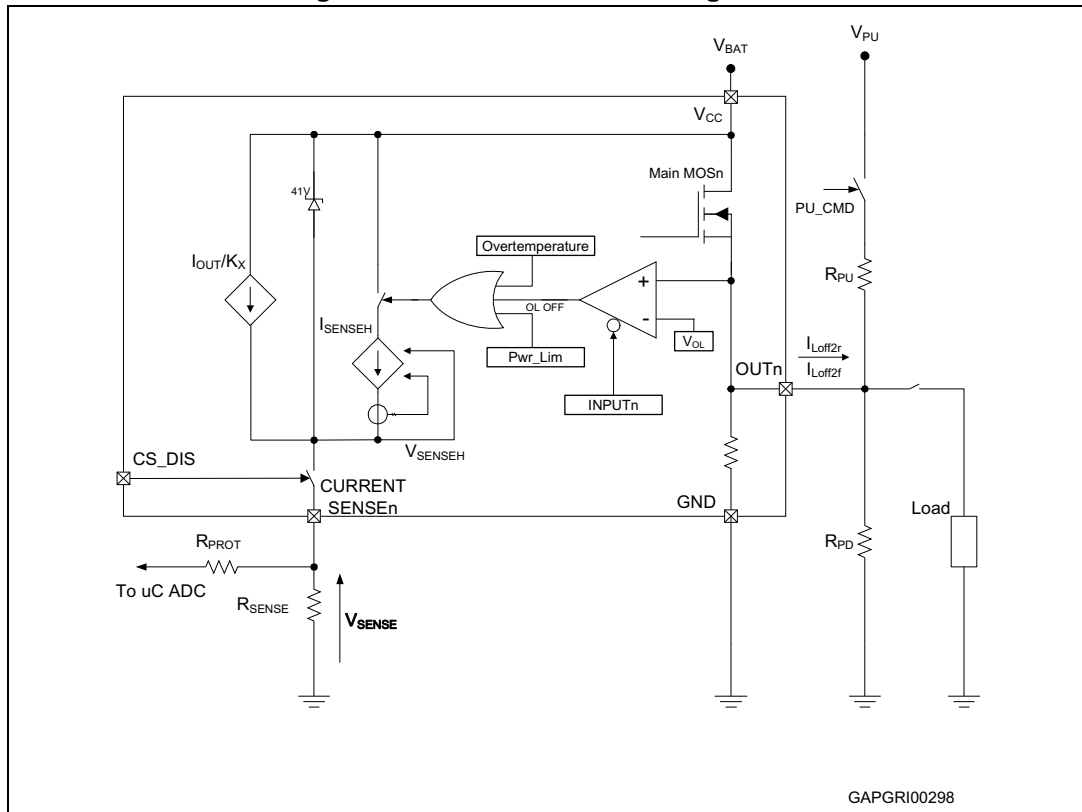
3.3 Current sense and diagnostic

The current sense pin performs a double function (see [Figure 33: Current sense and diagnostic](#)):

- **Current mirror of the load current in normal operation**, delivering a current proportional to the load one according to a known ratio K_x .
The current I_{SENSE} can be easily converted to a voltage V_{SENSE} by means of an external resistor R_{SENSE} . Linearity between I_{OUT} and V_{SENSE} is ensured up to 5 V minimum (see parameter V_{SENSE} in [Table 7: Current sense \(8V < \$V_{\text{CC}}\$ < 18V\)](#)). The current sense accuracy depends on the output current (refer to current sense electrical characteristics [Table 7: Current sense \(8V < \$V_{\text{CC}}\$ < 18V\)](#)).
- **Diagnostic flag in fault conditions**, delivering a fixed voltage V_{SENSEH} up to a maximum current I_{SENSEH} in case of the following fault conditions (refer to [Table 11: Truth table](#)):
 - Power limitation activation
 - Overtemperature
 - Short to V_{CC} in off-state
 - Open load in off-state with additional external components.

A logic level high on CS_DIS pin sets at the same time all the current sense pins of the device in a high-impedance state, thus disabling the current monitoring and diagnostic detection. This feature allows multiplexing of the microcontroller analog inputs by sharing of sense resistance and ADC line among different devices.

Figure 33. Current sense and diagnostic



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3.3.1 Short to V_{CC} and off-state open-load detection

Short to V_{CC}

A short-circuit between V_{CC} and output is indicated by the relevant current sense pin set to V_{SENSEH} during the device OFF-state. Small or no current is delivered by the current sense during the ON-state depending on the nature of the short-circuit.

Off-state open-load with external circuitry

Detection of an open load in off mode requires an external pull-up resistor R_{PU} connecting the output to a positive supply voltage V_{PU} .

It is preferable V_{PU} to be switched off during the module standby mode in order to avoid the overall standby current consumption to increase in normal conditions, i.e. when load is connected.

An external pull-down resistor R_{PD} connected between output and GND is mandatory to avoid misdetection in case of floating outputs in off-state (see [Figure 33: Current sense and diagnostic](#)).

R_{PD} must be selected in order to ensure $V_{OUT} < V_{OLmin}$ unless pulled-up by the external circuitry:

Equation 2

$$V_{\text{out}}|_{\text{Pull-up_off}} = R_{\text{PD}} \cdot I_{\text{L(off2)f}} < V_{\text{OLmin}} = 2\text{V}$$

$R_{\text{PD}} \leq 22 \text{ k}\Omega$ is recommended.

For proper open load detection in off-state, the external pull-up resistor must be selected according to the following formula:

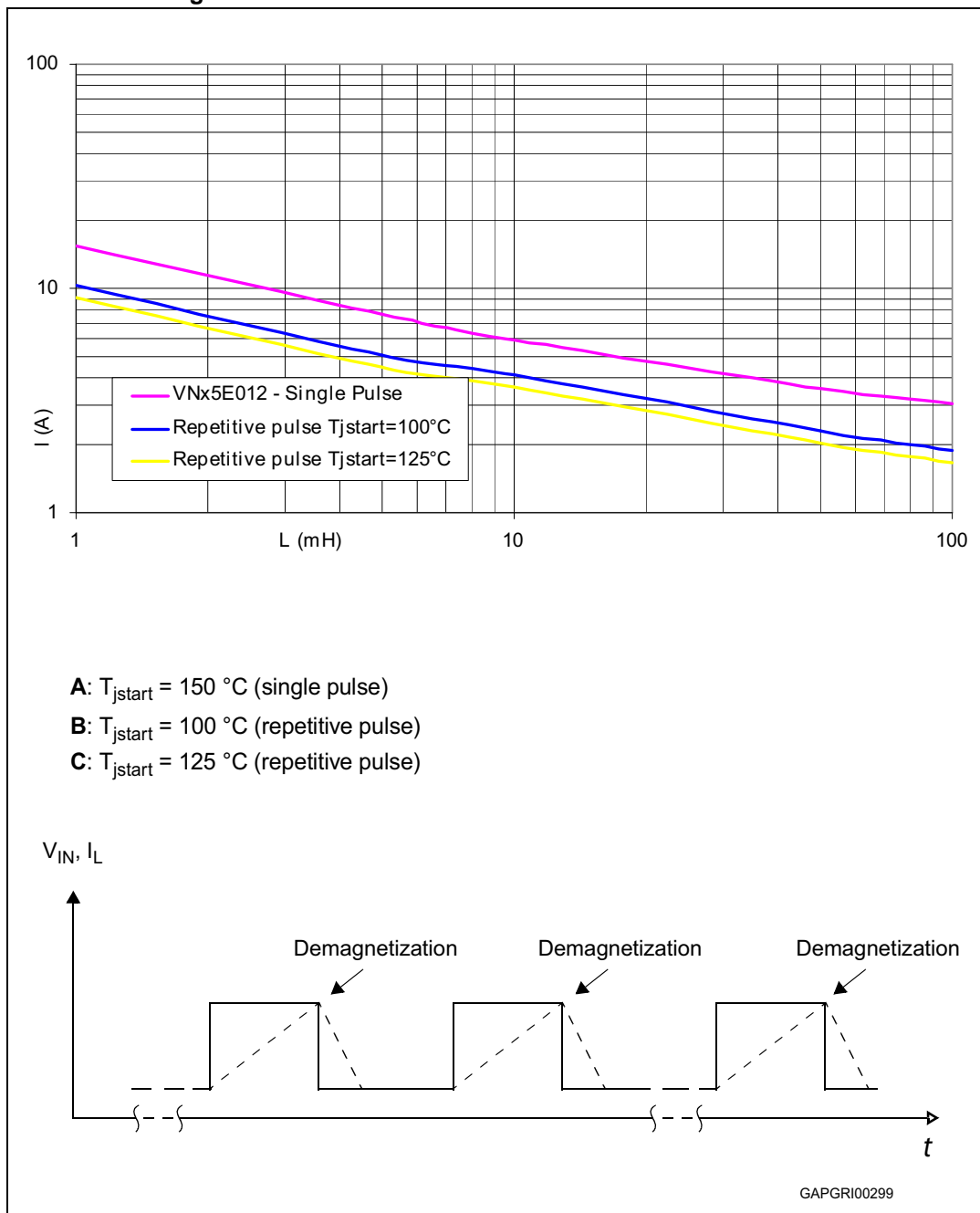
Equation 3

$$V_{\text{OUT}}|_{\text{Pull-up_ON}} = \frac{(R_{\text{PD}} \cdot V_{\text{PU}}) - (R_{\text{PU}} \cdot R_{\text{PD}} \cdot I_{\text{L(off2)r}})}{(R_{\text{PU}} + R_{\text{PD}})} > V_{\text{OLmax}} = 4\text{V}$$

For the values of V_{OLmin} , V_{OLmax} , $I_{\text{L(off2)r}}$ and $I_{\text{L(off2)f}}$ (see [Table 8: Open-load detection \(8V < V_{CC} < 18V\)](#)).

3.4 Maximum demagnetization energy ($V_{CC} = 13.5\text{ V}$)

Figure 34. Maximum turn-off current versus inductance⁽¹⁾



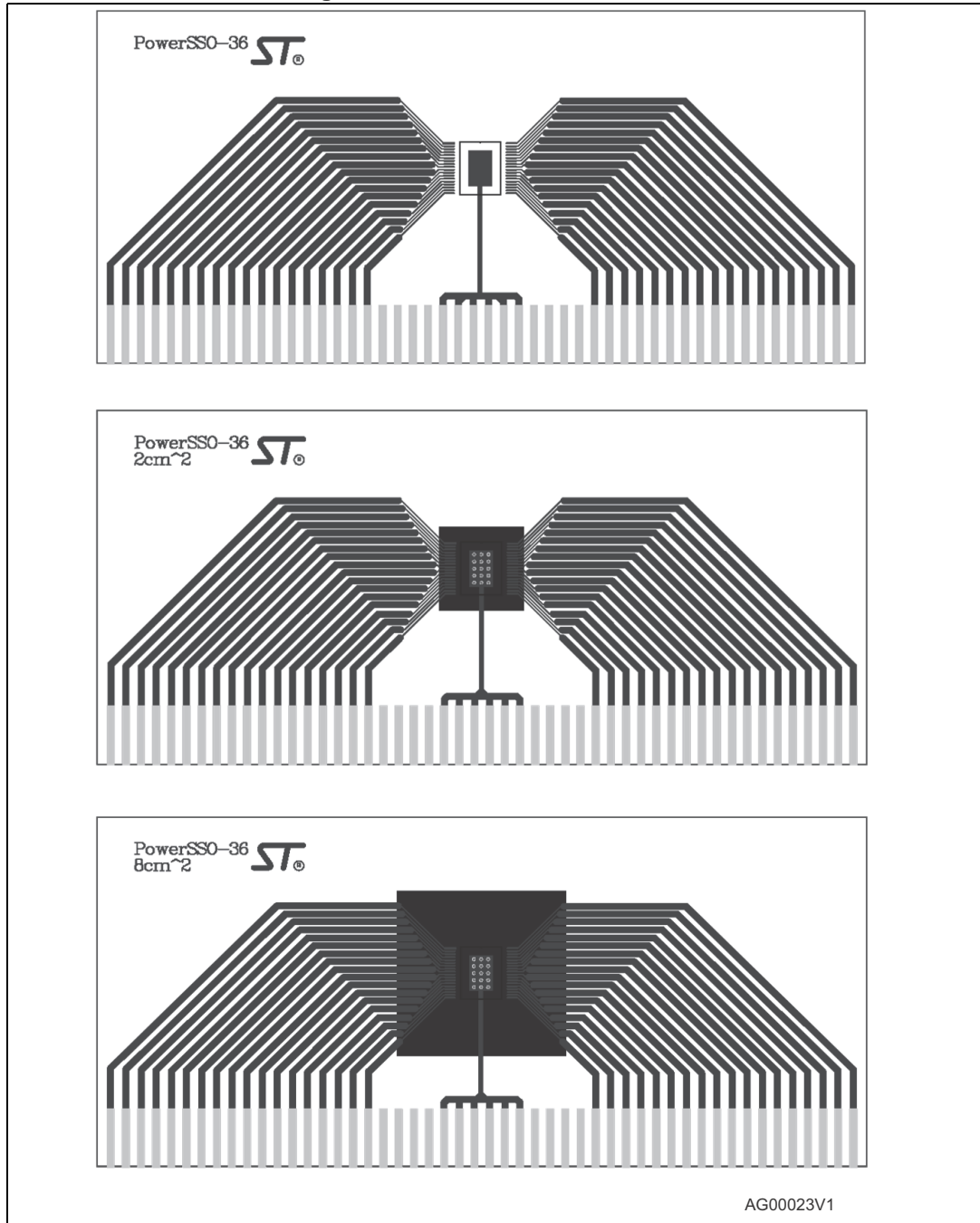
1. Values are generated with $R_L = 0\ \Omega$.

In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PCB thermal data

4.1 PowerSSO-36 thermal data

Figure 35. PowerSSO-36 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB: Double layer, Thermal Vias, FR4 area= 129mm x 60mm, PCB thickness=1.6mm, Cu thickness=70 μ m (front and back side), Copper areas: from minimum pad lay-out to 8cm²).

Figure 36. $R_{thj-amb}$ vs PCB copper area in open box free air condition (one channel ON)

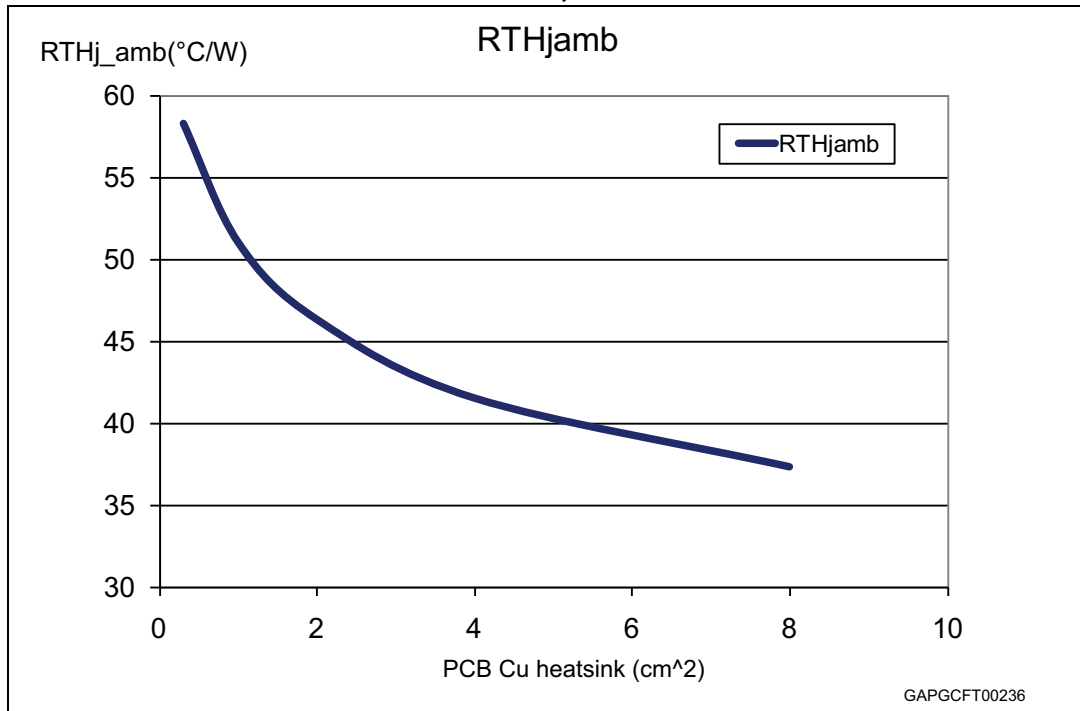


Figure 37. PowerSSO-36 Thermal impedance junction ambient single pulse (one channel ON)

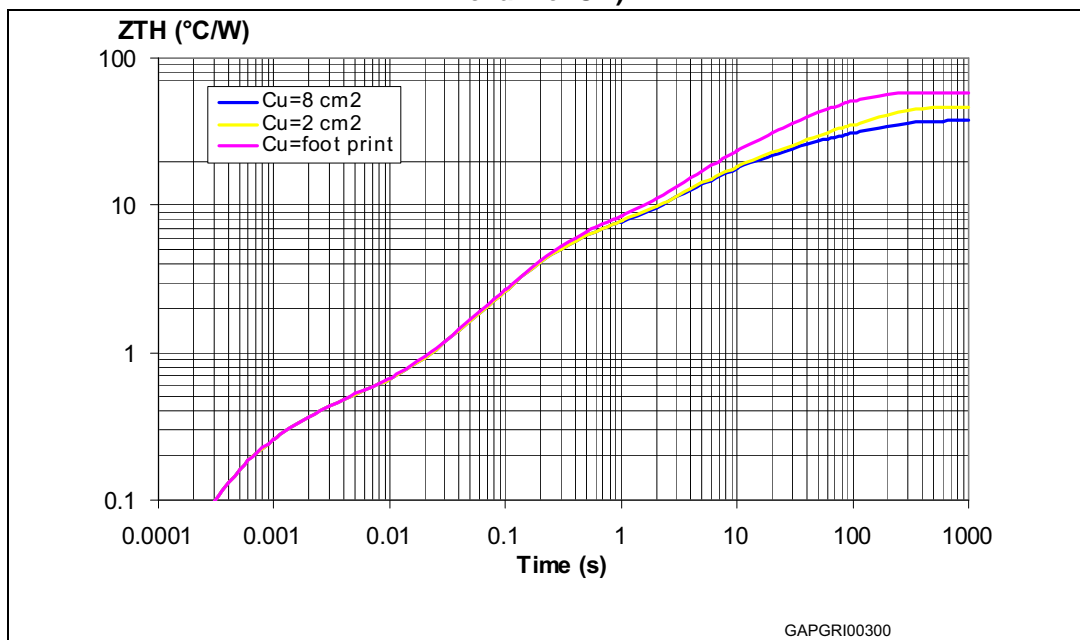
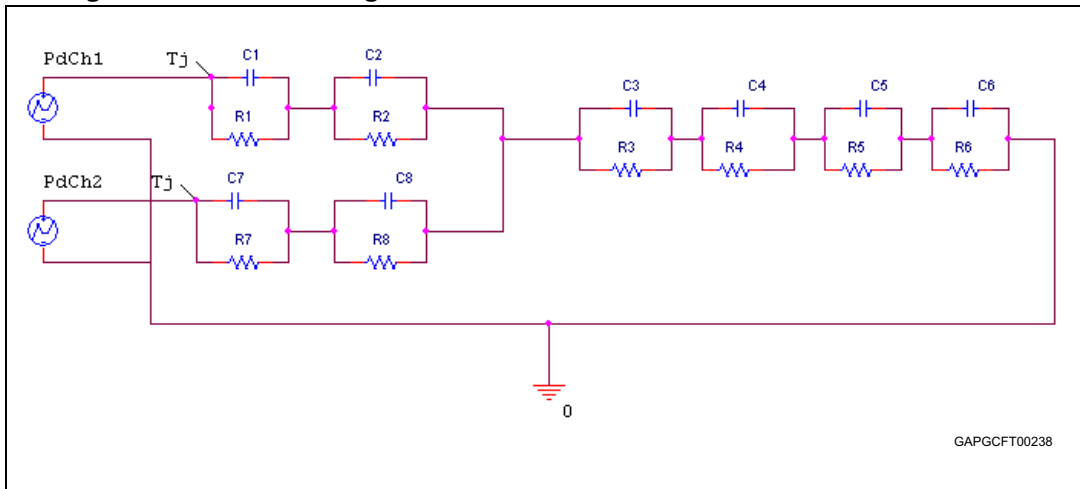


Figure 38. Thermal fitting model of a double channel HSD in PowerSSO-36⁽¹⁾



1. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered

Equation 4: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where:

Equation 5

$$\delta = t_p / T$$

Table 15. Thermal parameter

| Area/island (cm ²) | Footprint | 2 | 8 |
|--------------------------------|-----------|----|----|
| R1 (°C/W) | 0.1 | | |
| R2 (°C/W) | 0.3 | | |
| R3 (°C/W) | 5 | | |
| R4 (°C/W) | 8 | | |
| R5 (°C/W) | 18 | 10 | 10 |
| R6 (°C/W) | 27 | 23 | 14 |
| R7 (°C/W) | 0.1 | | |
| R8 (°C/W) | 0.3 | | |
| C1 (W.s/°C) | 0.0025 | | |
| C2 (W.s/°C) | 0.005 | | |
| C3 (W.s/°C) | 0.04 | | |
| C4 (W.s/°C) | 0.5 | | |
| C5 (W.s/°C) | 1 | 2 | 2 |
| C6 (W.s/°C) | 3 | 6 | 9 |

Table 15. Thermal parameter (continued)

| Area/island (cm ²) | Footprint | 2 | 8 |
|--------------------------------|-----------|---|---|
| C7 (W.s/°C) | 0.0025 | | |
| C8 (W.s/°C) | 0.005 | | |

5 Package information

5.1 ECOPACK[®] package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

5.2 PowerSSO-36 mechanical data

Figure 39. PowerSSO-36 package dimensions

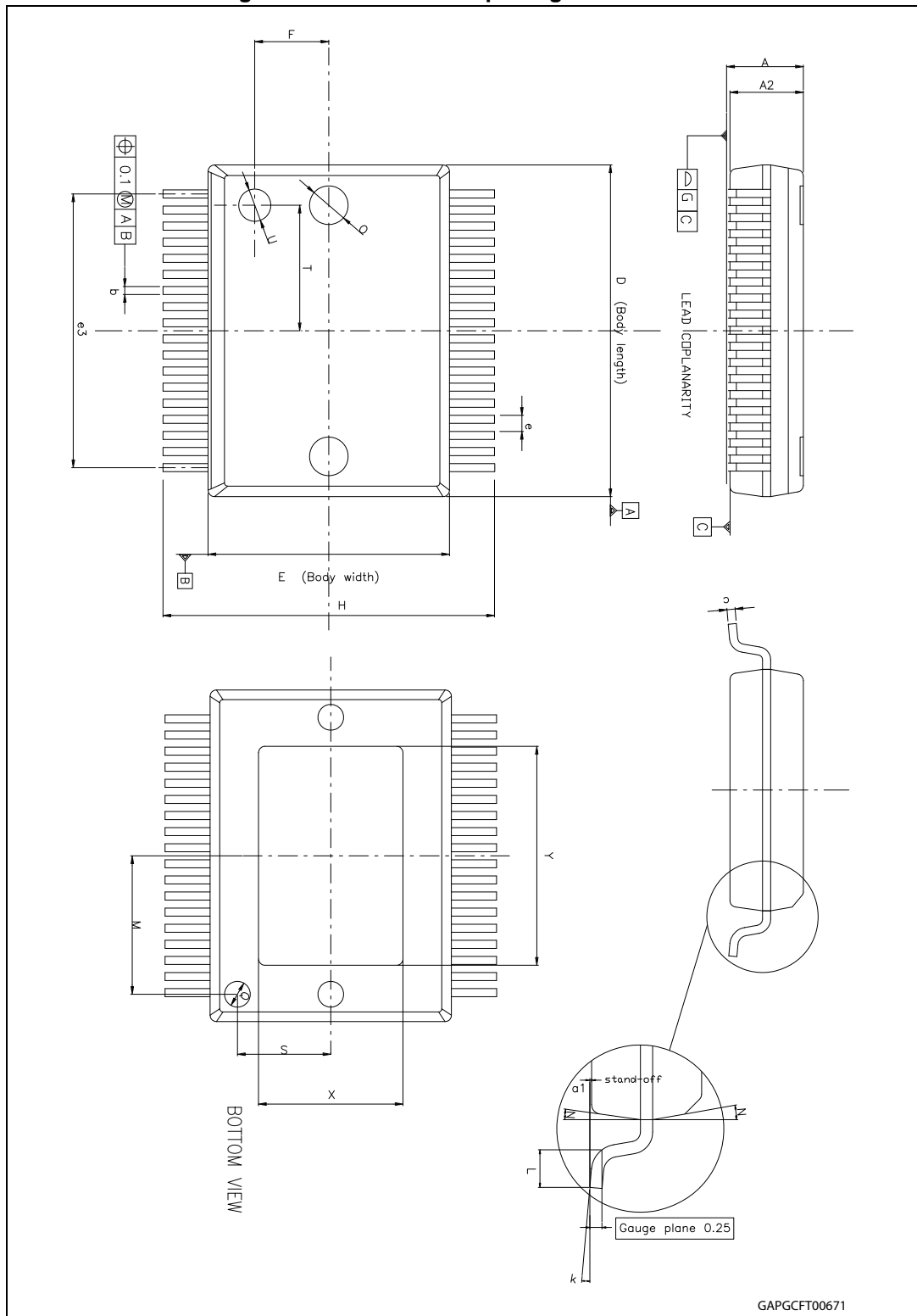


Table 16. PowerSSO-36 mechanical data

| Symbol | millimeters | | |
|--------|-------------|-----|--------|
| | Min | Typ | Max |
| A | 2.15 | - | 2.47 |
| A2 | 2.15 | - | 2.40 |
| a1 | 0 | - | 0.075 |
| b | 0.18 | - | 0.36 |
| c | 0.23 | - | 0.32 |
| D | 10.10 | - | 10.50 |
| E | 7.4 | - | 7.6 |
| e | - | 0.5 | - |
| e3 | - | 8.5 | - |
| G | - | - | 0.1 |
| G1 | - | - | 0.06 |
| H | 10.1 | - | 10.5 |
| h | - | - | 0.4 |
| L | 0.55 | - | 0.85 |
| N | - | - | 10 deg |
| X | 4.1 | - | 4.7 |
| Y | 6.5 | - | 7.1 |

5.3 Packing information

Figure 40. PowerSSO-36 tube shipment (no suffix)

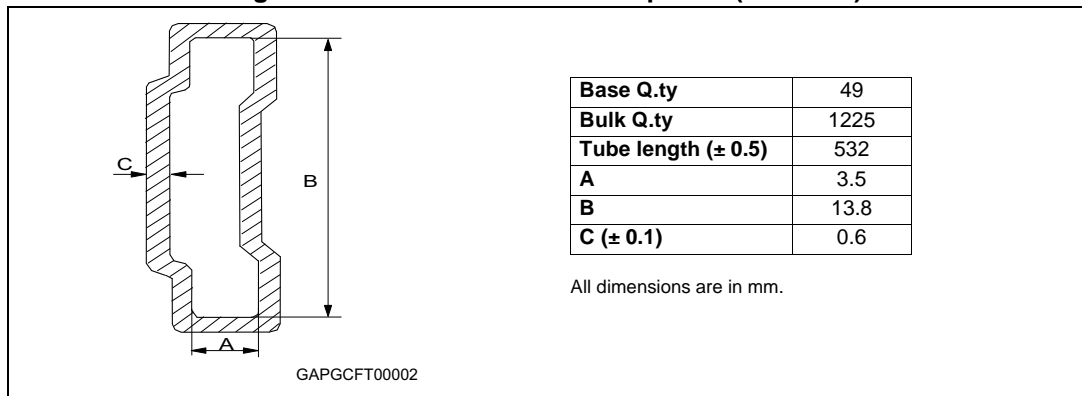
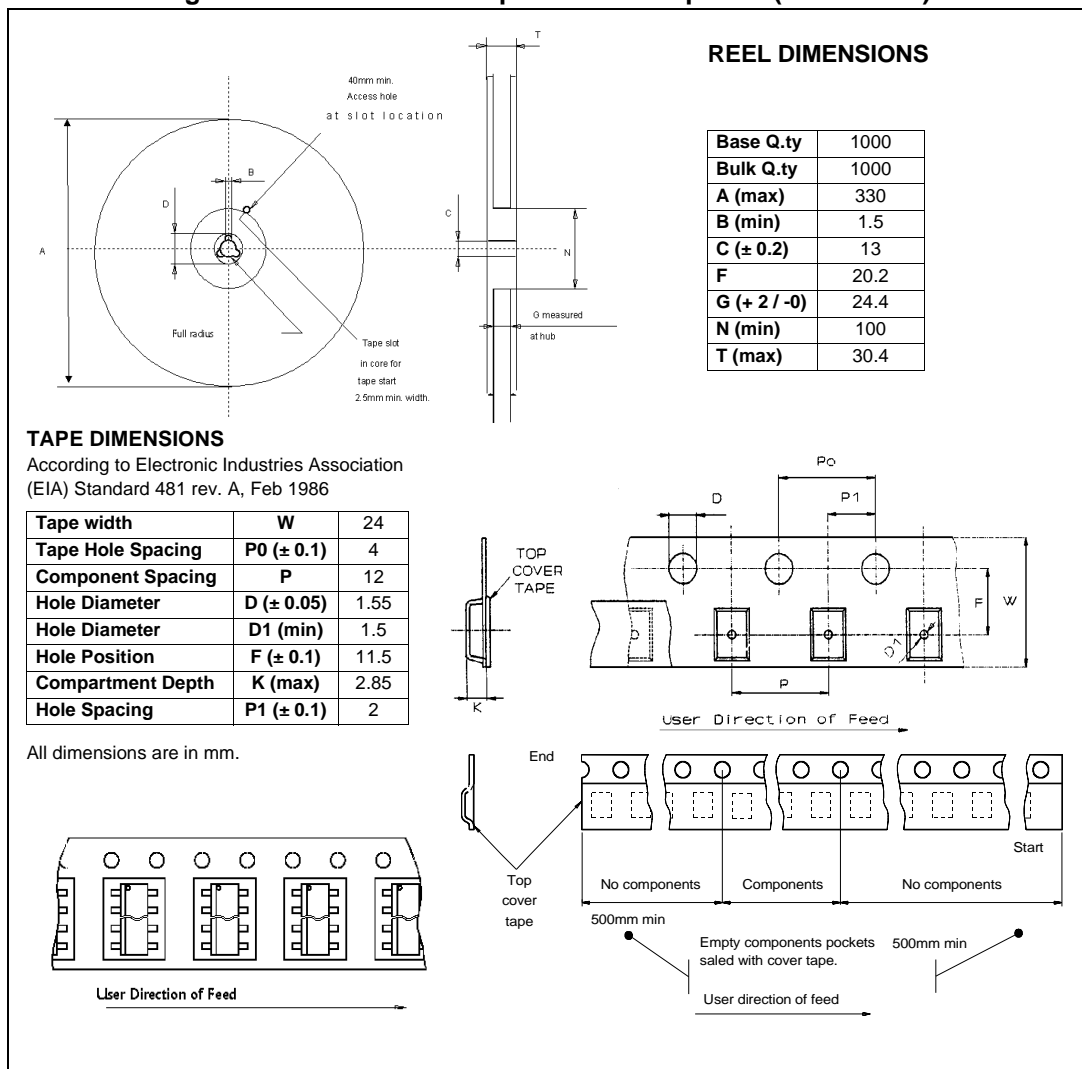


Figure 41. PowerSSO-36 tape and reel shipment (suffix "TR")



6 Order codes

Table 17. Device summary

| package | Order codes | |
|-------------|--------------|----------------|
| | Tube | Tape and reel |
| PowerSSO-36 | VND5E012AY-E | VND5E012AYTR-E |

7 Revision history

Table 18. Document revision history

| Date | Revision | Changes |
|--------------|----------|--|
| 05-Jun-2007 | 1 | Initial release. |
| 21-Oct-2009 | 2 | <p>Updated Figure 3: Current and voltage conventions.</p> <p>Updated following tables:</p> <ul style="list-style-type: none"> – Table 3: Absolute maximum ratings – Table 4: Thermal data – Table 5: Power section – Table 6: Switching (VCC = 13V; Tj = 25°C) – Table 7: Current sense (8V < VCC < 18V) – Table 8: Open-load detection (8V < VCC < 18V) <p>Added following figures:</p> <ul style="list-style-type: none"> – Figure 7: Maximum current sense ratio drift vs load current – Figure 8: Switching characteristics – Figure 9: Delay response time between rising edge of output current and rising edge of current sense (CS enabled) <p>Added Section 2.4: Waveforms and Section 2.5: Electrical characteristics curves.</p> <p>Updated Chapter 3: Application information.</p> <p>Updated Section 4.1: PowerSSO-36 thermal data:</p> <ul style="list-style-type: none"> – Added Figure 35: PowerSSO-36 PC board, Figure 36: Rthj-amb vs PCB copper area in open box free air condition (one channel ON) and Figure 37: PowerSSO-36 Thermal impedance junction ambient single pulse (one channel ON) – Updated Figure 38: Thermal fitting model of a double channel HSD in PowerSSO-36⁽¹⁾ – Added Table 15: Thermal parameter. <p>Updated Section 5.1: ECOPACK® package.</p> |
| 03-Dec-2009 | 3 | Updated Section 4.1: PowerSSO-36 thermal data |
| 09-July-2012 | 4 | Updated Figure 39: PowerSSO-36 package dimensions |
| 20-Sep-2013 | 5 | Updated Disclaimer |
| 28-Oct-2013 | 6 | Updated footnote 2 into the Table 12: Electrical transient requirements (part 1) and Table 13: Electrical transient requirements (part 2) . |

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