

## 2-Series, 3-Series, and 4-Series Li-Ion Battery Pack Manager

Check for Samples: [bq3050](#)

### FEATURES

- Fully Integrated 2-Series, 3-Series, and 4-Series Li-Ion or Li-Polymer Cell Battery Pack Manager and Protection
- Advanced Compensated End-of-Discharge Voltage (CEDV) Gauging
- High Side N-CH Protection FET Drive
- Integrated Pre-Charge FET
- Integrated Cell Balancing
- Low Power Modes
  - Low Power: < 180  $\mu$ A
  - Sleep < 76  $\mu$ A
- Full Array of Programmable Protection Features
  - Voltage
  - Current
  - Temperature
- Sophisticated Charge Algorithms
  - JEITA
  - Enhanced Charging
  - Adaptive Charging
- Supports Two-Wire SMBus v1.1 Interface
- SHA-1 Authentication
- Compact Package: 38-Lead TSSOP

### APPLICATIONS

- Notebook/Netbook PCs
- Medical and Test Equipment
- Portable Instrumentation

### DESCRIPTION

The bq3050 device is a fully integrated, single-chip, pack-based solution that provides a rich array of features for gas gauging, protection, and authentication for 2-series, 3-series, and 4-series cell Li-Ion and Li-Polymer battery packs.

Using its integrated high-performance analog peripherals, the bq3050 device measures and maintains an accurate record of available capacity, voltage, current, temperature, and other critical parameters in Li-Ion or Li-Polymer batteries, and reports this information to the system host controller over an SMBus v1.1 compatible interface.

The bq3050 provides software-based 1st-level and 2nd-level safety protection for overvoltage, undervoltage, overtemperature, and overcharge conditions, as well as hardware-based protection for overcurrent in discharge and short circuit in charge and discharge conditions.

SHA-1 authentication with secure memory for authentication keys enables identification of genuine battery packs beyond any doubt.

The compact 38-lead TSSOP package minimizes solution cost and size for smart batteries while providing maximum functionality and safety for battery gauging applications.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### ORDERING INFORMATION

T <sub>A</sub>	PART NUMBER	PACKAGE	PACKAGE DESIGNATOR	PACKAGE MARKING	ORDERING INFORMATION <sup>(1)</sup>	
					TUBE <sup>(2)</sup>	TAPE AND REEL <sup>(3)</sup>
–40°C to 85°C	bq3050	TSSOP-38	DBT	bq3050	bq3050DBT	bq3050DBTR

(1) For the most current package and ordering information, see the Package Option Addendum at the end of the document, or see the TI website at [www.ti.com](http://www.ti.com).

(2) A single tube quantity is 50 units.

(3) A single reel quantity is 2000 units.

### THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		bq3050	UNITS
		TSSOP	
		38 PINS	
$\theta_{JA, \text{High K}}$	Junction-to-ambient thermal resistance <sup>(2)</sup>	64.2	°C/W
$\theta_{JC(\text{top})}$	Junction-to-case(top) thermal resistance <sup>(3)</sup>	16.5	
$\theta_{JB}$	Junction-to-board thermal resistance <sup>(4)</sup>	31.2	
$\psi_{JT}$	Junction-to-top characterization parameter <sup>(5)</sup>	0.3	
$\psi_{JB}$	Junction-to-board characterization parameter <sup>(6)</sup>	26.9	
$\theta_{JC(\text{bottom})}$	Junction-to-case(bottom) thermal resistance <sup>(7)</sup>	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](http://www.ti.com/lit/zip/spra953).

(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

(5) The junction-to-top characterization parameter,  $\psi_{JT}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).

(6) The junction-to-board characterization parameter,  $\psi_{JB}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).

(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

TYPICAL IMPLEMENTATION

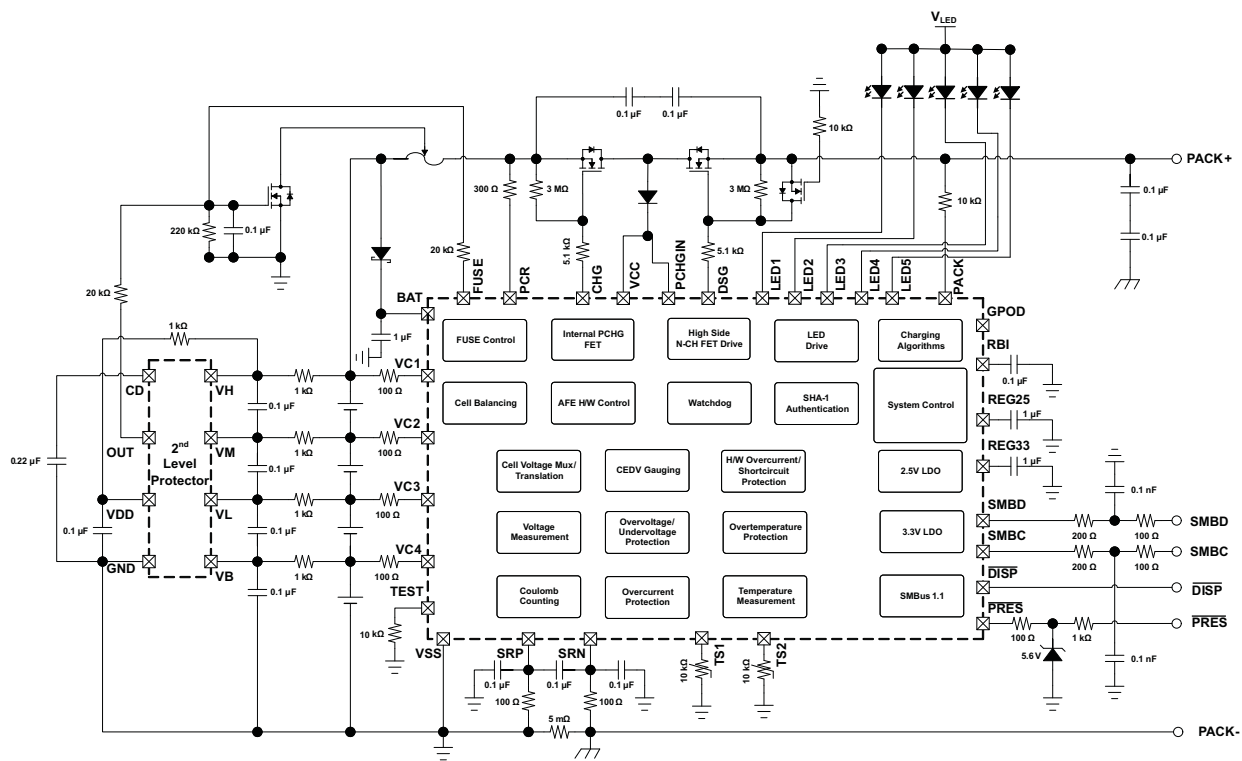
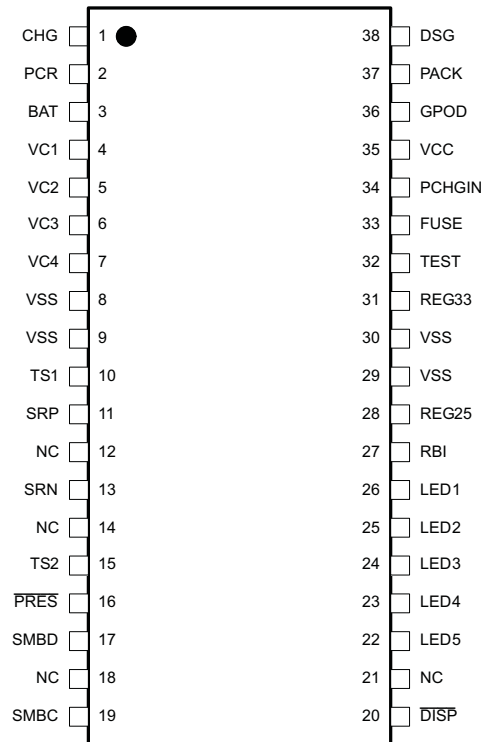


Figure 1. bq3050 Implementation

**Pin-Out Diagram**



**Figure 2. bq3050 Pin-Out Diagram**

**PIN FUNCTIONS**

PIN NAME	PIN NUMBER	TYPE <sup>(1)</sup>	DESCRIPTION
<b>bq3050-DBT</b>			
CHG	1	O	Charge N-FET gate drive
PCR	2	O	Internal Pre-Charge FET output
BAT	3	P	Alternate power source
VC1	4	I	Sense input for positive voltage of top most cell in stack and cell balancing input for top most cell in stack
VC2	5	I	Sense input for positive voltage of third lowest cell in stack and cell balancing input for third lowest cell in stack
VC3	6	I	Sense input for positive voltage of second lowest cell in stack and cell balancing input for second lowest cell in stack
VC4	7	I	Sense input for positive voltage of lowest cell in stack and cell balancing input for lowest cell in stack
VSS	8	P	Device ground
VSS	9	P	Device ground
TS1	10	AI	Temperature sensor 1 thermistor input
SRP	11	AI	Differential Coulomb Counter input
NC	12	—	Not internally connected, connect to VSS
SRN	13	AI	Differential Coulomb Counter input
NC	14	—	Not internally connected, connect to VSS
TS2	15	AI	Temperature sensor 2 thermistor input
PRES	16	I	Host system present input
SMBD	17	I/OD	SMBus v1.1 data line

(1) P = Power Connection, O = Digital Output, AI = Analog Input, I = Digital Input, I/OD = Digital Input/Output

**PIN FUNCTIONS (continued)**

PIN NAME	PIN NUMBER	TYPE <sup>(1)</sup>	DESCRIPTION
	<b>bq3050-DBT</b>		
NC	18	—	Not internally connected, connect to VSS
SMBC	19	I/OD	SMBus v1.1 clock line
DISP	20	I	Display active input
NC	21	—	Not internally connected, connect to VSS
LED5	22	O	LED display constant current sink
LED4	23	O	LED display constant current sink
LED3	24	O	LED display constant current sink
LED2	25	O	LED display constant current sink
LED1	26	O	LED display constant current sink
RBI	27	P	RAM backup
REG25	28	P	2.5-V regulator output
VSS	29	P	Device ground
VSS	30	P	Device ground
REG33	31	P	3.3-V regulator output
TEST	32	—	Test pin, connect to VSS through 10-kΩ resistor
FUSE	33	O	Fuse drive
PCHGIN	34	I	Internal Pre-Charge FET input
VCC	35	P	Power supply voltage
GPOD	36	I/OD	High voltage general purpose I/O
PACK	37	P	Alternate power source
DSG	38	O	Discharge N-FET gate drive

## ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

DESCRIPTION	PINS	VALUE
Supply voltage range, $V_{MAX}$	VCC, PCHGIN, PCR, TEST, PACK w.r.t. Vss	-0.3 V to 34 V
Input voltage range, $V_{IN}$	VC1, BAT	$V_{VC2} - 0.3$ V to $V_{VC2} + 8.5$ V or 34 V, whichever is lower
	VC2	$V_{VC3} - 0.3$ V to $V_{VC3} + 8.5$ V
	VC3	$V_{VC4} - 0.3$ V to $V_{VC4} + 8.5$ V
	VC4	$V_{SRP} - 0.3$ V to $V_{SRP} + 8.5$ V
	SRP, SRN	-0.3 V to 0.3 V
	LED1, LED2, LED3, LED4, LED5, SMBC, SMBD	$V_{SS} - 0.3$ V to 6.0 V
	$\overline{DISP}$ , TS1, TS2, $\overline{PRES}$	-0.3 V to $V_{REG25} + 0.3$ V
Output voltage range, $V_O$	DSG	-0.3 V to $V_{PACK} + 20$ V or $V_{SS} + 34$ V, whichever is lower
	CHG	-0.3 V to $V_{BAT} + 20$ V or $V_{SS} + 34$ V, whichever is lower
	GPOD, FUSE	-0.3 V to 34 V
	RBI, REG25	-0.3 V to 2.75 V
	REG33	-0.3 V to 5.0 V
Maximum VSS current, $I_{SS}$		50 mA
Current for cell balancing, $I_{CB}$		10 mA
ESD Rating	HBM, VCx Only	1 kV
Functional Temperature, $T_{FUNC}$		-40 to 110°C
Storage temperature range, $T_{STG}$		-65 to 150°C
Lead temperature (soldering, 10 s), $T_{SOLDER}$		300°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4$  V, Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 3.8$  V to 25 V (unless otherwise noted)

		MIN	TYP	MAX	UNIT
Supply voltage	VCC, PACK, PCHGIN, PCR			25	V
	BAT	3.8		$V_{VC2} + 5.0$	
$V_{STARTUP}$	Start up voltage at PACK	3.0		5.5	V
$V_{IN}$ Input voltage range	VC1, BAT	$V_{VC2}$		$V_{VC2} + 5.0$	V
	VC2	$V_{VC3}$		$V_{VC3} + 5.0$	
	VC3	$V_{VC4}$		$V_{VC4} + 5.0$	
	VC4	$V_{SRP}$		$V_{SRP} + 5.0$	
	$VC_n - VC_{(n+1)}$ , (n=1, 2, 3, 4)	0		5.0	
	PACK			25	
	SRP to SRN	-0.2		0.2	V
$C_{REG33}$	External 3.3V REG capacitor	1			$\mu\text{F}$
$C_{REG25}$	External 2.5V REG capacitor	1			$\mu\text{F}$
$T_{OPR}$	Operating temperature	-40		85	°C

### ELECTRICAL CHARACTERISTICS: Supply Current

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 3.8\text{ V}$  to  $25\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CC}$	Normal	CHG on, DSG on, no Flash write		410		$\mu\text{A}$
	Sleep	CHG on, DSG on, no SBS communication		160		$\mu\text{A}$
		CHG off, DSG off, no SBS communication		80		$\mu\text{A}$
	Shutdown				1	$\mu\text{A}$

### ELECTRICAL CHARACTERISTICS: Power On Reset (POR)

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 3.8\text{ V}$  to  $25\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT-}$	Negative-going voltage input	At REG25	1.9	2.0	2.1	V
$V_{HYS}$	POR Hysteresis	At REG25	65	125	165	mV

### ELECTRICAL CHARACTERISTICS: WAKE FROM SLEEP

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 3.8\text{ V}$  to  $25\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{WAKE}$	$V_{WAKE}$ Threshold	$V_{WAKE} = 1.2\text{ mV}$	0.2	1.2	2.0	mV
		$V_{WAKE} = 2.4\text{ mV}$	0.4	2.4	3.6	
		$V_{WAKE} = 5\text{ mV}$	2.0	5.0	6.8	
		$V_{WAKE} = 10\text{ mV}$	5.3	10	13	
$V_{WAKE\_TCO}$	Temperature drift of $V_{WAKE}$ accuracy			0.5		$\%/\text{C}$
$t_{WAKE}$	Time from application of current and wake of bq3050			0.2	1	ms

### ELECTRICAL CHARACTERISTICS: RBI RAM Backup

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 3.8\text{ V}$  to  $25\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(RBI)}$	RBI data-retention input current	$VRBI > V_{(RBI)MIN}$ , $V_{CC} < V_{IT}$		20	1100	nA
		$VRBI > V_{(RBI)MIN}$ , $V_{CC} < V_{IT}$ , $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$			500	
$V_{(RBI)}$	RBI data-retention voltage		1			V

### ELECTRICAL CHARACTERISTICS: 3.3V Regulator

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 3.8\text{ V}$  to  $25\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{REG33}$	Regulator output voltage	$3.8\text{ V} < V_{CC}$ or $BAT \leq 5\text{ V}$ , $I_{CC} \leq 4\text{ mA}$	2.4		3.5	V
		$5\text{ V} < V_{CC}$ or $BAT \leq 6.8\text{ V}$ , $I_{CC} \leq 13\text{ mA}$	3.1	3.3	3.5	V
		$6.8\text{ V} < V_{CC}$ or $BAT \leq 20\text{ V}$ , $I_{CC} \leq 30\text{ mA}$	3.1	3.3	3.5	V
$I_{REG33}$	Regulator output current		2			mA
$\Delta V_{(VDDTEMP)}$	Regulator output change with temperature	$V_{CC}$ or $BAT = 14.4\text{ V}$ , $I_{REG33} = 2\text{ mA}$		0.2		%

### ELECTRICAL CHARACTERISTICS: 3.3V Regulator (continued)

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 3.8\text{ V}$  to  $25\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\Delta V_{(VDDLIN)}$	Line regulation	$V_{CC}$ or $BAT = 14.4\text{ V}$ , $I_{REG33} = 2\text{ mA}$		1	13	mV
$\Delta V_{(VDDLLOAD)}$	Load regulation	$V_{CC}$ or $BAT = 14.4\text{ V}$ , $I_{REG33} = 2\text{ mA}$		5	18	mV
$I_{(REG33MAX)}$	Current limit	$V_{CC}$ or $BAT = 14.4\text{ V}$ , $V_{REG33} = 3\text{ V}$			70	mA
		$V_{CC}$ or $BAT = 14.4\text{ V}$ , $V_{REG33} = 0\text{ V}$			33	

### ELECTRICAL CHARACTERISTICS: 2.5V Regulator

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 3.8\text{ V}$  to  $25\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{REG25}$	Regulator output voltage	$I_{REG25} = 10\text{ mA}$	2.35	2.5	2.55	V
$I_{REG25}$	Regulator Output Current		3			mA
$\Delta V_{(VDDTEMP)}$	Regulator output change with temperature	$V_{CC}$ or $BAT = 14.4\text{ V}$ , $I_{REG25} = 2\text{ mA}$		0.25		%
$\Delta V_{(VDDLIN)}$	Line regulation	$V_{CC}$ or $BAT = 14.4\text{ V}$ , $I_{REG25} = 2\text{ mA}$		1	4	mV
$\Delta V_{(VDDLLOAD)}$	Load regulation	$V_{CC}$ or $BAT = 14.4\text{ V}$ , $I_{REG25} = 2\text{ mA}$		20	40	mV
$I_{(REG33MAX)}$	Current limit	$V_{CC}$ or $BAT = 14.4\text{ V}$ , $V_{REG25} = 2.3\text{ V}$			65	mA
		$V_{CC}$ or $BAT = 14.4\text{ V}$ , $V_{REG25} = 0\text{ V}$			23	

### ELECTRICAL CHARACTERISTICS: $\overline{DISP}$ , $\overline{PRES}$ , $\overline{SMBD}$ , $\overline{SMBC}$

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 3.8\text{ V}$  to  $25\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IH}$	High-level input	$\overline{DISP}$ , $\overline{PRES}$ , $\overline{SMBD}$ , $\overline{SMBC}$	2.0			V
$V_{IL}$	Low-level input	$\overline{DISP}$ , $\overline{PRES}$ , $\overline{SMBD}$ , $\overline{SMBC}$			0.8	V
$V_{OL}$	Low-level output voltage	$\overline{SMBD}$ , $\overline{SMBC}$			0.4	V
$C_{IN}$	Input capacitance	$\overline{DISP}$ , $\overline{PRES}$ , $\overline{SMBD}$ , $\overline{SMBC}$		5		pF
$I_{LKG}$	Input leakage current	$\overline{DISP}$ , $\overline{PRES}$ , $\overline{SMBD}$ , $\overline{SMBC}$			1	$\mu\text{A}$
$I_{WPU}$	Weak Pull Up Current	$\overline{PRES}$ , $V_{OH} = V_{REG25} - 0.5\text{ V}$ ,	60		120	$\mu\text{A}$
$I_{(\overline{DISP})}$	$\overline{DISP}$ source currents	$\overline{DISP}$ active, $\overline{DISP} = V_{REG25} - 0.6\text{ V}$	-3			mA
$I_{LKG(\overline{DISP})}$	$\overline{DISP}$ leakage current	$\overline{DISP}$ inactive	-0.22		0.22	$\mu\text{A}$
$R_{PD(\overline{SMBx})}$	$\overline{SMBC}$ , $\overline{SMBD}$ Pull-Down	$T_A = -40$ to $100^\circ\text{C}$	550	775	1000	k $\Omega$

### ELECTRICAL CHARACTERISTICS: CHG, DSG FET Drive

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 3.8\text{ V}$  to  $25\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(FETON)}$	Output voltage, charge, and discharge FETs on	$V_{O(FETONDSG)} = V_{(DSG)} - V_{PACK}$ , $V_{GS}$ connect $10\text{ M}\Omega$ , $V_{CC} 3.8\text{ V}$ to $8.4\text{ V}$	8.0	9.7	12	V
		$V_{O(FETONDSG)} = V_{(DSG)} - V_{PACK}$ , $V_{GS}$ connect $10\text{ M}\Omega$ , $V_{CC} > 8.4\text{ V}$	9.0	11	12	V
		$V_{O(FETONCHG)} = V_{(CHG)} - V_{BAT}$ , $V_{GS}$ connect $10\text{ M}\Omega$ , $V_{CC} 3.8\text{ V}$ to $8.4\text{ V}$	8.0	9.7	12	V
		$V_{O(FETONCHG)} = V_{(CHG)} - V_{BAT}$ , $V_{GS}$ connect $10\text{ M}\Omega$ , $V_{CC} > 8.4\text{ V}$	9.0	11	12	V
$V_{(FETOFF)}$	Output voltage, charge and discharge FETs off	$V_{O(FETOFFDSG)} = V_{(DSG)} - V_{PACK}$	-0.4		0.4	V
		$V_{O(FETOFFCHG)} = V_{(CHG)} - V_{BAT}$	-0.4		0.4	V



### ELECTRICAL CHARACTERISTICS: CHG, DSG FET Drive (continued)

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 3.8\text{ V}$  to  $25\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_r$	Rise time	$C_L = 4700\text{ pF}$ $R_G = 5.1\text{ k}\Omega$ $V_{CC} < 8.4$ $V_{DSG}: V_{BAT}$ to $V_{BAT} + 4\text{ V}$ $V_{CHG}: V_{PACK}$ to $V_{PACK} + 4\text{ V}$		800	1400	$\mu\text{s}$
		$C_L = 4700\text{ pF}$ $R_G = 5.1\text{ k}\Omega$ $V_{CC} > 8.4$ $V_{DSG}: V_{BAT}$ to $V_{BAT} + 4\text{ V}$ $V_{CHG}: V_{PACK}$ to $V_{PACK} + 4\text{ V}$		200	500	$\mu\text{s}$
$t_f$	Fall time	$C_L = 4700\text{ pF}$ $R_G = 5.1\text{ k}\Omega$ $V_{DSG}: V_{BAT} + V_{O(FETONDSG)}$ to $V_{BAT} + 1\text{ V}$ $V_{CHG}: V_{PACK} + V_{O(FETONCHG)}$ to $V_{PACK} + 1\text{ V}$		80	200	$\mu\text{s}$

### ELECTRICAL CHARACTERISTICS: INTERNAL PRE-CHARGE LIMITING

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 3.8\text{ V}$  to  $25\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{PCHGMAX}$	Maximum Pre-charge current	3-cell and 4-cell configuration			100	mA
$R_{PCHG\_RDS\ ON}$	Internal Pre-charge FET $R_{DS(ON)}$	$V_{DS(PRECHG)} \geq 1\text{ V}$ , $V_{CC} < 8.4\text{ V}$	30	55	85	$\Omega$
		$V_{DS(PRECHG)} \geq 1\text{ V}$ , $V_{CC} \geq 8.4\text{ V}$	15	30	55	$\Omega$

### ELECTRICAL CHARACTERISTICS: GPOD

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 3.8\text{ V}$  to  $25\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{PU\_GPOD}$	GPOD Pull-Up Voltage				$V_{CC}$	V
$V_{OL\_GPOD}$	GPOD Output Voltage Low	$I_{OL} = 1\text{ mA}$	0.3			V

### ELECTRICAL CHARACTERISTICS: FUSE

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 3.8\text{ V}$  to  $25\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH(FUSE)}$	High Level FUSE Output	$V_{CC} = 3.8\text{ V}$ to $9\text{ V}$	2.4		8.5	V
		$V_{CC} = 9\text{ V}$ to $25\text{ V}$	7	8	9	V
$V_{IH(FUSE)}$	Weak pull-up current in off state <sup>(1)</sup>		2.8			V
				100		nA
$t_{R(FUSE)}$	FUSE Output Rise Time	$C_L = 1\text{ nF}$ , $V_{CC} = 9\text{ V}$ to $25\text{ V}$ , $V_{OH(FUSE)} = 0\text{ V}$ to $5\text{ V}$		5	20	$\mu\text{s}$
$Z_{O(FUSE)}$	FUSE Output Impedance			2	5	k $\Omega$

(1) Verified by design. Not production tested.

### ELECTRICAL CHARACTERISTICS: LED5, LED4, LED3, LED2, LED1

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 3.8\text{ V}$  to  $25\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{IN}$	Input capacitance			5		pF
$I_{LKG}$	Input leakage current				1	$\mu\text{A}$
$I_{OL}$	Low-level output current	$V_{OL} = 0.4\text{ V}$ , 3 mA setting	2.5	3.5	4.5	mA
		$V_{OL} = 0.4\text{ V}$ , 4 mA setting	3.0	4.5	6.0	mA
		$V_{OL} = 0.4\text{ V}$ , 5 mA setting	3.5	5.5	7.5	mA
$I_{LEDx}$	Current matching between LEDx		0.1			mA

### ELECTRICAL CHARACTERISTICS: COULOMB COUNTER

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 3.8\text{ V}$  to  $25\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN}$	Input voltage range	SRP – SRN	-0.20		0.25	V
	Conversion time	Single conversion		250		ms
	Resolution (no missing codes)		16			Bits
	Effective resolution	Single conversion, signed	15			Bits
	Offset error	Post calibrated		10		$\mu\text{V}$
	Offset error drift			0.3	0.5	$\mu\text{V}/^\circ\text{C}$
	Full-scale error		-0.8%	0.2%	0.8%	
	Full-scale error drift				150	PPM/ $^\circ\text{C}$
	Effective input resistance		2.5			m $\Omega$

### ELECTRICAL CHARACTERISTICS: VC1, VC2, VC3, VC4

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 3.8\text{ V}$  to  $25\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN}$	Input voltage range	$VC4 - VC3$ , $VC3 - VC2$ , $VC2 - VC1$ , $VC1 - V_{SS}$	-0.20		8	V
	Conversion time	Single conversion		32		ms
	Resolution (no missing codes)		16			Bits
	Effective resolution	Single conversion, signed	15			Bits
$R_{(BAL)}$	$R_{DS(ON)}$ for internal FET at $V_{DS} > 2\text{ V}$	$V_{DS} = VC4 - VC3$ , $VC3 - VC2$ , $VC2 - VC1$ , $VC1 - V_{SS}$	200	310	430	$\Omega$
	$R_{DS(ON)}$ for internal FET at $V_{DS} > 4\text{ V}$	$V_{DS} = VC4 - VC3$ , $VC3 - VC2$ , $VC2 - VC1$ , $VC1 - V_{SS}$	60	125	230	$\Omega$

### ELECTRICAL CHARACTERISTICS: TS1, TS2

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 3.8\text{ V}$  to  $25\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R	Internal Pull Up Resistor		16.5	17.5	19.0	K $\Omega$
$R_{DRIFT}$	Internal Pull Up Resistor Drift From $25^\circ\text{C}$				200	PPM/ $^\circ\text{C}$
$R_{PAD}$	Internal Pin Pad resistance			84		$\Omega$

### ELECTRICAL CHARACTERISTICS: TS1, TS2 (continued)

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 3.8\text{ V}$  to  $25\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN}$	Input voltage range	TS1 – VSS, TS2 – VSS	-0.20		$0.8 \times V_{REG25}$	V
	Conversion Time			16		ms
	Resolution (no missing codes)		16			Bits
	Effective resolution		11	12		Bits

### ELECTRICAL CHARACTERISTICS: Internal Temperature Sensor

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 3.8\text{ V}$  to  $25\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(TEMP)}$	Temperature sensor voltage		-1.9	-2.0	-2.1	mV/ $^\circ\text{C}$
	Conversion Time			16		ms
	Resolution (no missing codes)		16			Bits
	Effective resolution		11	12		Bits

### ELECTRICAL CHARACTERISTICS: Internal Thermal Shutdown

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 3.8\text{ V}$  to  $25\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{MAX1}$	Maximum PCHG temperature		110		150	$^\circ\text{C}$
$T_{MAX2}$	Maximum REG33 temperature		125		175	
$T_{RECOVER}$	Recovery hysteresis temperature			10		$^\circ\text{C}$
$t_{PROTECT}$	Protection time			5		$\mu\text{s}$

### ELECTRICAL CHARACTERISTICS: High Frequency Oscillator

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 3.8\text{ V}$  to  $25\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(OSC)}$	Operating frequency of CPU Clock			4.194		MHz
$f_{(EIO)}$	Frequency error <sup>(1)(2)</sup>	$T_A = -20^\circ\text{C}$ to $70^\circ\text{C}$	-2%	$\pm 0.25\%$	2%	
		$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$	-3%	$\pm 0.25\%$	3%	
$t_{(SXO)}$	Start-up time <sup>(3)</sup>	$T_A = -25^\circ\text{C}$ to $85^\circ\text{C}$		3	6	ms

(1) The frequency error is measured from 4.194 MHz.

(2) The frequency drift is included and measured from the trimmed frequency at  $V_{REG25} = 2.5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

(3) The startup time is defined as the time it takes for the oscillator output frequency to be  $\pm 3\%$  when the device is already powered.

### ELECTRICAL CHARACTERISTICS: Low Frequency Oscillator

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 3.8\text{ V}$  to  $25\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(LOSC)}$	Operating frequency			32.768		kHz
$f_{(LEIO)}$	Frequency error <sup>(1)(2)</sup>	$T_A = -20^\circ\text{C}$ to $70^\circ\text{C}$	-1.5%	$\pm 0.25\%$	1.5%	
		$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$	-2.5%	$\pm 0.25\%$	2.5%	
$t_{(LSXO)}$	Start-up time <sup>(3)</sup>	$T_A = -25^\circ\text{C}$ to $85^\circ\text{C}$			100	$\mu\text{s}$

(1) The frequency drift is included and measured from the trimmed frequency at  $V_{CC} = 2.5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

(2) The frequency error is measured from 32.768 kHz.

(3) The startup time is defined as the time it takes for the oscillator output frequency to be  $\pm 3\%$ .

### ELECTRICAL CHARACTERISTICS: Internal Voltage Reference

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 3.8\text{ V}$  to  $25\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{REF}$	Internal Reference Voltage	1.215	1.225	1.230	V
$V_{REF\_DRIFT}$	Internal Reference Voltage Drift	$T_A = -25^\circ\text{C}$ to $85^\circ\text{C}$	$\pm 80$		PPM/ $^\circ\text{C}$
		$T_A = 0^\circ\text{C}$ to $60^\circ\text{C}$	$\pm 50$		PPM/ $^\circ\text{C}$

### ELECTRICAL CHARACTERISTICS: Flash

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 3.8\text{ V}$  to  $25\text{ V}$  (unless otherwise noted)

PARAMETER <sup>(1)</sup>	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Data retention		10			Years
Flash programming write-cycles	Data Flash	20k			Cycles
	Instruction Flash	1k			Cycles
$I_{CC(\text{PROG\_DF})}$	Data Flash-write supply current	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$	3	4	mA
$I_{CC(\text{ERASE\_DF})}$	Data Flash-erase supply current	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$	3	18	mA

(1) Verified by design. Not production tested.

### ELECTRICAL CHARACTERISTICS: OCD Current Protection

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 3.8\text{ V}$  to  $25\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$V_{(OCD)}$	OCD detection threshold voltage range, typical	$RSNS = 0$	50		200	mV
		$RSNS = 1$	25		100	mV
$\Delta V_{(OCDT)}$	OCD detection threshold voltage program step	$RSNS = 0$		10		mV
		$RSNS = 1$		5		mV
$V_{(OFFSET)}$	OCD offset		-10	10	mV	
$V_{(Scale\_Err)}$	OCD scale error		-10	10	%	
$t_{(OCDD)}$	Over Current in Discharge Delay		1	31	ms	
$t_{(OCDD\_STEP)}$	OCDD Step options		2		ms	
$t_{(DETECT)}$	Current fault detect time	$VS_{RP} - SRN = V_{THRESH} + 12.5\text{ mV}$		160	$\mu\text{s}$	
$t_{ACC}$	Over Current and Short Circuit delay time accuracy	Accuracy of typical delay time	-20	20	%	

### ELECTRICAL CHARACTERISTICS: SCD1 Current Protection

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 3.8\text{ V}$  to  $25\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$V_{(SDC1)}$	SCD1 detection threshold voltage range, typical	$RSNS = 0$	100		450	mV
		$RSNS = 1$	50		225	mV
$\Delta V_{(SDC1T)}$	SCD1 detection threshold voltage program step	$RSNS = 0$		50		mV
		$RSNS = 1$		25		mV
$V_{(OFFSET)}$	SCD1 offset		-10	10	mV	
$V_{(Scale\_Err)}$	SCD1 scale error		-10	10	%	
$t_{(SCD1D)}$	Short Circuit in Discharge Delay	$AFE.STATE\_CNTL[SCDDx2] = 0$	0		915	$\mu\text{s}$
		$AFE.STATE\_CNTL[SCDDx2] = 1$	0		1830	$\mu\text{s}$
$t_{(SCD1D\_STEP)}$	SCD1D Step options	$AFE.STATE\_CNTL[SCDDx2] = 0$		61		$\mu\text{s}$
		$AFE.STATE\_CNTL[SCDDx2] = 1$		122		$\mu\text{s}$
$t_{(DETECT)}$	Current fault detect time	$VS_{RP} - SRN = V_{THRESH} + 12.5\text{ mV}$		160	$\mu\text{s}$	

**ELECTRICAL CHARACTERISTICS: SCD1 Current Protection (continued)**

Typical values stated where TA = 25°C and VCC = 14.4 V, Min/Max values stated where TA = –40°C to 85°C and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>ACC</sub>	Over Current and Short Circuit delay time accuracy	Accuracy of typical delay time	–20	20	%

**ELECTRICAL CHARACTERISTICS: SCD2 Current Protection**

Typical values stated where TA = 25°C and VCC = 14.4 V, Min/Max values stated where TA = –40°C to 85°C and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>(SDC2)</sub>	SCD2 detection threshold voltage range, typical	RSNS = 0		450	mV
		RSNS = 1		225	mV
ΔV <sub>(SCD2T)</sub>	SCD2 detection threshold voltage program step	RSNS = 0	50		mV
		RSNS = 1	25		mV
V <sub>(OFFSET)</sub>	SCD2 offset		–10	10	mV
V <sub>(Scale_Err)</sub>	SCD2 scale error		–10	10	%
t <sub>(SCD1D)</sub>	Short Circuit in Discharge Delay	AFE.STATE_CNTL[SCDDx2] = 0		458	μs
		AFE.STATE_CNTL[SCDDx2] = 1		915	μs
t <sub>(SCD2D_STEP)</sub>	SCD2D Step options	AFE.STATE_CNTL[SCDDx2] = 0	30.5		μs
		AFE.STATE_CNTL[SCDDx2] = 1	61		μs
t <sub>(DETECT)</sub>	Current fault detect time	VSRP – SRN = VTHRESH + 12.5 mV		160	μs
t <sub>ACC</sub>	Over Current and Short Circuit delay time accuracy	Accuracy of typical delay time	–20	20	%

**ELECTRICAL CHARACTERISTICS: SCC Current Protection**

Typical values stated where TA = 25°C and VCC = 14.4 V, Min/Max values stated where TA = –40°C to 85°C and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>(SCCT)</sub>	SCC detection threshold voltage range, typical	RSNS = 0		–300	mV
		RSNS = 1		–225	mV
ΔV <sub>(SCCDT)</sub>	SCC detection threshold voltage program step	RSNS = 0	–50		mV
		RSNS = 1	–25		mV
V <sub>(OFFSET)</sub>	SCC offset		–10	10	mV
V <sub>(Scale_Err)</sub>	SCC scale error		–10	10	%
t <sub>(SCCD)</sub>	Short Circuit in Charge Delay		0	915	ms
t <sub>(SCCD_STEP)</sub>	SCCD Step options		61		ms
t <sub>(DETECT)</sub>	Current fault detect time	VSRP – SRN = VTHRESH + 12.5 mV		160	μs
t <sub>ACC</sub>	Over Current and Short Circuit delay time accuracy	Accuracy of typical delay time	–20	20	%

**ELECTRICAL CHARACTERISTICS: SBS Timing Characteristics**

Typical values stated where TA = 25°C and VCC = 14.4 V, Min/Max values stated where TA = –40°C to 85°C and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>SMB</sub>	SMBus operating frequency	Slave mode, SMBC 50% duty cycle	10	100	kHz
f <sub>MAS</sub>	SMBus master clock frequency	Master mode, no clock low slave extend	51.2		kHz
t <sub>BUF</sub>	Bus free time between start and stop		4.7		μs
t <sub>HD:STA</sub>	Hold time after (repeated) start		4.0		μs

### ELECTRICAL CHARACTERISTICS: SBS Timing Characteristics (continued)

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 14.4\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 3.8\text{ V}$  to  $25\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{\text{SU:STA}}$	Repeated start setup time	4.7			$\mu\text{s}$
$t_{\text{SU:STO}}$	Stop setup time	4.0			$\mu\text{s}$
$t_{\text{HD:DAT}}$	Data hold time	300			ns
$t_{\text{SU:DAT}}$	Data setup time	250			ns
$t_{\text{TIMEOUT}}$	Error signal/detect	See <sup>(1)</sup>		35	ms
$t_{\text{LOW}}$	Clock low period	4.7			$\mu\text{s}$
$t_{\text{HIGH}}$	Clock high period	See <sup>(2)</sup>		Disabled	
$t_{\text{HIGH}}$	Clock high period	See <sup>(2)</sup>		50	$\mu\text{s}$
$t_{\text{LOW:SEXT}}$	Cumulative clock low slave extend time	See <sup>(3)</sup>		25	ms
$t_{\text{LOW:MEXT}}$	Cumulative clock low master extend time	See <sup>(4)</sup>		10	ms
$t_{\text{F}}$	Clock/data fall time	See <sup>(5)</sup>		300	ns
$t_{\text{R}}$	Clock/data rise time	See <sup>(6)</sup>		1000	ns

- (1) The bq3050 times out when any clock low exceeds  $t_{\text{TIMEOUT}}$ .
- (2)  $t_{\text{HIGH, Max}}$  is the minimum bus idle time.  $\text{SMBC} = 1$  for  $t > 50\ \mu\text{s}$  causes reset of any transaction involving bq3050 that is in progress. This specification is valid when the  $\text{THIGH\_VAL} = 0$ . If  $\text{THIGH\_VAL} = 1$ , then the value of  $\text{THIGH}$  is set by  $\text{THIGH\_1,2}$  and the timeout is not SMBus standard.
- (3)  $t_{\text{LOW:SEXT}}$  is the cumulative time a slave device is allowed to extend the clock cycles in one message from initial start to the stop.
- (4)  $t_{\text{LOW:MEXT}}$  is the cumulative time a master device is allowed to extend the clock cycles in one message from initial start to the stop.
- (5) Rise time  $t_{\text{R}} = V_{\text{ILMAX}} - 0.15$  to  $(V_{\text{IHMIN}} + 0.15)$
- (6) Fall time  $t_{\text{F}} = 0.9 V_{\text{DD}}$  to  $(V_{\text{ILMAX}} - 0.15)$

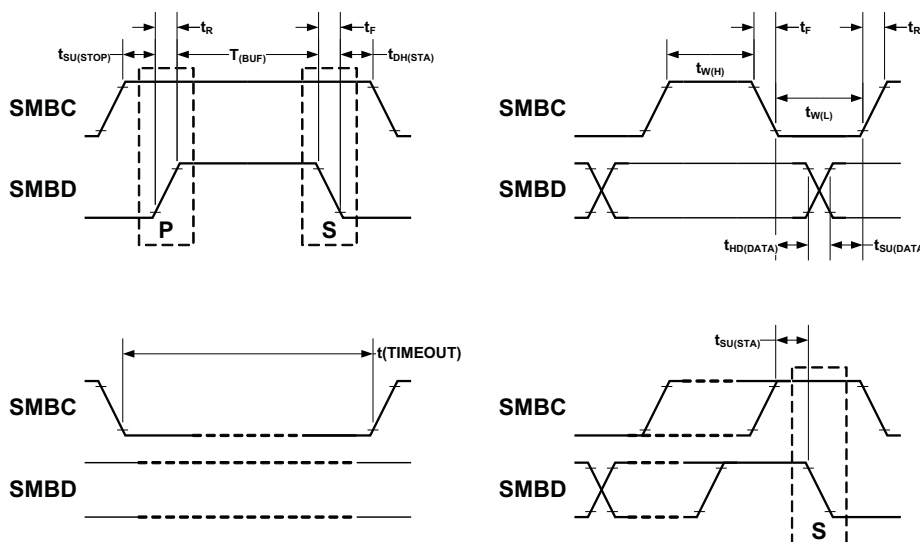


Figure 3. SMBus Timing Diagram

## FEATURE SET

### Primary (1st Level) Safety Features

The bq3050 supports a wide range of battery and system protection features that can easily be configured. The primary safety features include:

- Cell Overvoltage/Undervoltage Protection
- Charge and Discharge Overcurrent
- Short-Circuit
- Charge and Discharge Over-Temperature
- AFE Watchdog

### Secondary (2nd Level) Safety Features

The secondary safety features of the bq3050 can be used to indicate more serious faults via the FUSE pin. This pin can be used to blow an in-line fuse to permanently disable the battery pack from charging or discharging. The secondary safety protection features include:

- Safety Overvoltage
- Safety Overcurrent in Charge and Discharge
- Safety Over-Temperature in Charge and Discharge
- Charge FET, Discharge FET, and Pre-Charge FET Faults
- Cell Imbalance Detection
- Fuse Blow by Secondary Voltage Protection IC
- AFE Register Integrity Fault (AFE\_P)
- AFE Communication Fault (AFE\_C)

### Charge Control Features

The bq3050 charge control features include:

- Supports JEITA temperature ranges. Reports charging voltage and charging current according to the active temperature range
- Handles more complex charging profiles. Allows for splitting the standard temperature range into two sub-ranges and allows for varying the charging current according to the cell voltage
- Reports the appropriate charging current needed for constant current charging and the appropriate charging voltage needed for constant voltage charging to a smart charger using SMBus broadcasts
- Reduce the charge difference of the battery cells in fully charged state of the battery pack gradually using a voltage-based cell balancing algorithm during charging. A voltage threshold can be set up for cell balancing to be active. This prevents fully charged cells from overcharging and causing excessive degradation and also increases the usable pack energy by preventing premature charge termination.
- Supports pre-charging/zero-volt charging
- Supports charge inhibit and charge suspend if battery pack temperature is out of temperature range
- Reports charging fault and also indicate charge status via charge and discharge alarms

### Gas Gauging

The bq3050 uses the CEDV algorithm to measure and calculate the available capacity in battery cells. The bq3050 accumulates a measure of charge and discharge currents and compensates the charge current measurement for the temperature and state-of-charge of the battery. The bq3050 estimates self-discharge of the battery and also adjusts the self-discharge estimation based on temperature. See the *bq3050 Technical Reference Manual (SLUU440)* for further details.

### Lifetime Data Logging Features

The bq3050 offers limited lifetime data logging for the following critical battery parameters:

- Lifetime Maximum Temperature
- Lifetime Minimum Temperature

- Lifetime Maximum Battery Cell Voltage
- Lifetime Minimum Battery Cell Voltage

### Authentication

- The bq3050 supports authentication by the host using SHA-1.
- SHA-1 authentication by the gas gauge is required for unsealing and full access.

### Power Modes

The bq3050 supports three power modes to reduce power consumption:

- In Normal Mode, the bq3050 performs measurements, calculations, protection decisions, and data updates in 0.25-second intervals. Between these intervals, the bq3050 is in a reduced power stage.
- In Sleep Mode, the bq3050 performs measurements, calculations, protection decisions, and data updates in adjustable time intervals. Between these intervals, the bq3050 is in a reduced power stage. The bq3050 has a wake function that enables exit from Sleep mode when current flow or failure is detected.
- In Shutdown Mode, the bq3050 is completely disabled.

### Configuration

#### Oscillator Function

The bq3050 fully integrates the system oscillators and does not require any external components to support this feature.

#### System Present Operation

The bq3050 checks the  $\overline{\text{PRES}}$  pin periodically (1s). If  $\overline{\text{PRES}}$  input is pulled to ground by the external system, the bq3050 detects this as system present.

#### 2-, 3-, or 4-Cell Configuration

In a 2-cell configuration, VC1 is shorted to VC2 and VC3. In a 3-cell configuration, VC1 is shorted to VC2.

#### Cell Balancing

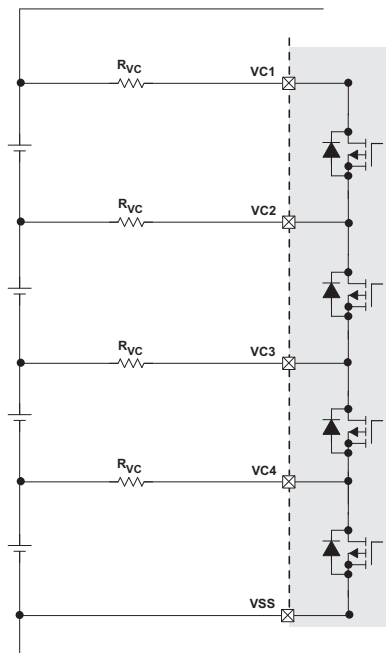
The device supports cell balancing by bypassing the current of each cell during charging or at rest. If the device's internal bypass is used, up to 10 mA can be bypassed and multiple cells can be bypassed at the same time. Higher cell balance current can be achieved by using an external cell balancing circuit. In external cell balancing mode, only one cell at a time can be balanced.

The cell balancing algorithm determines the amount of charge needed to be bypassed to balance the capacity of all cells.

#### Internal Cell Balancing

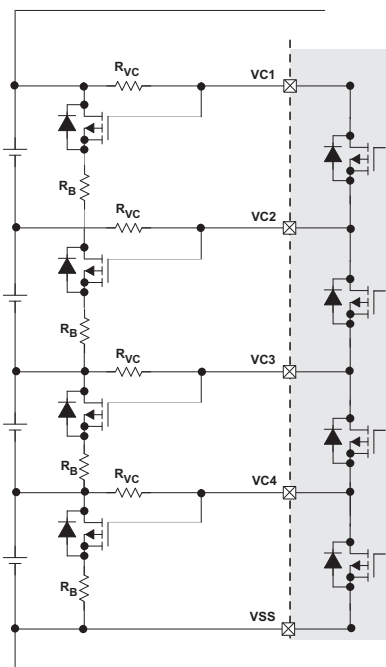
When internal cell balancing is configured, the cell balance current is defined by the external resistor  $R_{VC}$  at the VCx input.





**External Cell Balancing**

When external cell balancing is configured, the cell balance current is defined by  $R_B$ . Only one cell at a time can be balanced.



## BATTERY PARAMETER MEASUREMENTS

### Charge and Discharge Counting

The bq3050 uses an integrating delta-sigma analog-to-digital converter (ADC) for current measurement, and a second delta-sigma ADC for individual cell and battery voltage and temperature measurement.

The integrating delta-sigma ADC measures the charge/discharge flow of the battery by measuring the voltage drop across a small-value sense resistor between the SR1 and SR2 pins. The integrating ADC measures bipolar signals from  $-0.25\text{ V}$  to  $0.25\text{ V}$ . The bq3050 detects charge activity when  $V_{SR} = V_{(SRP)} - V_{(SRN)}$  is positive, and discharge activity when  $V_{SR} = V_{(SRP)} - V_{(SRN)}$  is negative. The bq3050 continuously integrates the signal over time, using an internal counter. The fundamental rate of the counter is  $0.65\text{ nVh}$ .

### Voltage

The bq3050 updates the individual series cell voltages at 0.25-second intervals. The internal ADC of the bq3050 measures the voltage, and scales and calibrates it appropriately. This data is also used to calculate the impedance of the cell for the CEDV gas-gauging.

### Current

The bq3050 uses the SRP and SRN inputs to measure and calculate the battery charge and discharge current using a  $5\text{-m}\Omega$  to  $20\text{-m}\Omega$  typ. sense resistor.

### Auto Calibration

The bq3050 provides an auto-calibration feature to cancel the voltage offset error across SRN and SRP for maximum charge measurement accuracy. The bq3050 performs auto-calibration when the SMBus lines stay low continuously for a minimum of 5 s.

### Temperature

The bq3050 has an internal temperature sensor and inputs for two external temperature sensors. All three temperature sensor options are individually enabled and configured for cell or FET temperature. Two configurable thermistor models are provided to allow the monitoring of cell temperature in addition to FET temperature, which may be of a higher temperature type.

### Communications

The bq3050 uses SMBus v1.1 with Master Mode and packet error checking (PEC) options per the SBS specification.

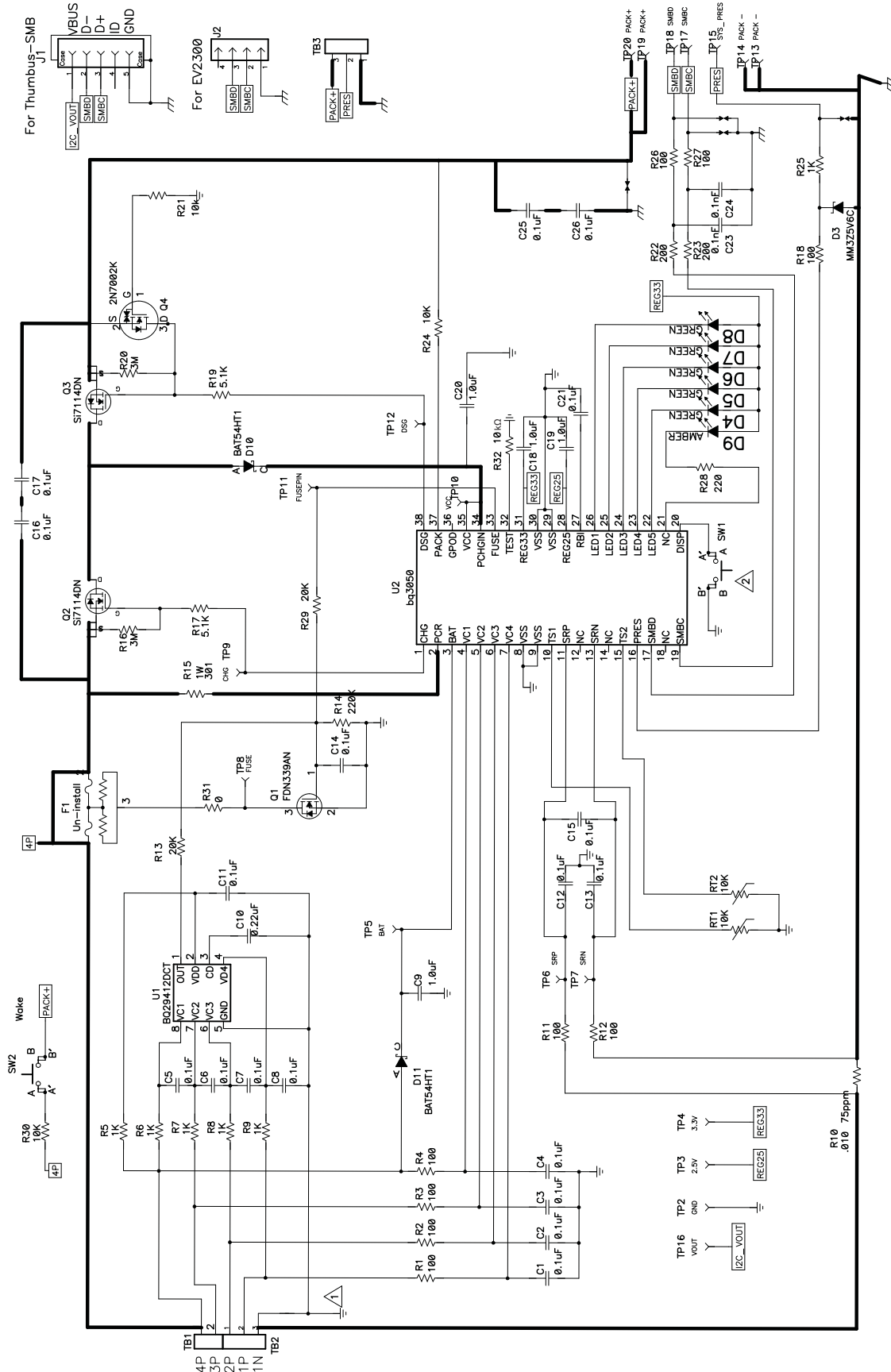
### SMBus On and Off State

The bq3050 detects an SMBus off state when SMBC and SMBD are low for two or more seconds. Clearing this state requires that either SMBC or SMBD transition high. The communication bus will resume activity within 1ms.

### SBS Commands

See the *bq3050 Technical Reference Manual (SLUU440)* for further details.

## APPLICATION SCHEMATIC





## REVISION HISTORY

Changes from Original (January 2011) to Revision A	Page
• Changed Block Diagram .....	3
• Changed TS2 pin number .....	4
• Changed TEST pin resistor value .....	5
• Changed schematic .....	20

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
BQ3050DBT	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
BQ3050DBTR	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

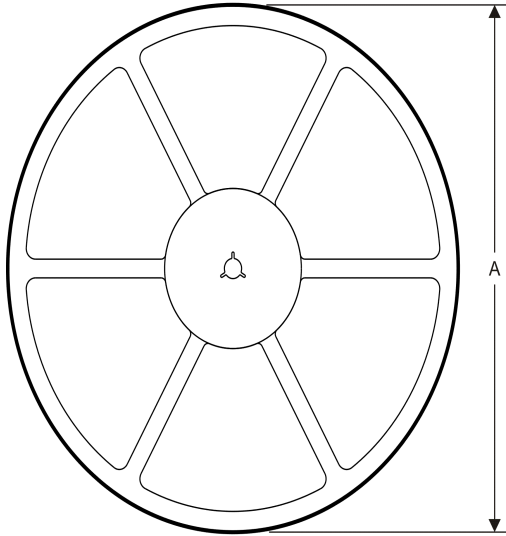
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**



**TAPE DIMENSIONS**



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ3050DBTR	TSSOP	DBT	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1



TAPE AND REEL BOX DIMENSIONS



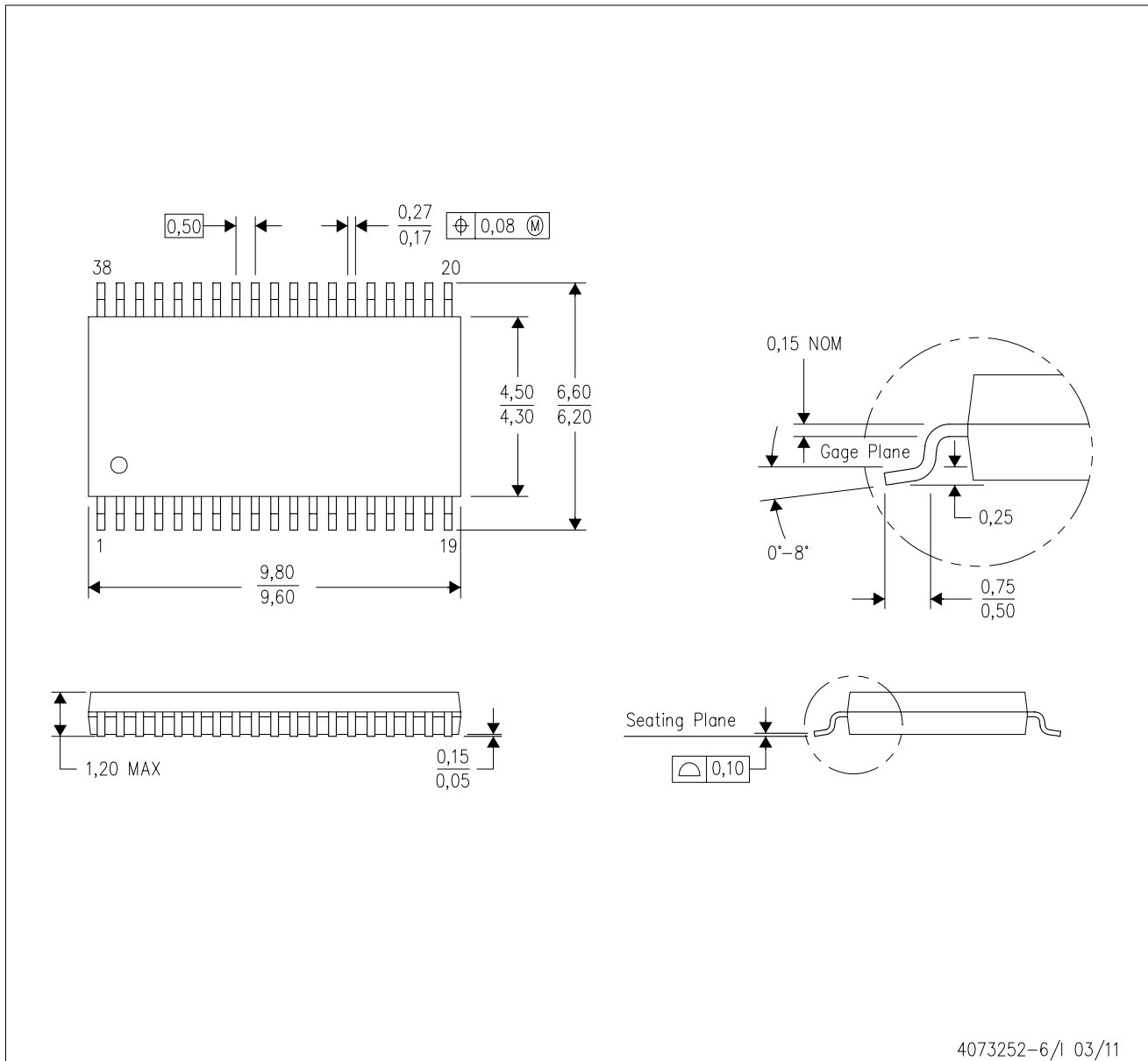
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ3050DBTR	TSSOP	DBT	38	2000	367.0	367.0	38.0

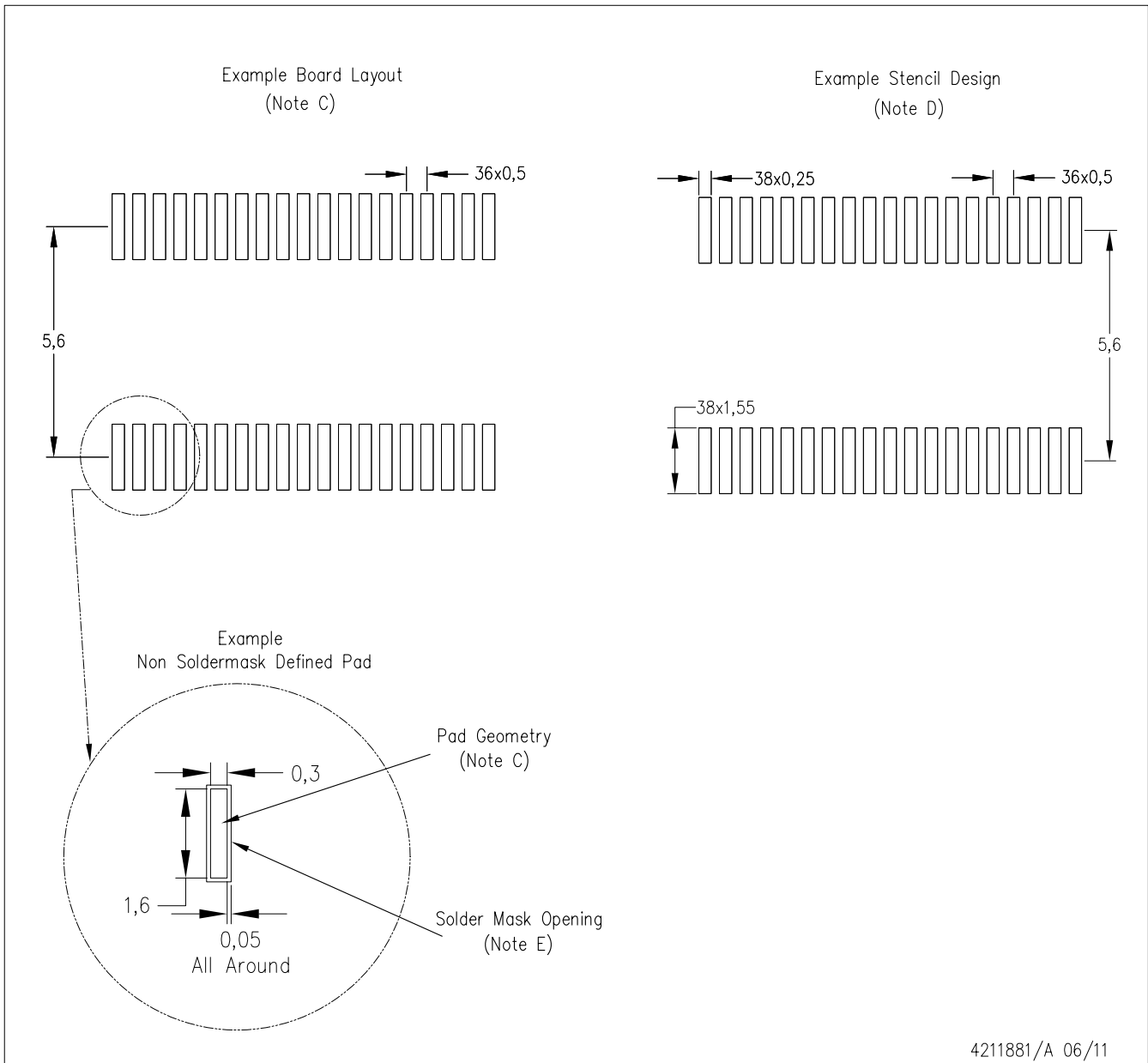
# MECHANICAL DATA

DBT (R-PDSO-G38)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion.
  - Falls within JEDEC MO-153.



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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