6-bit 0.5 dB Digital Step Attenuator　　　　　　　　　　　**100 MHz to 4000 MHz**

GENERAL DESCRIPTION

This document describes the specification for the F1951 Digital Step Attenuator. The F1951 is part of a family of *Glitch-Free*[TM] DSAs optimized for the demanding requirements of communications Infrastructure. These devices are offered in a compact 4x4 QFN package with 50 Ω impedances for ease of integration into the radio system.

COMPETITIVE ADVANTAGE

Digital step attenuators are used in Receivers and Transmitters to provide gain control. The F1951 is a 6-bit step attenuator optimized for these demanding applications. The silicon design has very low insertion loss and low distortion (+65 dBm IP3$_I$.). The device has pinpoint accuracy and settles to final attenuation value within 400 nsec. Most importantly, the F1951 includes IDT's *Glitch-Free*[TM] technology which results in less than 0.6 dB of overshoot ringing during MSB transitions. This is in stark contrast to competing DSAs that *glitch as much as 10 dB* during MSB transitions (see p.10).

✓ Lowest insertion loss for best SNR

✓ Glitch-Free[TM] when transitioning – won't damage PA or ADC

✓ Extremely accurate with low distortion

Glitch-Free[TM]

APPLICATIONS

- Base Station 2G, 3G, 4G, TDD radiocards
- Repeaters and E911 systems
- Digital Pre-Distortion
- Point to Point Infrastructure
- Public Safety Infrastructure
- WIMAX Receivers and Transmitters
- Military Systems, JTRS radios
- RFID handheld and portable readers
- Cable Infrastructure

FEATURES

- *Glitch-Free*[TM], < 0.6 dB transient overshoot
- Spurious Free Design
- 3 V to 5.25 V supply
- Attenuation Error < 0.2 dB @ 2 GHz
- Low Insertion Loss < 1.2 dB @ 2 GHz
- Excellent Linearity +65 dBm IP3$_I$
- Fast settling time, < 450 ns
- Class 2 JEDEC ESD (> 2kV HBM)
- Serial Interface 31.5 dB Range
- Stable Integral Non-Linearity over temperature
- 4x4 mm Thin QFN 24 pin package

DEVICE BLOCK DIAGRAM

ORDERING INFORMATION

0.8 mm height package　　　**Tape & Reel**

F1951NBGI8

Green　　　**Industrial Temp range**

PART# MATRIX

Part#	Freq range (MHz)	Resolution / Range (dB)	Control	IL (dB)	Pinout
F1951	100 - 4000	0.50 / 31.5	Serial Only	-1.2	HITT
F1950	150 - 4000	0.25 / 31.5	Serial Only	-1.3	PE
F1952	100 – 4000	0.50 / 15.5	Serial Only	-0.9	HITT
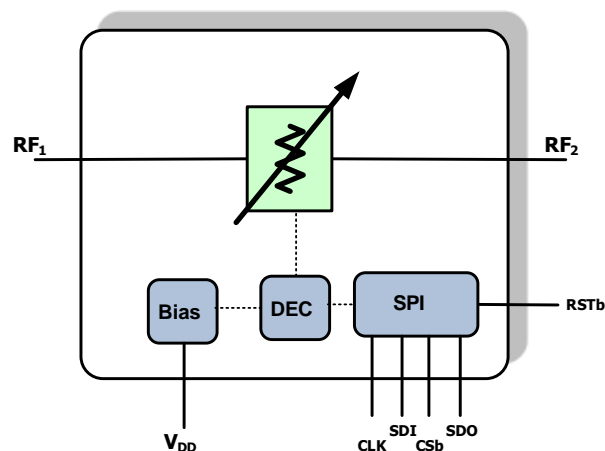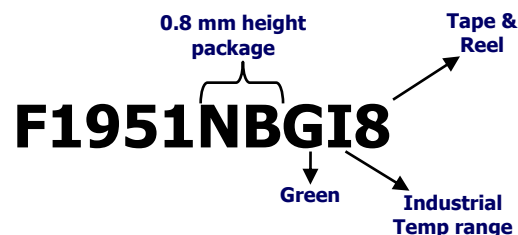
6-bit 0.5 dB Digital Step Attenuator   **100 MHz to 4000 MHz**

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND	-0.3 V to +5.50V
D[5:0], DATA, CLK, CSb, SDO, RSTb	-0.3 V to 3.6 V
RF Input Power (RF1, RF2) calibration and testing	+29 dBm
RF Input Power (RF1, RF2) continuous RF operation	+23 dBm
θ_{JA} (Junction – Ambient)	+50 °C/W
θ_{JC} (Junction – Case) The Case is defined as the exposed paddle	+3 °C/W
Operating Temperature Range (Case Temperature)	T_C = -40 °C to +100°C
Maximum Junction Temperature	140 °C
Storage Temperature Range	-65 °C to +150 °C
Lead Temperature (soldering, 10s)	+260 °C

F1951 SPECIFICATION (31.5 dB Range)

Specifications apply at **V_{DD} = +3.3V**, **f_{RF} = 2000MHz**, T_C= +25°C unless otherwise noted, EVKit losses are de-embedded (see p. 17)

Parameter	Comment	Sym.	Min	Typical	Max	Units
Logic Input High	CLK, CSb, DATA, D[5:0], RSTb	V_{IH}	*2.3[a]*		3.6[b]	V
Logic Input Low	CLK, CSb, DATA, D[5:0], RSTb	V_{IL}			*0.7*	V
Logic Current	V_{MODE}	I_{IH}, I_{IL}	*-5*		*+5*	µA
Supply Voltage(s)	Main Supply	V_{DD}	3.0		5.25	V
Supply Current	Total	I_{DD}		*1.1*	*2*	mA
Temperature Range	Operating Range (Case)	T_C	-40		100	°C
Frequency Range	Operating Range	f_{RF}	100		4000	MHz
RF1, RF2 Return Loss	dB(s11), dB(s22)	S_{11}, S_{22}		-22		dB
Minimum Attenuation	D[5:0] = [111111]	A_{MIN} or **IL**		*1.2*	*1.9*	dB
Maximum Attenuation	• D[5:0] = [000000] • V_{DD} = 3.3V	A_{MAX}	32.2	32.5		dB
Minimum Gain Step	Least Significant Bit	**LSB**		0.50		dB
Phase Delta	Phase change A_{MIN} vs. A_{MAX}	Φ_Δ		33		deg
Differential Non-Linearity	Error: adjacent steps	**DNL**		0.08		dB
Integral Non-Linearity	Error: absolute to 14 dB ATTN	INL_1		*0.03*	*0.34*	dB
Integral Non-Linearity	Max Error vs. line (A_{MIN} ref) to 31.5 dB ATTN [V_{DD} = 3.3V]	INL_2		0.21	0.38	dB
Input IP3	▪ P_{IN} = +10 dBm per tone ▪ 50 MHz Tone Separation ▪ V_{DD} = 3.3V					dBm
	D[5:0] = [111111] = A_{MIN}	$IP3I_1$	+61	+64		
	D[5:0] = [100000] = $A_{15.5}$	$IP3I_2$	+59	+61		
	D[5:0] = [000000] = A_{MAX}	$IP3I_3$	+57	+61		
0.1 dB Compression *Please note ABS MAX*	▪ D[5:0] = [111010] = $A_{2.5}$ ▪ Baseline P_{IN} = 20 dBm	$P_{0.1}$		29		dBm
Settling Time	▪ Start LE rising edge > V_{IH} ▪ End +/-0.10 dB Pout settling ▪ 15.5 – 16.0 transition	T_{LSB}		400		ns
Serial Clock Speed	SPI 4 wire bus	F_{CLK}		*20*	*50*	MHz
Reset to Serial Setup	SPI 4 wire bus	**A**	*20*			ns
Serial Data Hold Time	SPI 4 wire bus	**B**	*5*			ns
CSb setup delay	SPI 4 wire bus	**C**	*40*			ns
Serial Data Out Delay	SPI 4 wire bus	**D**	*8*	*8*	*8*	Cycles

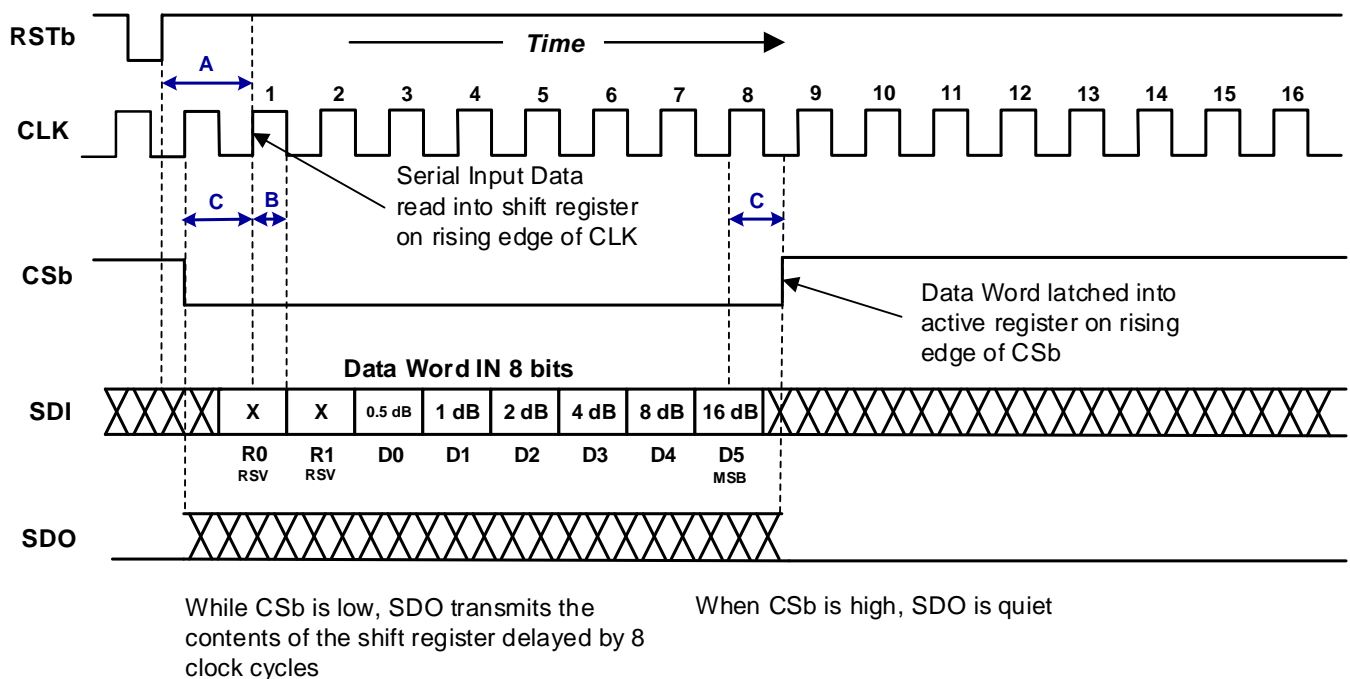[a] – Items in min/max columns in ***bold italics*** are Guaranteed by Test.
[b] – All other Items in min/max columns are Guaranteed by Design Characterization.

6-bit 0.5 dB Digital Step Attenuator　　　　　　　　　　　　　　**100 MHz to 4000 MHz**

SERIAL CONTROL MODE

Data is clocked in LSB first via serial mode. Note the timing diagram below.

An RSTb pulse resets the shift register to [00000000]. If the RSTb pulse is followed immediately by a CSb pulse the device will be set to **Maximum Attenuation**.

Note – *The F1951 includes a CLK inhibit feature designed to minimize sensitivity to CLK bus noise when the device is not being programmed. When CSb is high (> V_{IH}), the CLK input is disabled and serial data (SDI) will not be clocked into the shift register. It is recommended that CSb be pulled high (>V_{IH}) when the device is not being programmed*

SERIAL REGISTER TIMING DIAGRAM [SINGLE DEVICE]: (Note the Timing Spec Intervals in **Blue**)

While CSb is low, SDO transmits the contents of the shift register delayed by 8 clock cycles

When CSb is high, SDO is quiet

6-bit 0.5 dB Digital Step Attenuator   **100 MHz to 4000 MHz**

SERIAL REGISTER TIMING DIAGRAM [TWO OR MORE DEVICES]:

The SDO output is delayed by 8 clock cycles while CSb is low. The SDO low logic voltage is 0 volts and the SDO high logic voltage is VDD/2. This feature allows one to program multiple DSAs (in a MIMO transceiver for instance) with a single common CSb line by daisy-chaining the SDO of the 2nd DSA to the SDI of the 1st DSA and so forth:

SDO returns the 1st word written which will program DSA1
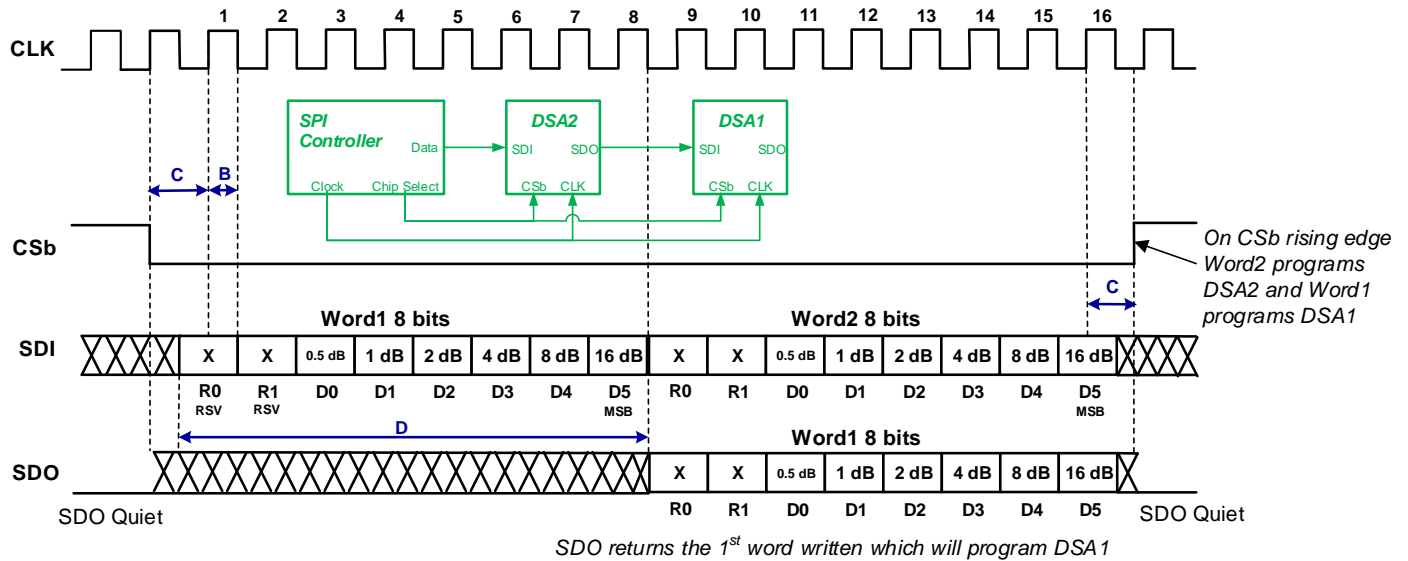
SERIAL REGISTER DEFAULT CONDITION [F1951]:

When the device is first powered up, it will default to the **Maximum Attenuation** setting as described below:
Note that for the F1951 (High or 1) = Attenuation Stepped __OUT__. (0 or Low) = Attenuation Stepped __IN__.

Default Register Settings

| 0	0	0	0	0	0	0	0
R0	R1	D0	D1	D2	D3	D4	D5
RSV	RSV	LSB					MSB

SERIAL REGISTER TIMING TABLE [F1951]:

| Interval Symbol	Description	Min Spec	Max Spec	Units
A	Reset to Serial Setup Time	20		ns
B	Serial Data Hold Time	5		ns
C	CSb setup delay	40		ns
D	Serial Data Out Delay	8	8	Cycles

6-bit 0.5 dB Digital Step Attenuator

## TYPICAL OPERATING PARAMETRIC CURVES (EVKit loss de-embedded, 3.3V unless otherwise noted)

Insertion Loss vs. Frequency [A_{MIN}]
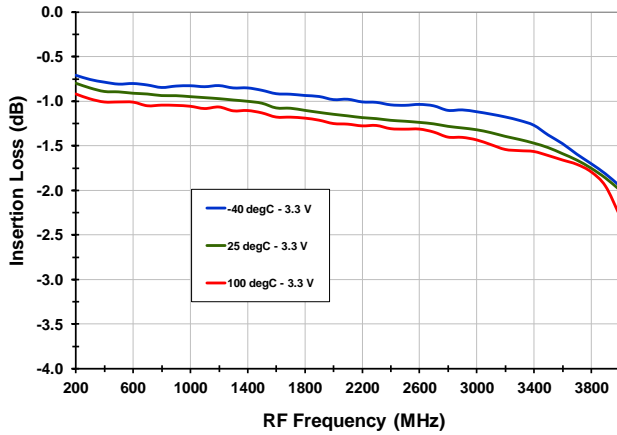
Attenuation vs. Freq [T_{CASE} = +25C, 0.5 dB steps]
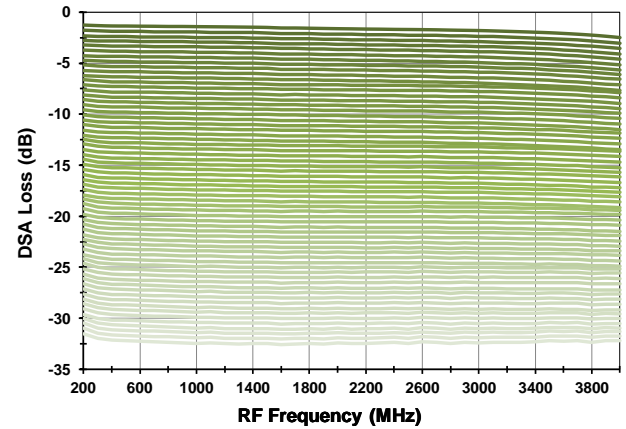
S_{11} vs. Frequency [T_{CASE} = +25C, 0.5 dB steps]
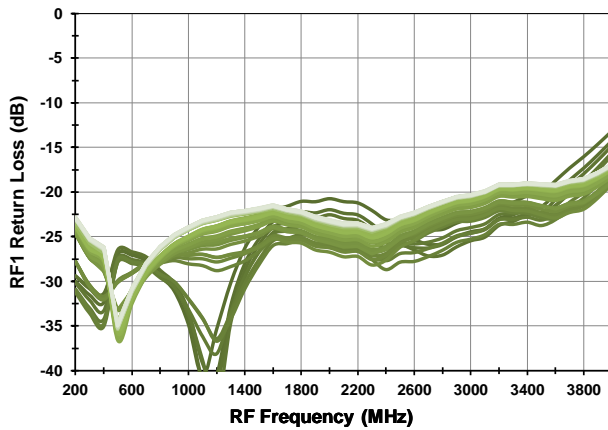
S_{22} vs. Frequency [T_{CASE} = +25C, 0.5 dB steps]
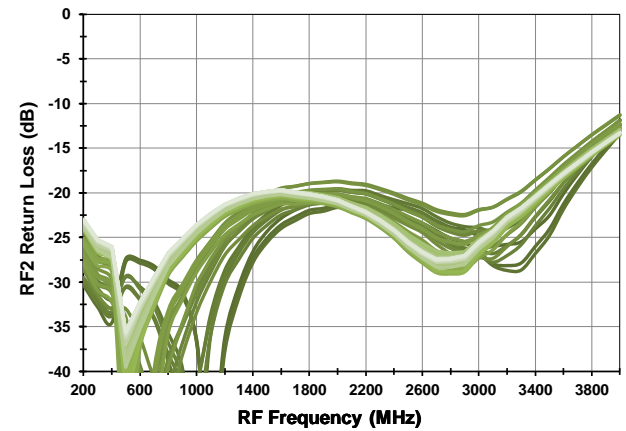
S_{11} vs. Attenuation State
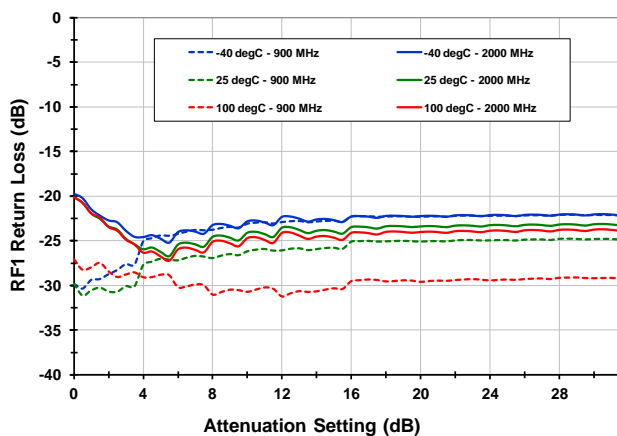
S_{22} vs. Attenuation State
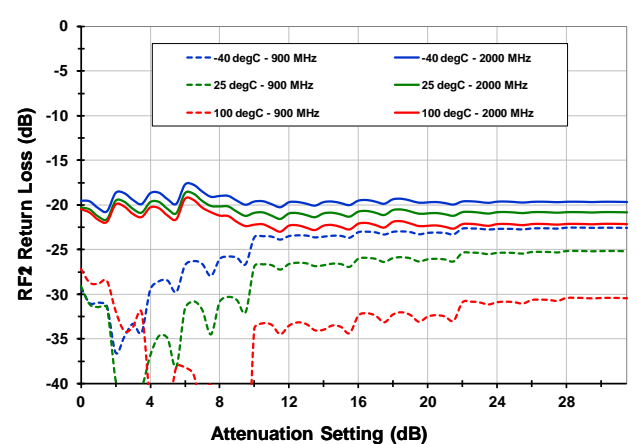
TOCs CONTINUED (-2-)

Phase vs. Frequency
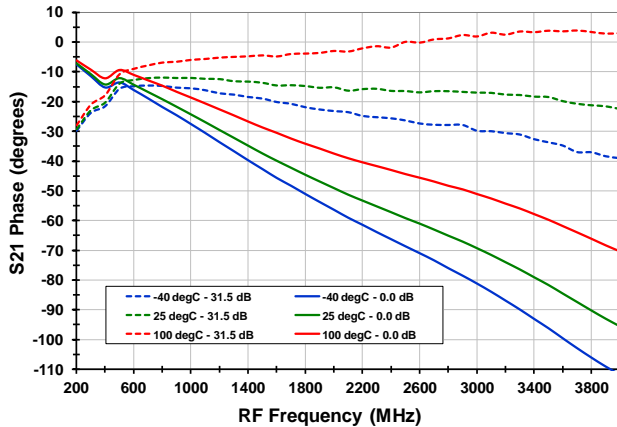
Phase vs. Attenuation Setting
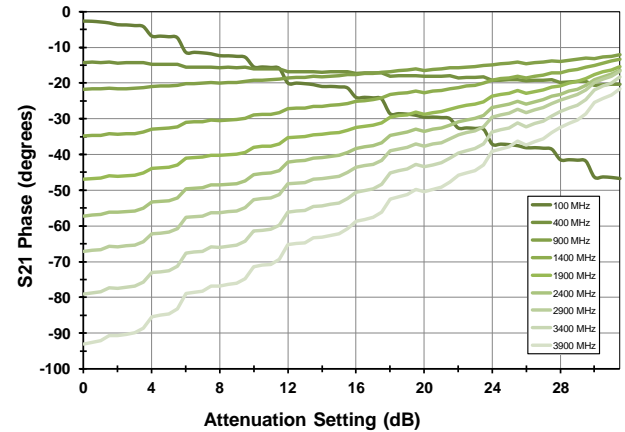
Supply Current I$_{DD}$
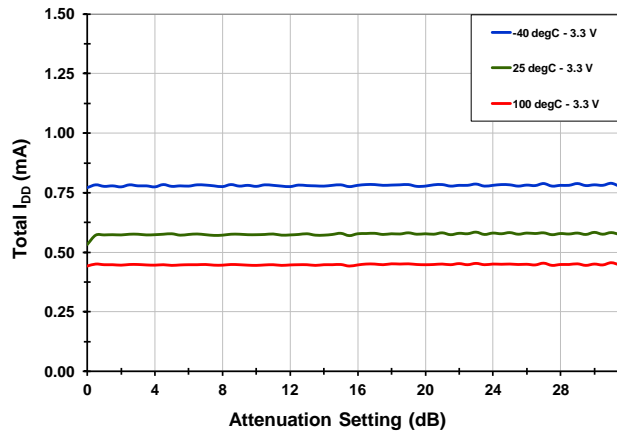
Input IP3 [f$_{RF}$ = 900 MHz]
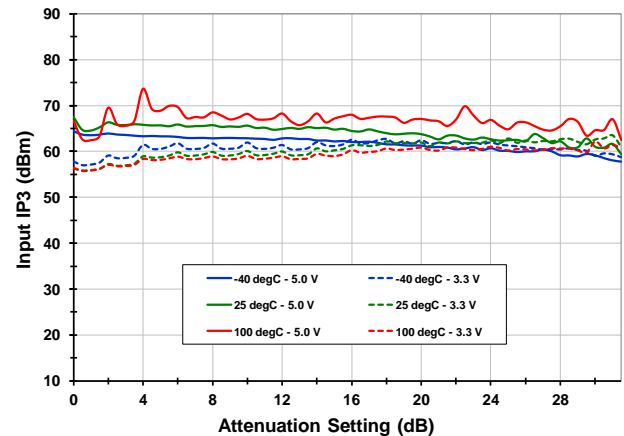
Input IP3 [f$_{RF}$ = 1900 MHz]
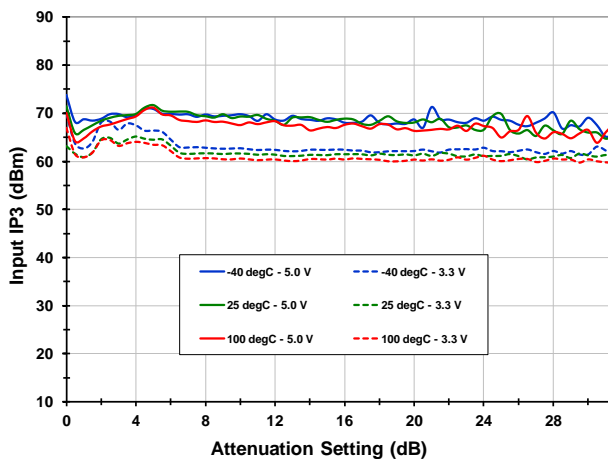
Compression [f$_{RF}$ = 2000 MHz, ATTN = 2.5 dB]
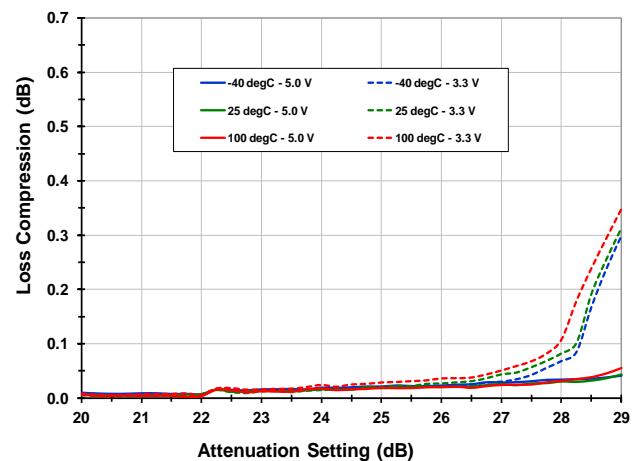
TOCs CONTINUED (-3-)

DNL [150 MHz]
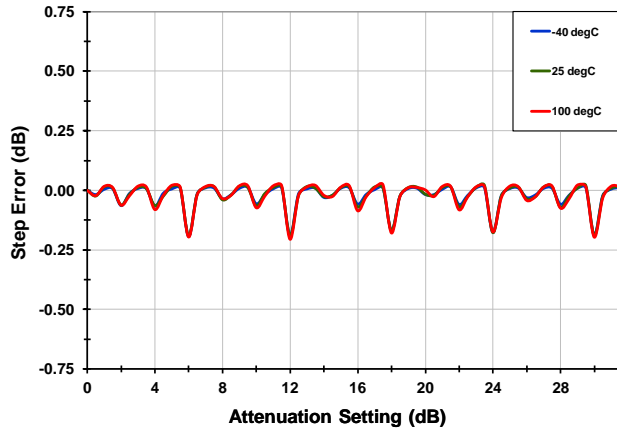
DNL [400 MHz]
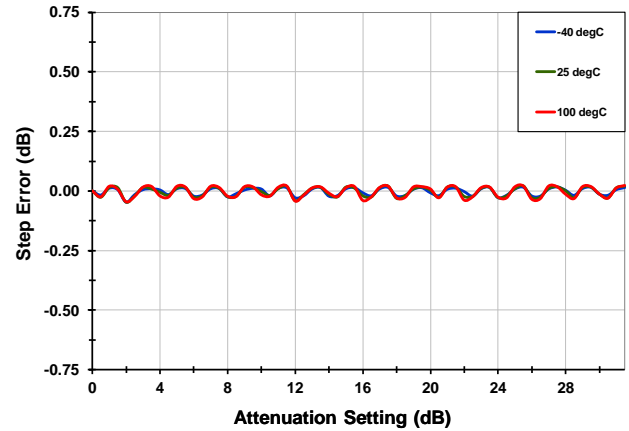
DNL [900 MHz]
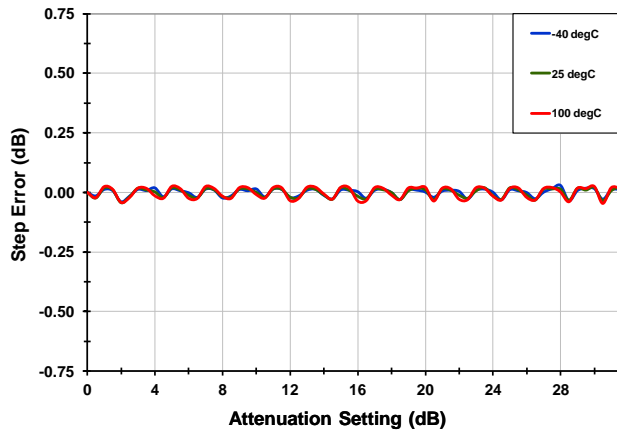
DNL [1900 MHz]
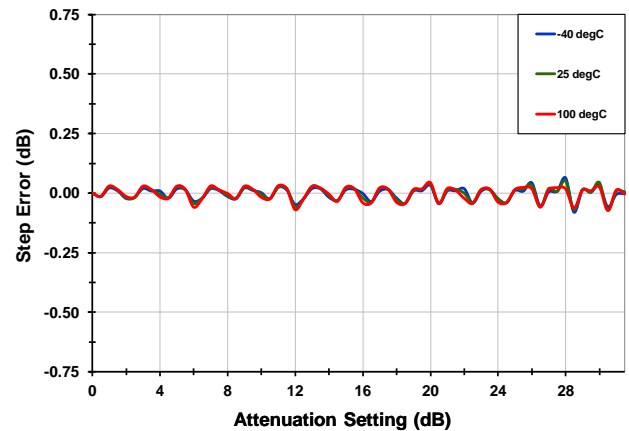
DNL [2800 MHz]
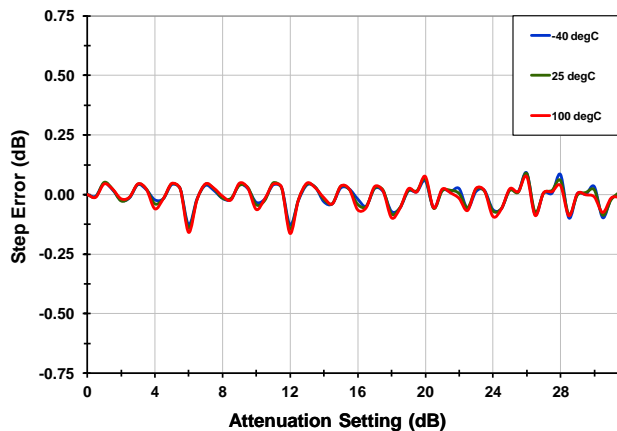
Worst Setting DNL
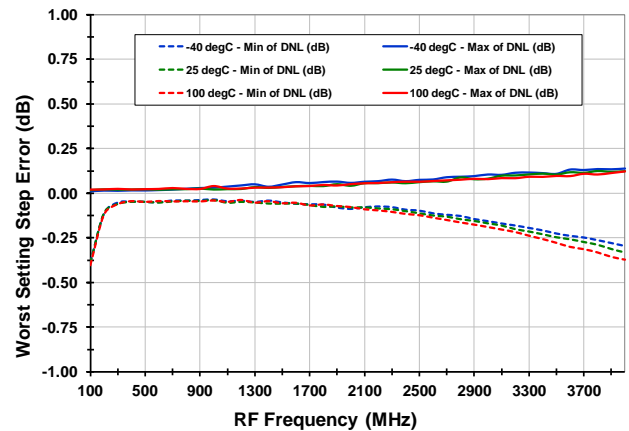
TOCs CONTINUED (-4-)

INL [150 MHz]
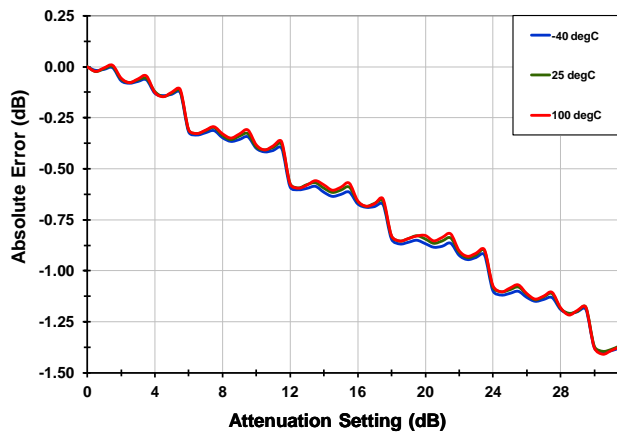
INL [400 MHz]
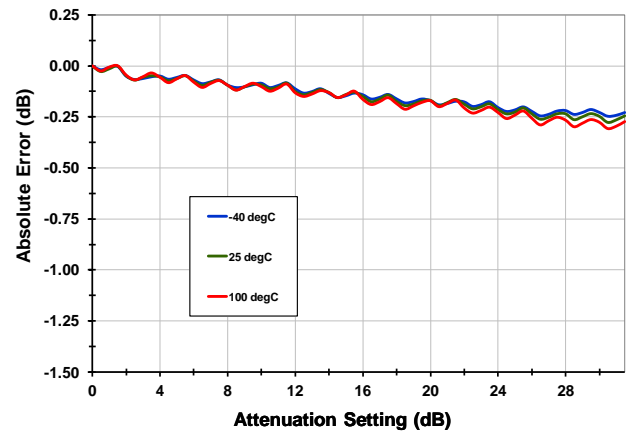
INL [900 MHz]
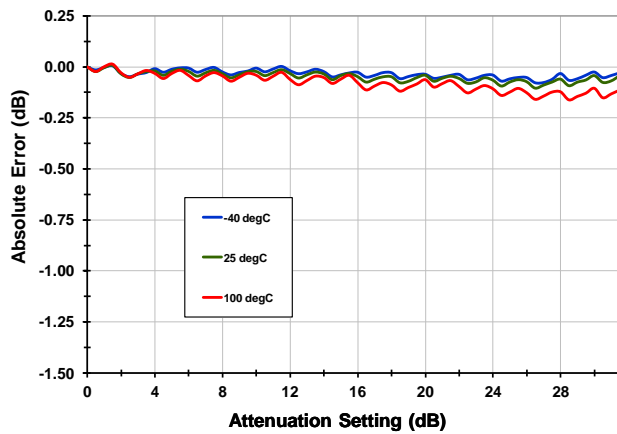
INL [1900 MHz]
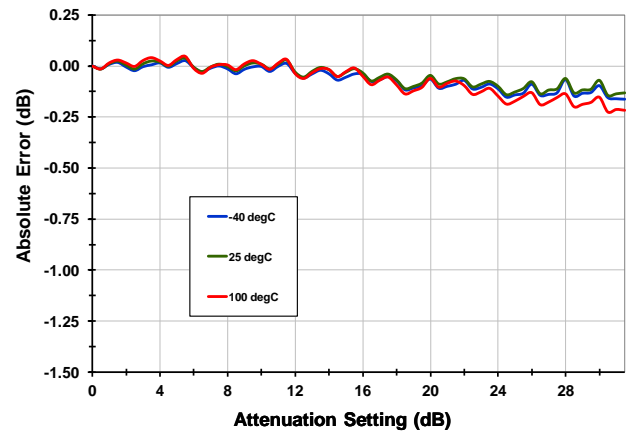
INL [2900 MHz]
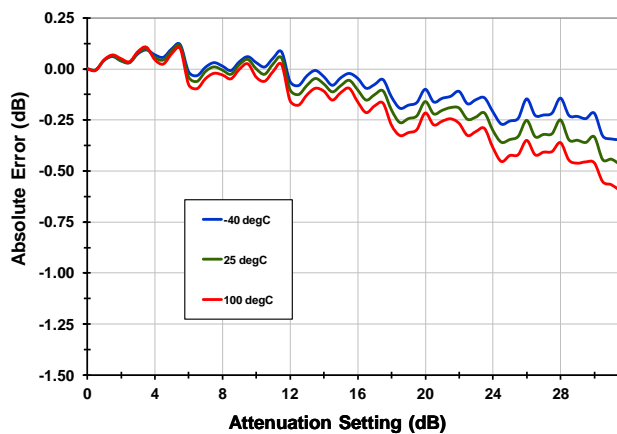
Worst Setting INL
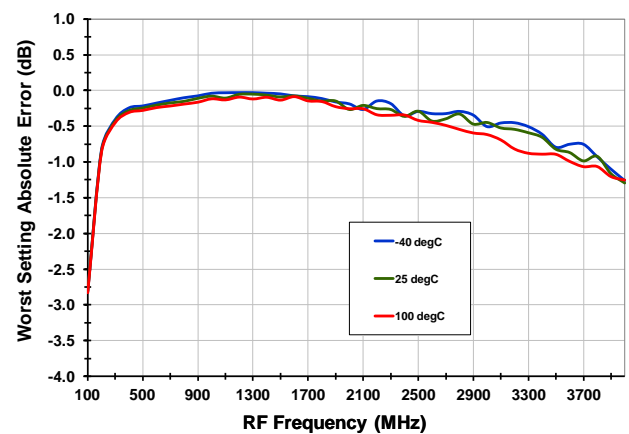
TOCs CONTINUED (-5-) [f_RF = 900 MHz]

Transient [15.5 to 16.0 (MSB+) 3.3V *F1951*]

Transient [16.0 to 15.5 (MSB-) 5.0V *F1951*]
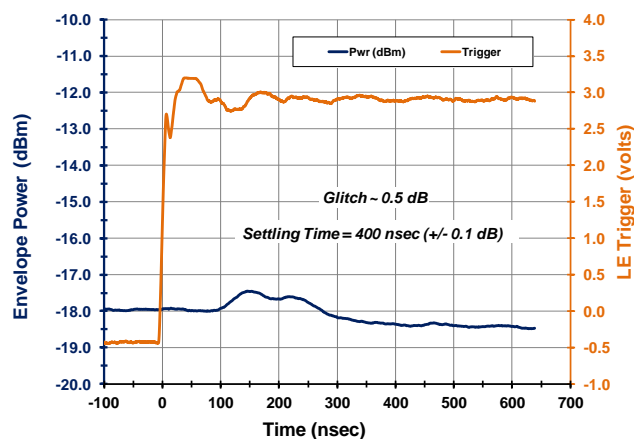
The graphs ABOVE show the transient overshoot and settling time performance for both the MSB+ and MSB- cases for the F1951. The device settles very quickly (~400 ns) with benign (~0.5 dB) overshoot.
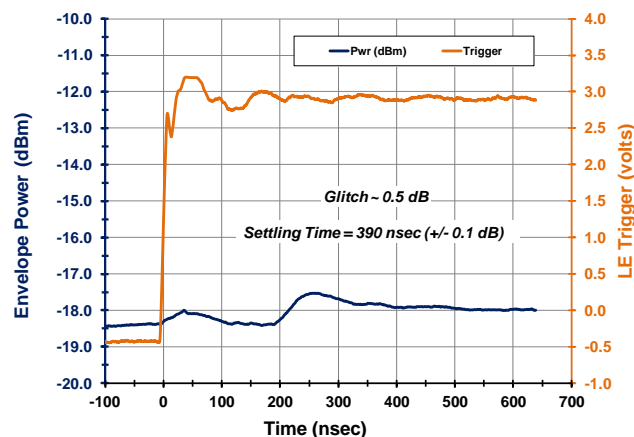
The graphs BELOW show the transient overshoot and settling time performance for a popular competing DSA. *Note the overshoot/undershoot excursion of almost 10 dB* and the very long settling time. For the MSB- case, the settling time is off the scale, ~ 3 µs.
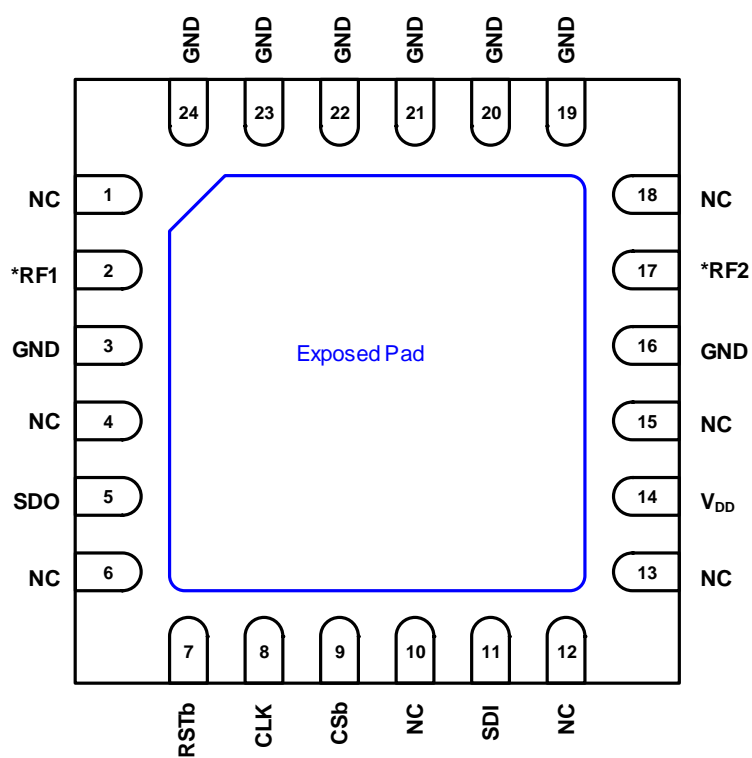
Transient [15.75 to 16.00 (MSB+) *Standard DSA*]
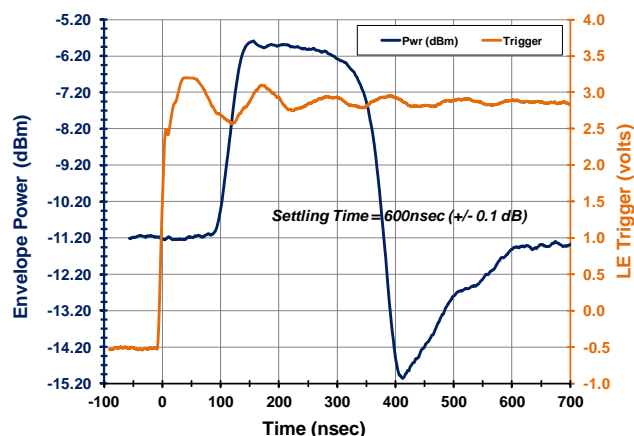
Transient [16.00 to 15.75 (MSB-) *Standard DSA*]
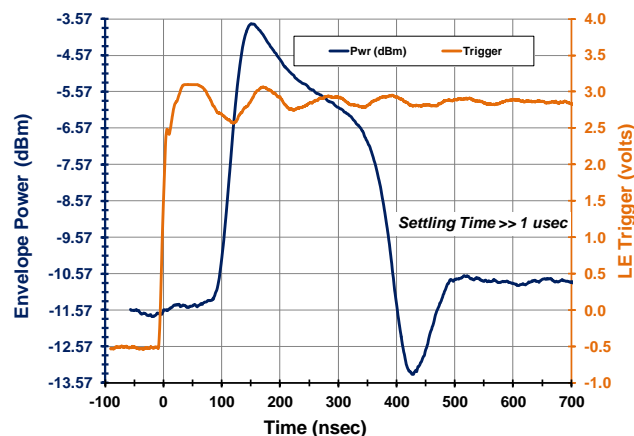
6-bit 0.5 dB Digital Step Attenuator

100 MHz to 4000 MHz

PIN DIAGRAM (F1951)

TOP View
(looking through the top of the package)

Pin diagram, top view.

Top pins (left to right): 24 GND, 23 GND, 22 GND, 21 GND, 20 GND, 19 GND

Left pins (top to bottom):
- 1 — NC
- 2 — *RF1
- 3 — GND
- 4 — NC
- 5 — SDO
- 6 — NC

Right pins (top to bottom):
- 18 — NC
- 17 — *RF2
- 16 — GND
- 15 — NC
- 14 — V$_{DD}$
- 13 — NC

Bottom pins (left to right): 7 RSTb, 8 CLK, 9 CSb, 10 NC, 11 SDI, 12 NC

Exposed Pad

* Device is RF Bi-Directional

6-bit 0.5 dB Digital Step Attenuator

100 MHz to 4000 MHz

PACKAGE DRAWING (4X4MM, 24 PIN)

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/24-vfqfpn-package-outline-drawing-40-x-40-x-075-mm-body-05mm-pitch-epad-26-x-26-mm-nbnbg24p2

6-bit 0.5 dB Digital Step Attenuator　　　　　　　　　　　**100 MHz to 4000 MHz**

PIN DESCRIPTIONS

Pin #	Pin Name	Pin Function
1	NC	No internal connection. These pins can be left unconnected, voltage applied, or connected to ground (recommended).
2	RF1	Device RF input or output (bi-directional). Requires a DC Block.
3	GND	Connect directly to paddle ground or as close as possible to pin with thru via.
4	NC	No internal connection. These pins can be left unconnected, voltage applied, or connected to ground (recommended).
5	SDO	Serial Data Out. Delayed 8 clock cycles from Serial Data In.
6	NC	No internal connection. These pins can be left unconnected, voltage applied, or connected to ground (recommended).
7	RSTb	Reset BAR. Falling Edge resets the device to Max Attenuation [D5:D0] = [000000].
8	CLK	Serial Clock.
9	CSb	Chip Select Bar. Serial Data latched into active register on Rising Edge.
10	NC	No internal connection. These pins can be left unconnected, voltage applied, or connected to ground (recommended).
11	SDI	Serial Data Input.
12	NC	No internal connection. These pins can be left unconnected, voltage applied, or connected to ground (recommended).
13	NC	No internal connection. These pins can be left unconnected, voltage applied, or connected to ground (recommended).
14	VDD	Main Supply. Use 3.3V or 5V. Current is < 1 mA.
15	NC	No internal connection. These pins can be left unconnected, voltage applied, or connected to ground (recommended).
16	GND	Connect directly to paddle ground or as close as possible to pin with thru via.
17	RF2	Device RF output or input (bi-directional). Requires a DC Block.
18	NC	No internal connection. These pins can be left unconnected, voltage applied, or connected to ground (recommended).
19	GND	Connect directly to paddle ground or as close as possible to pin with thru via.
20	GND	Connect directly to paddle ground or as close as possible to pin with thru via.
21	GND	Connect directly to paddle ground or as close as possible to pin with thru via.
22	GND	Connect directly to paddle ground or as close as possible to pin with thru via.
23	GND	Connect directly to paddle ground or as close as possible to pin with thru via.
24	GND	Connect directly to paddle ground or as close as possible to pin with thru via.
EP	Exposed Paddle	Connect to Ground with multiple vias for good thermal relief.

EVKit Schematic

The diagram below describes the recommended applications / EVKit circuit:
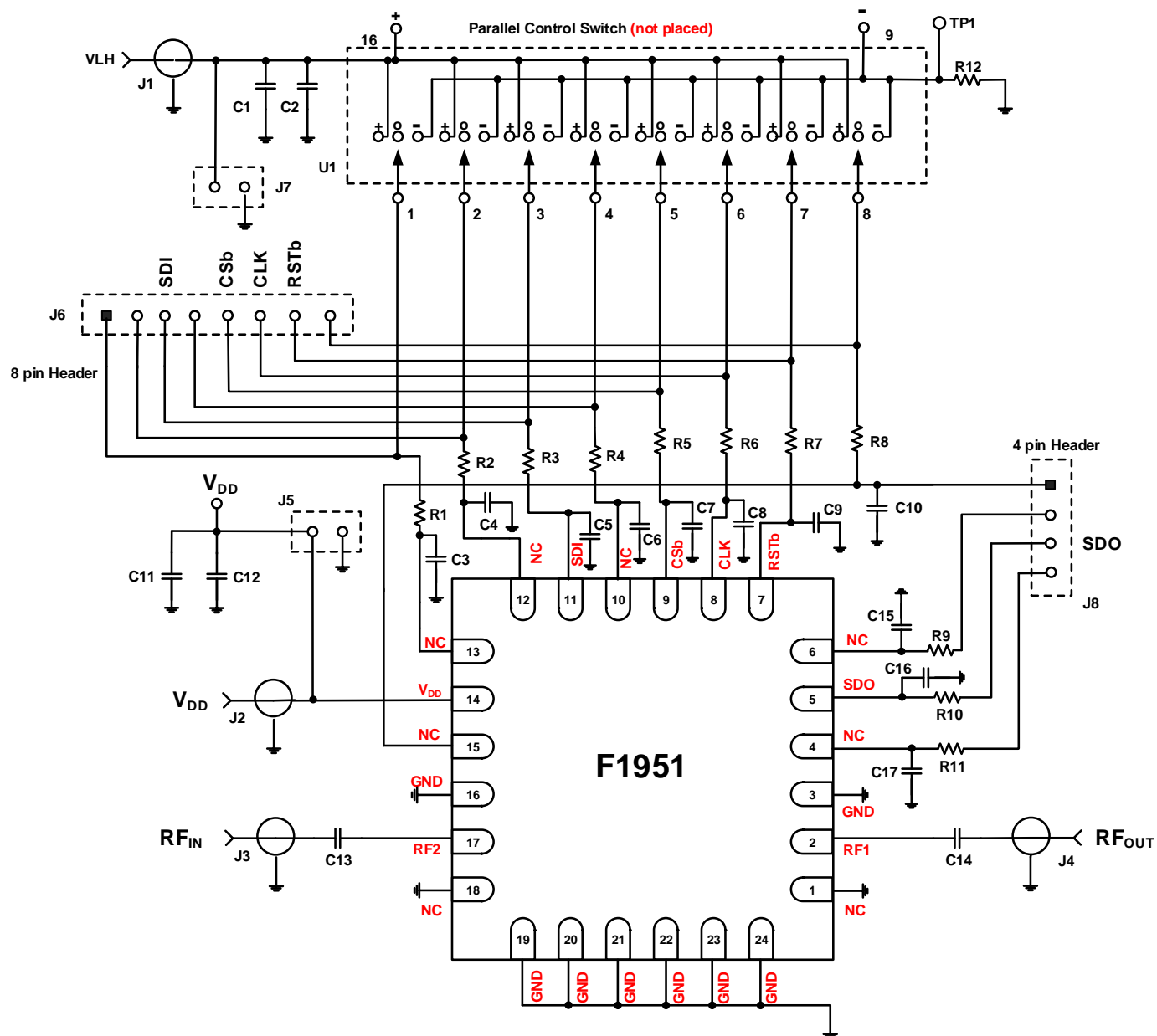
EVKIT OPERATION

(For support, visit www.IDT.com/go/support. To request an EVKit, Serial Control HW/SW, or TRL cal board, please call your local sales engineer or visit www.IDT.com/go/sales.)

The figure below shows the connections for operating the EVKit.

Please note that the RF ports (RF1 and RF2) labels on the evaluation board are reversed. The evaluation board is used for multiple devices.
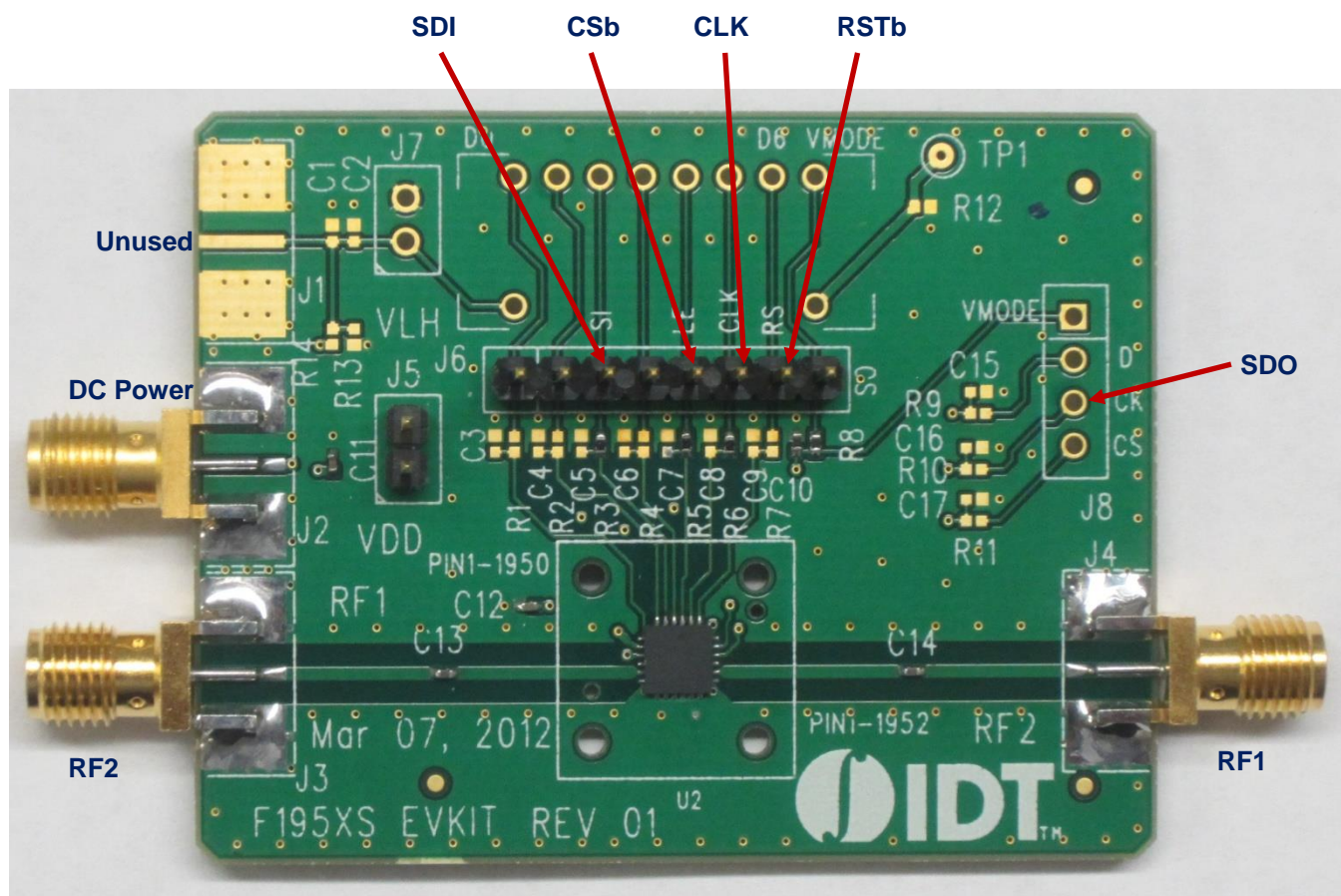
EVKIT BOM

F1951 BOM Rev 02 PCB Rev 01 10/26/2012

Item #	Value	Size	Description	Mfr. Part #	Mfr.	Ref Des	Qty
1	1000pF	0402	CAP CER 1000PF 50V C0G 0402	GRM1555C1H102JA01D	MURATA	C13,14	2
2	10nF	0402	CAP CER 10000PF 16V 10% X7R 0402	GRM155R71C103KA01D	MURATA	C12	1
3	0.1uF	0402	CAP CER 0.1UF 16V 10% X7R 0402	GRM155R71C104KA88D	MURATA	C11	1
4	Header 2 Pin	TH 2	CONN HEADER VERT SGL 2POS GOLD	961102-6404-AR	3M	J5	1
5	Header 4 Pin	TH 4	CONN HEADER VERT SGL 4POS GOLD	961104-6404-AR	3M	J8	1
6	Header 8 Pin	TH 8	CONN HEADER VERT SGL 8POS GOLD	961108-6404-AR	3M	J6	1
7	SMA_END_LAUNCH	.062	SMA_END_LAUNCH (Small)	142-0711-821	Emerson Johnson	J2,3,4	3
8	0	0402	RES 0.0 OHM 1/10W 0402 SMD	ERJ-2GE0R00X	Panasonic	R7,8,10	3
9	3K	0402	RES 3.00K OHM 1/10W 1% 0402 SMD	ERJ-2RKF3001X	Panasonic	R3,5,6	3
10	Digital Step Attenuator		F1951	F1951	IDT	U2	1
11	PCB		PCB Rev 01	F195XS Evkit Rev 01			1

Total   18

TOP MARKINGS

```
F19
51NBGI     ──── Part Number
Z207AGA    ──── Lot Code
●
```
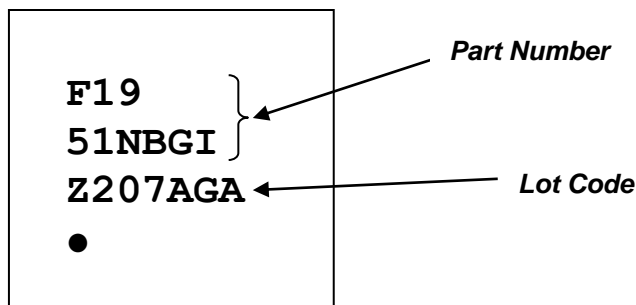
## EVKIT THROUGH-REFLECT-LINE (TRL) CALIBRATION

The "Through-Reflect-Line" (TRL) method [1] is used to de-embed the evaluation board losses from the S-parameter measurements of the F1951. This method requires the use of three standards: a through, a reflection, and a line. The TRL method has the advantage over other calibration methods in that it requires only one of these three standards to be well defined.

The TRL through which is used for the F1951 TRL calibration was constructed identically to the evaluation board, minus the DUT and its corresponding length. Therefore, the through corresponds to a precise zero length connection between the input and output reference planes of the DUT. This through satisfies the requirement of the TRL method that one of the three standards be precisely specified.

The TRL reflection standard used is constructed identically to the input and output lines of the evaluation board, with a short placed at the reference plane of the DUT. In accordance with the TRL method's requirements, the actual magnitude and phase were not accurately specified, but the phase was known to within 90 degrees and the TRL reflection standard has a magnitude close to one.

The TRL line standard is identical to the TRL through, but with an additional length of 0.8 inches (2 cm). This satisfies the TRL method's requirement that the TRL be a different length than the TRL through, that it have the same impedance and propagation constant as the through, and that the phase difference between the through and the line be between 20 degrees and 160 degrees. The difference in length yields a phase difference of approximately 20 degrees at 500 MHz, and a phase difference of 160 degrees at 4 GHz.

For characterization of performance from 150 to 500 MHz a separate TRL board with different "Line" length is used.
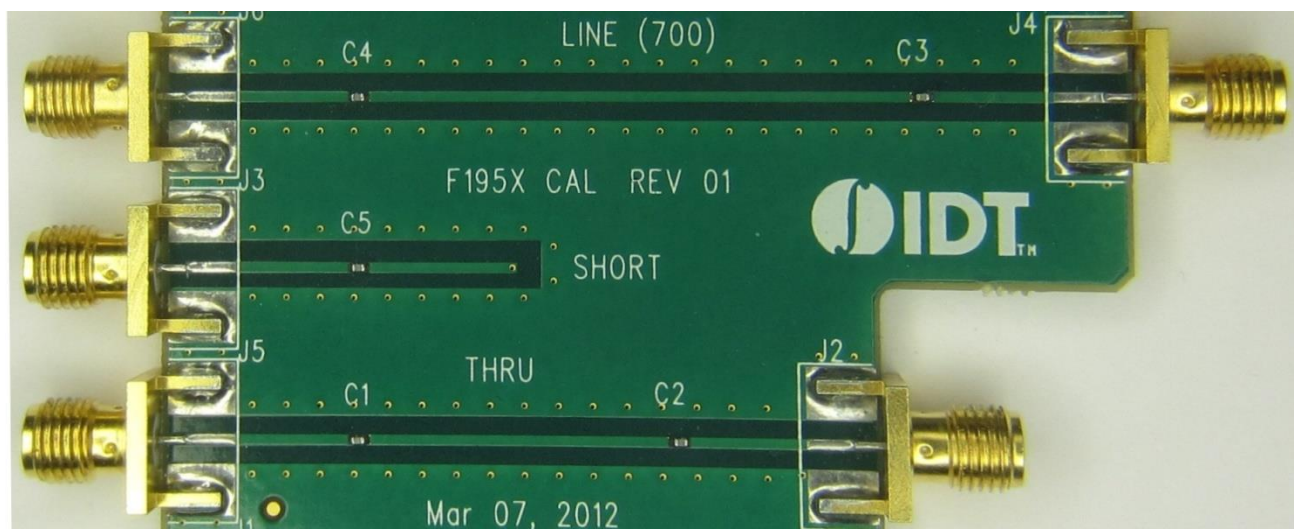
Standards used for F195x TRL calibration
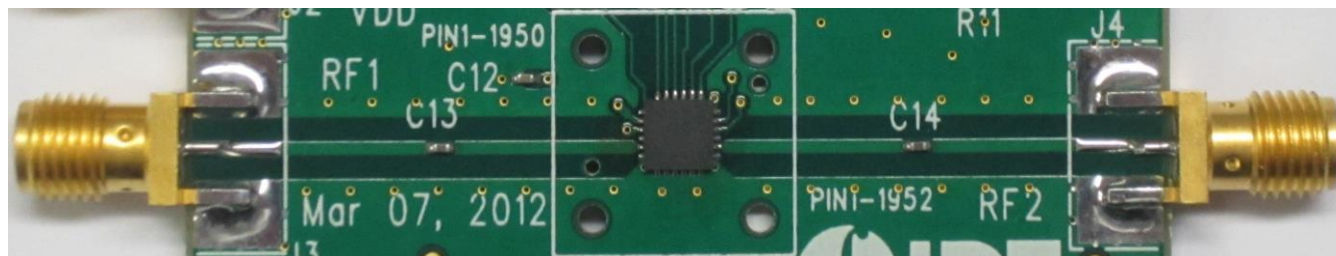
F1951 evaluation circuit

[1] Engen, G.F.; Hoer, C.A.; "Thru-Reflect-Line: An Improved Technique for Calibrating the Dual Six-Port Automatic Network Analyzer," **IEEE Transactions on Microwave Theory and Techniques**, Volume: 27 Issue:12, pp. 987 – 993, Dec 1979.

REVISION HISTORY SHEET

Rev	Date	Page	Description of Change
4	May 10, 2018	1, 3, 5, 12	Removed maximum spec for CSb timing. Revision of voltage supply range on page 1 to match specification table. Revision of the package outline drawing (POD) section to explain that the POD is now given at the end of the document and to provide a link to the POD on the IDT website. POD is now NBG24P2. Revision of references to part name from IDTF1951 to F1951. Minor edits.
3	July 21, 2017	2 4 18	Corrected Absolute Maximum Supply Voltage. Added information about Serial Output Line. Added Revision History Sheet
2	Apil 02, 2014	4	Corrected Timing Decriptions
1	March 20, 2013		Corrected Footer
O	January 15, 2013		Initial Release

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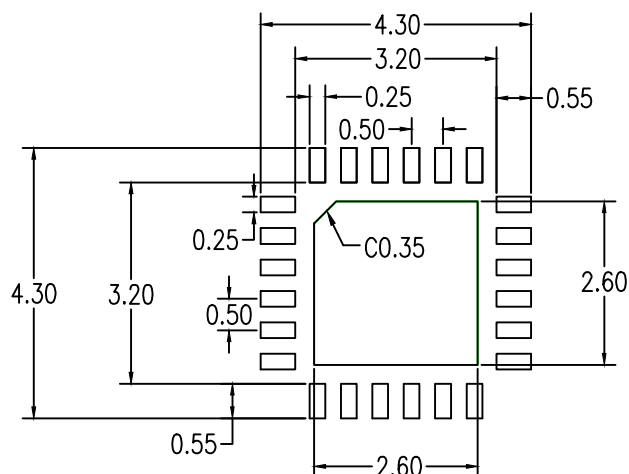**Tech Support**
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TOP VIEW

BOTTOM VIEW

SIDE VIEW

SEATING PLANE

NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M−1994
2. ALL DIMENSONS ARE IN MILLIMETERS
3. INDEX AREA PIN 1 IDENTIFIER

RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M−1994
2. ALL DIMENSONS ARE IN MILLIMETERS
3. LAND PATTERN RECOMMENDATION PER IPC−7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN

Package Revision History		
Date Created	Rev No.	Description
Jan 24, 2018	Rev 01	Change QFN to VFQFPN and New Format
May 11, 2016	Rev 00	Initial Release