

# SN54AS286, SN74AS286 9-BIT PARITY GENERATORS/CHECKERS WITH BUS-DRIVER PARITY I/O PORT

SDAS050B – DECEMBER 1983 – REVISED DECEMBER 1994

- Generate Either Odd or Even Parity for Nine Data Lines
- Cascadable for n-Bit Parity
- Direct Bus Connection for Parity Generation or Checking by Using the Parity I/O Port
- Glitch-Free Bus During Power Up/Down
- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

## description

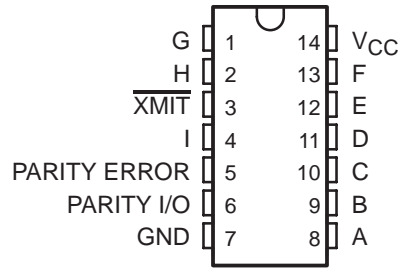
The SN54AS286 and SN74AS286 universal 9-bit parity generators/checkers feature a local output for parity checking and a 48-mA bus-driving parity input/output (I/O) port for parity generation/checking. The word-length capability is easily expanded by cascading.

The transmit ( $\overline{\text{XMIT}}$ ) control input is implemented specifically to accommodate cascading. When  $\overline{\text{XMIT}}$  is low, the parity tree is disabled and PARITY ERROR remains at a high logic level regardless of the input levels. When  $\overline{\text{XMIT}}$  is high, the parity tree is enabled. PARITY ERROR indicates a parity error when either an even number of inputs (A–I) are high and PARITY I/O is forced to a low logic level, or when an odd number of inputs are high and PARITY I/O is forced to a high logic level.

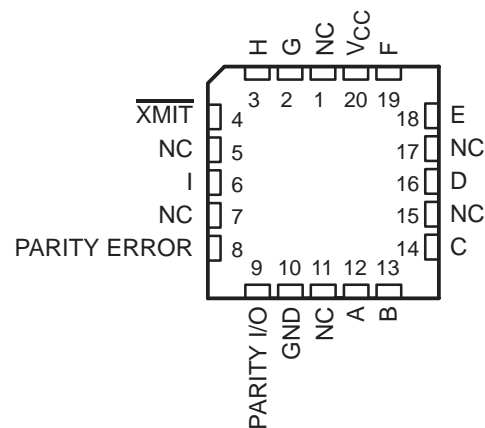
The I/O control circuitry was designed so that the I/O port remains in the high-impedance state during power up or power down to prevent bus glitches.

The SN54AS286 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74AS286 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54AS286 . . . J PACKAGE  
SN74AS286 . . . D OR N PACKAGE  
(TOP VIEW)



SN54AS286 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

NUMBER OF INPUTS (A–I) THAT ARE HIGH	$\overline{\text{XMIT}}$	PARITY I/O	PARITY ERROR
0, 2, 4, 6, 8	l	H	H
1, 3, 5, 7, 9	l	L	H
0, 2, 4, 6, 8	h	h	H
	h	l	L
1, 3, 5, 7, 9	h	h	L
	h	l	H

h = high input level  
H = high output level

l = low input level  
L = low output level

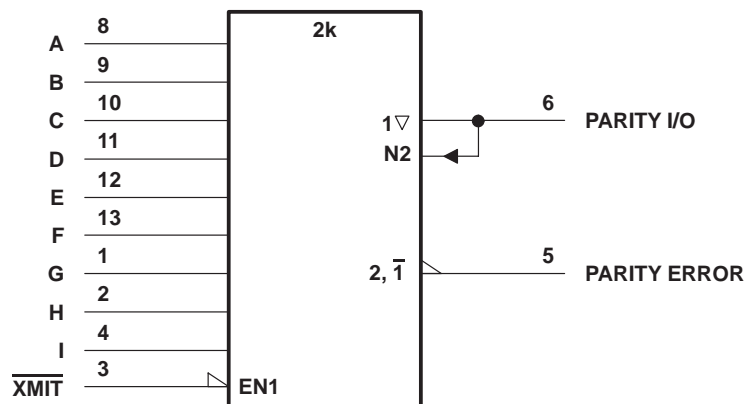
# SN54AS286, SN74AS286

## 9-BIT PARITY GENERATORS/CHECKERS

### WITH BUS-DRIVER PARITY I/O PORT

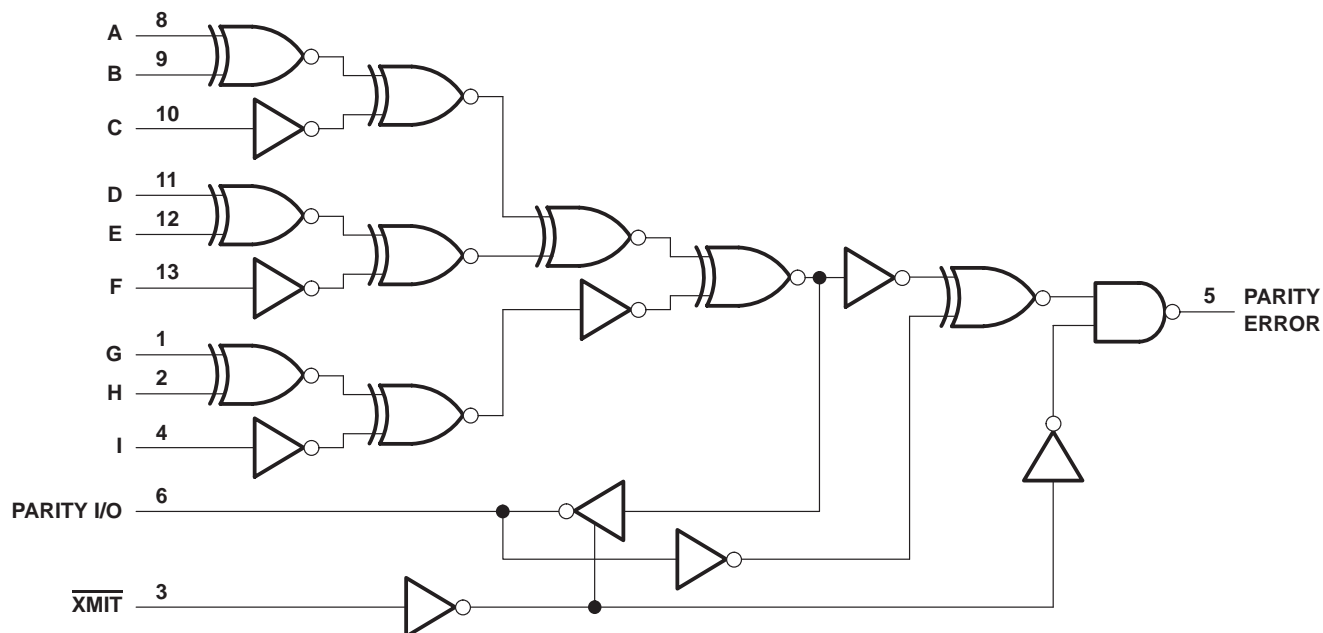
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#### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for the D, J, and N packages.

#### logic diagram (positive logic)



Pin numbers shown are for the D, J, and N packages.

**SN54AS286, SN74AS286**  
**9-BIT PARITY GENERATORS/CHECKERS**  
**WITH BUS-DRIVER PARITY I/O PORT**  
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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, $T_A$ : SN54AS286	–55°C to 125°C
SN74AS286	0°C to 70°C
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**recommended operating conditions**

			SN54AS286			SN74AS286			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage		2			2			V
V <sub>IL</sub>	Low-level input voltage		0.8			0.8			V
I <sub>OH</sub>	High-level output current	PARITY ERROR	−2			−2			mA
		PARITY I/O	−12			−15			
I <sub>OL</sub>	Low-level output current	PARITY ERROR	20			20			mA
		PARITY I/O	32			48			
T <sub>A</sub>	Operating free-air temperature		−55	125		0	70		°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		SN54AS286			SN74AS286			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = –18 mA	–1.2			–1.2			V
V <sub>OH</sub>	All outputs	V <sub>CC</sub> = 4.5 V to 5.5 V,	I <sub>OH</sub> = –2 mA	V <sub>CC</sub> – 2			V <sub>CC</sub> – 2			V
	PARITY I/O	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = –3 mA	2.4	2.9		2.4	3		
			I <sub>OH</sub> = –12 mA	2.4						
			I <sub>OH</sub> = –15 mA			2.4				
V <sub>OL</sub>	PARITY ERROR	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 20 mA	0.35	0.5		0.35	0.5	V	
	PARITY I/O		I <sub>OL</sub> = 32 mA		0.5					
			I <sub>OL</sub> = 48 mA			0.5				
I <sub>I</sub>	PARITY I/O	V <sub>CC</sub> = 5.5 V	V <sub>I</sub> = 5.5 V		0.1		0.1	mA		
	All other inputs		V <sub>I</sub> = 7 V		0.1		0.1			
I <sub>IH</sub>	PARITY I/O§	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V		50		50	µA		
	All other inputs				20		20			
I <sub>IL</sub>	PARITY I/O§	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.4 V		–0.5		–0.5	mA		
	All other inputs				–0.5		–0.5			
I <sub>O</sub> ¶		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.25 V	–30	–112		–30	–112	mA	
I <sub>CC</sub>	Transmit	V <sub>CC</sub> = 5.5 V		30	43		30	43	mA	
	Receive			35	50		35	50		

‡ All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

§ For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

¶ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .



# SN54AS286, SN74AS286

## 9-BIT PARITY GENERATORS/CHECKERS

### WITH BUS-DRIVER PARITY I/O PORT

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#### switching characteristics (see Figure 3)

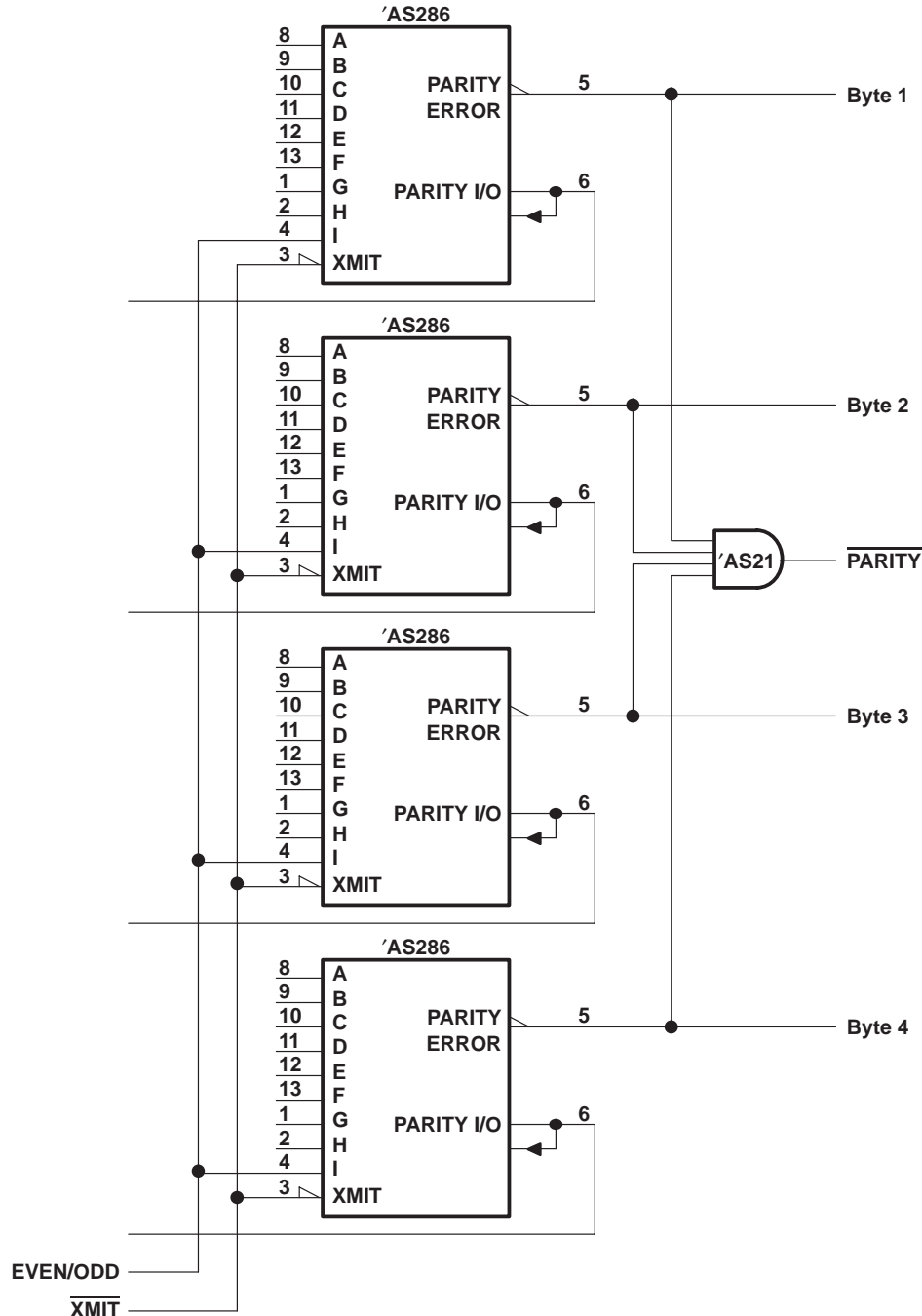
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 500 Ω, R <sub>2</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX†				UNIT
			SN54AS286		SN74AS286		
			MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	Any A – I	PARITY I/O	3	17	3	15	ns
t <sub>PHL</sub>			3	15	3	14	
t <sub>PLH</sub>	Any A – I	PARITY ERROR	3	20	3	16.5	ns
t <sub>PHL</sub>			3	18	3	16.5	
t <sub>PLH</sub>	PARITY I/O	PARITY ERROR	3	10	3	9	ns
t <sub>PHL</sub>			3	10	3	9	
t <sub>PZH</sub>	$\overline{\text{XMIT}}$	PARITY I/O	3	14	3	13	ns
t <sub>PZL</sub>			3	17	3	16	
t <sub>PHZ</sub>	$\overline{\text{XMIT}}$	PARITY I/O	3	13	3	11.5	ns
t <sub>PLZ</sub>			3	11	3	10	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



## APPLICATION INFORMATION

Figure 1 shows a 32-bit parity generator/checker with output polarity switching, parity-error detection, and parity on every byte.



Pin numbers shown are for the D, J, and N packages.

**Figure 1. 32-Bit Parity Generator/Checker**

# SN54AS286, SN74AS286

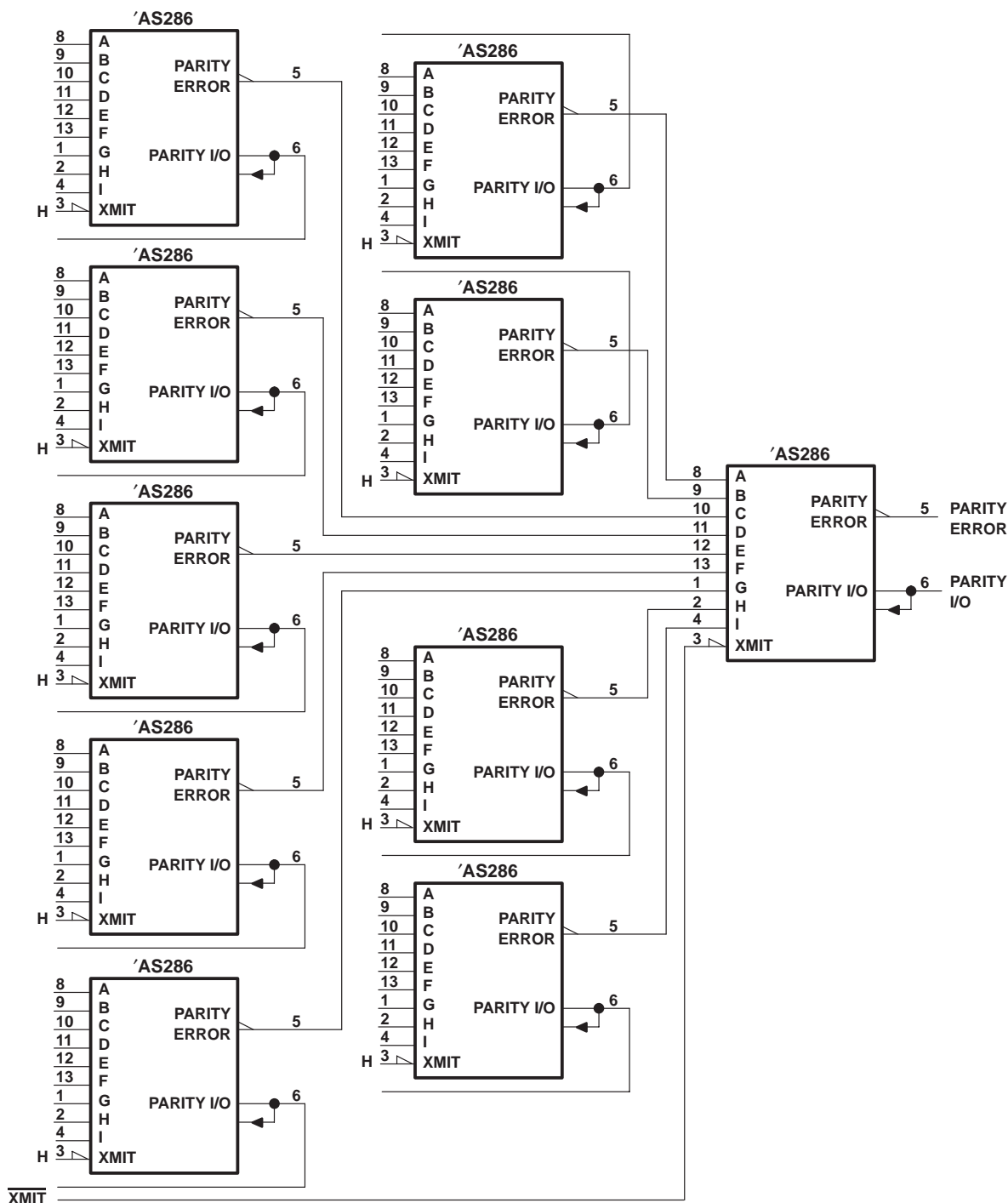
## 9-BIT PARITY GENERATORS/CHECKERS

### WITH BUS-DRIVER PARITY I/O PORT

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#### APPLICATION INFORMATION

Figure 2 shows a 90-bit parity generator/checker with  $\overline{\text{XMIT}}$  on the last stage available for use with parity detection.



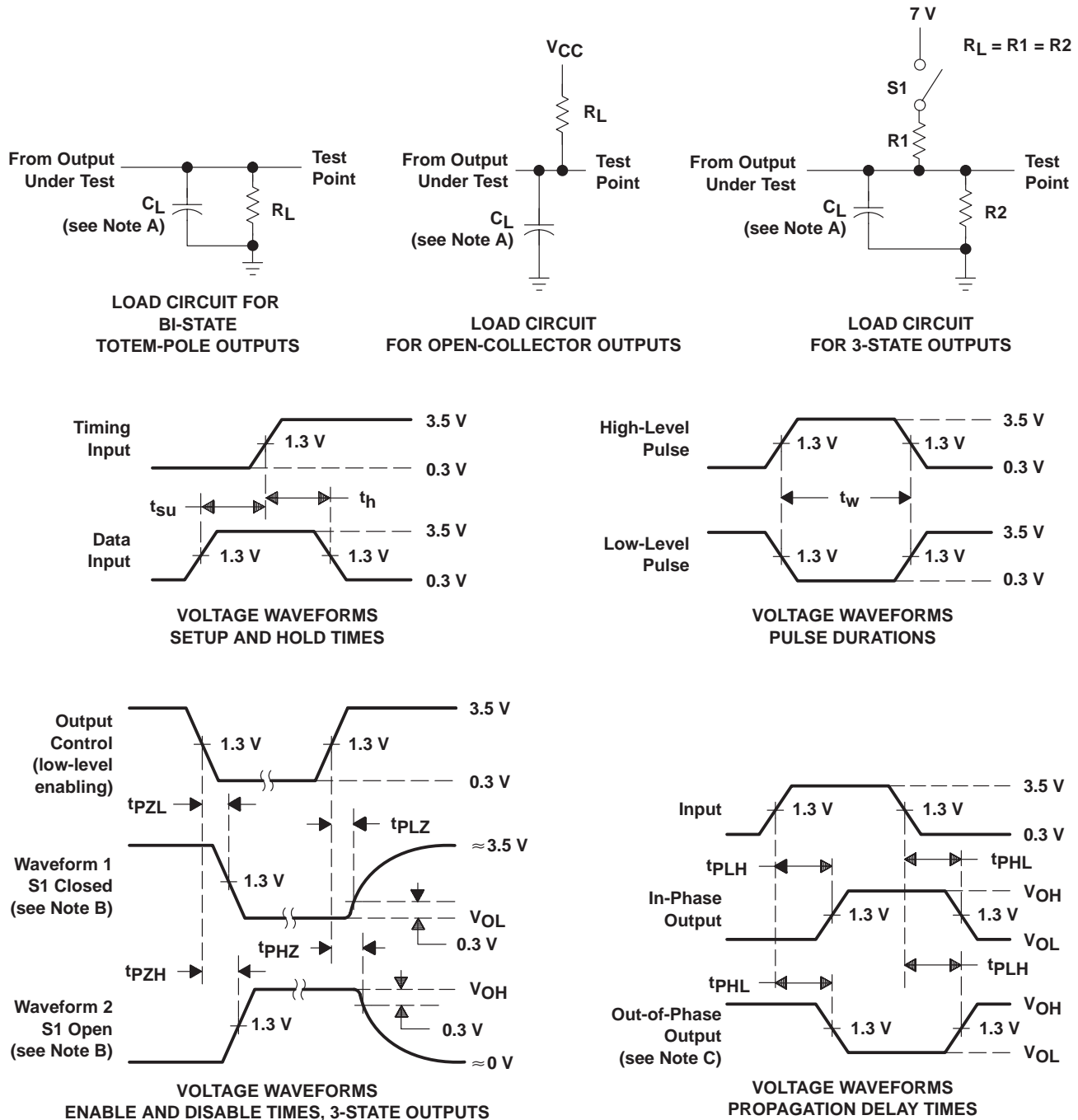
Pin numbers shown are for the D, J, and N packages.

**Figure 2. 90-Bit Parity Generator/Checker With Parity-Error Detection**



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265  
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251-1443

## PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
E. The outputs are measured one at a time with one transition per measurement.

**Figure 3. Load Circuits and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
5962-8966301CA	ACTIVE	CDIP	J	14		TBD	Call TI	Call TI	-55 to 125		<a href="#">Samples</a>
SN54AS286J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	-55 to 125		
SN74AS286D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AS286	<a href="#">Samples</a>
SN74AS286DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AS286	<a href="#">Samples</a>
SN74AS286DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AS286	<a href="#">Samples</a>
SN74AS286DR	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70	AS286	
SN74AS286DRE4	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70		
SN74AS286DRG4	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70		
SN74AS286N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74AS286N	<a href="#">Samples</a>
SN74AS286NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74AS286N	<a href="#">Samples</a>
SNJ54AS286FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



<sup>(4)</sup> Only one of markings shown within the brackets will appear on the physical device.

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**OTHER QUALIFIED VERSIONS OF SN54AS286, SN74AS286 :**

- Catalog: [SN74AS286](#)
- Military: [SN54AS286](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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### Applications

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