DG408, DG409

Single 8-Channel/Differential 4-Channel, CMOS Analog Multiplexers

FN3283
Rev 8.00
Jun 13, 2006

The DG408 Single 8-Channel, and DG409 Differential 4-Channel monolithic CMOS analog multiplexers are drop-in replacements for the popular DG508A and DG509A series devices. They each include an array of eight analog switches, a TTL/CMOS compatible digital decode circuit for channel selection, a voltage reference for logic thresholds and an ENABLE input for device selection when several multiplexers are present.

The DG408 and DG409 feature lower signal ON resistance (<100Ω) and faster switch transition time (t_{TRANS} < 250ns) compared to the DG508A or DG509A. Charge injection has been reduced, simplifying sample and hold applications. The improvements in the DG408 series are made possible by using a high-voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. Power supplies may be single-ended from +5V to +34V, or split from ±5V to ±20V.

The analog switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a ±5V analog input range.

Features

- ON Resistance (Max, 25°C) 100Ω
- Low Power Consumption (P_D) . . . . . <11mW
- Fast Switching Action
  - t_{TRANS} . . . . . <250ns
  - $t_{ON/OFF(EN)}$ . . . . . <150ns
- Low Charge Injection
- Upgrade from DG508A/DG509A
- TTL, CMOS Compatible
- Single or Split Supply Operation
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Data Acquisition Systems
- Audio Switching Systems
- Automatic Testers
- Hi-Rel Systems
- Sample and Hold Circuits
- Communication Systems
- Analog Selector Switch

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
DG408DJ	DG408DJ	-40 to 85	16 Ld PDIP	E16.3
DG408DJZ (Note)	DG408DJZ	-40 to 85	16 Ld PDIP** (Pb-free)	E16.3
DG408DY*	DG408DY	-40 to 85	16 Ld SOIC	M16.15
DG408DYZ* (Note)	DG408DYZ	-40 to 85	16 Ld SOIC (Pb-free)	M16.15
DG408DVZ* (Note)	DG408DVZ	-40 to 85	16 Ld TSSOP (Pb-free)	M16.173
DG409DJ	DG409DJ	-40 to 85	16 Ld PDIP	E16.3
DG409DJZ (Note)	DG409DJZ	-40 to 85	16 Ld PDIP** (Pb-free)	E16.3
DG409DY*	DG409DY	-40 to 85	16 Ld SOIC	M16.15
DG409DYZ* (Note)	DG409DYZ	-40 to 85	16 Ld SOIC (Pb-free)	M16.15
DG409DVZ* (Note)	DG409DVZ	-40 to 85	16 Ld TSSOP (Pb-free)	M16.173

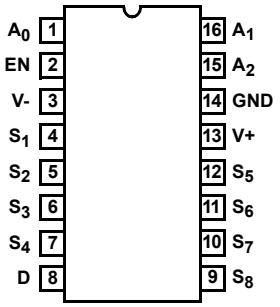
*Add "-T" suffix for tape and reel.

**Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

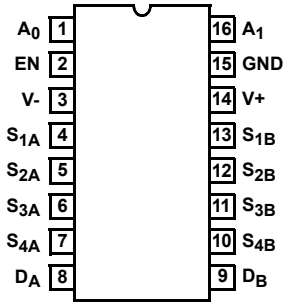
NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinouts

DG408 (PDIP, SOIC, TSSOP)
TOP VIEW

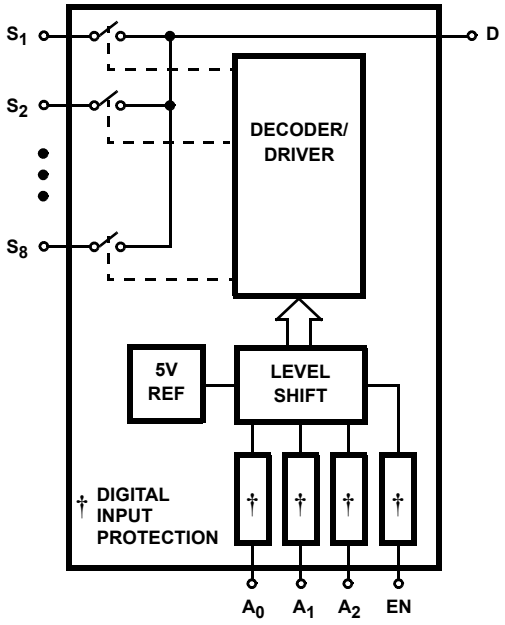


DG409 (PDIP, SOIC, TSSOP)
TOP VIEW

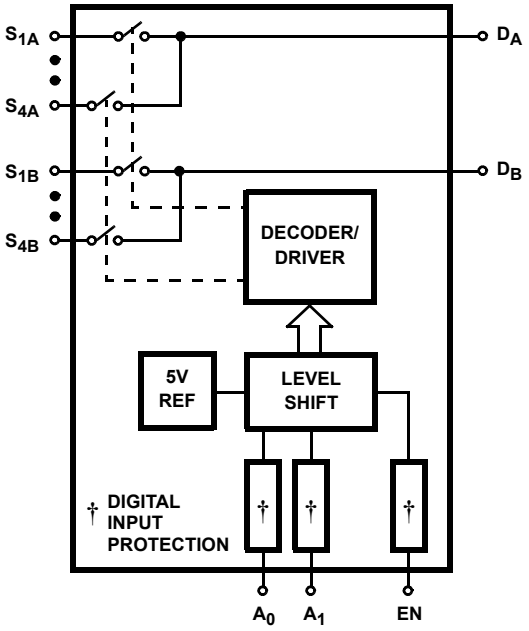


Functional Block Diagrams

DG408



DG409



TRUTH TABLE DG408

A_2	A_1	A_0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

TRUTH TABLE DG409

A_1	A_0	EN	ON SWITCH
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

NOTES:

1. V_{AH} Logic “1” ≥2.4V.
2. V_{AL} Logic “0” ≤0.8V.

Pin Descriptions - (DG408)

PIN	SYMBOL	DESCRIPTION
1	A_0	Logic Decode Input (Bit 0, LSB)
2	EN	Enable Input
3	V-	Negative Power Supply Terminal
4	S_1	Source (Input) for Channel 1
5	S_2	Source (Input) for Channel 2
6	S_3	Source (Input) for Channel 3
7	S_4	Source (Input) for Channel 4
8	D	Drain (Output)
9	S_8	Source (Input) for Channel 8
10	S_7	Source (Input) for Channel 7
11	S_6	Source (Input) for Channel 6
12	S_5	Source (Input) for Channel 5
13	V+	Positive Power Supply Terminal (Substrate)
14	GND	Ground Terminal (Logic Common)
15	A_2	Logic Decode Input (Bit 2, MSB)
16	A_1	Logic Decode Input (Bit 1)

Pin Descriptions - (DG409)

PIN	SYMBOL	DESCRIPTION
1	A_0	Logic Decode Input (Bit 0, LSB)
2	EN	Enable Input
3	V-	Negative Power Supply Terminal
4	S_{1A}	Source (Input) for Channel 1a
5	S_{2A}	Source (Input) for Channel 2a
6	S_{3A}	Source (Input) for Channel 3a
7	S_{4A}	Source (Input) for Channel 4a
8	D_A	Drain a (Output a)
9	D_B	Drain b (Output b)
10	S_{4B}	Source (Input) for Channel 4b
11	S_{3B}	Source (Input) for Channel 3b
12	S_{2B}	Source (Input) for Channel 2b
13	S_{1B}	Source (Input) for Channel 1b
14	V+	Positive Power Supply Terminal
15	GND	Ground Terminal (Logic Common)
16	A_1	Logic Decode Input (Bit 1, MSB)

Absolute Maximum Ratings

V+ to V- 44.0V
GND to V-. 25V
Digital Inputs, V_S, V_D (Note 3). . . . . .(V-) -2V to (V+) + 2V or 20mA, Whichever Occurs First
Continuous Current (Any Terminal) 30mA
Peak Current, S or D (Pulsed 1ms, 10% Duty Cycle Max) . . 100mA

Operating Conditions

Temperature Range . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 4)	θ_{JA} (°C/W)
PDIP Package	90
SOIC Package	110
TSSOP Package	150

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 125°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC and TSSOP - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

3. Signals on S_X, D_X, EN or A_X exceeding V+ or V- are clamped by internal diodes. Limit diode current to maximum current ratings.
4. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Test Conditions: V+ = +15V, V- = -15V, V_{AL} = 0.8V, V_{AH} = 2.4V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 5) MIN	(NOTE 6) TYP	(NOTE 5) MAX	UNITS
DYNAMIC CHARACTERISTICS						
Transition Time, t_{TRANS}	(See Figure 1)	Full	-	160	250	ns
Break-Before-Make Interval, t_{OPEN}	(See Figure 3)	25	10	-	-	ns
Enable Turn-ON Time, $t_{ON(EN)}$	(See Figure 2)	25	-	115	150	ns
		Full	-	-	225	ns
Enable Turn-OFF Time, $t_{OFF(EN)}$	(See Figure 2)	Full	-	105	150	ns
Charge Injection, Q	C_L = 10nF, V_S = 0V	25	-	20	-	pC
OFF Isolation	V_{EN} = 0V, R_L = 1kΩ, f = 100kHz (Note 9)	25	-	-75	-	dB
Logic Input Capacitance, C_{IN}	f = 1MHz	25	-	8	-	pF
Source OFF Capacitance, $C_{S(OFF)}$	V_{EN} = 0V, V_S = 0V, f = 1MHz	25	-	3	-	pF
Drain OFF Capacitance, $C_{D(OFF)}$ DG408	V_{EN} = 0V, V_D = 0V, f = 1MHz	25	-	26	-	pF
DG409		25	-	14	-	pF
Drain ON Capacitance, $C_{D(ON)}$ DG408	V_{EN} = 3V, V_D = 0V, f = 1MHz, V_A = 0V or 3V	25	-	37	-	pF
DG409		25	-	25	-	pF
DIGITAL INPUT CHARACTERISTICS						
Logic Input Current, Input Voltage High, I_{AH}	V_A = 2.4V, 15V	Full	-10	-	10	µA
Logic Input Current, Input Voltage Low, I_{AL}	V_{EN} = 0V, 2.4V, V_A = 0V	Full	-10	-	10	µA
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	-15	-	15	V
Drain-Source ON Resistance, $r_{DS(ON)}$	V_D = ±10V, I_S = -10mA (Note 7)	25	-	40	100	Ω
		Full	-	-	125	Ω
$r_{DS(ON)}$ Matching Between Channels, $\Delta r_{DS(ON)}$	V_D = 10V, -10V (Note 8)	25	-	-	15	Ω
Source OFF Leakage Current, $I_{S(OFF)}$	V_{EN} = 0V, V_S = ±10V, V_D = ∓10V	25	-0.5	-	0.5	nA
		Full	-5	-	5	nA

Electrical Specifications Test Conditions: V+ = +15V, V- = -15V, V_{AL} = 0.8V, V_{AH} = 2.4V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 5) MIN	(NOTE 6) TYP	(NOTE 5) MAX	UNITS
Drain OFF Leakage Current, $I_{D(OFF)}$ DG408	V_{EN} = 0V, V_D = ±10V, V_S = ∓10V	25	-1	-	1	nA
		Full	-20	-	20	nA
DG409		25	-1	-	1	nA
		Full	-10	-	10	nA
Drain ON Leakage Current, $I_{D(ON)}$ DG408	V_S = V_D = ±10V (Note 7)	25	-1	-	1	nA
		Full	-20	-	20	nA
DG409		25	-1	-	1	nA
		Full	-10	-	10	nA
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V_{EN} = 0V, V_A = 0V (Standby)	Full	-	10	75	µA
Negative Supply Current, I-		Full	-75	1	-	µA
Positive Supply Current, I+	V_{EN} = 2.4V, V_A = 0V (Enabled)	25	-	0.2	0.5	mA
		Full	-	-	2	mA
Negative Supply Current, I-		Full	-500	-	-	µA

Electrical Specifications Single Supply Test Conditions: V+ = 12V, V- = 0V, V_{AL} = 0.8V, V_{AH} = 2.4V, Unless Otherwise Specified

PARAMETER	TEST CONDITION	TEMP (°C)	(NOTE 5) MIN	(NOTE 6) TYP	(NOTE 5) MAX	UNITS
DYNAMIC CHARACTERISTICS						
Switching Time of Multiplexer, t_{TRANS}	V_{S1} = 8V, V_{S8} = 0V, V_{IN} = 2.4V	25	-	180	-	ns
Enable Turn-ON Time, $t_{ON(EN)}$	V_{INH} = 2.4V, V_{INL} = 0V, V_{S1} = 5V	25	-	180	-	ns
Enable Turn-OFF Time, $t_{OFF(EN)}$		25	-	120	-	ns
Charge Injection, Q	C_L = 10nF, V_{GEN} = 0V, R_{GEN} = 0Ω	25	-	5	-	pC
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	12	V
Drain-Source ON-Resistance, $r_{DS(ON)}$	V_D = 3V, 10V, I_S = -1mA (Note 7)	25	-	90	-	Ω

NOTES:

5. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
6. Typical values are for DESIGN AID ONLY, not guaranteed nor production tested.
7. Sequence each switch ON.
8. $\Delta r_{DS(ON)} = r_{DS(ON)}$ (Max) - $r_{DS(ON)}$ (Min).
9. Worst case isolation occurs on channel 4 due to proximity to the drain pin.

Test Circuits and Waveforms

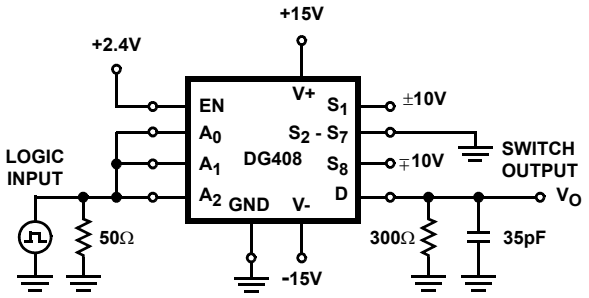


FIGURE 1A. DG408 TEST CIRCUIT

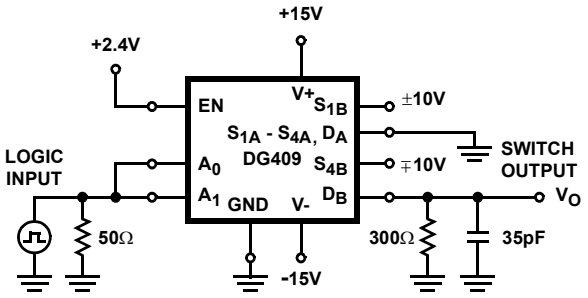


FIGURE 1B. DG409 TEST CIRCUIT

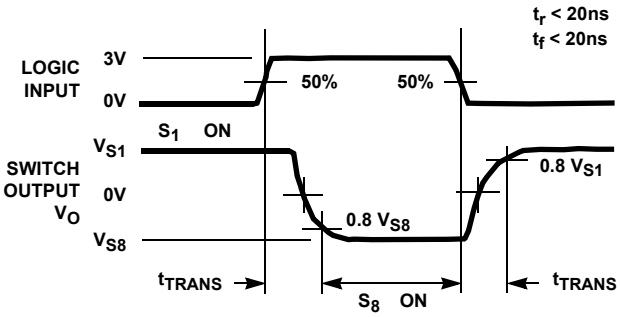


FIGURE 1C. MEASUREMENT POINTS

FIGURE 1. TRANSITION TIME

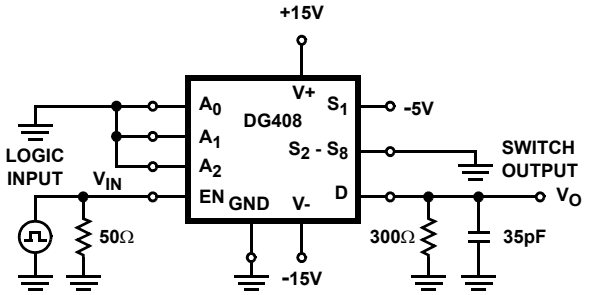


FIGURE 2A. DG408 TEST CIRCUIT

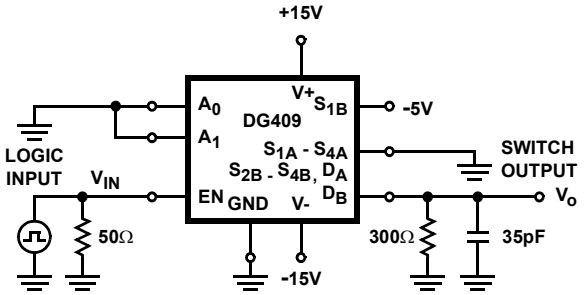


FIGURE 2B. DG409 TEST CIRCUIT

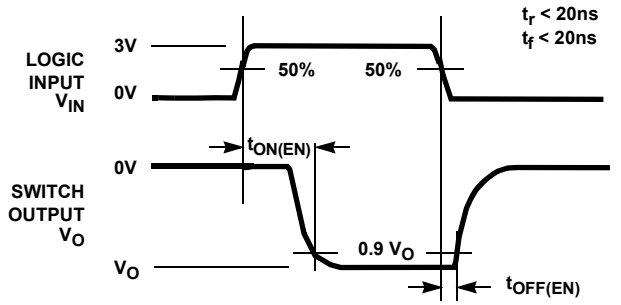


FIGURE 2C. MEASUREMENT POINTS

FIGURE 2. ENABLE SWITCHING TIMES

Test Circuits and Waveforms (Continued)

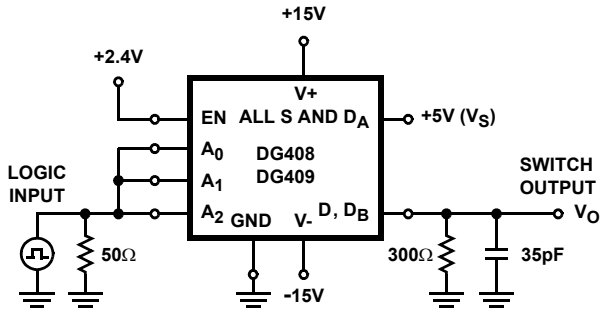


FIGURE 3A. TEST CIRCUIT

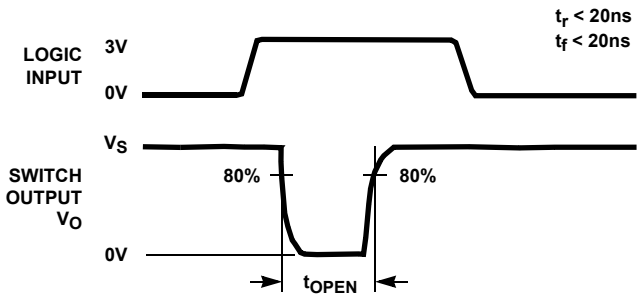


FIGURE 3B. MEASUREMENT POINTS

FIGURE 3. BREAK-BEFORE-MAKE INTERVAL

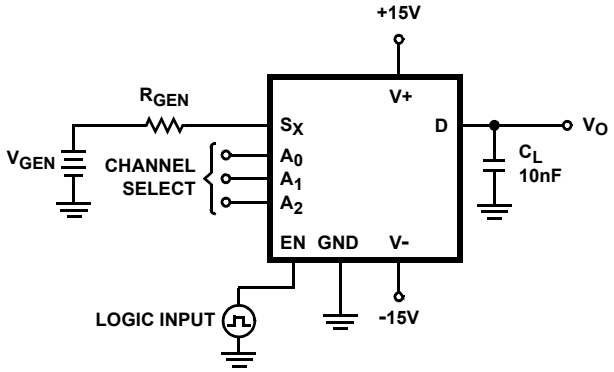


FIGURE 4A. TEST CIRCUIT

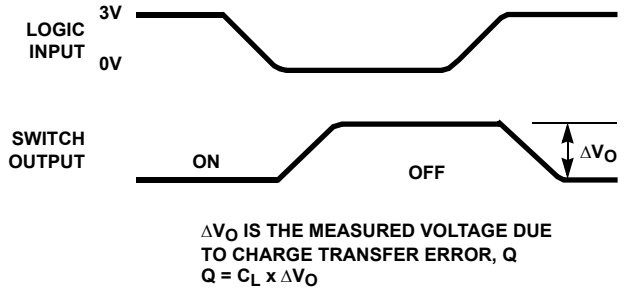


FIGURE 4B. MEASUREMENT POINTS

FIGURE 4. CHARGE INJECTION

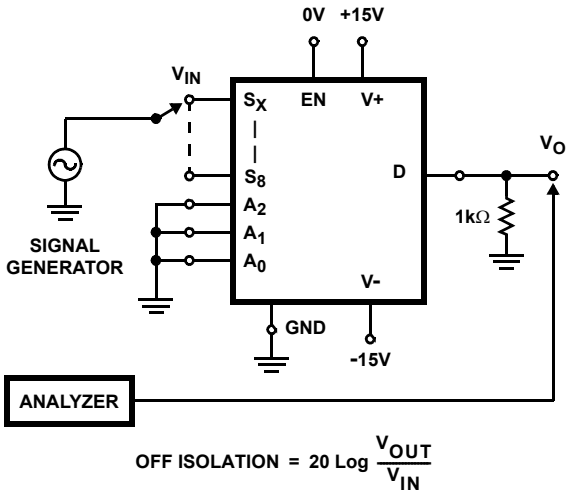


FIGURE 5. OFF ISOLATION

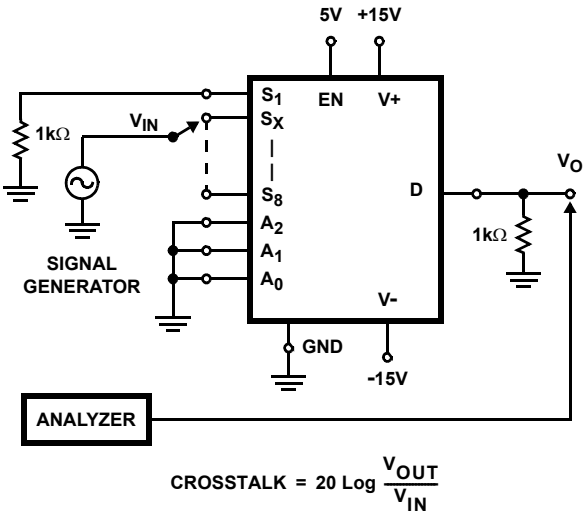


FIGURE 6. CROSSTALK

Test Circuits and Waveforms (Continued)

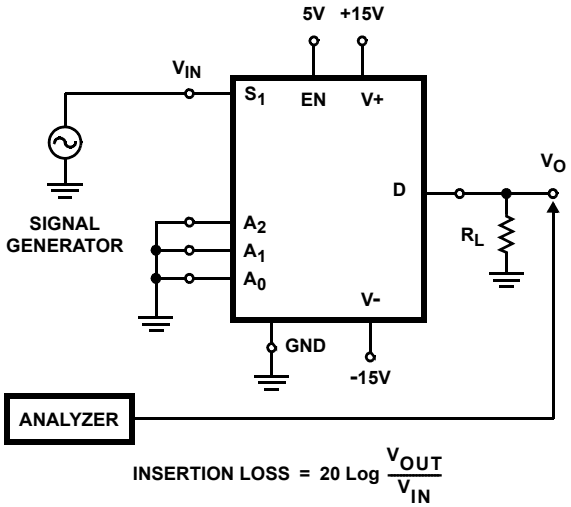


FIGURE 7. INSERTION LOSS

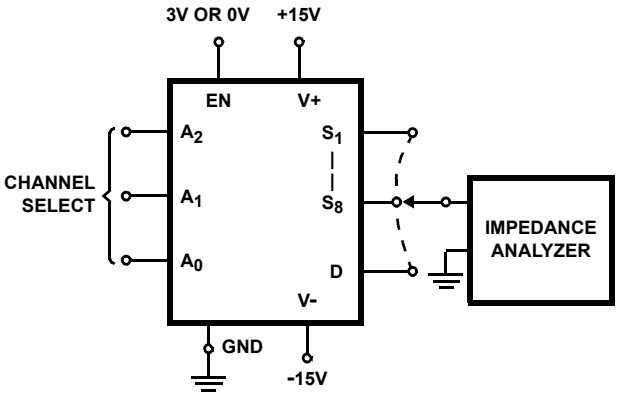


FIGURE 8. SOURCE/DRAIN CAPACITANCES

Typical Applications

Overvoltage Protection

A very convenient form of overvoltage protection consists of adding two small signal diodes (1N4148, 1N914 type) in series with the supply pins (see Figure 9). This arrangement effectively blocks the flow of reverse currents. It also floats the supply pin above or below the normal V+ or V- value. In this case the overvoltage signal actually becomes the power supply of the IC. From the point of view of the chip, nothing has changed, as long as the difference V+ - (V-) doesn't exceed 44V. The addition of these diodes will reduce the analog signal range to 1V below V+ and 1V above V-, but it preserves the low channel resistance and low leakage characteristics.

Typical application information is for Design Aid Only, not guaranteed and not subject to production testing.

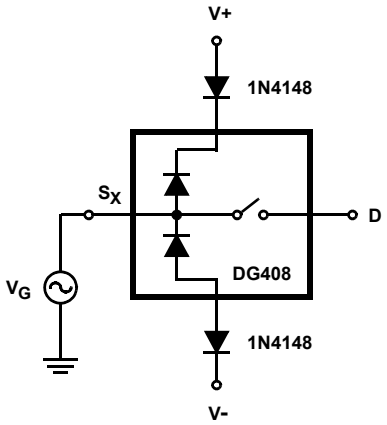


FIGURE 9. OVERVOLTAGE PROTECTION USING BLOCKING DIODES

Typical Performance Curves

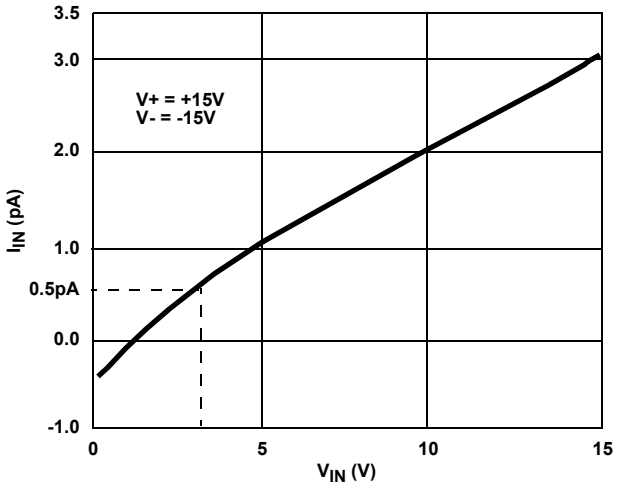


FIGURE 10. INPUT LOGIC CURRENT vs LOGIC INPUT VOLTAGE

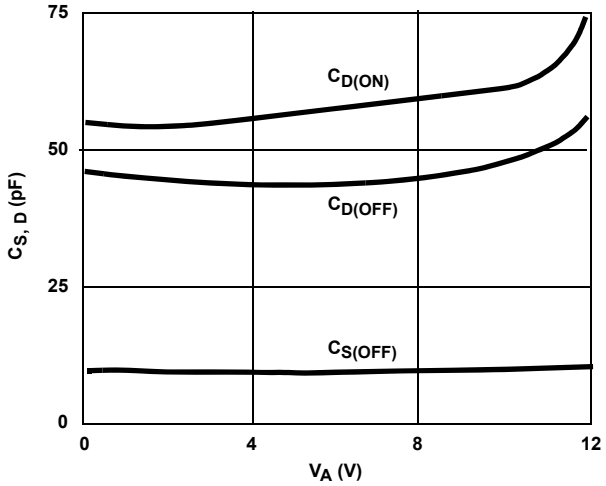


FIGURE 11. SOURCE/DRAIN CAPACITANCE vs ANALOG VOLTAGE (SINGLE 12V SUPPLY)

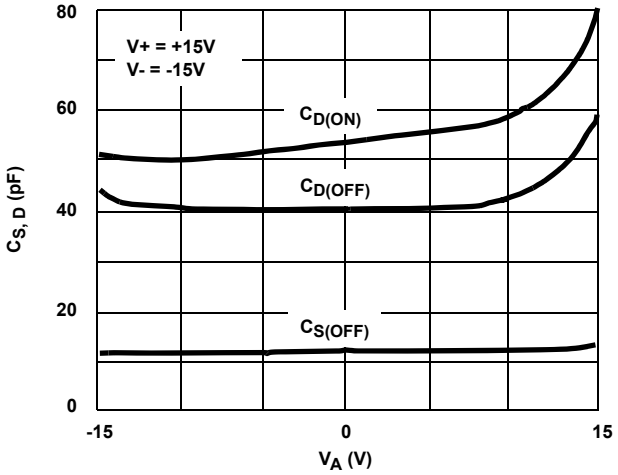


FIGURE 12. SOURCE/DRAIN CAPACITANCE vs ANALOG VOLTAGE

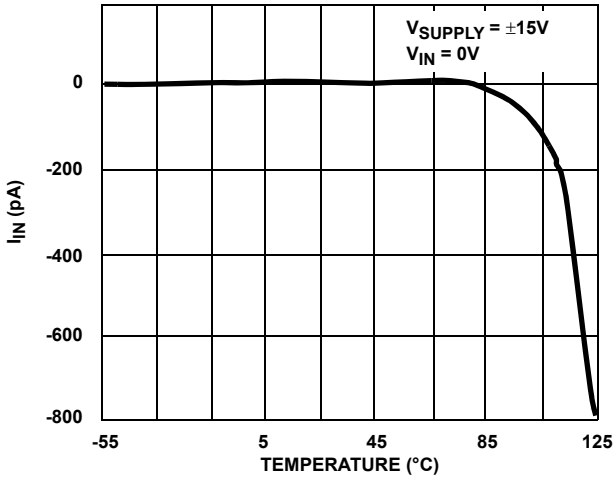


FIGURE 13. LOGIC INPUT CURRENT vs TEMPERATURE

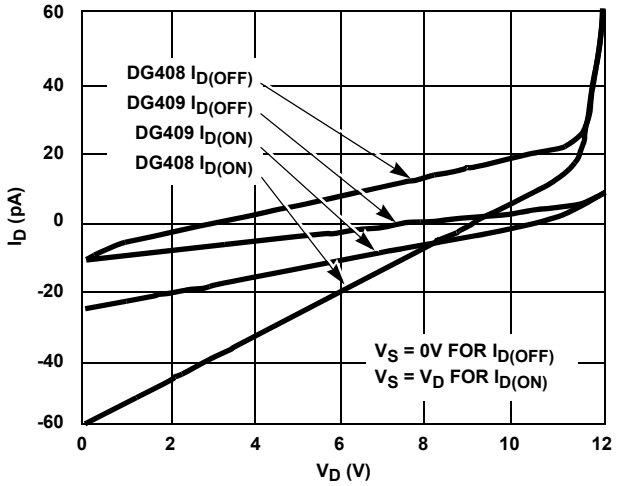


FIGURE 14. DRAIN LEAKAGE CURRENT vs SOURCE/DRAIN VOLTAGE (SINGLE 12V SUPPLY)

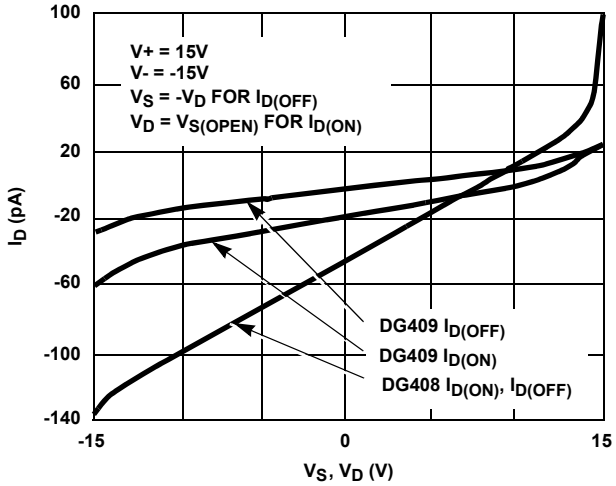


FIGURE 15. DRAIN LEAKAGE CURRENT vs SOURCE/DRAIN VOLTAGE

Typical Performance Curves (Continued)

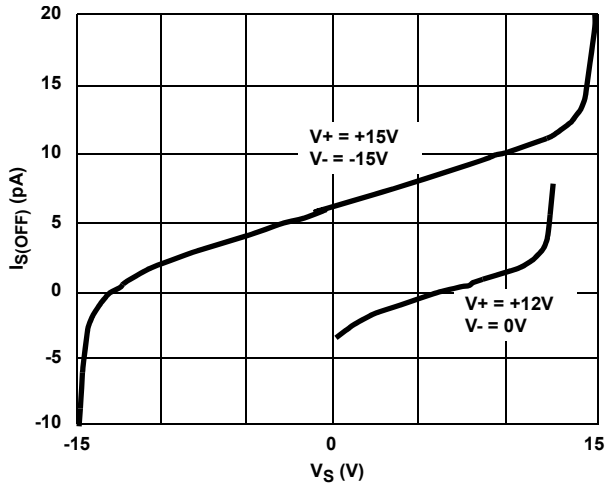


FIGURE 16. SOURCE LEAKAGE CURRENT vs SOURCE VOLTAGE

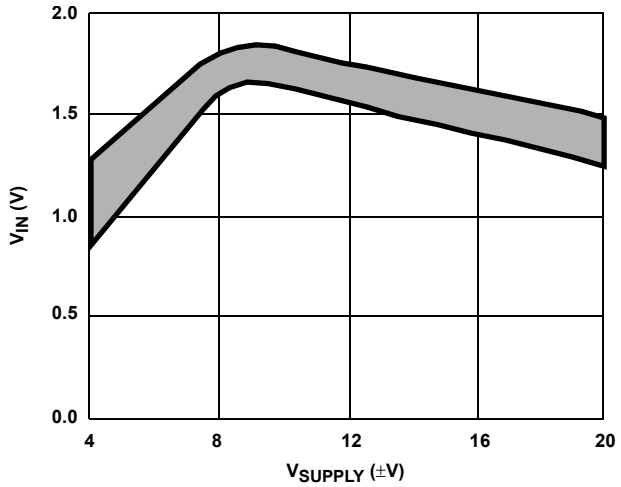


FIGURE 17. INPUT SWITCHING THRESHOLD vs SUPPLY VOLTAGE

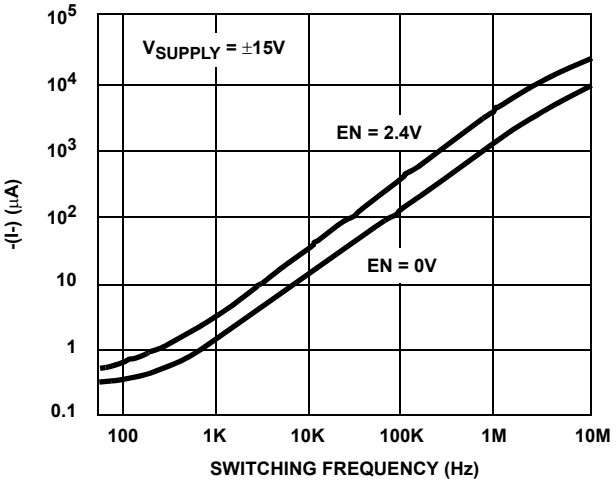


FIGURE 18. NEGATIVE SUPPLY CURRENT vs SWITCHING FREQUENCY

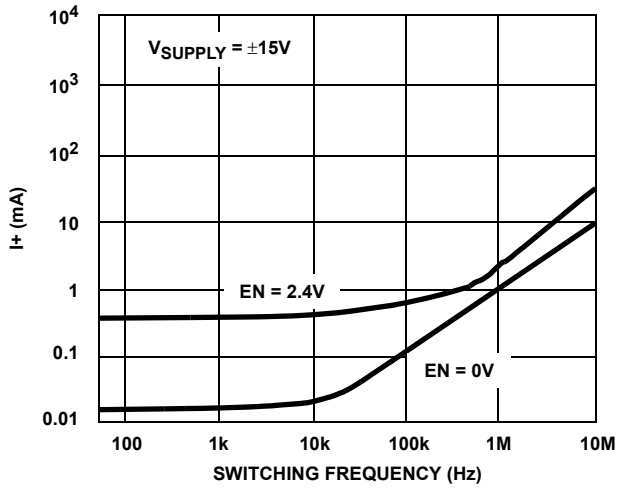


FIGURE 19. POSITIVE SUPPLY CURRENT vs SWITCHING FREQUENCY

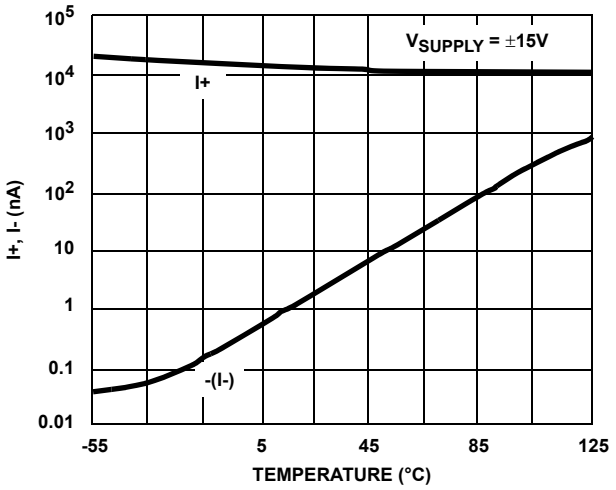


FIGURE 20. I_{SUPPLY} vs TEMPERATURE

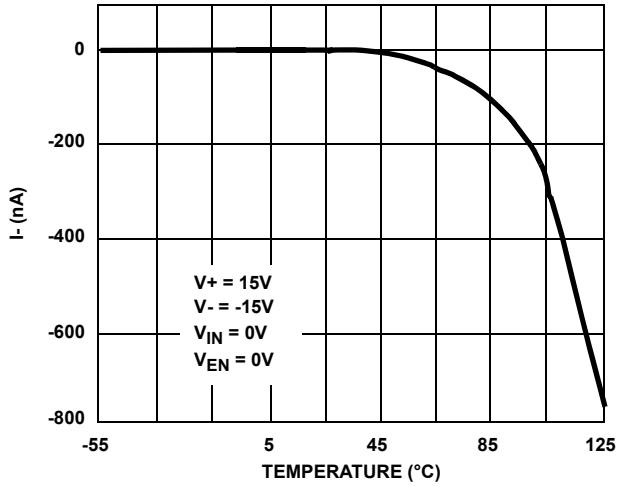


FIGURE 21. NEGATIVE SUPPLY CURRENT vs TEMPERATURE

Typical Performance Curves (Continued)

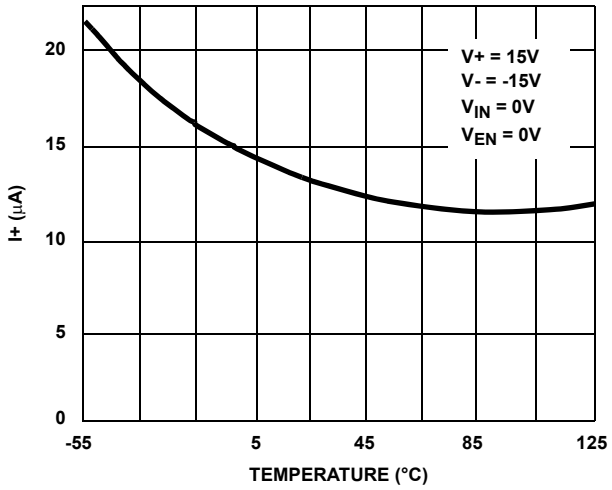


FIGURE 22. POSITIVE SUPPLY CURRENT vs TEMPERATURE (DG408)

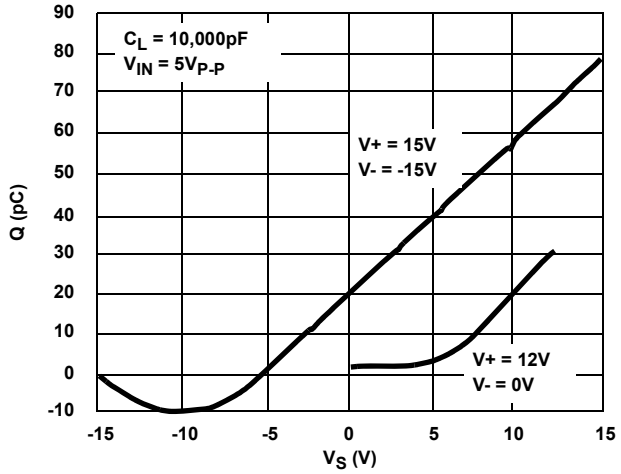


FIGURE 23. CHARGE INJECTION vs ANALOG VOLTAGE

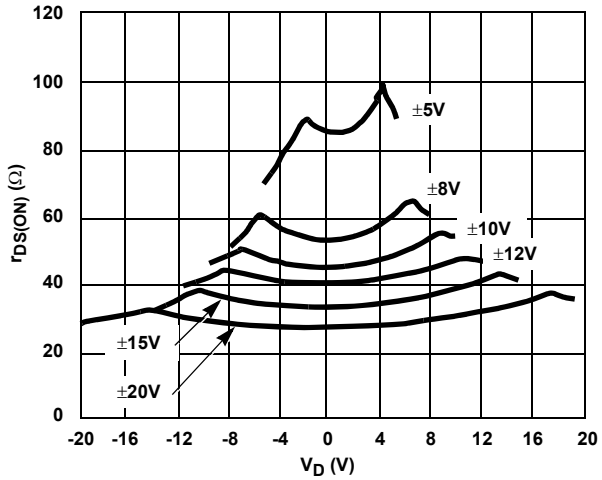


FIGURE 24. $r_{DS(ON)}$ vs V_D AND SUPPLY

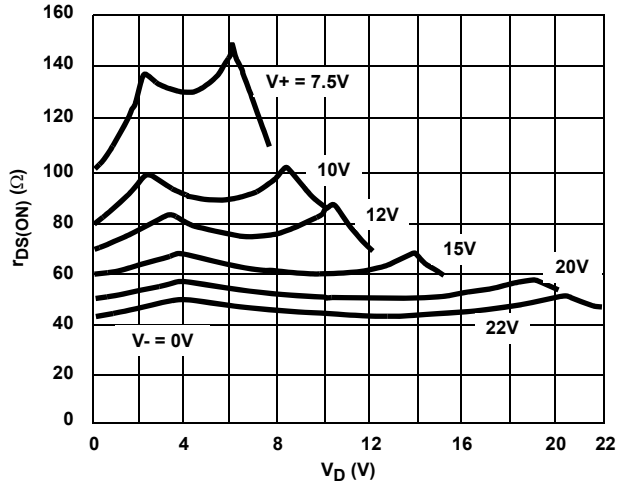


FIGURE 25. $r_{DS(ON)}$ vs V_D (SINGLE SUPPLY)

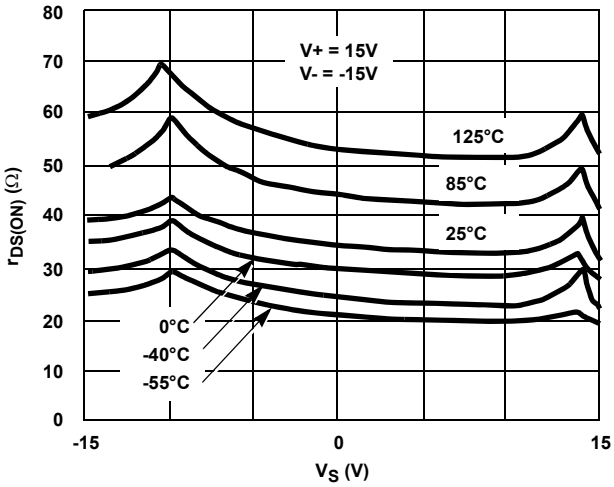


FIGURE 26. $r_{DS(ON)}$ vs V_S AND TEMPERATURE

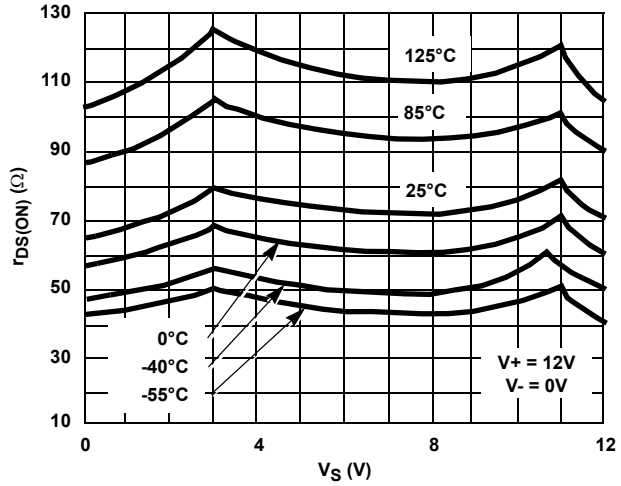


FIGURE 27. $r_{DS(ON)}$ vs V_S AND TEMPERATURE (SINGLE SUPPLY)

Typical Performance Curves (Continued)

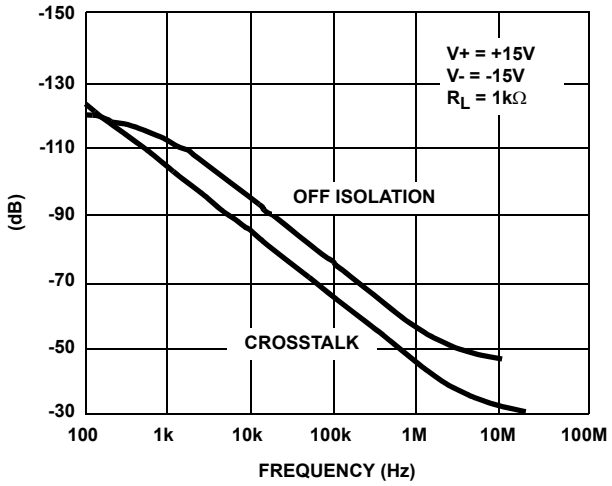


FIGURE 28. OFF ISOLATION AND CROSSTALK vs FREQUENCY

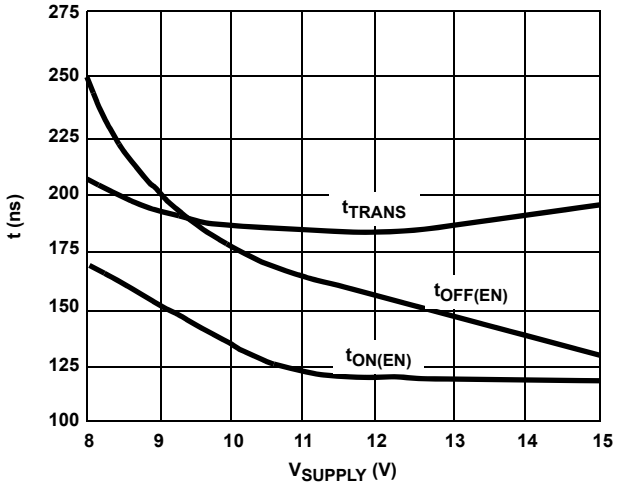


FIGURE 29. SWITCHING TIME vs SINGLE SUPPLY

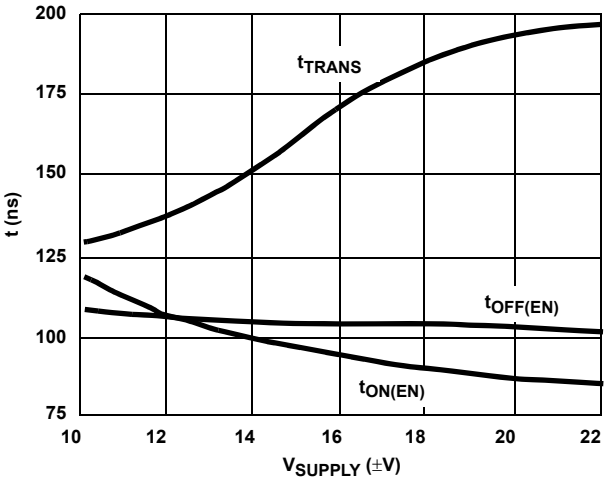


FIGURE 30. SWITCHING TIME vs BIPOLAR SUPPLY

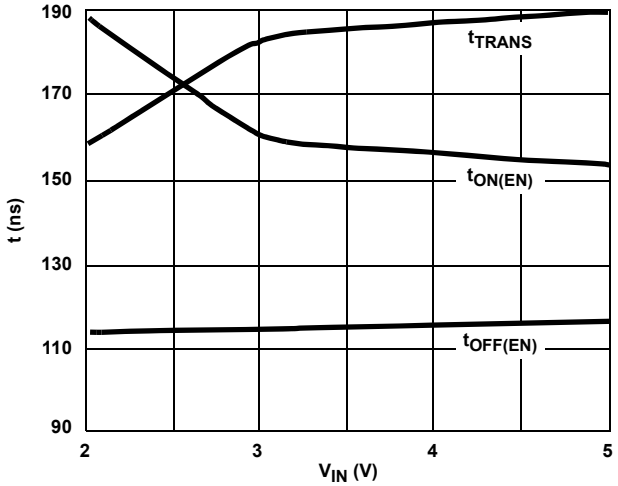


FIGURE 31. SWITCHING TIME vs V_{IN} (SINGLE SUPPLY)

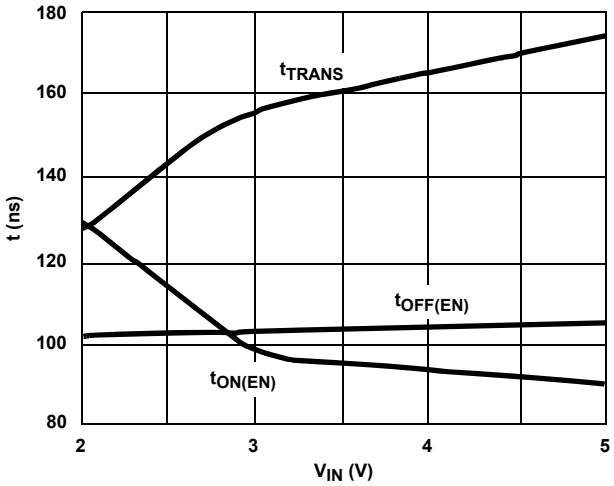


FIGURE 32. SWITCHING TIME vs V_{IN} (BIPOLAR SUPPLY)

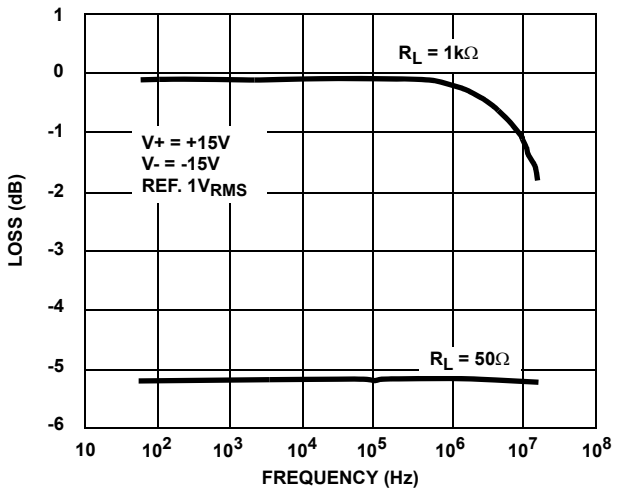


FIGURE 33. INSERTION LOSS vs FREQUENCY

Die Characteristics

DIE DIMENSIONS:

1800μm x 3320μm x 485μm

METALLIZATION:

Type: SiAl
Thickness: 12kÅ ±1kÅ

PASSIVATION:

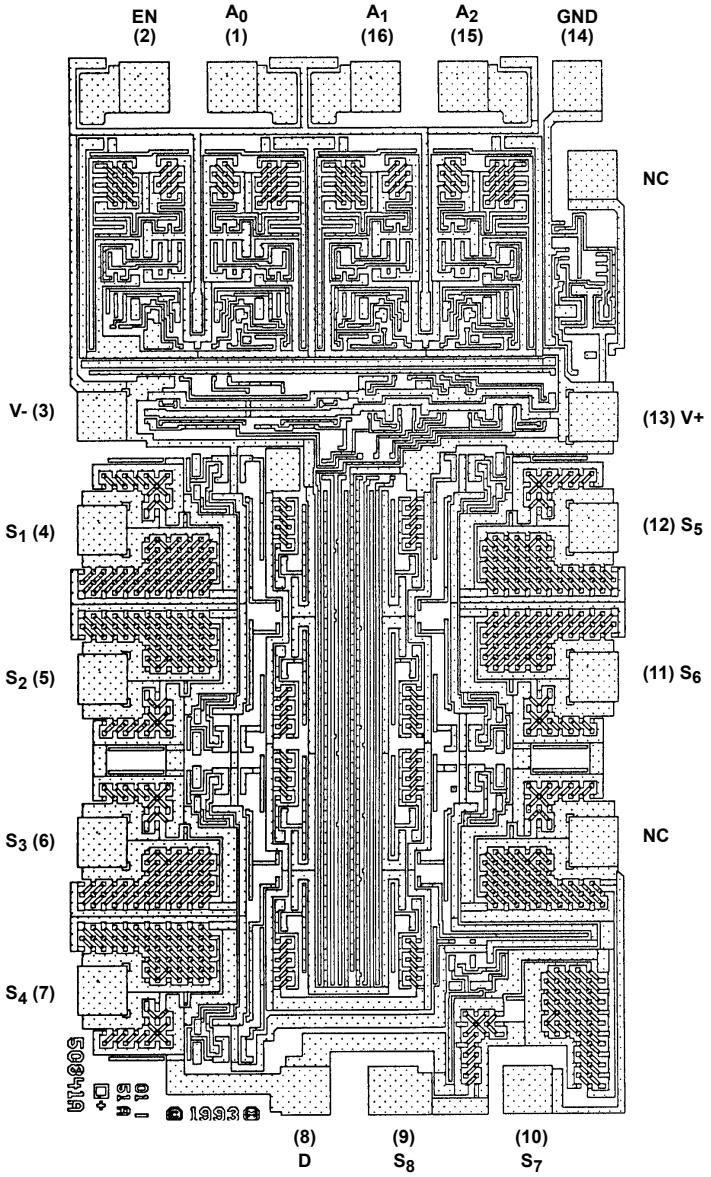
Type: Nitride
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

9.1×10^4 A/cm^2

Metallization Mask Layout

DG408



Die Characteristics

DIE DIMENSIONS:

1800μm x 3320μm x 485μm

METALLIZATION:

Type: SiAl
Thickness: 12kÅ ±1kÅ

PASSIVATION:

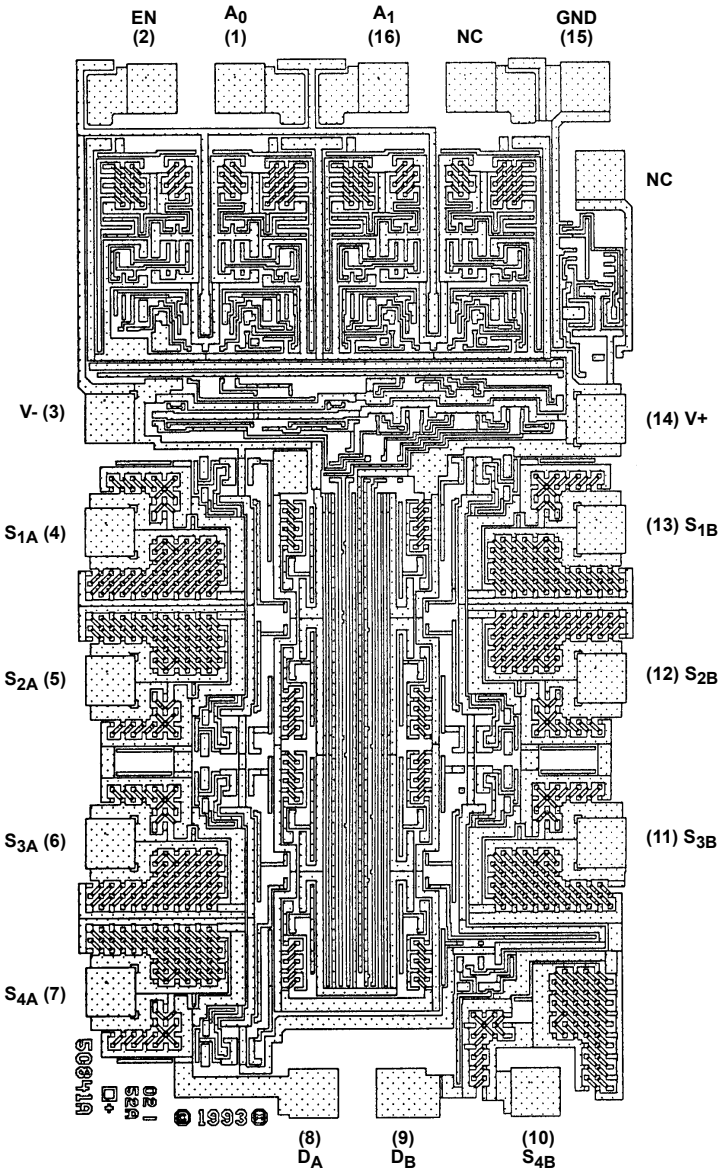
Type: Nitride
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

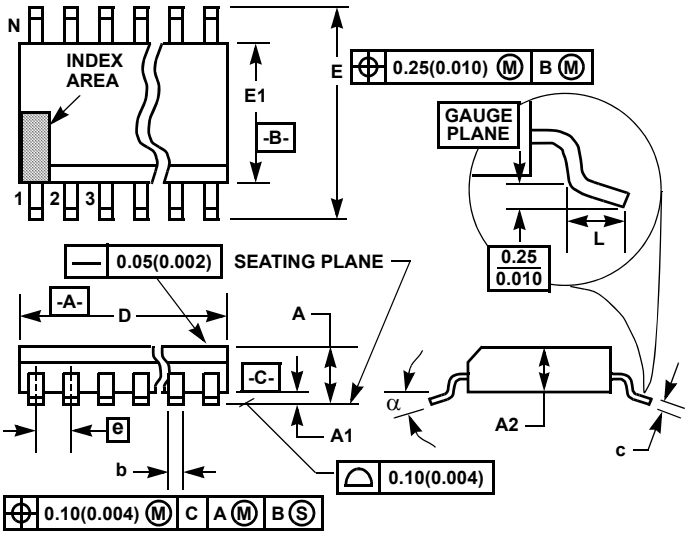
9.1×10^4 A/cm^2

Metallization Mask Layout

DG409



Thin Shrink Small Outline Plastic Packages (TSSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AB, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

M16.173

16 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.043	-	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.033	0.037	0.85	0.95	-
b	0.0075	0.012	0.19	0.30	9
c	0.0035	0.008	0.09	0.20	-
D	0.193	0.201	4.90	5.10	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.020	0.028	0.50	0.70	6
N	16		16		7
α	0°	8°	0°	8°	-

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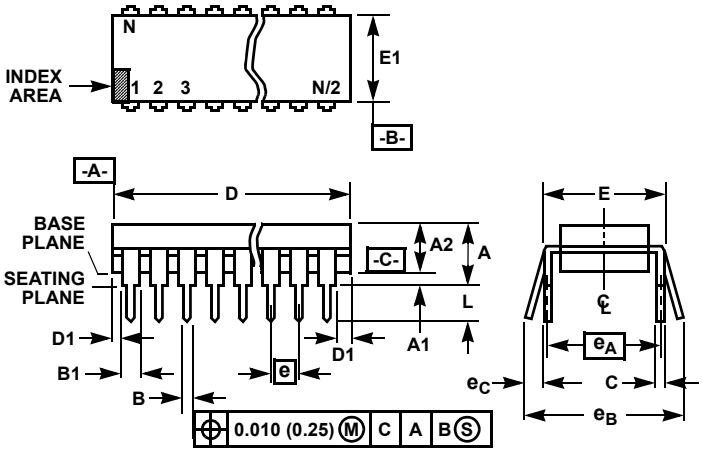
Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E16.3 **(JEDEC MS-001-BB ISSUE D)**
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

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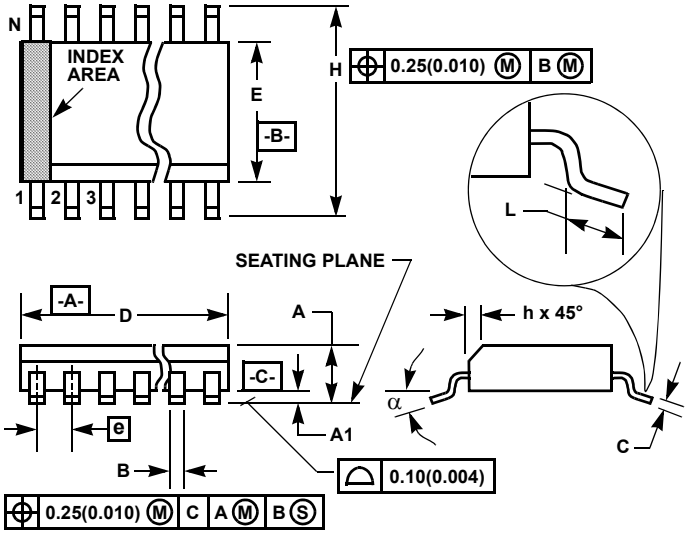
Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M16.15 **(JEDEC MS-012-AC ISSUE C)**
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

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