

PASSIVATED ASSEMBLED CIRCUIT ELEMENTS

Features

- Glass passivated junctions for greater reliability
- Electrically isolated base plate
- Available up to 1200 V_{RRM}, V_{DRM}
- High dynamic characteristics
- Wide choice of circuit configurations
- Simplified mechanical design and assembly
- UL E78996 approved 

25A

Description

The P100 series of Integrated Power Circuits consists of power thyristors and power diodes configured in a single package. With its isolating base plate, mechanical designs are greatly simplified giving advantages of cost reduction and reduced size.

Applications include power supplies, control circuits and battery chargers.

Major Ratings and Characteristics

Parameters	P100	Units
I_D	25	A
@ T_C	85	°C
I_{FSM} @ 50Hz	357	A
@ 60Hz	375	A
I^2t @ 50Hz	637	A ² s
@ 60Hz	580	A ² s
$I^2\sqrt{t}$	6365	A ² √s
V _{RRM}	400 to 1200	V
V _{INS}	2500	V
T _J	- 40 to 125	°C

P100 Series

Bulletin I27125 rev. A 04/99

International
IR Rectifier

ELECTRICAL SPECIFICATIONS

Voltage Ratings

Type number	V_{RRM} maximum repetitive peak reverse voltage V	V_{RSM} maximum non-repetitive peak reverse voltage V	V_{DRM} maximum repetitive peak off-state voltage V	I_{RRM} max. @ T_J max. mA
P101, P121, P131	400	500	400	10
P102, P122, P132	600	700	600	
P103, P123, P133	800	900	800	
P104, P124, P134	1000	1100	1000	
P105, P125, P135	1200	1300	1200	

On-state Conduction

Parameter	P100	Units	Conditions
I_D Maximum DC output current	25	A	@ $T_C = 85^\circ\text{C}$, full bridge
I_{TSM} Max. peak one-cycle non-repetitive on-state or forward current	357	A	t = 10ms No voltage
I_{FSM}	375		t = 8.3ms reapplied
	300		t = 10ms 100% V_{RRM}
	315		t = 8.3ms reapplied
I^2t Maximum I^2t for fusing	637	A^2s	t = 10ms No voltage
	580		t = 8.3ms reapplied
	450		t = 10ms 100% V_{RRM}
	410		t = 8.3ms reapplied
$I^2\sqrt{t}$ Maximum $I^2\sqrt{t}$ for fusing	6365	$\text{A}^2\sqrt{\text{s}}$	t = 0.1 to 10ms, no voltage reapplied I^2t for time tx = $I^2\sqrt{t} \cdot \sqrt{tx}$
$V_{T(To)}$ Max. value of threshold voltage	0.82	V	$T_J = 125^\circ\text{C}$
r_{t1} Max. level value of on-state slope resistance	12	m Ω	$T_J = 125^\circ\text{C}$, Av. power = $V_{T(To)} \cdot I_{T(AV)} + r_t + (I_{T(RMS)})^2$
V_{TM} Max. peak on-state or forward voltage drop V_{FM}	1.35	V	$T_J = 25^\circ\text{C}$, $I_{TM} = \pi \times I_{T(AV)}$
di/dt Maximum non repetitive rate of rise of turned on current	200	A/ μs	$T_J = 125^\circ\text{C}$ from 0.67 V_{DRM} $I_{TM} = \pi \times I_{T(AV)}$, $I_g = 500\text{mA}$, tr < 0.5 μs , tp > 6 μs
I_H Maximum holding current	130	mA	$T_J = 25^\circ\text{C}$ anode supply = 6V, resistive load, gate open
I_L Maximum latching current	250	mA	$T_J = 25^\circ\text{C}$ anode supply = 6V, resistive load

Blocking

Parameter	P100	Units	Conditions
dv/dt Maximum critical rate of rise of off-state voltage	200	V/ μ s	$T_J = 125^\circ\text{C}$, exponential to $0.67 V_{\text{DRM}}$ gate open
I_{RRM} Max. peak reverse and off-state leakage current at V_{RRM} , V_{DRM}	10	mA	$T_J = 125^\circ\text{C}$, gate open circuit
I_{RRM} Max peak reverse leakage current	100	μ A	$T_J = 25^\circ\text{C}$
V_{INS} RMS isolation voltage	2500	V	50Hz, circuit to base, all terminal shorted, $T_J = 25^\circ\text{C}$, $t = 1\text{s}$

Triggering

Parameter	P100	Units	Conditions
P_{GM} Maximum peak gate power	8	W	
$P_{\text{G(AV)}}$ Maximum average gate power	2		
I_{GM} Maximum peak gate current	2	A	
$-V_{\text{GM}}$ Maximum peak negative gate voltage	10	V	$T_J = -40^\circ\text{C}$ $T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$ Anode Supply = 6V resistive load
V_{GT} Maximum gate voltage required to trigger	3 2 1		
I_{GD} Maximum gate current required to trigger	90 60 35		
V_{GD} Maximum gate voltage that will not trigger	0.2	V	$T_J = 125^\circ\text{C}$, rated V_{DRM} applied
I_{GD} Maximum gate current that will not trigger	2	mA	$T_J = 125^\circ\text{C}$, rated V_{DRM} applied

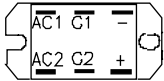
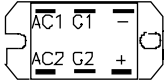
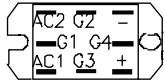
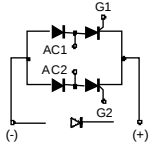
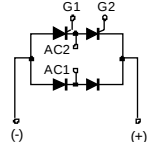
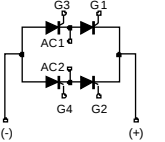
Thermal and Mechanical Specification

Parameter	P100	Units	Conditions
T_J Max. operating temperature range	-40 to 125	$^\circ\text{C}$	
T_{stg} Max. storage temperature range	-40 to 125		
R_{thJC} Max. thermal resistance, junction to case	2.24	K/W	DC operation per junction
R_{thCS} Max. thermal resistance, case to heatsink	0.10	K/W	Mounting surface, smooth and greased
T Mounting torque, base to heatsink	4	Nm	A mounting compound is recommended and the torque should be checked after a period of 3 hours to allow for the spread of the compound
wt Approximate weight	58 (2.0)	g (oz)	

P100 Series

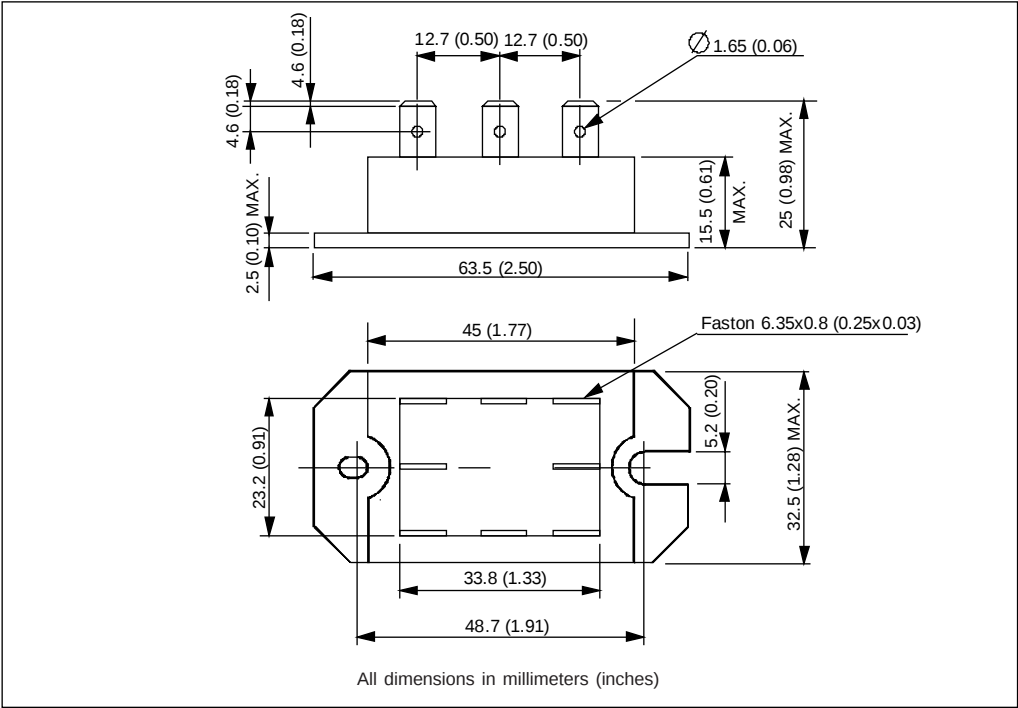
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Circuit Type and Coding *

	Circuit"0"	Circuit"2"	Circuit"3"
Terminal Positions			
Schematic diagram			
	SinglePhase Hybrid Bridge Common Cathode	SinglePhase Hybrid Bridge Doubler	SinglePhase AllSCR Bridge
Basic series	P10.	P12.	P13.
With voltage suppression	P10.K	P12.K	P13.K
With free-wheeling diode	P10.W	-	-
With both voltage suppression and free-wheeling diode	P10.KW	-	-

* To complete code refer to voltage ratings table, i.e.: for 600V P10.W complete code is P102W

Outline Table



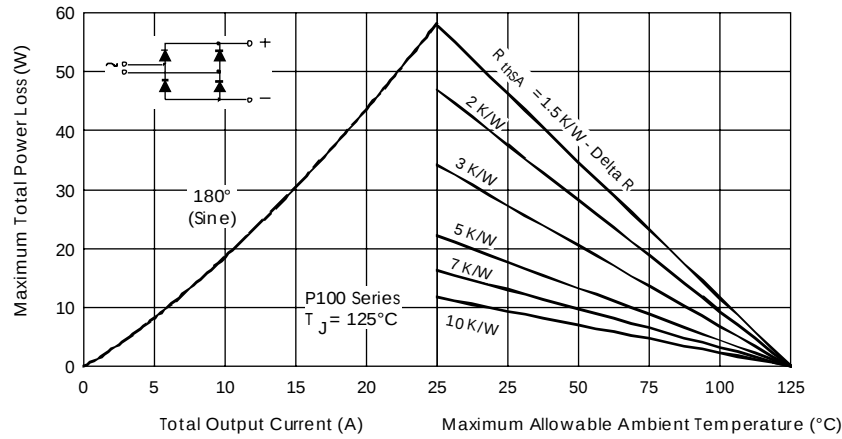


Fig. 1 - Current Ratings Nomogram (1 Module Per Heatsink)

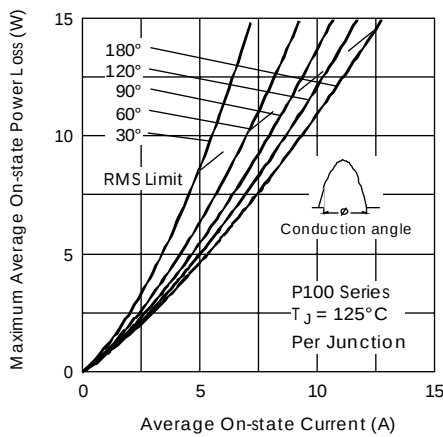


Fig. 2 - On-state Power Loss Characteristics

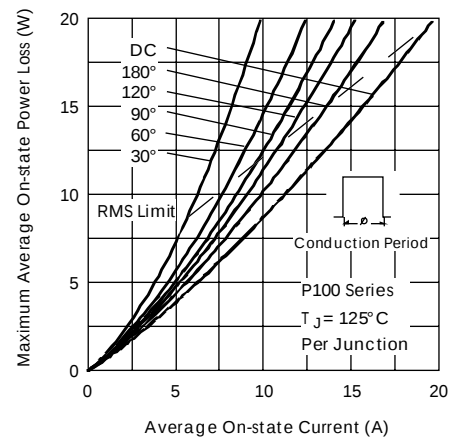


Fig. 3 - On-state Power Loss Characteristics

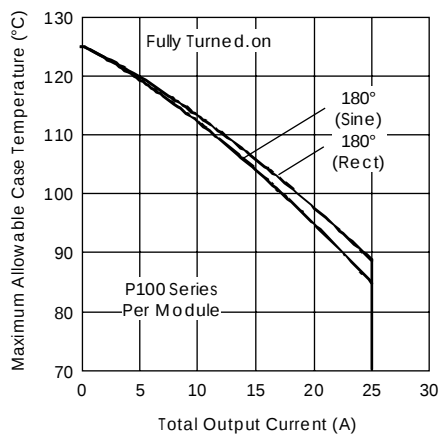


Fig. 4 - Current Ratings Characteristics

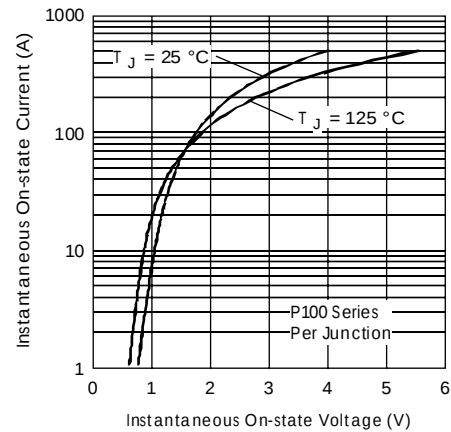


Fig. 5 - On-state Voltage Drop Characteristics

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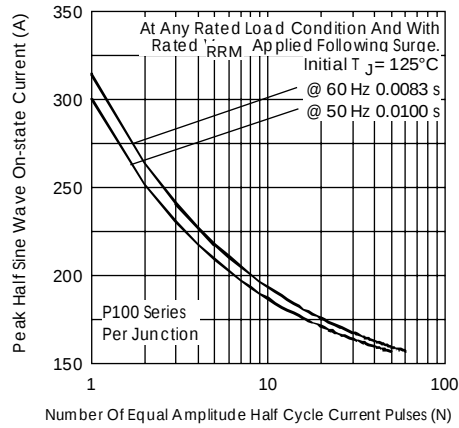


Fig. 6 - Maximum Non-Repetitive Surge Current

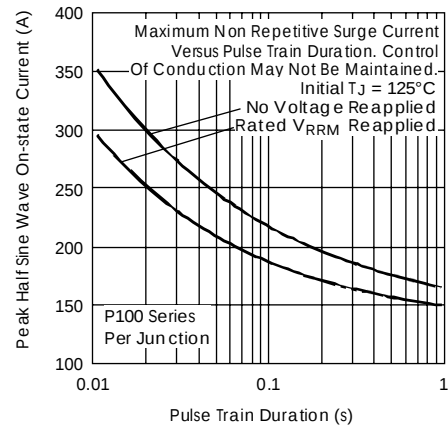


Fig. 7 - Maximum Non-Repetitive Surge Current

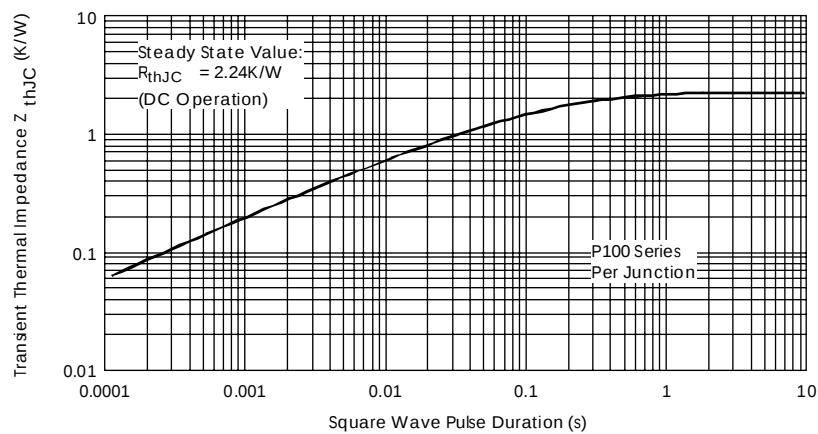


Fig. 8 - Thermal Impedance Z_{thJC} Characteristics

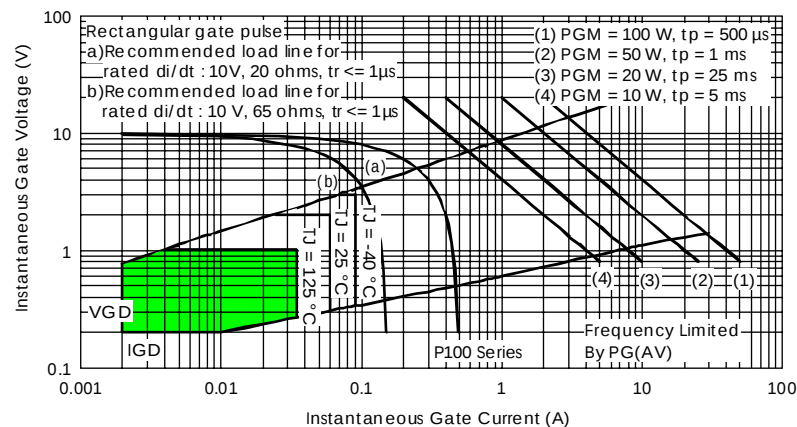


Fig. 9 - Gate Characteristics

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Data and specifications subject to change without notice.