0.8 GHz to 2.5 GHz Quadrature Modulator

AD8346

FEATURES

High accuracy
- **1 degree rms quadrature error @ 1.9 GHz**
- **0.2 dB I/Q amplitude balance @ 1.9 GHz**

Broad frequency range: 0.8 GHz to 2.5 GHz
Sideband suppression: −46 dBc @ 0.8 GHz
Sideband suppression: −36 dBc @ 1.9 GHz
Modulation bandwidth: dc to 70 MHz
0 dBm output compression level @ 0.8 GHz
Noise floor: −147 dBm/Hz
Single 2.7 V to 5.5 V supply
Quiescent operating current: 45 mA
Standby current: 1 µA
16-lead TSSOP

APPLICATIONS

Digital and spread spectrum communication systems
Cellular/PCS/ISM transceivers
Wireless LAN/wireless local loop
QPSK/GMSK/QAM modulators
Single-sideband (SSB) modulators
Frequency synthesizers
Image reject mixer

FUNCTIONAL BLOCK DIAGRAM

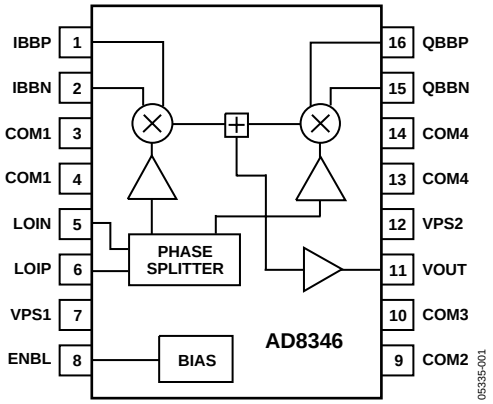

Figure 1.

GENERAL DESCRIPTION

The AD8346 is a silicon RFIC I/Q modulator for use from 0.8 GHz to 2.5 GHz. Its excellent phase accuracy and amplitude balance allow high performance direct modulation to RF.

The differential LO input is applied to a polyphase network phase splitter that provides accurate phase quadrature from 0.8 GHz to 2.5 GHz. Buffer amplifiers are inserted between two sections of the phase splitter to improve the signal-to-noise ratio. The I and Q outputs of the phase splitter drive the LO inputs of two Gilbert-cell mixers. Two differential V-to-I converters connected to the baseband inputs provide the baseband modulation signals for the mixers. The outputs of the two mixers are summed together at an amplifier which is designed to drive a 50 Ω load.

This quadrature modulator can be used as the transmit modulator in digital systems such as PCS, DCS, GSM, CDMA, and ISM transceivers. The baseband quadrature inputs are directly modulated by the LO signal to produce various QPSK and QAM formats at the RF output.

Additionally, this quadrature modulator can be used with direct digital synthesizers in hybrid phase-locked loops to generate signals over a wide frequency range with millihertz resolution.

The AD8346 comes in a 16-lead TSSOP package, measuring 6.5 mm × 5.1 mm × 1.1 mm. It is specified to operate over a −40°C to +85°C temperature range and a 2.7 V to 5.5 V supply voltage range. The device is fabricated on Analog Devices' high performance 25 GHz bipolar silicon process.

Rev. A
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REVISION HISTORY

6/05—Rev. 0 to Rev. A

Updated Format ... Universal
Changes to Figures 30, 31, 32 ... 14
Update Outline Dimensions ... 18
Changes to Ordering Guide ... 18

3/99—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V; T_A = 25°C; LO frequency = 1900 MHz; LO level = −10 dBm; BB frequency = 100 kHz; BB inputs are dc-biased to 1.2 V; BB input level = 1.0 V p-p each pin for 2.0 V p-p differential drive; LO source and RF output load impedances are 50 Ω, dBm units are referenced to 50 Ω unless otherwise noted.

Table 1.

Parameters	Conditions	Min	Typ	Max	Unit
RF OUTPUT					
Operating Frequency		0.8		2.5	GHz
Quadrature Phase Error	See Figure 35 for setup		1		Degree rms
I/Q Amplitude Balance	See Figure 35 for setup		0.2		dB
Output Power	I and Q channels in quadrature	−13	−10	−6	dBm
Output VSWR			1.25:1		
Output P1 dB			−3		dBm
Carrier Feedthrough			−42	−35	dBm
Sideband Suppression			−36	−25	dBc
IM3 Suppression			−60		dBc
Equivalent Output IP3			20		dBm
Output Noise Floor	20 MHz offset from LO		−147		dBm/Hz
RESPONSE TO CDMA IS95 BASEBAND SIGNALS					
ACPR (Adjacent Channel Power Ratio)	See Figure 35 for setup		−72		dBc
EVM (Error Vector Magnitude)	See Figure 35 for setup		2.5		%
Rho (Waveform Quality Factor)	See Figure 35 for setup		0.9974		
MODULATION INPUT					
Input Resistance			12		kΩ
Modulation Bandwidth	−3 dB		70		MHz
LO INPUT					
LO Drive Level		−12		−6	dBm
Input VSWR			1.9:1		
ENABLE					
ENBL HI Threshold				2.0	V
ENBL LO Threshold		0.5			V
ENBL Turn-On Time	Settle to within 0.5 dB of final SSB output power		2.5		µs
ENBL Turn-Off Time	Time for supply current to drop below 2 mA		12		µs
POWER SUPPLIES					
Voltage		2.7		5.5	V
Current Active (ENBL HI)		35	45	55	mA
Current Standby (ENBL LO)			1	20	µA

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Min Rating
Supply Voltage VPS1, VPS2	5.5 V
Input Power LOIP, LOIN (relative to 50 Ω)	10 dBm
Min Input Voltage IBBP, IBBN, QBBP, QBBN	0 V
Max Input Voltage IBBP, IBBN, QBBP, QBBN	2.5 V
Internal Power Dissipation	500 mW
θJA	125°C/W
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other condition s above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

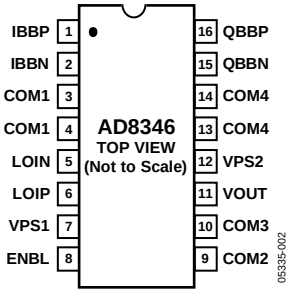

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description	Equivalent Circuit
1	IBBP	I Channel Baseband Positive Input Pin. Input should be dc-biased to approximately 1.2 V. Nominal characterized ac swing is 1 V p-p (0.7 V to 1.7 V). This makes the differential input 2 V p-p when IBBN is 180 degrees out of phase from IBBP.	Circuit A
2	IBBN	I Channel Baseband Negative Input Pin. Input should be dc-biased to approximately 1.2 V. Nominal characterized ac swing is 1 V p-p (0.7 V to 1.7 V). This makes the differential input 2 V p-p when IBBN is 180 degrees out of phase from IBBP.	Circuit A
3	COM1	Ground Pin for the LO phase splitter and LO buffers.	
4	COM1	Ground Pin for the LO phase splitter and LO buffers.	
5	LOIN	LO Negative Input Pin. Internal dc bias (approximately VPS1 to 800 mV) is supplied. This pin must be ac coupled.	Circuit B
6	LOIP	LO Positive Input Pin. Internal dc bias (approximately VPS1 to 800 mV) is supplied. This pin must be ac-coupled.	Circuit B
7	VPS1	Power Supply Pin for the bias cell and LO buffers. This pin should be decoupled using local 100 pF and 0.01 µF capacitors.	
8	ENBL	Enable Pin. A high level enables the device; a low level puts the device in sleep mode.	Circuit C
9	COM2	Ground Pin for the input stage of output amplifier.	
10	COM3	Ground Pin for the output stage of output amplifier.	
11	VOUT	50 Ω DC-Coupled RF Output. User must provide ac coupling on this pin.	Circuit D
12	VPS2	Power Supply Pin for baseband input voltage to current converters and mixer core. This pin should be decoupled using local 100 pF and 0.01 µF capacitors.	
13	COM4	Ground Pin for baseband input voltage to current converters and mixer core.	
14	COM4	Ground Pin for baseband input voltage to current converters and mixer core.	
15	QBBN	Q Channel Baseband Negative Input. Input should be dc biased to approximately 1.2 V. Nominal characterized ac swing is 1 V p-p. This makes the differential input 2 V p-p when QBBN is 180° out of phase from QBBP.	Circuit A
16	QBBP	Q Channel Baseband Positive Input. Input should be dc-biased to approximately 1.2 V. Nominal characterized ac swing is 1 V p-p. This makes the differential input 2 V p-p when QBBN is 180° out of phase from QBBP.	Circuit A

EQUIVALENT CIRCUITS

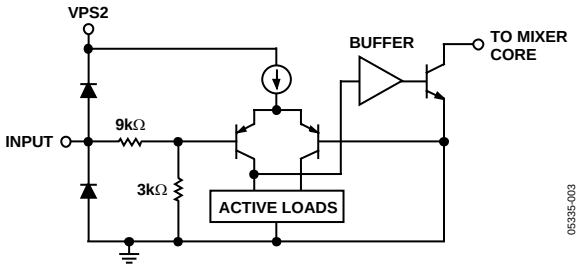

Figure 3. Circuit A

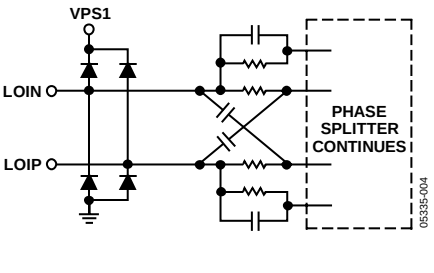

Figure 4. Circuit B

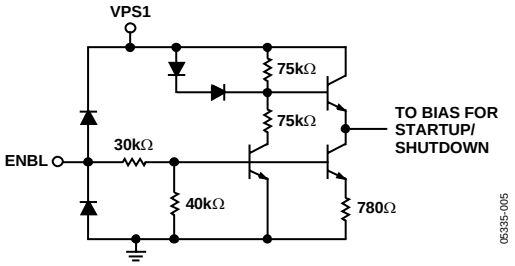

Figure 5. Circuit C

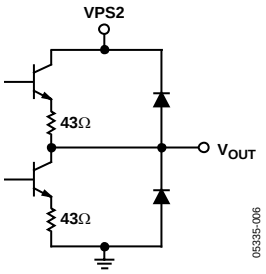

Figure 6. Circuit D

TYPICAL PERFORMANCE CHARACTERISTICS

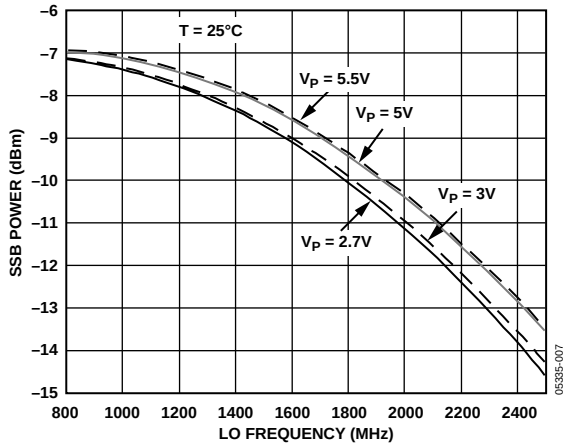

Figure 7. Single Sideband (SSB) Output Power (P_{OUT}) vs. LO Frequency (F_{LO}). I and Q inputs driven in quadrature at baseband frequency (F_{BB}) = 100 kHz with differential amplitude of 2.00 V p-p.

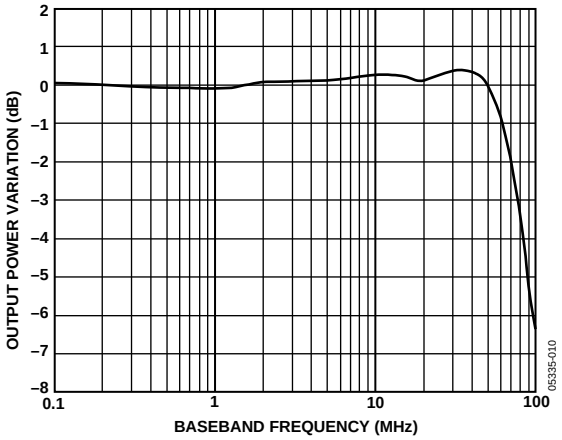

Figure 10. I and Q Input Bandwidth. F_{LO} =1900 MHz, I or Q inputs driven with differential amplitude of 2.00 V p-p.

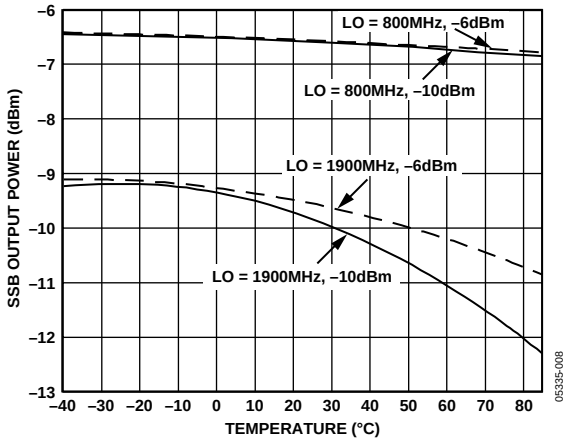

Figure 8. SSB P_{OUT} vs. Temperature. I and Q inputs driven in quadrature with differential amplitude of 2.00 V p-p at F_{BB} = 100 kHz.

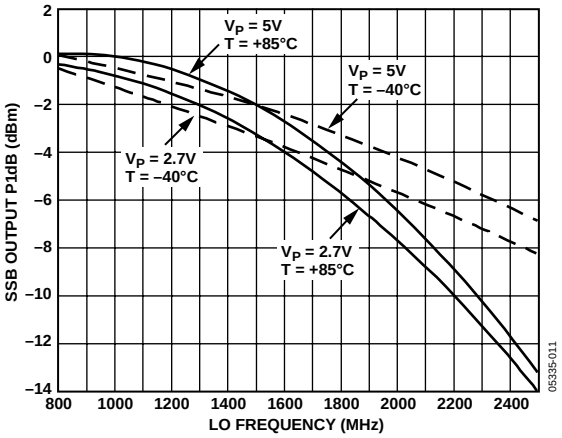

Figure 11. SSB Output 1 dB Compression Point (OP 1 dB) vs. FLO. I and Q inputs driven in quadrature at F_{BB} = 100 kHz.

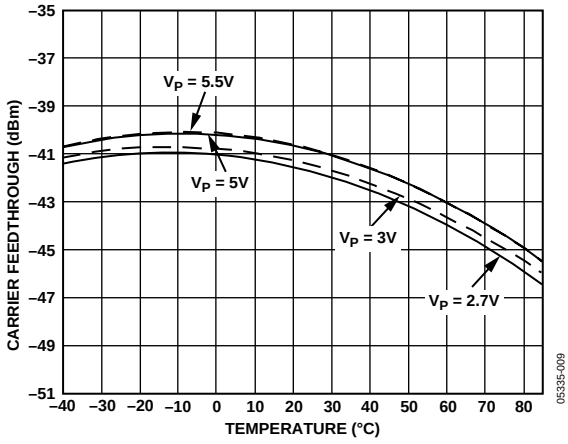

Figure 9. Carrier Feedthrough vs. Temperature. F_{LO} = 1900 MHz, LO input level = –10 dBm.

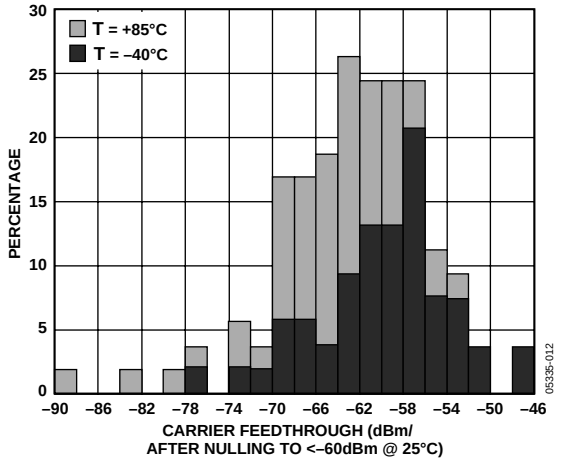

Figure 12. Histogram Showing Carrier Feedthrough Distributions at the Temperature Extremes after Nulling at Ambient at F_{LO} = 1900 MHz, LO Input Level = –10 dBm.

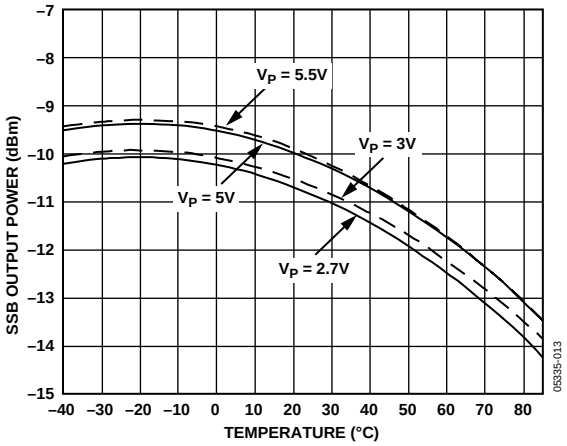

Figure 13. SSB P_{OUT} vs. Temperature. F_{LO} = 1900 MHz, I and Q inputs driven in quadrature with differential amplitude of 2.00 V p-p at F_{BB} = 100 kHz.

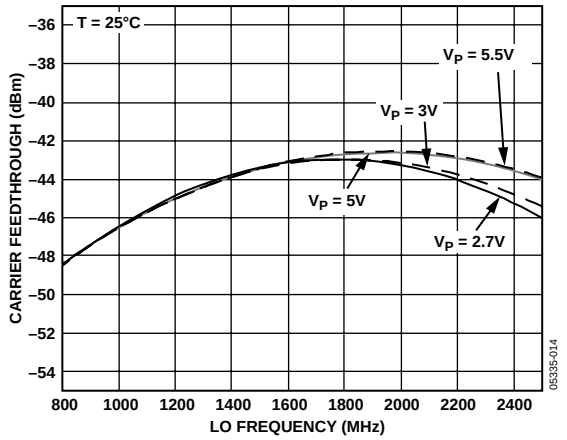

Figure 14. Carrier Feedthrough vs. F_{LO}. LO input level = –10 dBm.

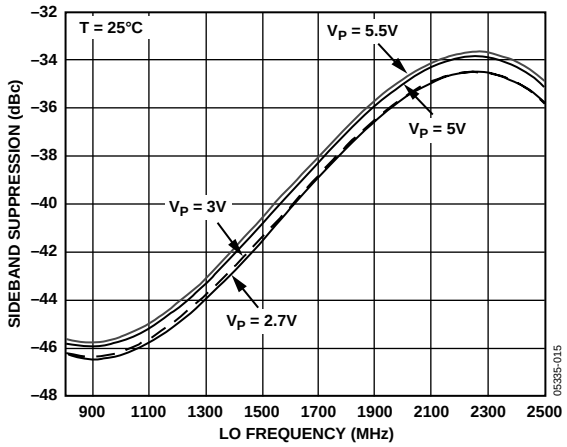

Figure 15. Sideband Suppression vs. F_{LO}. V_{POS} = 2.7 V, I and Q inputs driven in quadrature with differential amplitude of 2.00 V p-p at F_{BB} = 100 kHz.

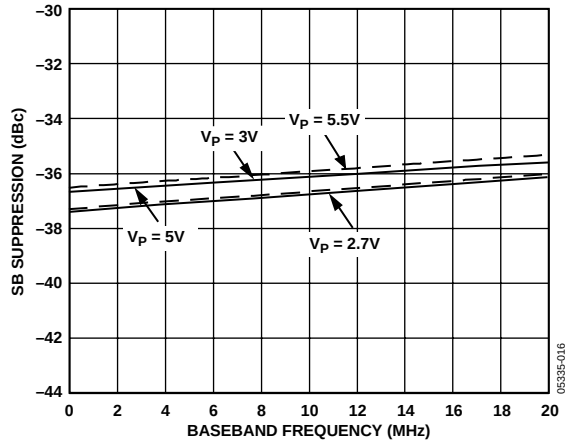

Figure 16. Sideband Suppression vs. F_{BB}. F_{LO} = 1900 MHz, I and Q inputs driven in quadrature with differential amplitude of 2.00 V p-p.

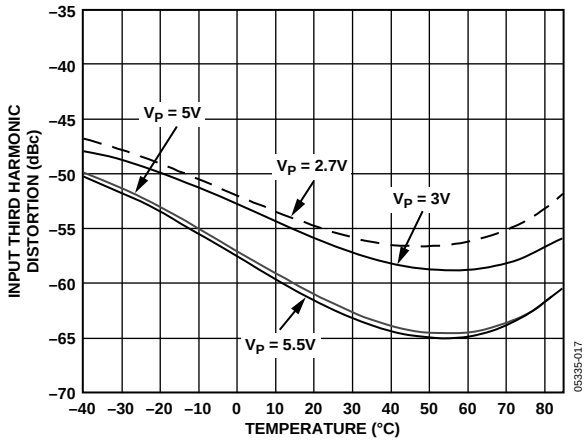

Figure 17. Third Harmonic Distortion vs. Temperature. F_{LO} =1900 MHz, I and Q inputs driven in quadrature with differential amplitude of 2.00 V p-p at F_{BB} = 100 kHz.

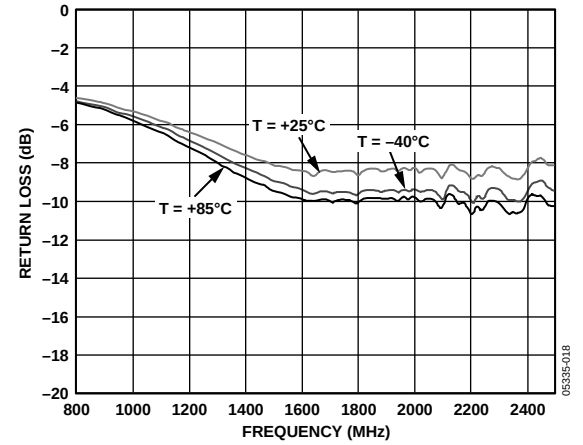

Figure 18. Return Loss of LOIN Input vs. F_{LO}. V_{POS} = 5.0 V, LOIP pin ac-coupled to ground.

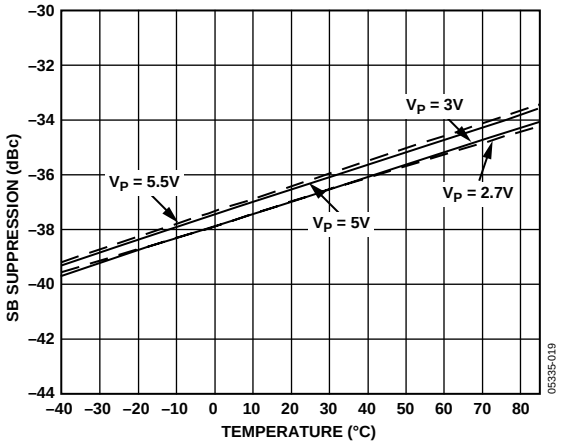

Figure 19. Sideband Suppression vs. Temperature. F_{LO} = 1900 MHz, I and Q inputs driven in quadrature with differential amplitude of 2.00 V p-p at F_{BB} = 100 kHz.

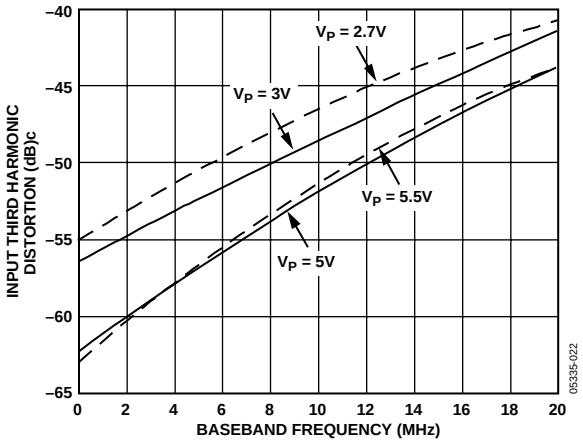

Figure 22. Third Harmonic Distortion vs. F_{BB}. F_{LO} =1900 MHz, I and Q inputs driven in quadrature with differential amplitude of 2.00 V p-p.

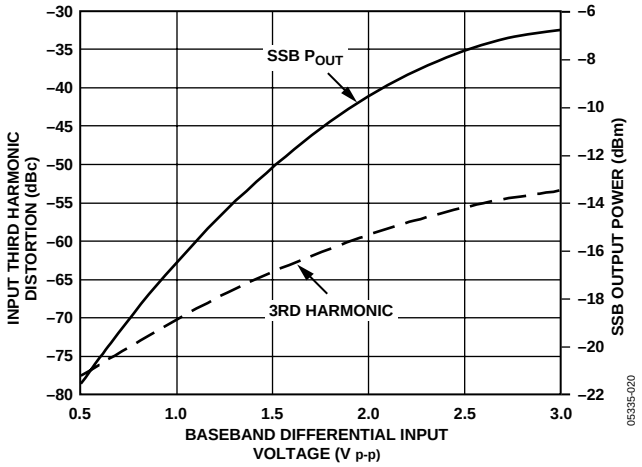

Figure 20. Third Harmonic Distortion and SSB Output Power vs. Baseband Differential Input Voltage Level. F_{LO} = 1900 MHz, I and Q inputs driven in quadrature at F_{BB} = 100 kHz.

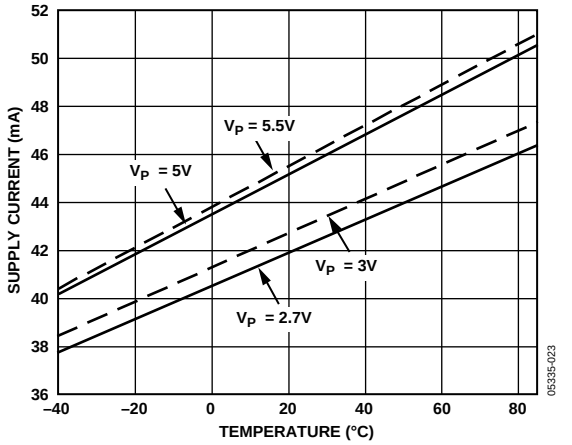

Figure 23. Power Supply Current vs. Temperature

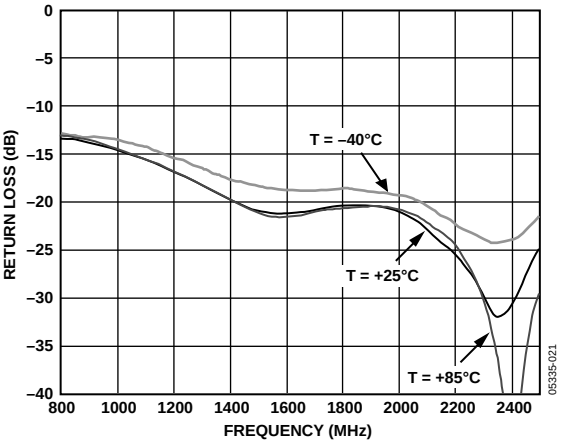

Figure 21. Return Loss of V_{OUT} Output vs. F_{LO}. V_{POS} = 2.7 V.

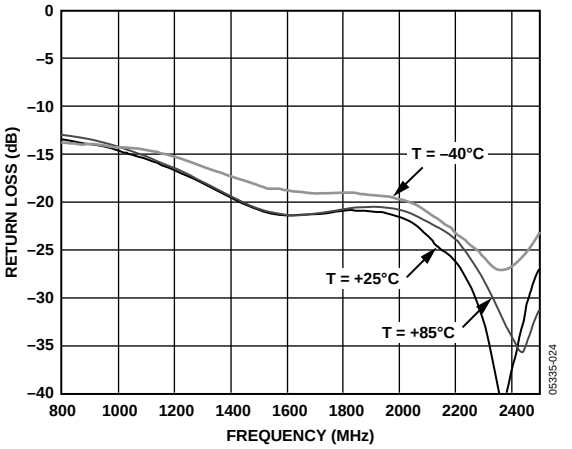

Figure 24. Return Loss of V_{OUT} Output vs. F_{LO}. V_{POS} = 5.0 V.

CIRCUIT DESCRIPTION

OVERVIEW

The AD8346 can be divided into the following sections: local oscillator (LO) interface, mixer, voltage-to-current (V-to-I) converter, differential-to-single-ended (D-to-S) converter, and bias. A detailed block diagram of the part is shown in Figure 25.

The LO interface generates two LO signals, with 90° of phase difference between them, to drive two mixers in quadrature. Baseband voltage signals are converted into current form in the V-to-I converters, feeding into two mixers. The output of the mixers are combined to feed the D-to-S converter which provides the 50 Ω output interface. Bias currents to each section are controlled by the Enable (ENBL) signal. Detailed descriptions of each section follows.

LO INTERFACE

The differential LO inputs allow the user to drive the LO differentially in order to achieve maximum performance. The LO can be driven single-endedly but the LO feedthrough performance is degraded, especially towards the higher end of the frequency range. The LO interface consists of interleaved stages of polyphase network phase splitters and buffer amplifiers. The phase-splitter contains resistors and capacitors connected in a circular manner to split the LO signal into I and Q paths in precise quadrature with each other. The signal on each path goes through a buffer amplifier to make up for the loss and high frequency roll-off. The two signals then go through another polyphase network to enhance the quadrature accuracy. The broad operating frequency range of 0.8 GHz to 2.5 GHz is achieved by staggering the RC time constants in each stage of the phase-splitters. The outputs of the second phase-splitter are fed into the driver amplifiers for the mixers' LO inputs.

V-TO-I CONVERTER

Each baseband input pin is connected to an op amp driving an emitter follower. Feedback at the emitter maintains a current proportional to the input voltage through the transistor. This current is fed to the two mixers in differential form.

MIXERS

There are two double-balanced mixers, one for the in-phase channel (I-channel) and one for the quadrature channel (Q channel). Each mixer uses the gilbert cell design with four cross-connected transistors. The bases of the transistors are driven by the LO signal of the corresponding channel. The output currents from the two mixers are summed together in two resistors in series with two coupled on-chip inductors. The signal developed across the R-L loads is sent to the D-to-S stage.

DIFFERENTIAL-TO-SINGLE-ENDED CONVERTER

The differential-to-single-ended converter consists of two emitter followers driving a totem-pole output stage. Output impedance is established by the emitter resistors in the output transistors. The output of this stage is connected to the output (VOUT) pin.

BIAS

A band gap reference circuit based on the Δ-V_{BE} principle generates the proportional-to-absolute-temperature (PTAT) currents used by the different sections as references. The band gap voltage is also used to generate a temperature-stable current in the V-to-I converters to produce a temperature-independent slew rate. When the band gap reference is disabled by pulling down the ENBL pin, all other sections are shut off accordingly.

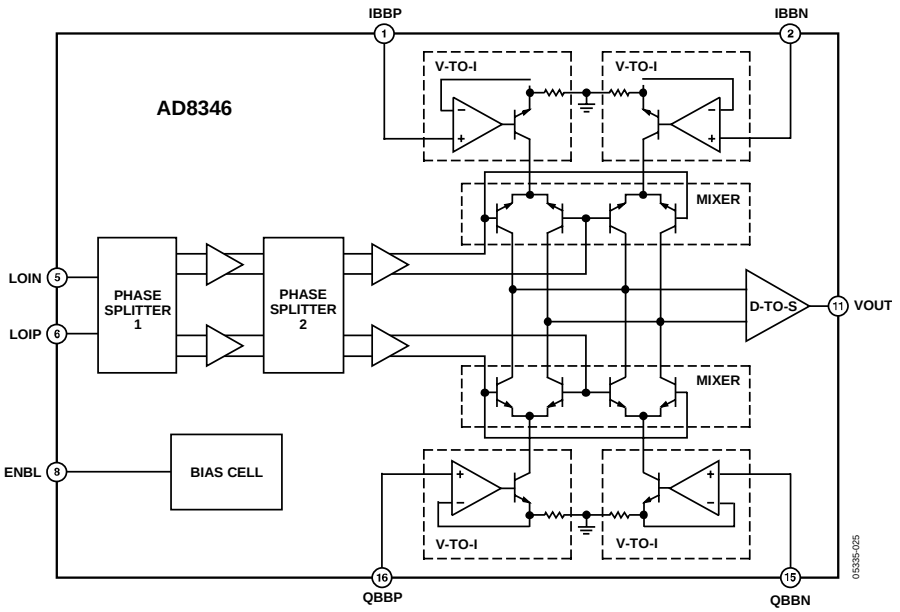

Figure 25. Detailed Block Diagram

BASIC CONNECTIONS

The basic connections for operating the AD8346 are shown in Figure 27. A single power supply of between 2.7 V and 5.5 V is applied to pins VPS1 and VPS2. A pair of ESD protection diodes are connected internally between VPS1 and VPS2 so these must be tied to the same potential. Both pins should be individually decoupled using 100 pF and 0.01 μF capacitors, located as close as possible to the device. For normal operation, the enable pin, ENBL, must be pulled high. The turn-on threshold for ENBL is 2 V. To put the device in its power-down mode, ENBL must be pulled below 0.5 V. Pins COM1 to COM4 should all be tied to a low impedance ground plane.

The I and Q ports should be driven differentially. This is convenient as most modern high speed DACs have differential outputs. For optimal performance, the drive signal should be a 2 V p-p (differential) signal with a bias level of 1.2 V, that is, each input swings from 0.7 V to 1.7 V. The I and Q inputs have input impedances of 12 kΩ. By dc coupling the DAC to the AD8346 and applying small offset voltages, the LO feedthrough can be reduced to well below its nominal value of −42 dBm (see Figure 12).

LO DRIVE

The return loss of the LO port is shown in Figure 18. No additional matching circuitry is required to drive this port from a 50 Ω source. For maximum LO suppression at the output, a differential LO drive is recommended. In Figure 27, this is achieved using a balun (M/A-COM Part Number ETC1-1-13). The output of the balun is ac-coupled to the LO inputs which have a bias level about 800 mV below supply. An LO drive level of between −6 dBm and −12 dBm is required. For optimal performance, a drive level of −10 dBm is recommended, although a level of −6 dBm results in more stable temperature performance (see Figure 8). Higher levels degrade linearity while lower levels tend to increase the noise floor.

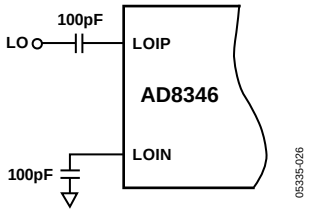

Figure 26. Single-Ended LO Drive

The LO terminal can be driven single-ended, as shown in Figure 26 at the expense of slightly higher LO feedthrough. LOIN is ac coupled to ground using a capacitor and LOIP is driven through a coupling capacitor from a (single-ended) 50 Ω source (this scheme could also be reversed with LOIP being ac-coupled to ground).

RF OUTPUT

The RF output is designed to drive a 50 Ω load, but must be ac-coupled, as shown in Figure 27. If the I and Q inputs are driven in quadrature by 2 V p-p signals, the resulting output power is about −10 dBm (see Figure 7 for variations in output power over frequency).

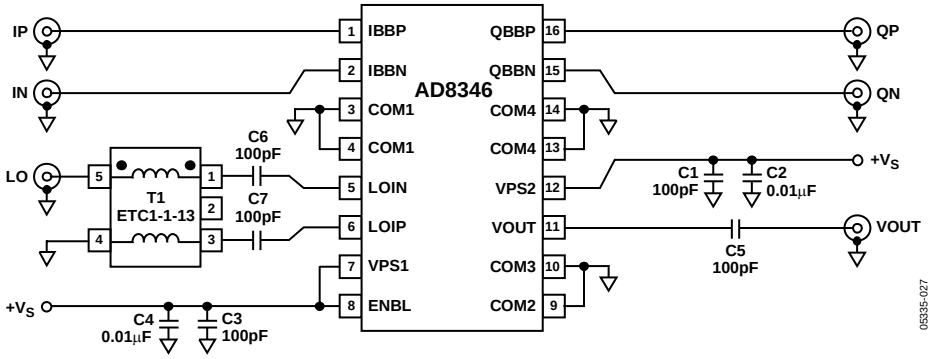

Figure 27. Basic Connections

INTERFACE TO AD9761 TxDAC®

Figure 28 shows a dc-coupled current output DAC interface. The use of dual-integrated DACs, such as the AD9761 with specified ±0.02 dB and ±0.004 dB gain and offset matching characteristics, ensures minimum error contribution (over temperature) from this portion of the signal chain. The use of a precision thin-film resistor network sets the bias levels precisely to prevent the introduction of offset errors, which increase LO feedthrough. For instance, selecting resistor networks with a 0.1% ratio matching characteristics maintains 0.03 dB gain and offset matching performance.

Using resistive division, the dc bias level at the I and Q inputs to the AD8346 is set to approximately 1.2 V. Each of the four current outputs of the DAC delivers a full-scale current of 10 mA, giving a voltage swing of 0 V to 1 V (at the DAC output). This results in a 0.5 V p-p swing at the I and Q inputs of the AD8346 (resulting in a 1 V p-p differential swing).

Note that the ratio matching characteristics of the resistive network, as opposed to its absolute accuracy, is critical in preserving the gain and offset balance between the I and Q signal path.

By applying small dc offsets to the I and Q signals from the DAC, the LO suppression can be reduced from its nominal value of −42 dBm to as low as −60 dBm while holding to approximately −50 dBm over temperature (see Figure 12 for a plot of LO feedthrough over temperature for an offset compensated circuit).

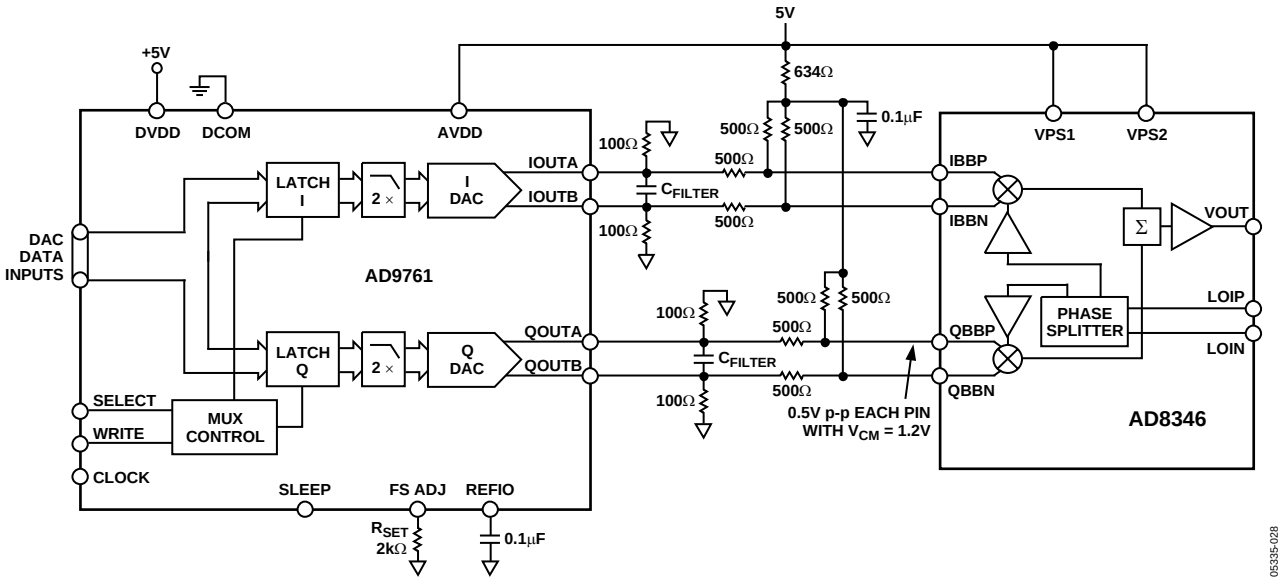

Figure 28. AD8346 Interface to AD9761 TxDAC

AC-COUPLED INTERFACE

An ac-coupled interface can also be implemented, as shown in Figure 29. This is an advantage because there is almost no voltage loss due to the biasing network, allowing the AD8346 inputs to be driven by the full 2 V p-p differential signal from the AD9761 (each of the DAC's 4 outputs delivering 1 V p-p).

As in the dc-coupled case, the bias levels on the I and Q inputs should be set to as precise a level as possible, relative to each other. This prevents the introduction of additional input offset voltages. In Figure 29, the bias level on each input is set to approximately 1.2 V. The 2.43 kΩ resistors should have a ratio tolerance of 0.1% or better.

The network shown has a high-pass corner frequency of approximately 14.3 kHz (note that the 12 kΩ input impedance of the AD8346 has been factored into this calculation). Increasing the resistors in the network or increasing the coupling capacitance reduces the corner frequency further.

Note that the LO suppression can be manually optimized by replacing a portion of the four top 2.43 kΩ resistors with potentiometers. In this case, the bottom four resistors in the biasing network no longer need to be precision devices.

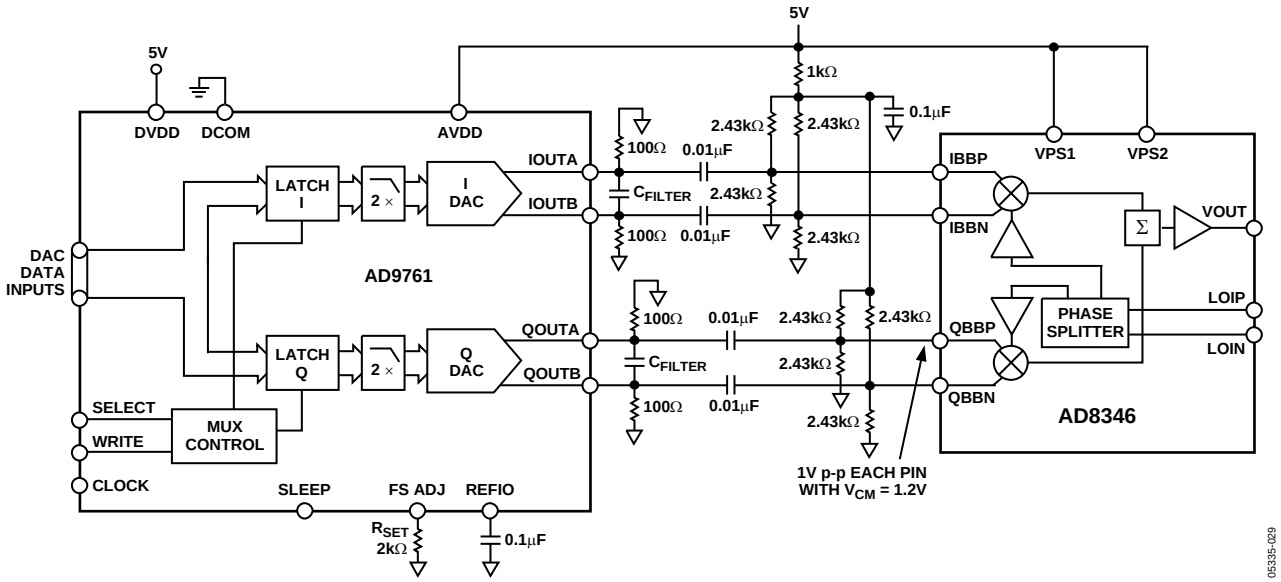

Figure 29. AC-Coupled DAC Interface

EVALUATION BOARD

The schematic of the AD8346 evaluation board is shown in Figure 30. This is a 4-layer FR4 board; the two center layers are used as ground planes and the top and bottom layers are used for signal and power. Figure 31 shows the layout and Figure 32 shows the silkscreen. The evaluation board circuit closely follows the basic connections circuit shown in Figure 27.

Slide SW1 to the A position to connect the ENBL pin to $+V_S$ via the 10 kΩ pull-up resistor REP. Slide SW1 to the B position to disable the device by grounding the ENOP pin through the 49.9 Ω pull-down resistor REG. The device may be enabled via an external voltage applied to the SMA connector ENOP or TP2.

All connectors are of the SMA type. The I and Q inputs are provided with pads for implementing a simple RC filter network. The local oscillator input is driven through a balun (M/A-COM Part Number ETC1-1-13).

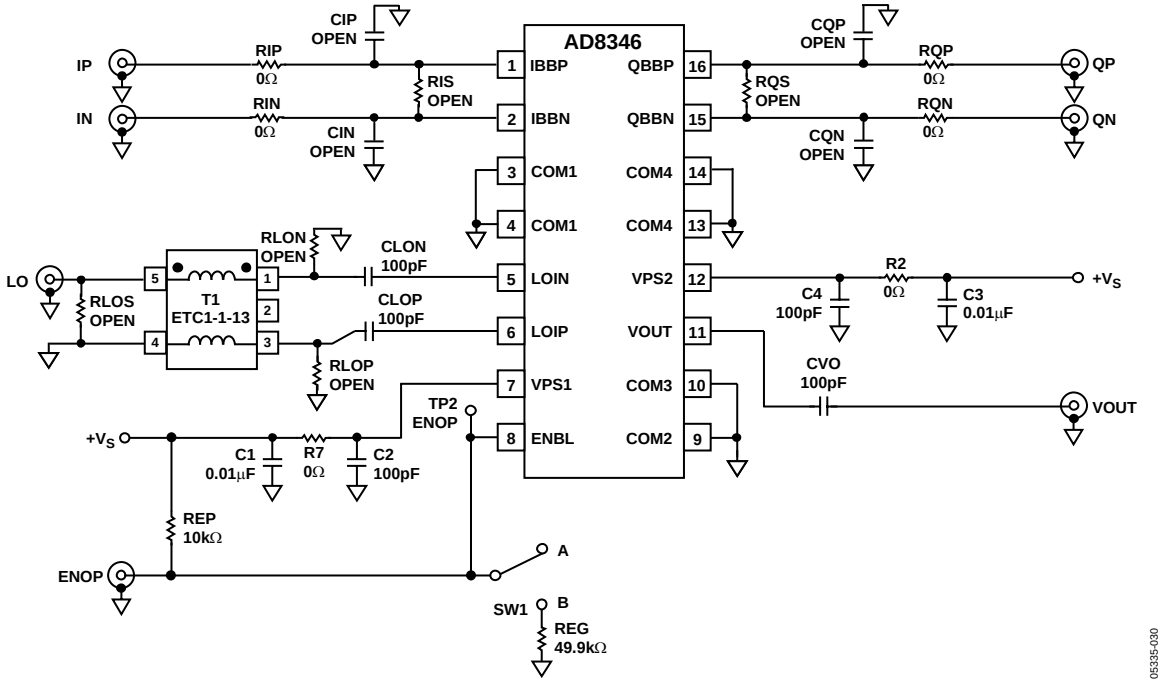

Figure 30. Evaluation Board Schematic

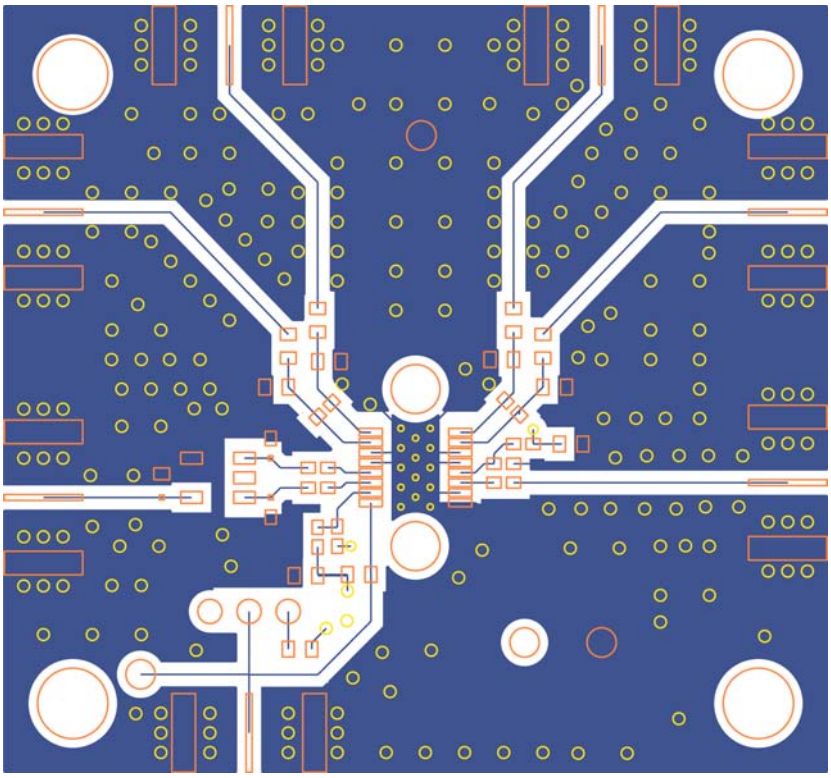

Figure 31. Layout of Evaluation Board

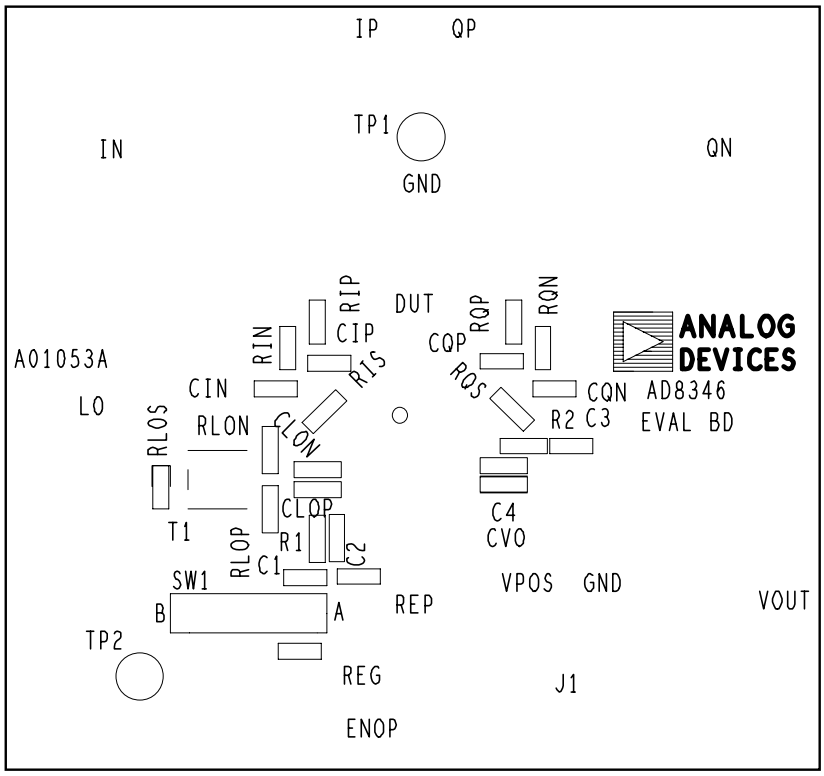

Figure 32. Silkscreen of Evaluation Board

CHARACTERIZATION SETUPS

SSB SETUP

Two main setups were used to characterize this product. These setups are shown in Figure 33 and Figure 35. Figure 33 shows the setup used to evaluate the product as an SSB. The AD8346 motherboard had circuitry that converted the single-ended I and Q inputs from the arbitrary function generator to differential inputs with a dc bias of approximately 1.2 V. In addition, the motherboard also provided connections for power supply routing. The HP34970A and its associated plug-in 34901 were used to monitor power supply currents and voltages being supplied to the AD8346 evaluation board (a full schematic of the AD8346 evaluation board can be found in Figure 30). The two HP34907 plug-ins were used to provide additional miscellaneous dc and control signals to the motherboard. The LO was driven by an RF signal generator (through the balun on the evaluation board to present a differential LO signal to the device) and the output was measured with a spectrum analyzer. With the I channel driven with a sine wave and the Q channel driven with a cosine wave, the lower sideband is the single sideband output. The typical SSB output spectrum is shown in Figure 34.

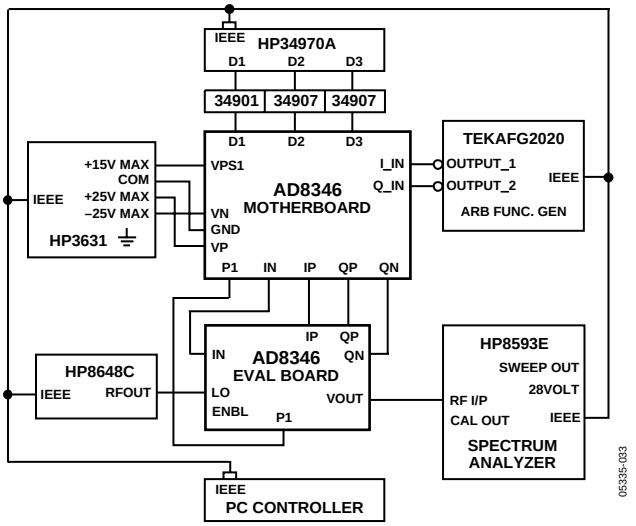

Figure 33. Evaluation Board SSB Test Setup

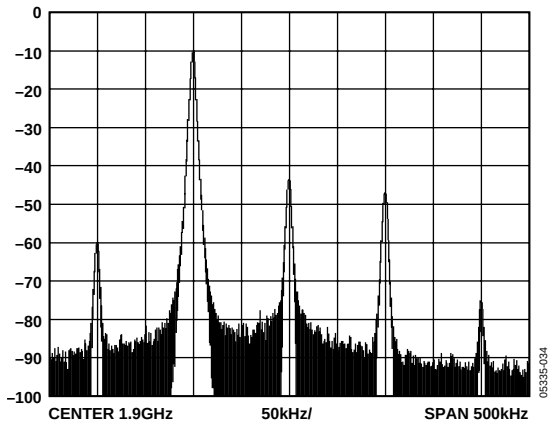

Figure 34. Typical SSB Output Spectrum

CDMA SETUP

For evaluating the AD8346 with CDMA waveforms, the setup shown in Figure 35 was used. This is essentially the same setup as that used for the single sideband characterization, except that the AFG2020 was replaced with the AWG2021 for providing the I and Q input signals, and the spectrum analyzer used to monitor the output was changed to an FSEA30 Rohde & Schwarz analyzer with vector demodulation capability. The I/Q input signals for these measurements were IS95 baseband signals generated with Tektronix I/Q SIM software and downloaded to the AWG2021.

For measuring ACPR, the I/Q input signals used were generated with Pilot (Walsh Code 00), Sync (WC 32), Paging (WC 01), and 6 Traffic (WC 08, 09, 10, 11, 12, 13) channels active. The I/Q SIM software was set for 32× oversampling and was using a BS equifilter. Figure 36 shows the typical output spectrum for this configuration. The ACPR was measured 885 kHz away from the carrier frequency.

For performing EVM, Rho, phase, and amplitude balance measurements, the I/Q input signals used were generated with only the pilot channel (Walsh Code 00) active. The I/Q SIM software was set for 32× oversampling using a CDMA equifilter.

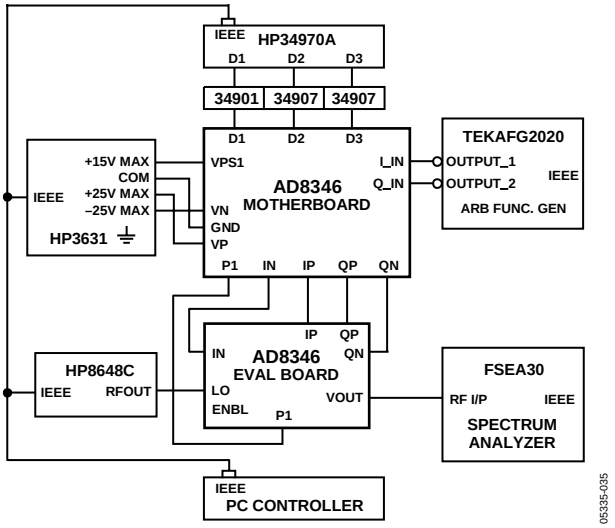

Figure 35. Evaluation Board CDMA Test Setup

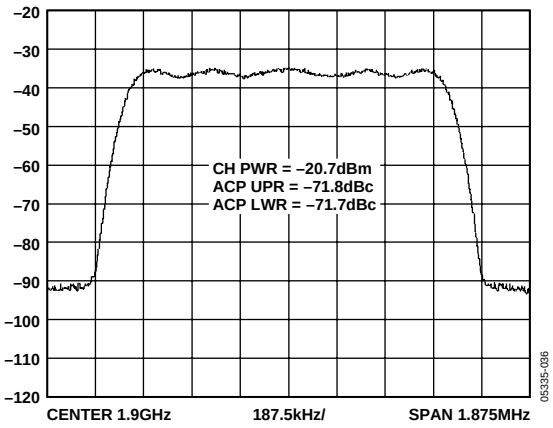

Figure 36. Typical CDMA Output Spectrum

OUTLINE DIMENSIONS

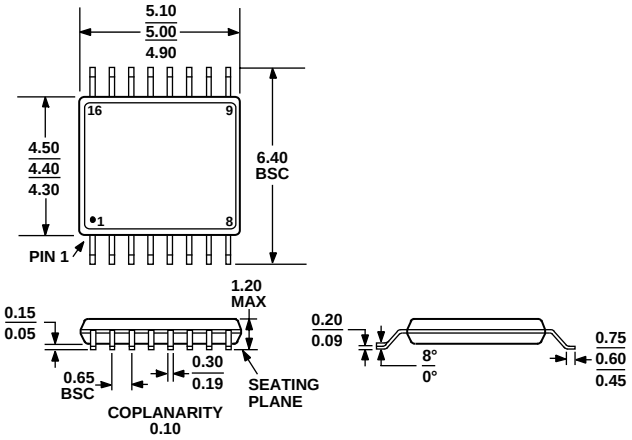

Figure 37.16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8346ARU	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
AD8346ARU-REEL	−40°C to +85°C	16-Lead (TSSOP) 13" Tape and Reel	RU-16
AD8346ARU-REEL7	−40°C to +85°C	16-Lead (TSSOP) 7" Tape and Reel	RU-16
AD8346ARUZ-REEL[1]	−40°C to +85°C	16-Lead (TSSOP) 13" Tape and Reel	RU-16
AD8346ARUZ-REEL7[1]	−40°C to +85°C	16-Lead (TSSOP) 7" Tape and Reel	RU-16
AD8346-EVAL		Evaluation Board	

[1] Z = Pb-free part.

NOTES

NOTES

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