IS31LT3948

PFM Mode Boost LED Driver With the External NMOS

December 2012

General Description

The IS31LT3948 is a PFM step-up DC-DC converter designed for driving the white LED arrays for large size LCD panel backlighting applications. It can deliver stable constant output current from a few milliamps up to 2A, programmed via an external resistor.

The IS31LT3948 utilizes a control scheme in which the output is automatically adjusted to the optimum output voltage for the system, maximizing the efficiency. Furthermore, the control scheme is inherently stable removing the need to provide additional loop compensation.

The device features external PWM dimming, which allows the flexible control of the back-lighting luminance.

The IS31LT3948 has a wide input voltage range from 5V to 100V *(Note)*. An integrated OVP circuit protects the chip and the system even under no-load conditions.

Note: The IS31LT3948 has an internal 5V shunt regulator connected to the VCC pin. A dropping resistor must be connected between the VCC pin and VIN to limit current flow. VIN voltages above 100V are allowed but care must be taken to ensure that the output voltage remains greater than VIN, and that the NMOS voltage rating is sufficiently large.

Features

- Wide input voltage range: 5V-100V
- Constant Current Output limited only by external component selection (*Note*)
- No loop compensation required
- Internal over-voltage protection
- Internal over-temperature protection
- Operating temperature range -40°C to 85°C
- SOP-8 package

Note: The maximum output current is determined by Vout/Vin ratio as well as the external components. If output current and Vout/Vin ratio is high, high current components of inductor and NMOS are needed.

Applications

- TV Monitor Backlighting,
- Notebook
- Automotive
- Street Lamp
- LED Lighting

Typical Operating Circuit

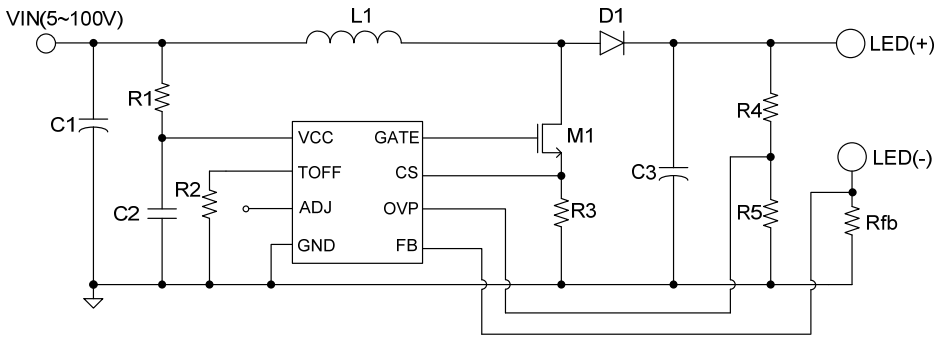
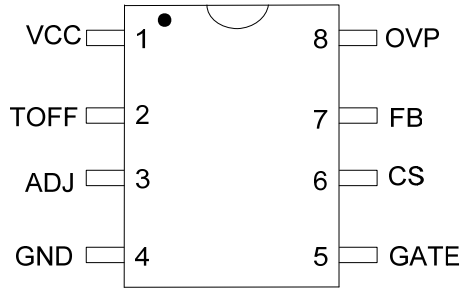


Figure 1 Typical Operating Circuit

Pin Configurations

Package	Top View
SOP-8	

Pin Descriptions

Pin	Name	Function
1	VCC	Positive power supply input pin. Internally clamped at 5V (typical).
2	TOFF	Off time setting pin. An external resistor connected to this PIN forms an RC discharge path to generate a constant minimum off time of the NMOS
3	ADJ	Enable and input peak current control pin. Pulled up to 4.5V internally to set V_{CSTH} =0.24V when ADJ is floating. If V_{ADJ}<0.5V, NMOS will always shutdown. If 0.5≤V_{ADJ}≤2.4V, V_{CSTH} = V_{ADJ}/10. If V_{ADJ}>2.4V, V_{CSTH} =0.24V. Note: During the start up(VCC voltage is rising), ADJ must not be connected to low(recommended floating).
4	GND	Ground
5	GATE	Driver's output for the gate of the external NMOS
6	CS	Current sense input for the boost, peak current control loop
7	FB	Feedback voltage input pin. Used to regulate the current of LEDs by keeping VFB=0.3V.
8	OVP	Overvoltage protection input pin., if the voltage of OVP exceed 1V, Gate will always shutdown

Ordering Information

Order Part No.	Package	QTY/Reel
IS31LT3948-GRLS2-TR	SOP-8, Lead-free	2500

Absolute Maximum Ratings

Parameter	Value
VCC to GND	-0.3V to 6V
CS, ADJ,GATE,TOFF,OVP,FB	-0.3V to 6V
VCC Max. Input Current*(note)*	10mA
Junction Temperature Range	-40°C to +150°C
Storage Temperature Range	-65°C to +150°C
ESD Human Model	3500V

Note: Exceeding VCC maximum input current may cause the pin not to clamp at 5V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(Unless otherwise specified, Vin=10V, Rin=10KΩ, ADJ floating, T_{amb}=25 °C)

Symbol	Parameter	Conditions	spec			Unit
			Min	Typ	Max	
V_{INDC}	Input voltage	Supply voltage connected to V_{CC} via a appropriate resistor *(Note)*	5		100	V
V_{CC}	V_{CC} clamp voltage	Rin=10KOhm	4.3	5	5.6	V
UVLO	Undervoltage threshold	V_{CC} rising	2.0	2.7	3.0	V
ΔUVLO	Undervoltage threshold hysteresis			300		mV
I_{SS}	Quiescent supply current	V_{CC}= V_{CC} clamp voltage		250	400	uA
	Quiescent supply current when V_{CC} undervoltage	V_{CC}=2.5V		50	75	uA
V_{CSTH}	Peak current sense threshold	ADJ=5V	215	240	265	mV
T_{BLANK}	Peak current sense blank interval	V_{CS}=V_{CSTH}+50mV		500		ns
T_{OFF}	Fixed turn-off interval	Rext=250KΩ		10		us
V_{ADJ}	Peak current control low threshold			0.5		V
	Peak current control high threshold			2.4		V
T_{SD}	Thermal shutdown threshold			150		°C
T_{SD-HYS}	Thermal shutdown hysteresis			20		°C
V_{fbTH}	Feedback voltage threshold		0.29	0.3	0.31	V
V_{OVP-TH}	Overvoltage input threshold		0.9	1	1.1	V

Note: VIN is the input voltage. When VIN≤5V, connect input voltage directly to Vcc. When VIN>5V, input voltage should be connected to Vcc pin via an appropriately valued resistor.

Typical Performance Characteristics

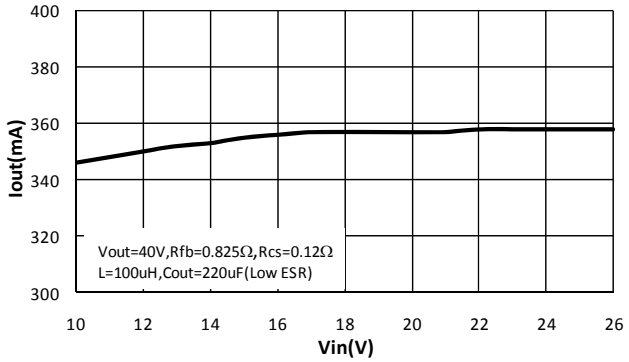


Figure 2. Vin & Iout

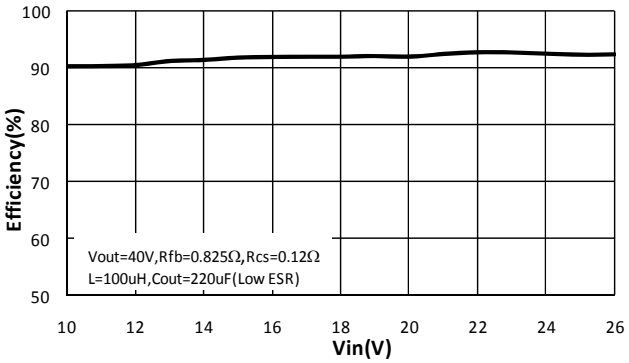


Figure 3. Vin & Efficiency

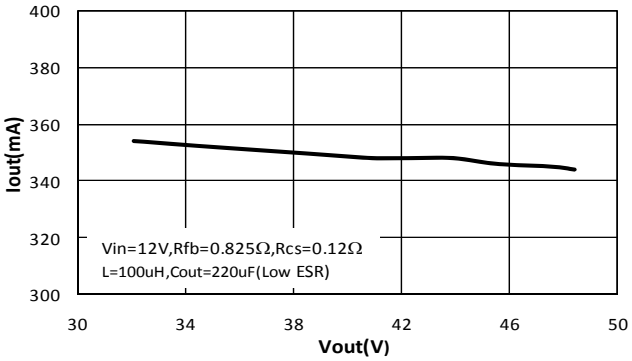


Figure 4. Vout & Iout

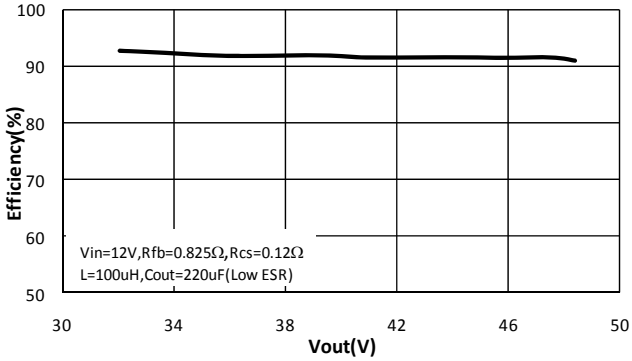


Figure 5. Vout & Efficiency

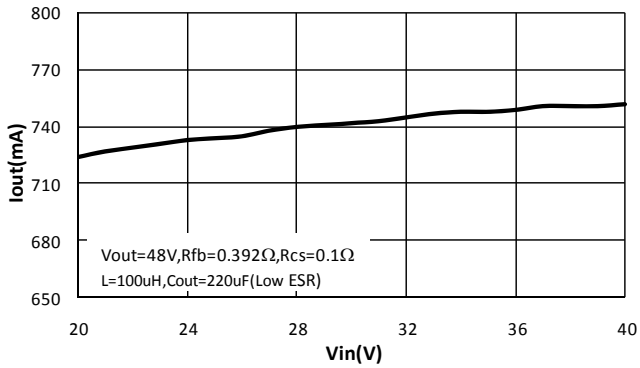


Figure 6. Vin & Iout

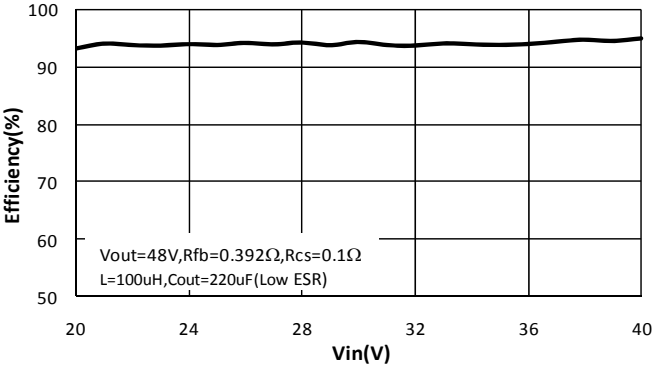


Figure 7. Vin & Efficiency

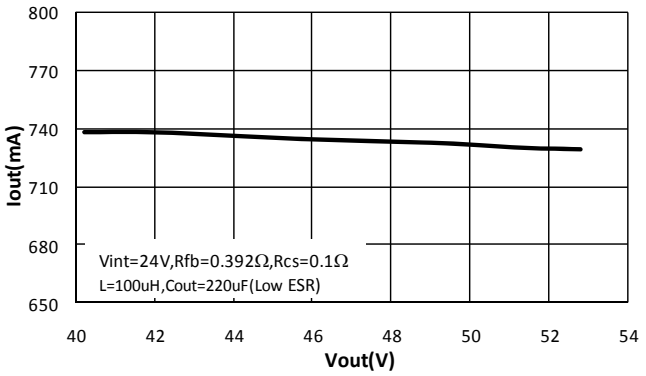


Figure 8. Vout & Iout

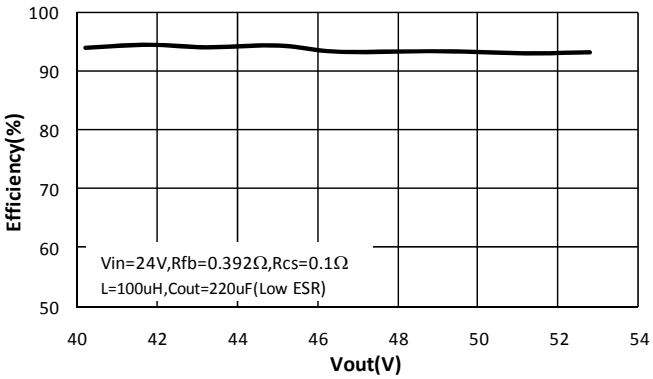


Figure 9.Vout & Efficiency

Application Information

Internal 5V Regulator

The IS31LT3948 includes an internal shunt regulator of 5V (typical) connected to the V_{CC} pin. When the input voltage is higher than 5V, connect V_{CC} to VIN using an appropriately valued, current limiting resistor. The regulator maintains a 5V power supply for the internal NMOS switch gate driver and the internal control circuitry. In applications where the input voltage is 5V, connect the input voltage directly to V_{CC}. When V_{CC} is connected directly to VIN, VIN may not exceed 5V. Bypass the V_{CC} pin using a low ESR capacitor (recommended 10μF ceramic capacitor) to provide a high frequency path to GND.

The current required by IS31LT3948 is 0.25mA (typical) plus the switching current of the external switch. The switching frequency of the external NMOS affects the amount of current required, as does the NMOS's gate charge requirement (found on the NMOS data sheet).

$$I_{IN} \approx 0.25mA + Q_G \times f_S \qquad (1)$$

Where f_S is the switching frequency and Q_G is the external NMOS gate charge.

Under Voltage Lockout

IS31LT3948 features an under voltage lockout threshold of 2.7V (typical) with a hysteresis of 300mV. The chip is disabled when V_{CC} is lower than 2.4V and enabled when V_{CC} exceeds 2.7V.

Step-up Converter

IS31LT3948's step-up converter uses a peak current mode topology wherein the CS pin voltage determines the peak current in the inductor of the converter and hence the duty cycle of the GATE switching waveform. The basic loop uses a pulse from an internal oscillator to set an RS flip-flop and turn on the external power NMOS. After the blanking time, the inductor current is sensed during the GATE on period by a sense resistor, R_{CS}, in the source of the external power NMOS. The current increases in the NMOS and inductor until the voltage across the sense resistor reaches the CS threshold, at which time NMOS is turned off. Once the NMOS is turned off, the inductor reverses polarity, providing the voltage boost, and the current of inductor will decrease until the FB pin voltage drops below internal reference voltage and the NMOS is then turned on again. This operation repeats each cycle.

Note: In the case where the FB pin voltage does not exceed the FB reference voltage of 0.3V, such as at start-up, the NMOS will remain off for the programmed minimum TOFF time, then the NMOS is switched on again.

LED Current Control

IS31LT3948 regulates the LED current by sensing the voltage across an external sense resistor in series with the LEDs. The voltage is sensed via the FB pin where the internal feedback reference voltage is 0.3V(typical). The LED current can be set from following equation easily.

$$I_{out} = \frac{0.3}{R_{fb}} \qquad (2)$$

In order to have an accurate LED current, precision resistors are required (1% is recommended).

Setting the Over Voltage Protection

The open string protection is achieved through the over voltage protection (OVP). In some cases, an LED string failure results in a feedback voltage that is always zero. If this happens, the part then keeps boosting the output voltage higher and higher. If the output voltage reaches the programmed OVP threshold, the protection will be triggered and stop the switching action. To make sure that the circuit functions properly, the OVP setting resistor divider must be set with an appropriate value. The recommended V_{OVP} point is about 1.2 times or 5V (choose the larger one) higher than the output voltage for normal operation.

$$V_{OVP} = V_{OVP-TH} \times \frac{R_4 + R_5}{R_5} \qquad (3)$$

Where, V_{OVP-TH} is 1V, and V_{OVP} is the output voltage OVP level.

Dimming Control

There are two methods for dimming.

1) External NMOS PWM dimming:

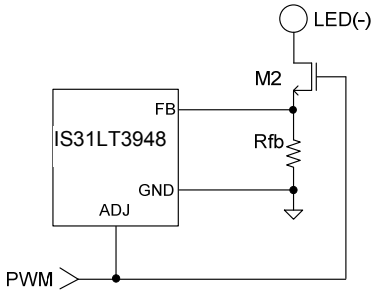


Figure 10

When the PWM input is high (V_H>2.4V), M2 is on and IS31LT3948 operates normally to regulate the output current. When PWM is low logic (V_L<0.5V), M2 is off and IS31LT3948 is shutdown. Using a fixed frequency PWM signal and changing the duty cycle adjusts the average output current. The recommended 5V PWM frequency is between 200Hz and 1KHz. M2 is recommended to use AP2306.

2) RC filter PWM dimming:

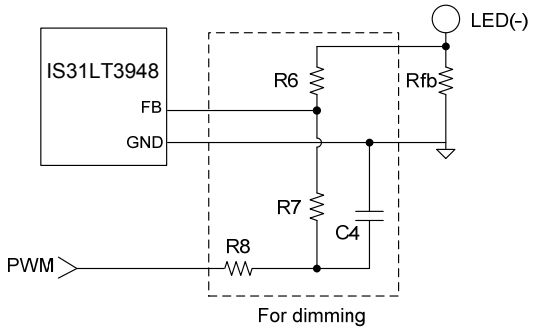


Figure 11

A filtered PWM signal can be used as an adjustable DC voltage for LED dimming control. The filtered PWM signal becomes DC voltage which is summed together with the FB voltage to regulate the output current. Fix the frequency of the PWM signal and change the duty cycle to adjust the LED current. The LED current can be calculated by the following equation:

$$Iout = \frac{V_{fbTH} - R6 \times (V_{PWM} \times Duty - V_{fbTH})/(R7 + R8)}{Rfb} \quad (4)$$

The PWM duty cycle is inversely proportional to the LED current. That is, when the PWM signal is 100% duty cycle, the output current is minimum, ideally zero, and when the PWM signal is 0% duty cycle, the output current is maximum.

See details value in the Example section.

Note: When the V_{OUT}/V_{IN} ratio is less than 2, careful consideration must be given to ensure that V_{OUT} remains greater than V_{IN} at the minimum dimming level.

Input Peak Current control

IS31LT3948 limits the peak inductor current, and thus peak input current through the feedback of R3 connected from source of NMOS to ground. The required average input current is based on the boost ratio, Vout/Vin, and the designed value for average LED current. The required average input current can be calculated as:

$$I_{avg(IN)} = \frac{V_{out} \times I_{out}}{V_{in} \times \eta} \quad (5)$$

η: assumed power conversion efficiency (the recommended value is 0.9)

Generally, setting the peak inductor current to 1.5 times the average input current is sufficient to maintain a good regulation of the output current.

$$I_{peak(IN)} = 1.5 \times I_{avg(IN)} = \frac{V_{CSTH}}{R_{CS}} \quad (6)$$

V_{CSTH}: If 0.5<V_{ADJ}<2.4V, V_{CSTH} = V_{ADJ}/10. If V_{ADJ}>2.4V, V_{CSTH} =0.24V. ADJ floating, V_{CSTH}=0.24V.

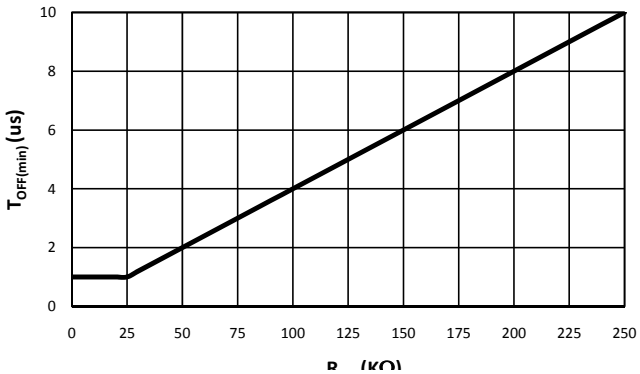
Input Capacitor

The input capacitor of the IS31LT3948 will supply the transient input current of the power inductor. Value of 100μF or higher is recommended to prevent excessive input voltage ripple.

Setting $T_{OFF(min)}$

IS31LT3948 operates in a pulsed frequency modulation mode. The boost control loop is a constant off-time architecture. The off time is programmable and set by an external resistor connected between the T_{OFF} pin and GND. In most application, the recommended $T_{OFF(min)}$ is 1μs. The governing equation for the off time is:

$$T_{OFF(min)} = 40 \times 10^{-12} \times R_{EXT} \quad (7)$$



Note: The minimum $T_{OFF(min)}$ is 1μs.

Inductor Selection

Inductor value directly determines the switching frequency of the converter. To the fixed condition and the larger inductor value the lower switching frequency. The higher frequency will reduce the value of inductor, but will increase the switching loss on NMOS.

The switching frequency can be calculated blow.

Switching frequency: $f = 1/(T_{ON} + T_{OFF})$ (8)

The current ripple in the inductor:

$$I_{Ripple} = 2 \times (I_{peak(IN)} - I_{avg(IN)}) \quad (9)$$

NMOS on time:

$$T_{ON} = \frac{I_{Ripple} \times L}{V_{in} - I_{avg(IN)} \times (R_L + R_{DS(ON)} + R_{CS})} \quad (10)$$

NMOS off time:

$$T_{OFF} = \frac{I_{Ripple} \times L}{V_{out} + V_D - V_{in} - I_{avg(IN)} \times R_L} \quad (11)$$

Note: the selection of inductor must ensure that the T_{OFF} larger than the $T_{OFF(min)}$,or else the converter can not output the required current.

Where:

V_{in}: Input voltage (V)

V_{out}: Output voltage (V)
I_{Ripple}: Current ripple in the inductor (A)
L: inductor value (H)
$I_{peak(IN)}$: Input peak current (A)
$I_{avg(IN)}$: Input average current (A)
R_L: Inductor DCR (Ω)
$R_{DS(ON)}$: NMOS on resistance (Ω)
V_D: diode forward voltage at the required load current (V)
The recommended switching frequency: 20KHz < f < 200KHz (Lower than 20KHz will cause audio noice of the inductor and too high frequency will increase the switching loss on NMOS).
To the fixed V_{in}, V_{out}, $I_{avg(IN)}$, $I_{peak(IN)}$ and the switching frequency is inversely proportional to the inductor value. Select an inductor with a rating current over input average current and the saturation current over the calculated peak current. To calculate the worst case inductor peak current, use the minimum input voltage, maximum output voltage, and maximum total LED current. Also ensure that the inductor has a low DCR (copper wire resistance) to minimize I^2R power loss.

Output Capacitor
The output capacitor holds the output current during NMOS on. The capacitor directly impacts the line regulation and the loading regulation.
Low ESR capacitors using at the IS31LT3948 converter output can minimize output ripple voltage and improve output current regulation. For most applications, a 220μF low ESR capacitor will be sufficient. Proportionally lower ripple can be achieved with higher capacitor values.

Schottky Rectifier
The external diode for the IS31LT3948 must be a Schottky diode, with low forward voltage drop and fast switching speed. The diode's average current rating must exceed the application's average output current. The diode's maximum reverse voltage rating must exceed the over voltage protection of the application. For PWM dimming applications, be aware of the reverse leakage of the Schottky diode. Lower leakage current will drain the output capacitor less during PWM low periods, allowing for higher PWM dimming ratios.

Power NMOS Selection
The power NMOS selected should have a V_{DS} rating which exceeds the maximum over voltage protection (OVP) level programmed for the application. The $V_{GS(th)}$ of NMOS should be not higher than 4V. The $R_{DS\ (ON)}$ of the NMOS will determine DC power loss. The DC power loss can be calculated by:

$$P_{loss} = I_{M1}{}^2 \times R_{DS(ON)} = \left(\frac{V_{out} \times I_{out} \times Duty}{V_{in} \times \eta} \right)^2 \times R_{DS(ON)} \quad (12)$$

The recommended NMOS rating current is 5 times (or higher) to the input peak current ($I_{peak(IN)}$). Be aware of the power dissipation within the NMOS and deciding if the thermal resistance of the NMOS package causes the junction temperature to exceed maximum ratings.

PCB layout consideration
As for all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If layout is not carefully done, the regulator could show instability as well as EMI problems.

- Wide traces should be used for connection of the high current loop to minimize the EMI and unnecessary loss.
- The external components ground should be connected to IS31LT3948 ground as short as possible. Especially the R_{fb} ground to IS31LT3948 ground connection should be as short and wide as possible to have an accurate LED current.
- The capacitor C1, C2, C3 should be placed as close as possible to IS31LT3948 for good filtering. Especially the output capacitor C3 connection should be as short and wide as possible.
- NMOS drain is a fast switching node. The inductor and Schottky diode should be placed as close as possible to the drain and the connection should be kept as short and wide as possible. Avoid other traces crossing and routing too long in parallel with this node to minimize the noise coupling into these traces. The feedback pin (e.g. CS, FB, OVP) should be as short as possible and routed away from the inductor, the schottky diode and NMOS. The feedback pin and feedback network should be shielded with a ground plane or trace to minimize noise coupling into this circuit.
- The thermal pad on the back of NMOS package must be soldered to the large ground plane for ideal power dissipation.

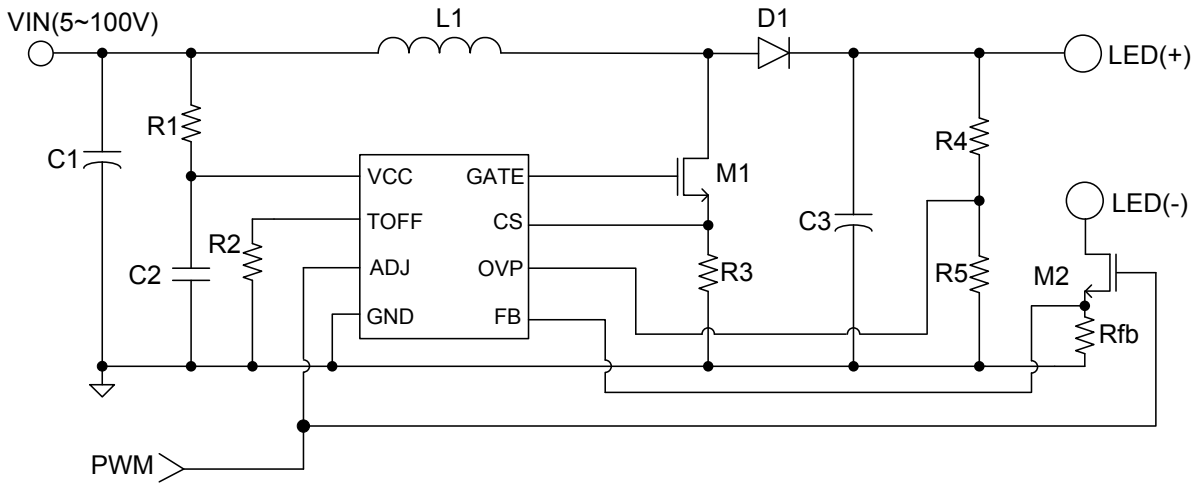


Figure.12 External NMOS PWM dimming

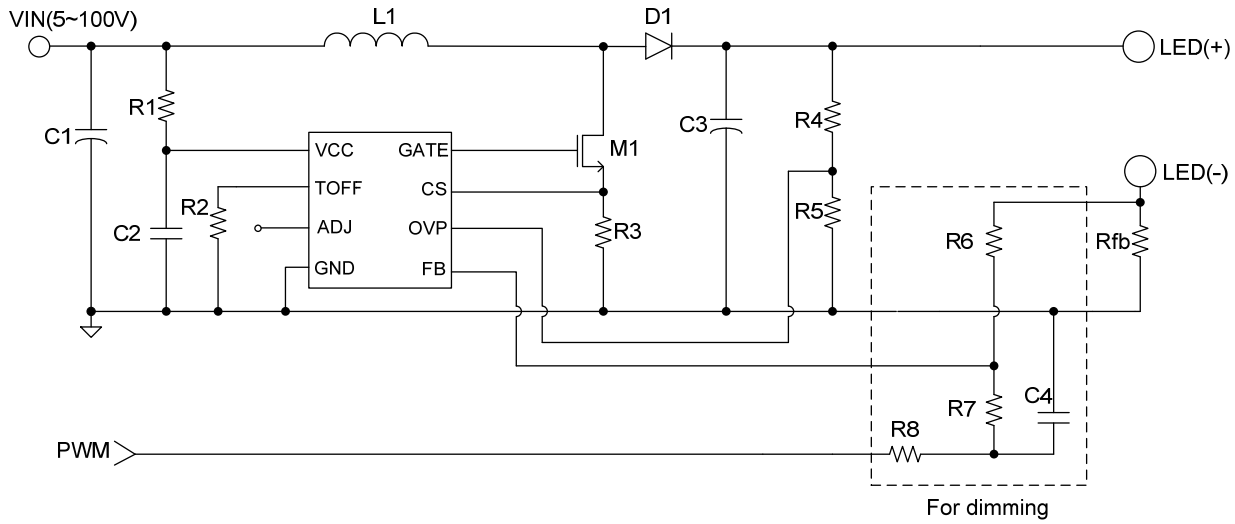


Figure.13 RC filter PWM dimming

Example
Input: Vin = 12~24V
Output: Iout = 350mA, Vout≈30~40V (9~12LEDs, Vf=3.3V)

To calculate the worst case parameter, use the minimum input voltage, the maximum output voltage, and maximum output current. So choose: Vin = 12V, Iout = 350mA, Vout≈40V (12LEDs, Vf=3.3V)

1. R1 and C1&C2
Assume Iin = 2.5mA

$$R1 = \frac{Vin - Vcc}{Iin} \approx 3k\Omega$$

→ Choose C1 as 220μF/35V
C2 as 10μF/16V

2. R2 to set minimal-TOFF
The recommended value is 1μs

$$T_{OFF(\min)} = 40 \times 10^{-12} \times R_{EXT} = 1\mu s$$

→ Choose R2 = 24kΩ

3. Rfb to set output current and C3

$$Rfb = \frac{V_{fbTH}}{Iout} \approx 0.86\Omega$$

→ Choose C3 = 220μF/63V (Low ESR electrolytic capacitor)

4. R6, R7, R8 and C4
R6、R7、R8 can be calculate by:

$$Iout = \frac{V_{fbTH} - R6 \times (V_{PWM} \times Duty - V_{fbTH}) / (R7 + R8)}{Rfb}$$

Take Duty=100%, V_{PWM} = 5V and Iout=0 into the equation, then we have:

$$0 = \frac{0.3 - R6 \times (5 \times 100\% - 0.3) / (R7 + R8)}{0.86}$$

Which Simplifies to:

$$15.66 \times R6 = R7 + R8$$

The lowpass filter formed by R8 & C4 must have a corner frequency much lower than the PWM frequency. As the corner frequency of the filter decreases, the response time of the LED current to changes in PWM increases. Choose a corner frequency 50 times lower than f_{PWM}.

$$R8 \times C4 \geq \frac{50}{2\pi f_{PWM}}$$

Assuming f_{PWM} is 200Hz (or higher), and choosing C4 = 0.1μF, we find R8 ≥ 400kΩ.
→ Choose C4 = 0.1μF, R8 = 400kΩ.
Choose a nominal value for R7, then compute R6.
→ Choose R7 = 10kΩ, then R6 = 26.2kΩ
Take Duty=0, V_{PWM} = 5V and Iout=350mA into the equation, then we have:

$$Iout = \frac{V_{fbTH} - R6 \times (V_{PWM} \times Duty - V_{fbTH}) / (R7 + R8)}{Rfb}$$

$$= \frac{0.3 - 26.2 \times (5 \times 0\% - 0.3) / (400 + 10)}{Rfb} = 0.35A$$

So R_{fb}=0.91Ω (With the RC filter PWM dimming, the R_{fb} will be different from the no dimming application.)

4. R3 to set input peak current
Assume: $I_{peak(IN)} = 1.5 \times I_{avg(IN)}$

$$I_{peak(IN)} = 1.5 \times I_{avg(IN)} = 1.5 \times \frac{V_{out} \times I_{out}}{V_{in} \times \eta}$$

$$= 1.5 \times \frac{40 \times 0.35}{12 \times 0.9} \approx 1.95A$$

η: assumed power conversion efficiency (the recommended value is 0.9)

$$R_{cs} = \frac{V_{CSTH}}{I_{peak(IN)}} = 0.123\Omega$$

→ Choose R3=0.123Ω, Ipeak=1.95A

5. L1 to set frequency

Input average current: $I_{avg(IN)} = \frac{V_{out} \times I_{out}}{V_{in} \times \eta} = 1.3A$

The current ripple in the inductor:

$$I_{Ripple} = 2 \times \left(I_{peak(IN)} - I_{avg(IN)}\right) = 1.3A$$

According to $T_{off} > T_{OFF(\min)}$:

$$T_{OFF} = \frac{I_{Ripple} \times L}{V_{out} + V_D - V_{in} - I_{avg(IN)} \times R_L} > 1\mu s$$

This gives L>22μH. Assuming L=22μH and $R_L + R_{DS(ON)} + R_{CS} = 0.4\Omega$.

$$T_{ON} = \frac{I_{Ripple} \times L}{V_{in} - I_{avg(IN)} \times (R_L + R_{DS(ON)} + R_{CS})} \approx 2.5\mu s$$

Then the assumed switching frequency:

$$f' = 1/\left(T_{ON} + T_{OFF}\right) \approx 285KHz$$

The recommended switching frequency:
20KHz < f < 200KHz, according to the switching frequency is inversely proportional to the inductor value, choose L=100 μH. Therefore:

$$f = f' \times \frac{22}{100} \approx 63KHz$$

The saturation current of the inductor must exceed the input peak current ($I_{peak(IN)}$).

6. R4, R5 to set OVP

Set V_{OVP} = Vout+5V = 45V

$$V_{OVP} = V_{OVP-TH} \times \frac{R_4 + R_5}{R_5}$$

→Choose R5=10kΩ, then R4 = 470kΩ.

7. NMOS M1 and diode D1

$I1_{(NMOS)} > I_{peak\ (IN)}$

$V1_{(NMOS)} > V_{OVP}$

Lower $R_{DS(on)}$ NMOS can improve the converter efficiency. The recommended NMOS rating current is 5 times (or higher) to the input peak current ($I_{peak(IN)}$).

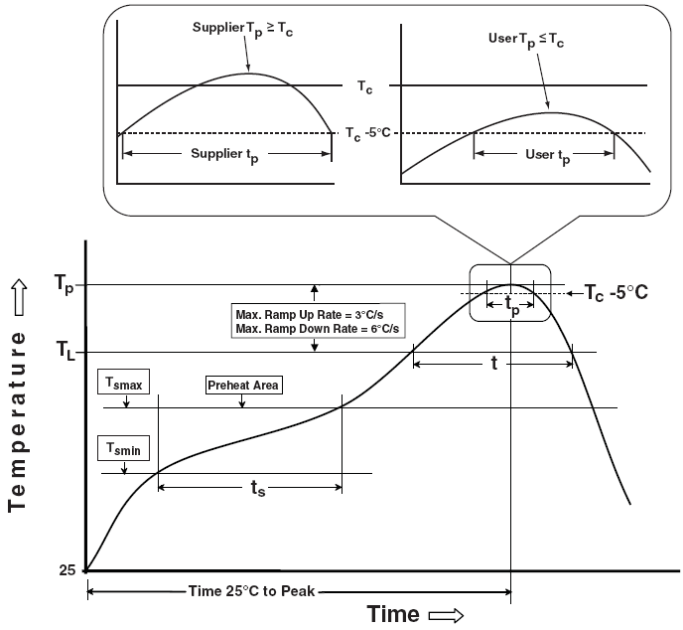
→ Choose 13N10L as M1

The average and peak current of diode must exceed the output average current and input peak current. The diode's maximum reverse voltage rating must exceed the over voltage protection of the application.

→ Choose SS310 as D1

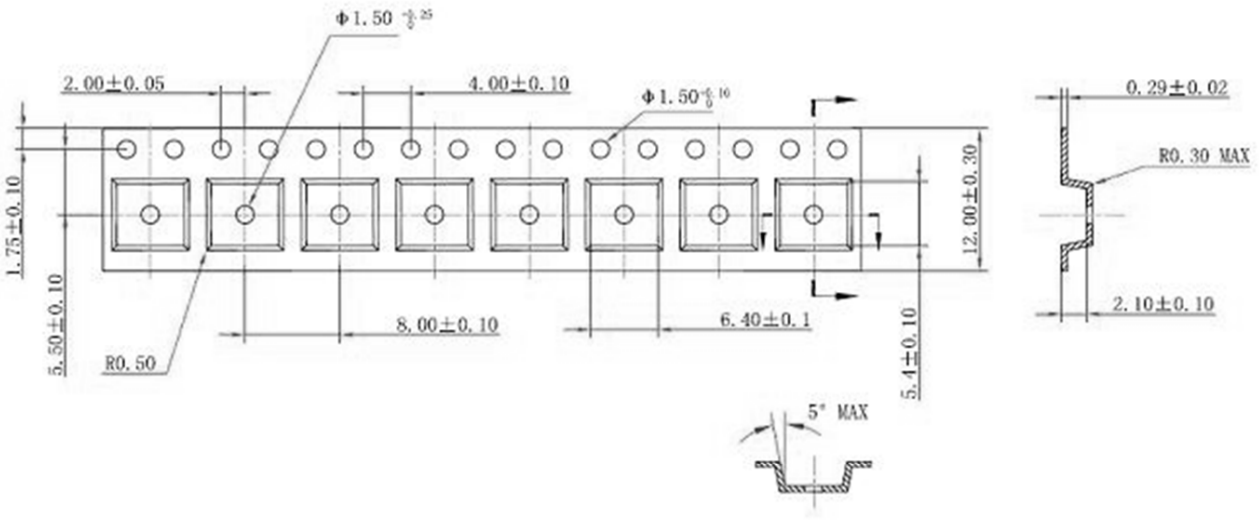
Classification Reflow Profiles

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.



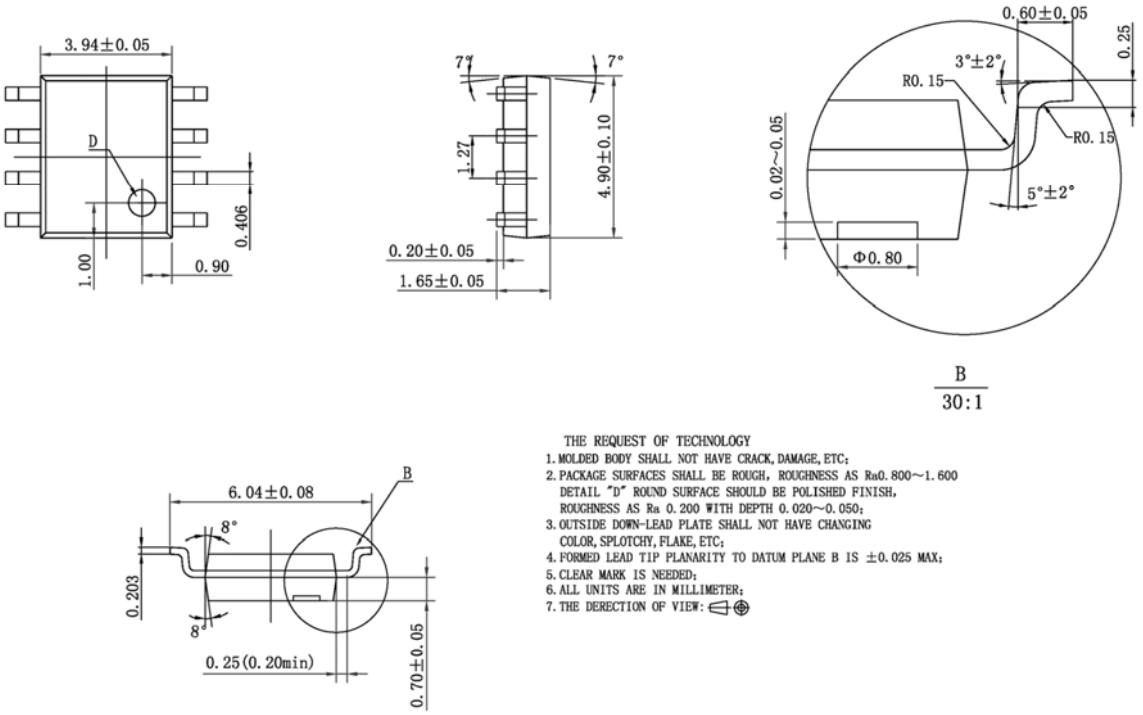
Classification Profile

Tape and Reel Information



NOTES:

1.CARRIER TAPE COLOR:BLACK
2.COVER TAPE WIDTH:9.50±0.10
3.COVER TAPE COLOR:TRANSPARENT
4. SURFACE ANTISTATIC COATED 10^{5} ~ 10^{11} OHMS/SQ.
5.10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.20MAX.
6. IN A REEL CARRIER THE THICKNESS CUMULATIVE TOLERANCE ±0.05MAX.
7.CAMBER NOT TO EXCEED 1 MM IN 100 MM(载带直线弯曲度: ≤1mm/100mm.)
8.MOLD# SOP8
9.ALL DIMS IN mm.
10.THE DERECTION OF VIEW:



THE REQUEST OF TECHNOLOGY

1. MOLDED BODY SHALL NOT HAVE CRACK, DAMAGE, ETC;
2. PACKAGE SURFACES SHALL BE ROUGH, ROUGHNESS AS Ra0.800~1.600 DETAIL "D" ROUND SURFACE SHOULD BE POLISHED FINISH, ROUGHNESS AS Ra 0.200 WITH DEPTH 0.020~0.050;
3. OUTSIDE DOWN-LEAD PLATE SHALL NOT HAVE CHANGING COLOR, SPLOTCHY, FLAKE, ETC;
4. FORMED LEAD TIP PLANARITY TO DATUM PLANE B IS ±0.025 MAX;
5. CLEAR MARK IS NEEDED;
6. ALL UNITS ARE IN MILLIMETER;
7. THE DERECTION OF VIEW: