RF PLL Frequency Synthesizers

Data Sheet

ADF4110/ADF4111/ADF4112/ADF4113

FEATURES

- ADF4110: 550 MHz; ADF4111: 1.2 GHz; ADF4112: 3.0 GHz; ADF4113: 4.0 GHz
- 2.7 V to 5.5 V power supply
- Separate charge pump supply (V_P) allows extended tuning voltage in 3 V systems
- Programmable dual-modulus prescaler 8/9, 16/17, 32/33, 64/65
- Programmable charge pump currents
- Programmable antibacklash pulse width
- 3-wire serial interface
- Analog and digital lock detect
- Hardware and software power-down mode

APPLICATIONS

- Base stations for wireless radio (GSM, PCS, DCS, CDMA, WCDMA)
- Wireless handsets (GSM, PCS, DCS, CDMA, WCDMA)
- Wireless LANS
- Communications test equipment
- CATV equipment

GENERAL DESCRIPTION

The ADF4110 family of frequency synthesizers can be used to implement local oscillators in the upconversion and downconversion sections of wireless receivers and transmitters. They consist of a low noise digital PFD (phase frequency detector), a precision charge pump, a programmable reference divider, programmable A and B counters, and a dual-modulus prescaler (P/P + 1). The A (6-bit) and B (13-bit) counters, in conjunction with the dual-modulus prescaler (P/P + 1), implement an N divider (N = BP + A). In addition, the 14-bit reference counter (R counter) allows selectable REFIN frequencies at the PFD input. A complete phase-locked loop (PLL) can be implemented if the synthesizer is used with an external loop filter and voltage controlled oscillator (VCO).

Control of all the on-chip registers is via a simple 3-wire interface. The devices operate with a power supply ranging from 2.7 V to 5.5 V and can be powered down when not in use.

FUNCTIONAL BLOCK DIAGRAM

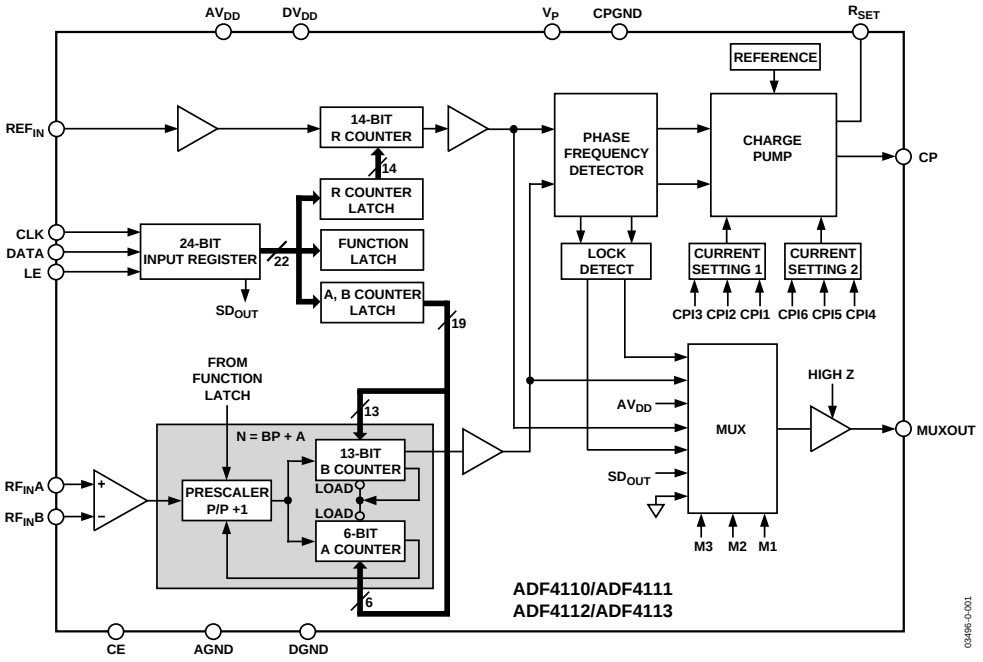

Figure 1. Functional Block Diagram

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support
www.analog.com

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SPECIFICATIONS

AV_{DD} = DV_{DD} = 3 V ± 10%, 5 V ± 10%; $AV_{DD} \le V_P \le 6.0$ V; AGND = DGND = CPGND = 0 V; R_{SET} = 4.7 kΩ; dBm referred to 50 Ω; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Operating temperature range is as follows: B Version: −40°C to +85°C.

Table 1.

Parameter	B Version	B Chips[1]	Unit	Test Conditions/Comments
RF CHARACTERISTICS (3 V)				See Figure 29 for input circuit.
RF Input Sensitivity	−15/0	−15/0	dBm min/max	
RF Input Frequency				
ADF4110	80/550	80/550	MHz min/max	For lower frequencies, ensure slew rate (SR) > 30 V/µs.
ADF4110	50/550	50/550	MHz min/max	Input level = −10 dBm.
ADF4111	0.08/1.2	0.08/1.2	GHz min/max	For lower frequencies, ensure SR > 30 V/µs.
ADF4112	0.2/3.0	0.2/3.0	GHz min/max	For lower frequencies, ensure SR > 75 V/µs.
ADF4112	0.1/3.0	0.1/3.0	GHz min/max	Input level = −10 dBm.
ADF4113	0.2/3.7	0.2/3.7	GHz min/max	Input level = −10 dBm. For lower frequencies, ensure SR > 130 V/µs.
Maximum Allowable Prescaler Output Frequency[2]	165	165	MHz max	
RF CHARACTERISTICS (5 V)				
RF Input Sensitivity	−10/0	−10/0	dBm min/max	
RF Input Frequency				
ADF4110	80/550	80/550	MHz min/max	For lower frequencies, ensure SR > 50 V/µs.
ADF4111	0.08/1.4	0.08/1.4	GHz min/max	For lower frequencies, ensure SR > 50 V/µs.
ADF4112	0.1/3.0	0.1/3.0	GHz min/max	For lower frequencies, ensure SR > 75 V/µs.
ADF4113	0.2/3.7	0.2/3.7	GHz min/max	For lower frequencies, ensure SR > 130 V/µs.
ADF4113	0.2/4.0	0.2/4.0	GHz min/max	Input level = −5 dBm.
Maximum Allowable Prescaler Output Frequency[2]	200	200	MHz max	
REFIN CHARACTERISTICS				
REFIN Input Frequency	5/104	5/104	MHz min/max	For f < 5 MHz, ensure SR > 100 V/µs.
Reference Input Sensitivity	0.4/AV_{DD}	0.4/AV_{DD}	V p-p min/max	AV_{DD} = 3.3 V, biased at AV_{DD}/2. See Note 3.
	3.0/AV_{DD}	3.0/AV_{DD}	V p-p min/max	AV_{DD} = 5 V, biased at AV_{DD}/2. See Note [3].
REFIN Input Capacitance	10	10	pF max	
REFIN Input Current	±100	±100	µA max	
PHASE DETECTOR FREQUENCY[4]	55	55	MHz max	
CHARGE PUMP				
I_{CP} Sink/Source				Programmable (see Table 9).
High Value	5	5	mA typ	With R_{SET} = 4.7 kΩ.
Low Value	625	625	µA typ	
Absolute Accuracy	2.5	2.5	% typ	With R_{SET} = 4.7 kΩ.
R_{SET} Range	2.7/10	2.7/10	kΩ typ	See Table 9.
I_{CP} 3-State Leakage Current	1	1	nA typ	
Sink and Source Current Matching	2	2	% typ	0.5 V ≤ V_{CP} ≤ V_P − 0.5 V.
I_{CP} vs. V_{CP}	1.5	1.5	% typ	0.5 V ≤ V_{CP} ≤ V_P − 0.5 V.
I_{CP} vs. Temperature	2	2	% typ	V_{CP} = V_P/2.
LOGIC INPUTS				
V_{INH}, Input High Voltage	0.8 × DV_{DD}	0.8 × DV_{DD}	V min	
V_{INL}, Input Low Voltage	0.2 × DV_{DD}	0.2 × DV_{DD}	V max	
I_{INH}/I_{INL}, Input Current	±1	±1	µA max	
C_{IN}, Input Capacitance	10	10	pF max	
LOGIC OUTPUTS				
V_{OH}, Output High Voltage	DV_{DD} − 0.4	DV_{DD} − 0.4	V min	I_{OH} = 500 µA.
V_{OL}, Output Low Voltage	0.4	0.4	V max	I_{OL} = 500 µA.

Parameter	B Version	B Chips[1]	Unit	Test Conditions/Comments
POWER SUPPLIES				
AV_{DD}	2.7/5.5	2.7/5.5	V min/V max	
DV_{DD}	AV_{DD}	AV_{DD}		
V_P	AV_{DD}/6.0	AV_{DD}/6.0	V min/V max	$AV_{DD} \le V_P \le 6.0$ V. See Figure 25 and Figure 26.
I_{DD}[5] ($AI_{DD} + DI_{DD}$)				
ADF4110	5.5	4.5	mA max	4.5 mA typical.
ADF4111	5.5	4.5	mA max	4.5 mA typical.
ADF4112	7.5	6.5	mA max	6.5 mA typical.
ADF4113	11	8.5	mA max	8.5 mA typical.
I_P	0.5	0.5	mA max	T_A = 25°C.
Low Power Sleep Mode	1	1	µA typ	
NOISE CHARACTERISTICS				
ADF4113 Normalized Phase Noise Floor[6]	−215	−215	dBc/Hz typ	
Phase Noise Performance[7]				@ VCO output.
ADF4110: 540 MHz Output[8]	−91	−91	dBc/Hz typ	@ 1 kHz offset and 200 kHz PFD frequency.
ADF4111: 900 MHz Output[9]	−87	−87	dBc/Hz typ	@ 1 kHz offset and 200 kHz PFD frequency.
ADF4112: 900 MHz Output[9]	−90	−90	dBc/Hz typ	@ 1 kHz offset and 200 kHz PFD frequency.
ADF4113: 900 MHz Output[9]	−91	−91	dBc/Hz typ	@ 1 kHz offset and 200 kHz PFD frequency.
ADF4111: 836 MHz Output[10]	−78	−78	dBc/Hz typ	@ 300 Hz offset and 30 kHz PFD frequency.
ADF4112: 1750 MHz Output[11]	−86	−86	dBc/Hz typ	@ 1 kHz offset and 200 kHz PFD frequency.
ADF4112: 1750 MHz Output[12]	−66	−66	dBc/Hz typ	@ 200 Hz offset and 10 kHz PFD frequency.
ADF4112: 1960 MHz Output[13]	−84	−84	dBc/Hz typ	@ 1 kHz offset and 200 kHz PFD frequency.
ADF4113: 1960 MHz Output[13]	−85	−85	dBc/Hz typ	@ 1 kHz offset and 200 kHz PFD frequency.
ADF4113: 3100 MHz Output[14]	−86	−86	dBc/Hz typ	@ 1 kHz offset and 1 MHz PFD frequency.
Spurious Signals				
ADF4110: 540 MHz Output[9]	−97/−106	−97/−106	dBc typ	@ 200 kHz/400 kHz and 200 kHz PFD frequency.
ADF4111: 900 MHz Output[9]	−98/−110	−98/−110	dBc typ	@ 200 kHz/400 kHz and 200 kHz PFD frequency.
ADF4112: 900 MHz Output[9]	−91/−100	−91/−100	dBc typ	@ 200 kHz/400 kHz and 200 kHz PFD frequency.
ADF4113: 900 MHz Output[9]	−100/−110	−100/−110	dBc typ	@ 200 kHz/400 kHz and 200 kHz PFD frequency.
ADF4111: 836 MHz Output[10]	−81/−84	−81/−84	dBc typ	@ 30 kHz/60 kHz and 30 kHz PFD frequency.
ADF4112: 1750 MHz Output[11]	−88/−90	−88/−90	dBc typ	@ 200 kHz/400 kHz and 200 kHz PFD frequency.
ADF4112: 1750 MHz Output[12]	−65/−73	−65/−73	dBc typ	@ 10 kHz/20 kHz and 10 kHz PFD frequency.
ADF4112: 1960 MHz Output[13]	−80/−84	−80/−84	dBc typ	@ 200 kHz/400 kHz and 200 kHz PFD frequency.
ADF4113: 1960 MHz Output[13]	−80/−84	−80/−84	dBc typ	@ 200 kHz/400 kHz and 200 kHz PFD frequency.
ADF4113: 3100 MHz Output[14]	−80/−82	−82/−82	dBc typ	@ 1 MHz/2 MHz and 1 MHz PFD frequency.

[1]The B chip specifications are given as typical values.
[2]This is the maximum operating frequency of the CMOS counters. The prescaler value should be chosen to ensure that the RF input is divided down to a frequency that is less than this value.
[3]AC coupling ensures AV_{DD}/2 bias. See Figure 33 for a typical circuit.
[4]Guaranteed by design.
[5] T_A = 25°C; $AV_{DD} = DV_{DD}$ = 3 V; P = 16; SYNC = 0; DLY = 0; RF_{IN} for ADF4110 = 540 MHz; RF_{IN} for ADF4111, ADF4112, ADF4113 = 900 MHz.
[6] The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO, PN_{TOT}, and subtracting 20logN (where N is the N divider value) and $10\log F_{PFD}$: $PN_{SYNTH} = PN_{TOT} - 10\log F_{PFD} - 20\log N$.
[7] The phase noise is measured with the EV-ADF411XSD1Z evaluation board and the HP8562E spectrum analyzer. The spectrum analyzer provides the REFIN for the synthesizer (f_{REFOUT} = 10 MHz @ 0 dBm). SYNC = 0; DLY = 0 (Table 7).
[8] f_{REFIN} = 10 MHz; f_{PFD} = 200 kHz; offset frequency = 1 kHz; f_{RF} = 540 MHz; N = 2700; loop B/W = 20 kHz.
[9] f_{REFIN} = 10 MHz; f_{PFD} = 200 kHz; offset frequency = 1 kHz; f_{RF} = 900 MHz; N = 4500; loop B/W = 20 kHz.
[10] f_{REFIN} = 10 MHz; f_{PFD} = 30 kHz; offset frequency = 300 Hz; f_{RF} = 836 MHz; N = 27867; loop B/W = 3 kHz.
[11] f_{REFIN} = 10 MHz; f_{PFD} = 200 kHz; offset frequency = 1 kHz; f_{RF} = 1750 MHz; N = 8750; loop B/W = 20 kHz
[12] f_{REFIN} = 10 MHz; f_{PFD} = 10 kHz; offset frequency = 200 Hz; f_{RF} = 1750 MHz; N = 175000; loop B/W = 1 kHz.
[13] f_{REFIN} = 10 MHz; f_{PFD} = 200 kHz; offset frequency = 1 kHz; f_{RF} = 1960 MHz; N = 9800; loop B/W = 20 kHz.
[14] f_{REFIN} = 10 MHz; f_{PFD} = 1 MHz; offset frequency = 1 kHz; f_{RF} = 3100 MHz; N = 3100; loop B/W = 20 kHz.

TIMING CHARACTERISTICS

Guaranteed by design but not production tested. $AV_{DD} = DV_{DD} = 3$ V ± 10%, 5 V ± 10%; $AV_{DD} \le V_P \le 6$ V; AGND = DGND = CPGND = 0 V; $R_{SET} = 4.7$ kΩ; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Limit at T_{MIN} to T_{MAX} (B Version)	Unit	Test Conditions/Comments
t_1	10	ns min	DATA to CLOCK setup time
t_2	10	ns min	DATA to CLOCK hold time
t_3	25	ns min	CLOCK high duration
t_4	25	ns min	CLOCK low duration
t_5	10	ns min	CLOCK to LE setup time
t_6	20	ns min	LE pulse width

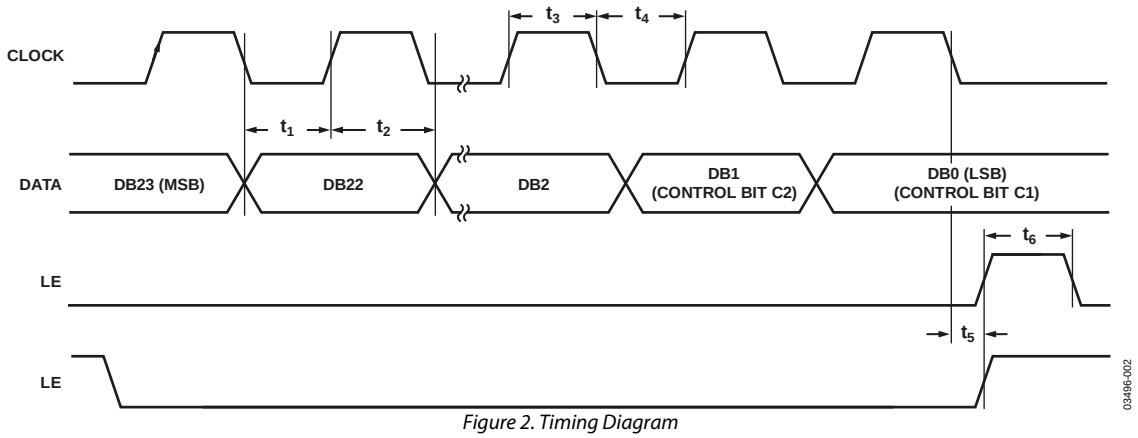

Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted

Table 3.

Parameter	Rating
AV_{DD} to GND[1]	−0.3 V to +7 V
AV_{DD} to DV_{DD}	−0.3 V to +0.3 V
V_P to GND	−0.3 V to +7 V
V_P to AV_{DD}	−0.3 V to +5.5 V
Digital I/O Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Analog I/O Voltage to GND	−0.3 V to V_P + 0.3 V
REF_{IN}, $RF_{IN}A$, $RF_{IN}B$ to GND	−0.3 V to V_{DD} + 0.3 V
$RF_{IN}A$ to $RF_{IN}B$	±320 mV
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
TSSOP θ_{JA} Thermal Impedance	150.4°C/W
LFCSP θ_{JA} Thermal Impedance (Paddle Soldered)	122°C/W
LFCSP θ_{JA} Thermal Impedance (Paddle Not Soldered)	216°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

[1] GND = AGND = DGND = 0 V.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance RF integrated circuit with an ESD rating of <2 kV, and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

TRANSISTOR COUNT

6425 (CMOS) and 303 (Bipolar).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

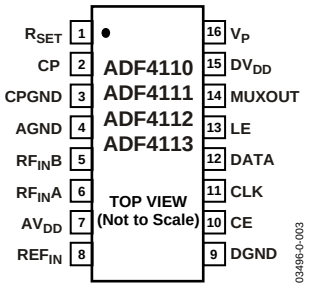

Figure 3. TSSOP Pin Configuration

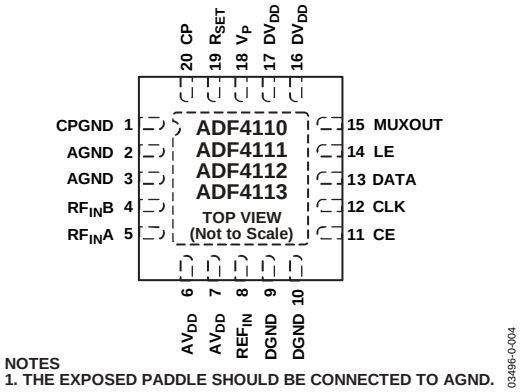

Figure 4. LFCSP Pin Configuration

Table 4. Pin Function Descriptions

TSSOP Pin No.	LFCSP Pin No.	Mnemonic	Function
1	19	R_{SET}	Connecting a resistor between this pin and CPGND sets the maximum charge pump output current. The nominal voltage potential at the R_{SET} pin is 0.56 V. The relationship between I_{CP} and R_{SET} is $I_{CPmax} = \frac{23.5}{R_{SET}}$ So, with R_{SET} = 4.7 kΩ, I_{CPmax} = 5 mA.
2	20	CP	Charge Pump Output. When enabled, this provides ±I_{CP} to the external loop filter, which in turn drives the external VCO.
3	1	CPGND	Charge Pump Ground. This is the ground return path for the charge pump.
4	2, 3	AGND	Analog Ground. This is the ground return path of the prescaler.
5	4	$RF_{IN}B$	Complementary Input to the RF Prescaler. This point should be decoupled to the ground plane with a small bypass capacitor, typically 100 pF. See Figure 29.
6	5	$RF_{IN}A$	Input to the RF Prescaler. This small-signal input is ac-coupled from the VCO.
7	6, 7	AV_{DD}	Analog Power Supply. This may range from 2.7 V to 5.5 V. Decoupling capacitors to the analog ground plane should be placed as close as possible to this pin. AV_{DD} must be the same value as DV_{DD}.
8	8	REF_{IN}	Reference Input. This is a CMOS input with a nominal threshold of V_{DD}/2, and an equivalent input resistance of 100 kΩ. See Figure 28. This input can be driven from a TTL or CMOS crystal oscillator, or can be ac-coupled.
9	9, 10	DGND	Digital Ground.
10	11	CE	Chip Enable. A logic low on this pin powers down the device and puts the charge pump output into three-state mode. Taking the pin high powers up the device depending on the status of the power-down Bit F2.
11	12	CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
12	13	DATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs being the control bits. This input is a high impedance CMOS input.
13	14	LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches; the latch is selected using the control bits.
14	15	MUXOUT	This multiplexer output allows either the lock detect, the scaled RF, or the scaled reference frequency to be accessed externally.
15	16, 17	DV_{DD}	Digital Power Supply. This may range from 2.7 V to 5.5 V. Decoupling capacitors to the digital ground plane should be placed as close as possible to this pin. DV_{DD} must be the same value as AV_{DD}.
16	18	V_P	Charge Pump Power Supply. This should be greater than or equal to V_{DD}. In systems where V_{DD} is 3 V, V_P can be set to 6 V and used to drive a VCO with a tuning range of up to 6 V. 1
		EPAD	Exposed Pad (LFCSP Only). The exposed paddle should be connected to AGND.

TYPICAL PERFORMANCE CHARACTERISTICS

FREQ –UNIT	PARAM –TYPE	DATA –FORMAT	KEYWORD		IMPEDANCE –OHMS
GHz	S	MA	R		50
FREQ	MAGS11	ANGS11	FREQ	MAGS11	ANGS11
0.05	0.89207	–2.0571	1.05	0.9512	–40.134
0.10	0.8886	–4.4427	1.10	0.93458	–43.747
0.15	0.89022	–6.3212	1.15	0.94782	–44.393
0.20	0.96323	–2.1393	1.20	0.96875	–46.937
0.25	0.90566	–12.13	1.25	0.92216	–49.6
0.30	0.90307	–13.52	1.30	0.93755	–51.884
0.35	0.89318	–15.746	1.35	0.96178	–51.21
0.40	0.89806	–18.056	1.40	0.94354	–53.55
0.45	0.89565	–19.693	1.45	0.95189	–56.786
0.50	0.88538	–22.246	1.50	0.97647	–58.781
0.55	0.89699	–24.336	1.55	0.98619	–60.545
0.60	0.89927	–25.948	1.60	0.95459	–61.43
0.65	0.87797	–28.457	1.65	0.97945	–61.241
0.70	0.90765	–29.735	1.70	0.98864	–64.051
0.75	0.88526	–31.879	1.75	0.97399	–66.19
0.80	0.81267	–32.681	1.80	0.97216	–63.775
0.85	0.90357	–31.522			
0.90	0.92954	–34.222			
0.95	0.92087	–36.961			
1.00	0.93788	–39.343			

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Figure 5. S-Parameter Data for the ADF4113 RF Input (up to 1.8 GHz)

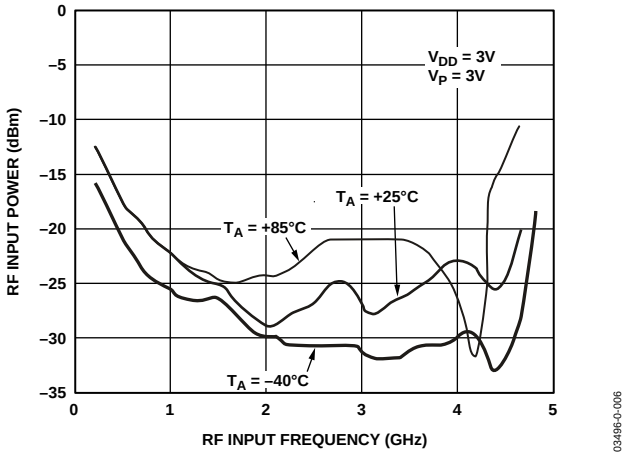

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Figure 6. Input Sensitivity (ADF4113)

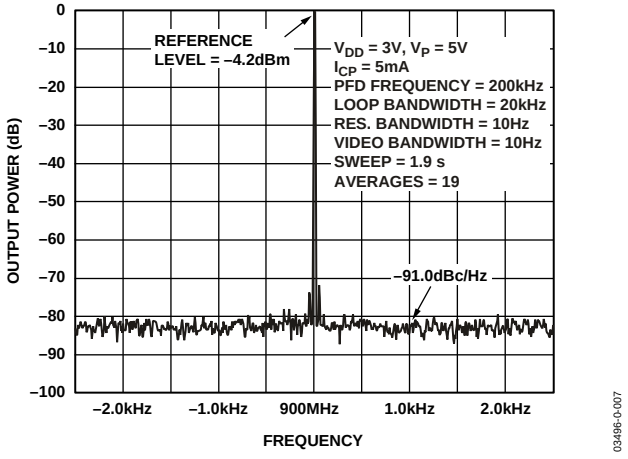

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Figure 7. ADF4113 Phase Noise (900 MHz, 200 kHz, 20 kHz)

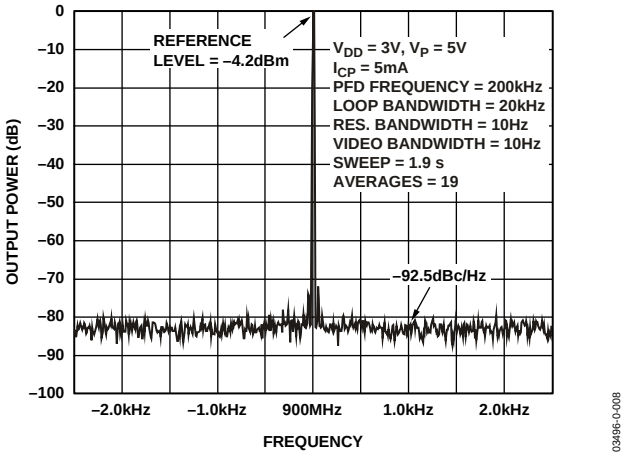

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Figure 8. ADF4113 Phase Noise (900 MHz, 200kHz, 20 kHz) with DLY and SYNC Enabled

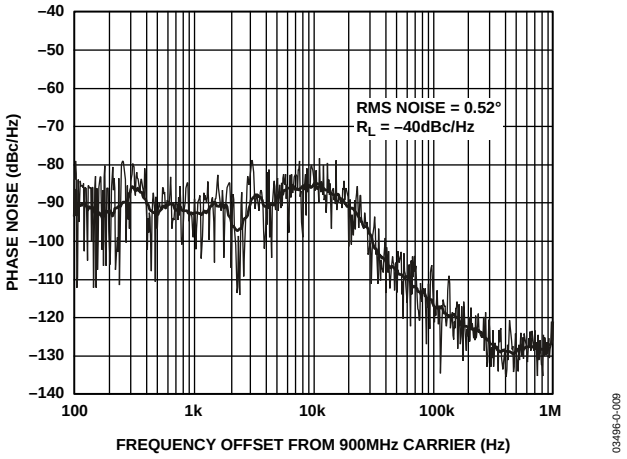

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Figure 9. ADF4113 Integrated Phase Noise (900 MHz, 200 kHz, 20 kHz, Typical Lock Time: 400 µs)

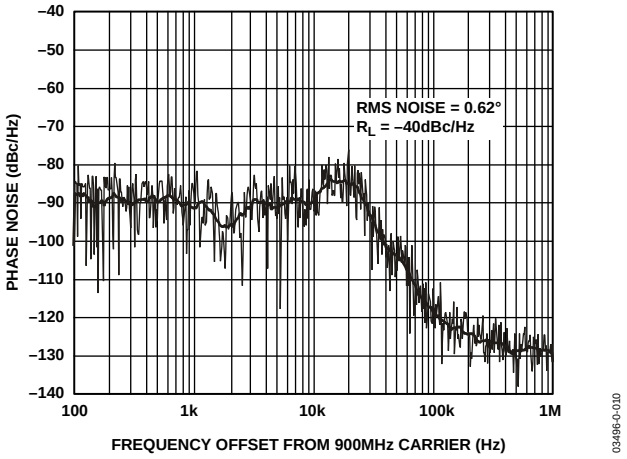

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Figure 10. ADF4113 Integrated Phase Noise (900 MHz, 200 kHz, 35 kHz, Typical Lock Time: 200 µs)

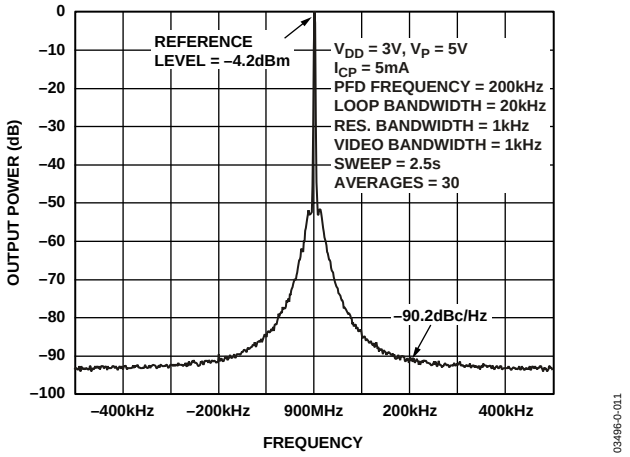

Figure 11. ADF4113 Reference Spurs (900 MHz, 200 kHz, 20 kHz)

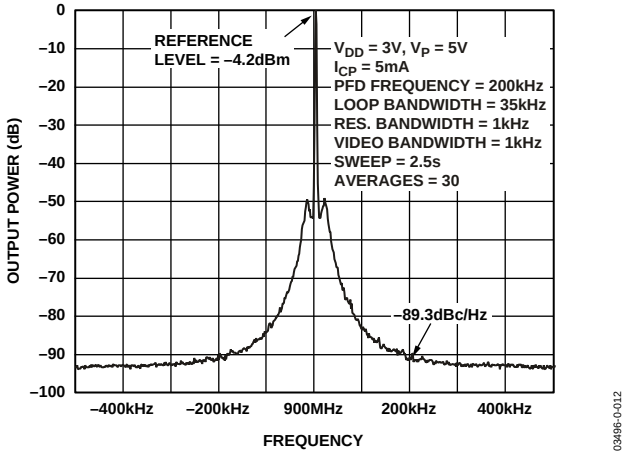

Figure 12. ADF4113 (900 MHz, 200 kHz, 35 kHz)

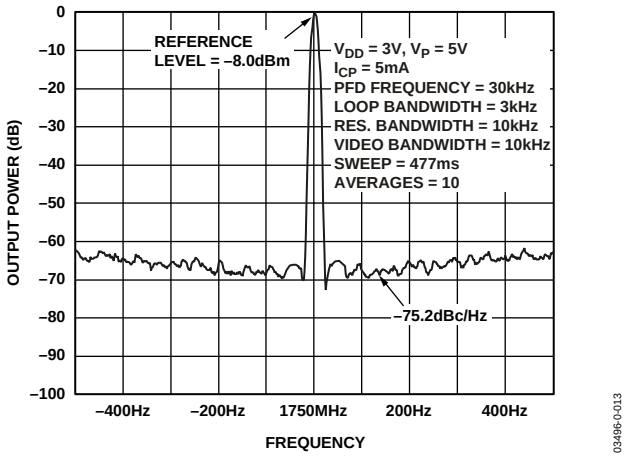

Figure 13. ADF4113 Phase Noise (1750 MHz, 30 kHz, 3 kHz)

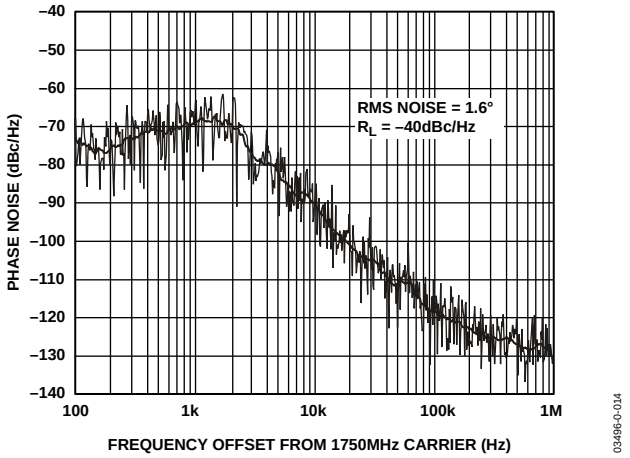

Figure 14. ADF4113 Integrated Phase Noise (1750 MHz, 30 kHz, 3 kHz)

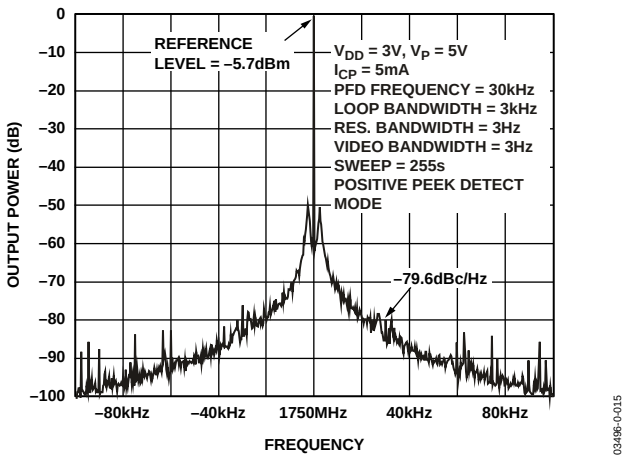

Figure 15. ADF4113 Reference Spurs (1750 MHz, 30 kHz, 3 kHz)

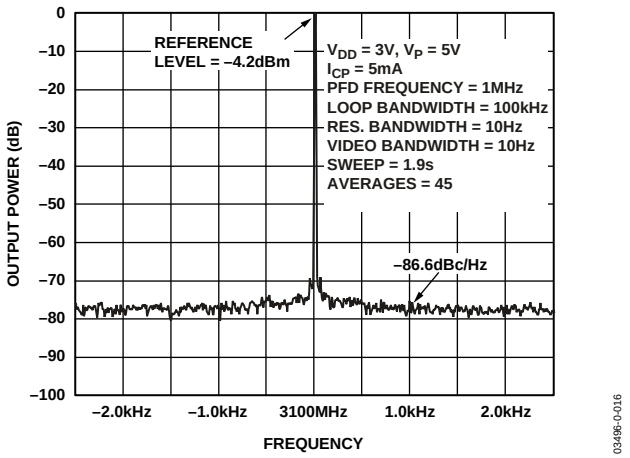

Figure 16. ADF4113 Phase Noise (3100 MHz, 1 MHz, 100 kHz)

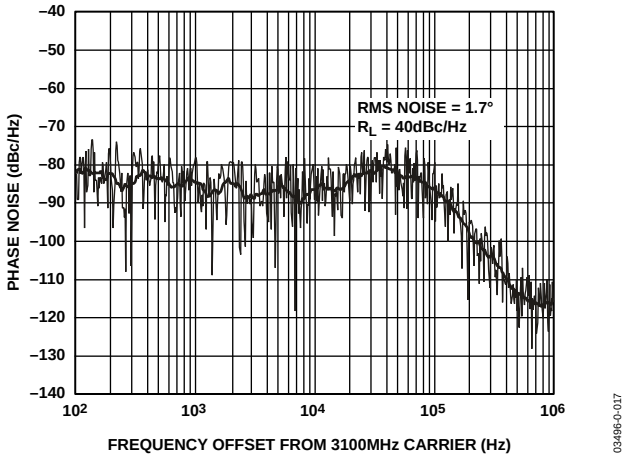

Figure 17. ADF4113 Integrated Phase Noise (3100 MHz, 1 MHz, 100 kHz)

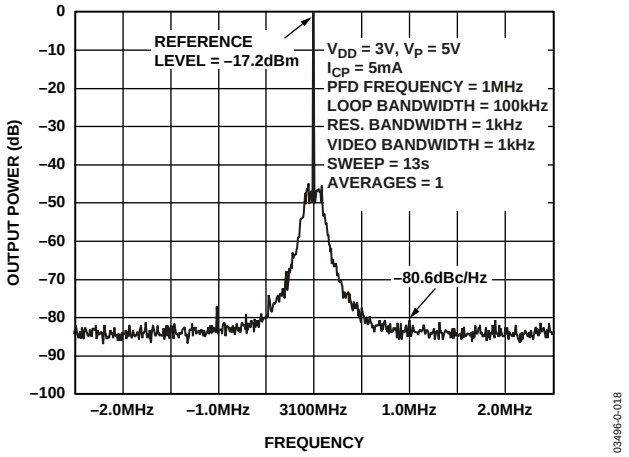

Figure 18. Reference Spurs (3100 MHz, 1 MHz, 100 kHz)

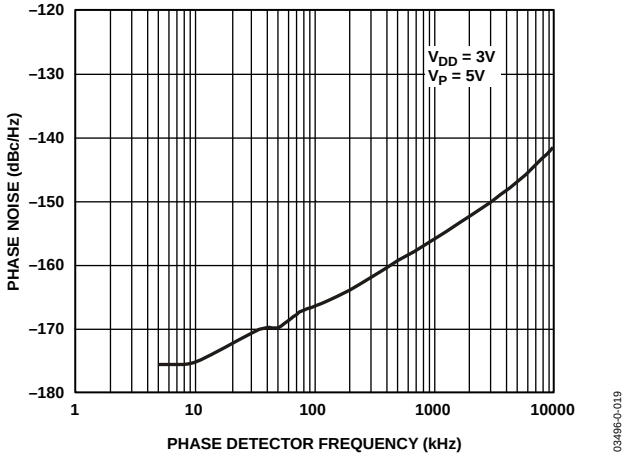

Figure 19. ADF4113 Phase Noise (Referred to CP Output) vs. Phase Detector Frequency

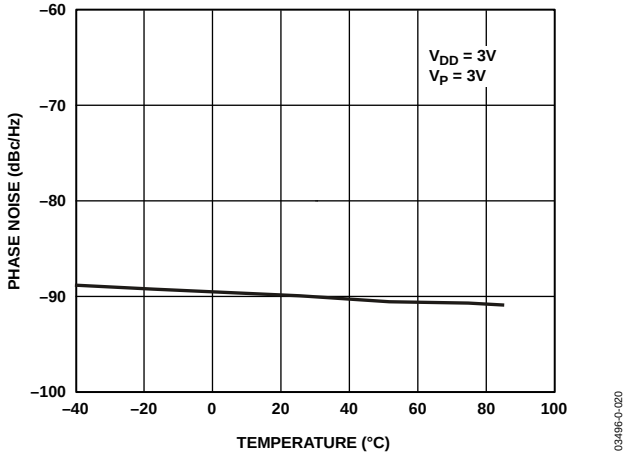

Figure 20. ADF4113 Phase Noise vs. Temperature (900 MHz, 200 kHz, 20 kHz)

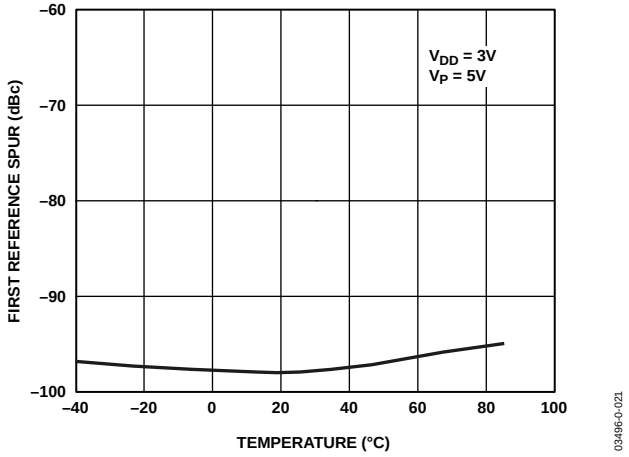

Figure 21. ADF4113 Reference Spurs vs. Temperature (900 MHz, 200 kHz, 20 kHz)

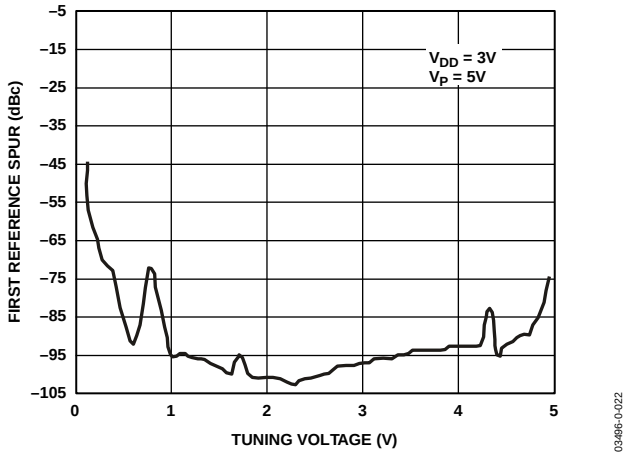

Figure 22. ADF4113 Reference Spurs (200 kHz) vs. V_{TUNE} (900 MHz, 200 kHz, 20 kHz)

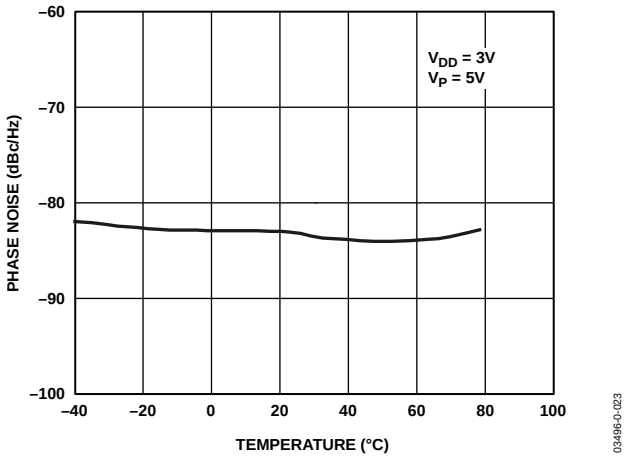

Figure 23. ADF4113 Phase Noise vs. Temperature (836 MHz, 30 kHz, 3 kHz)

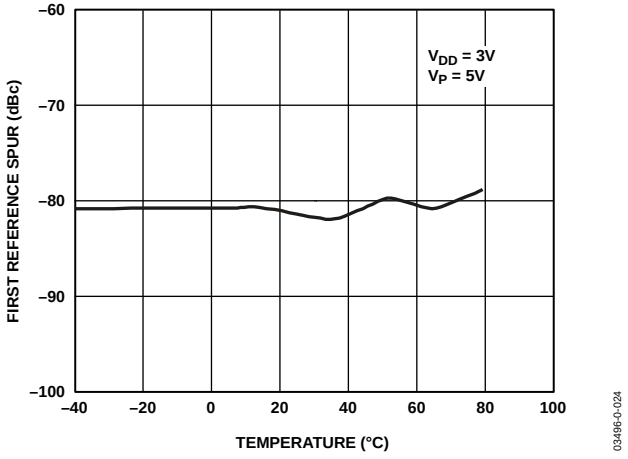

Figure 24. ADF4113 Reference Spurs vs. Temperature (836 MHz, 30 kHz, 3 kHz)

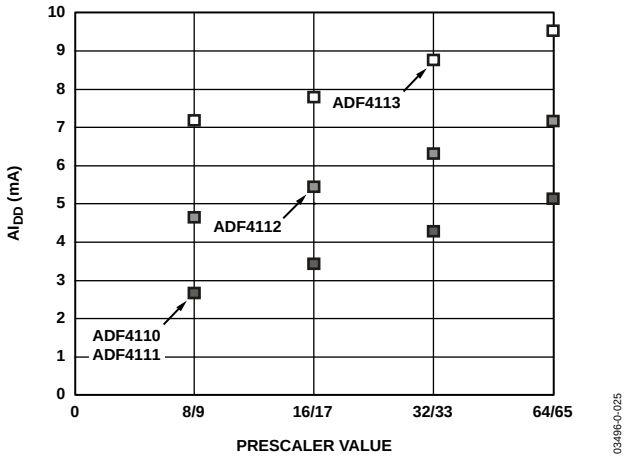

Figure 25. AI_{DD} vs. Prescaler Value

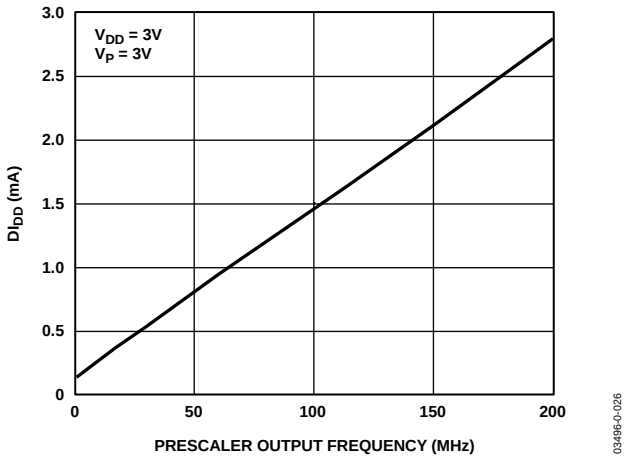

Figure 26. DI_{DD} vs. Prescaler Output Frequency (ADF4110, ADF4111, ADF4112, ADF4113)

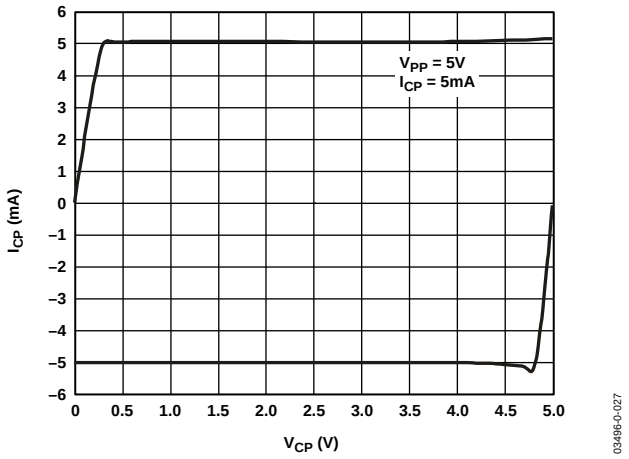

Figure 27. Charge Pump Output Characteristics for ADF4110 Family

CIRCUIT DESCRIPTION

REFERENCE INPUT SECTION

The reference input stage is shown in Figure 28. SW1 and SW2 are normally closed switches. SW3 is normally open. When power-down is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that there is no loading of the REF_{IN} pin on power-down.

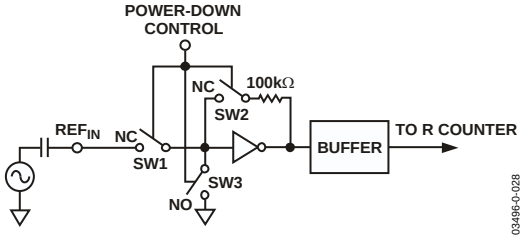

Figure 28. Reference Input Stage

RF INPUT STAGE

The RF input stage is shown in Figure 29. It is followed by a two-stage limiting amplifier to generate the current mode logic (CML) clock levels needed for the prescaler.

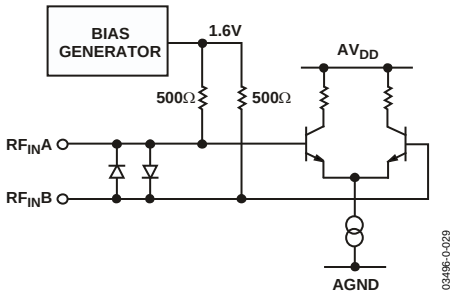

Figure 29. RF Input Stage

PRESCALER (P/P + 1)

Along with the A and B counters, the dual-modulus prescaler (P/P + 1) enables the large division ratio, N, to be realized (N = BP + A). The dual-modulus prescaler, operating at CML levels, takes the clock from the RF input stage and divides it down to a manageable frequency for the CMOS A and B counters. The prescaler is programmable; it can be set in software to 8/9, 16/17, 32/33, or 64/65. It is based on a synchronous 4/5 core.

A AND B COUNTERS

The A and B CMOS counters combine with the dual-modulus prescaler to allow a wide ranging division ratio in the PLL feedback counter. The counters are specified to work when the prescaler output is 200 MHz or less. Thus, with an RF input frequency of 2.5 GHz, a prescaler value of 16/17 is valid but a value of 8/9 is not.

Pulse Swallow Function

The A and B counters, in conjunction with the dual-modulus prescaler, make it possible to generate output frequencies that are spaced only by the reference frequency divided by *R*. The equation for the VCO frequency is

$$f_{VCO} = [(P \times B) + A]f_{REFIN}/R$$

where:

f_{VCO} = output frequency of external voltage controlled oscillator (VCO)
P = preset modulus of dual-modulus prescaler
B = preset divide ratio of binary 13-bit counter(3 to 8191)
A = preset divide ratio of binary 6-bit swallow counter (0 to 63)
f_{REFIN} = output frequency of the external reference frequency oscillator
R = preset divide ratio of binary 14-bit programmable reference counter (1 to 16383)

R COUNTER

The 14-bit R counter allows the input reference frequency to be divided down to produce the reference clock to the phase frequency detector (PFD). Division ratios from 1 to 16,383 are allowed.

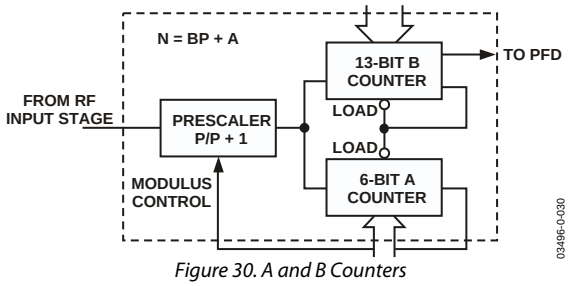

Figure 30. A and B Counters

PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the R counter and N counter (N = BP + A) and produces an output proportional to the phase and frequency difference between them. Figure 31 is a simplified schematic. The PFD includes a programmable delay element that controls the width of the antibacklash pulse. This pulse ensures that there is no dead zone in the PFD transfer function and minimizes phase noise and reference spurs. Two bits in the reference counter latch, ABP2 and ABP1, control the width of the pulse. See Table 7.

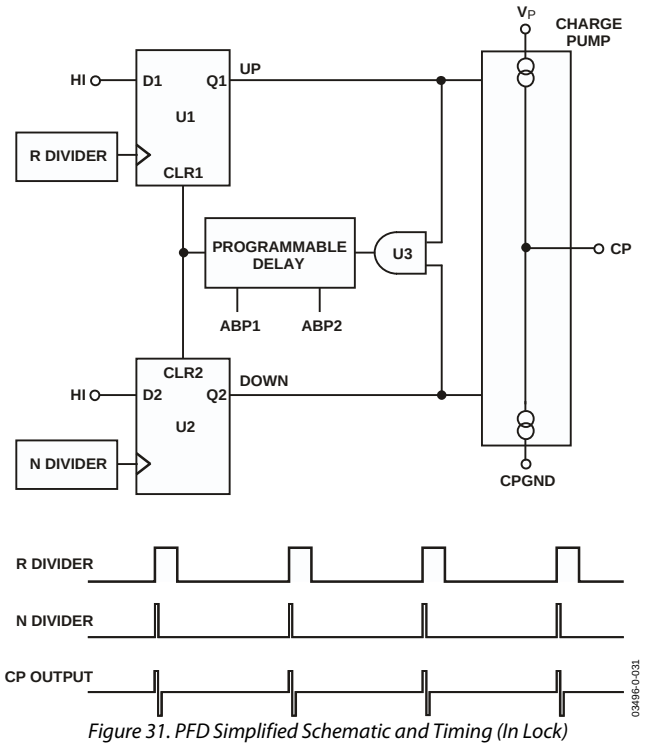

Figure 31. PFD Simplified Schematic and Timing (In Lock)

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4110 family allows the user to access various internal points on the chip. The state of MUXOUT is controlled by M3, M2, and M1 in the function latch. Table 9 shows the full truth table. Figure 32 shows the MUXOUT section in block diagram form.

Lock Detect

MUXOUT can be programmed for two types of lock detect: digital lock detect and analog lock detect.

Digital lock detect is active high. When LDP in the R counter latch is set to 0, digital lock detect is set high when the phase error on three consecutive phase detector (PD) cycles is less than 15 ns. With LDP set to 1, five consecutive cycles of less than 15 ns are required to set the lock detect. It stays high until a phase error greater than 25 ns is detected on any subsequent PD cycle.

The N-channel open-drain analog lock detect should be operated with a 10 kΩ nominal external pull-up resistor. When lock has been detected, this output is high with narrow low-going pulses.

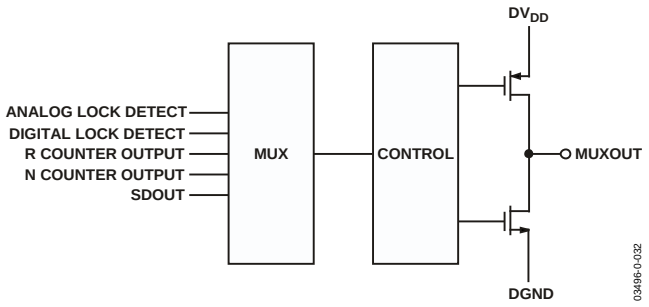

Figure 32. MUXOUT Circuit

INPUT SHIFT REGISTER

The ADF4110 family digital section includes a 24-bit input shift register, a 14-bit R counter, and a 19-bit N counter comprised of a 6-bit A counter and a 13-bit B counter. Data is clocked into the 24-bit shift register on each rising edge of CLK MSB first. Data is transferred from the shift register to one of four latches on the rising edge of LE. The destination latch is determined by the state of the two control bits (C2, C1) in the shift register. These are the two LSBs, DB1 and DB0, as shown in Figure 2. The truth table for these bits is shown in Table 5.

Table 6 shows a summary of how the latches are programmed.

Table 5. C2, C1 Truth Table

Control Bits		
C2	**C1**	**Data Latch**
0	0	R Counter
0	1	N Counter (A and B)
1	0	Function Latch (Including Prescaler)
1	1	Initialization Latch

Table 6. ADF4110 Family Latch Summary

REFERENCE COUNTER LATCH

RESERVED	DLY	SYNC	LOCK DETECT PRECISION	TEST MODE BITS		ANTI-BACKLASH WIDTH		14-BIT REFERENCE COUNTER, R													CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	DLY	SYNC	LDP	T2	T1	ABP2	ABP1	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (0)

X = DON'T CARE

N COUNTER LATCH

RESERVED		CP GAIN	13-BIT B COUNTER													6-BIT A COUNTER						CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	X	G1	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A6	A5	A4	A3	A2	A1	C2 (0)	C1 (1)

X = DON'T CARE

FUNCTION LATCH

PRESCALER VALUE		POWER-DOWN 2	CURRENT SETTING 2			CURRENT SETTING 1			TIMER COUNTER CONTROL				FASTLOCK MODE	FASTLOCK ENABLE	CP THREE-STATE	PD POLARITY	MUXOUT CONTROL			POWER-DOWN 1	COUNTER RESET	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (0)

INITIALIZATION LATCH

PRESCALER VALUE		POWER-DOWN 2	CURRENT SETTING 2			CURRENT SETTING 1			TIMER COUNTER CONTROL				FASTLOCK MODE	FASTLOCK ENABLE	CP THREE-STATE	PD POLARITY	MUXOUT CONTROL			POWER-DOWN 1	COUNTER RESET	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (1)

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Table 7. Reference Counter Latch Map

RESERVED	DLY	SYNC	LOCK DETECT PRECISION	TEST MODE BITS		ANTI-BACKLASH WIDTH		14-BIT REFERENCE COUNTER												CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	DLY	SYNC	LDP	T2	T1	ABP2	ABP1	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (0)

X = DON'T CARE

R14	R13	R12	•••••••••••	R3	R2	R1	DIVIDE RATIO
0	0	0	•••••••••••	0	0	1	1
0	0	0	•••••••••••	0	1	0	2
0	0	0	•••••••••••	0	1	1	3
0	0	0	•••••••••••	1	0	0	4
•	•	•	•••••••••••	•	•	•	•
•	•	•	•••••••••••	•	•	•	•
•	•	•	•••••••••••	•	•	•	•
1	1	1	•••••••••••	1	0	0	16380
1	1	1	•••••••••••	1	0	1	16381
1	1	1	•••••••••••	1	1	0	16382
1	1	1	•••••••••••	1	1	1	16383

ABP2	ABP1	ANTIBACKLASH PULSE WIDTH
0	0	3.0ns
0	1	1.5ns
1	0	6.0ns
1	1	3.0ns

TEST MODE BITS SHOULD BE SET TO 00 FOR NORMAL OPERATION

LDP	OPERATION
0	THREE CONSECUTIVE CYCLES OF PHASE DELAY LESS THAN 15ns MUST OCCUR BEFORE LOCK DETECT IS SET.
1	FIVE CONSECUTIVE CYCLES OF PHASE DELAY LESS THAN 15ns MUST OCCUR BEFORE LOCK DETECT IS SET.

DLY	SYNC	OPERATION
0	0	NORMAL OPERATION
0	1	OUTPUT OF PRESCALER IS RESYNCHRONIZED WITH NONDELAYED VERSION OF RF INPUT
1	0	NORMAL OPERATION
1	1	OUTPUT OF PRESCALER IS RESYNCHRONIZED WITH DELAYED VERSION OF RF INPUT

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Table 8. AB Counter Latch Map

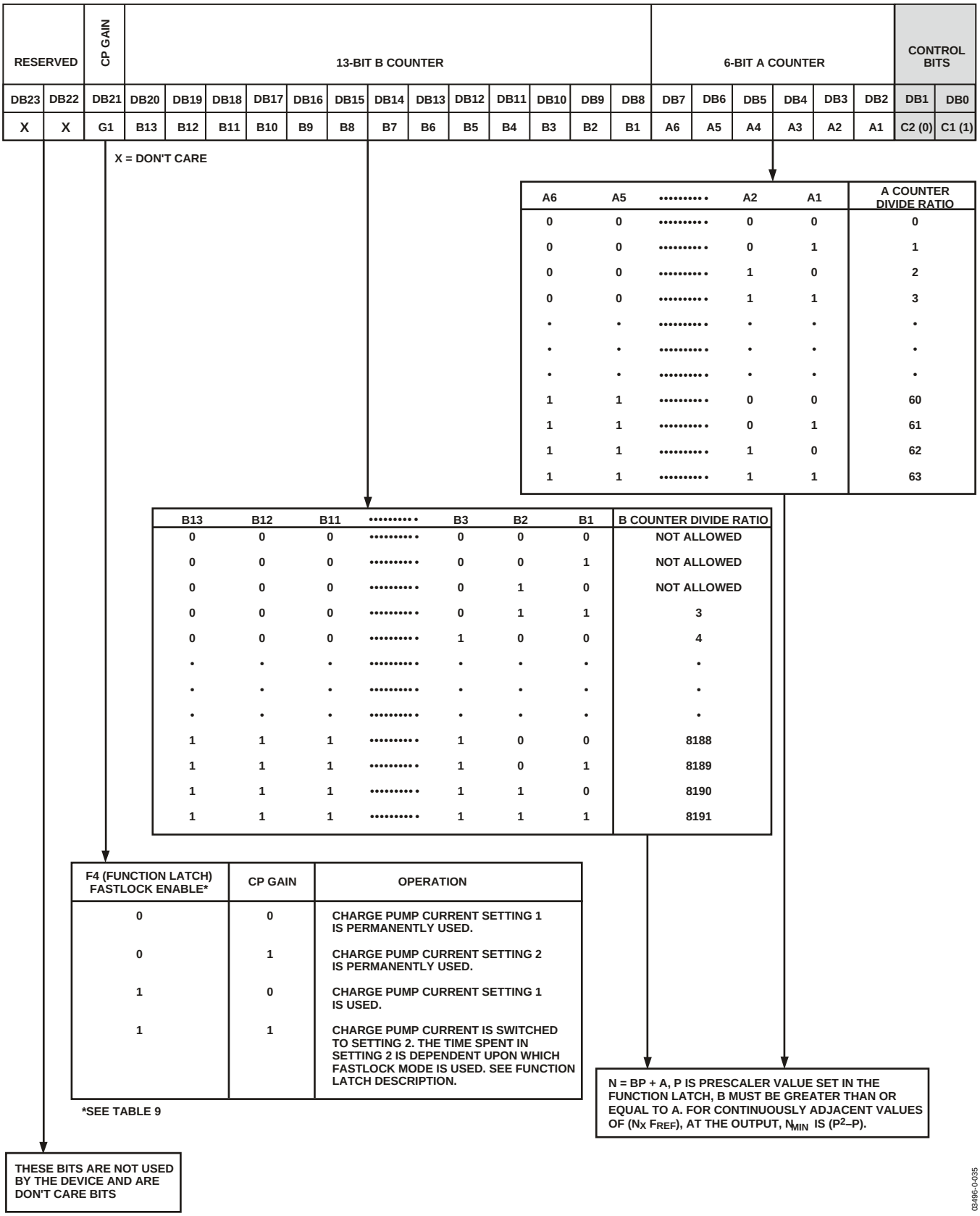
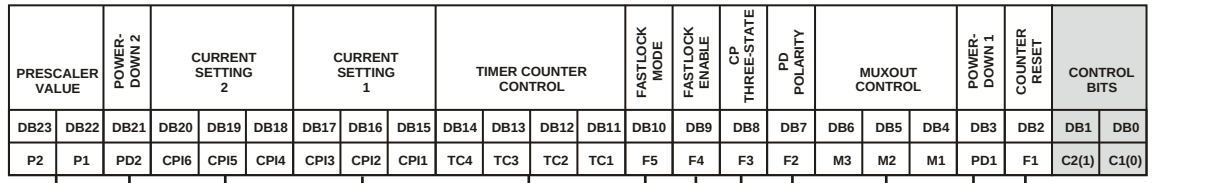


Table 9. Function Latch Map



PRESCALER VALUE		POWER-DOWN 2	CURRENT SETTING 2			CURRENT SETTING 1			TIMER COUNTER CONTROL				FASTLOCK MODE	FASTLOCK ENABLE	CP THREE-STATE	PD POLARITY	MUXOUT CONTROL			POWER-DOWN 1	COUNTER RESET	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2(1)	C1(0)

F1	COUNTER OPERATION
0	NORMAL
1	R, A, B COUNTERS HELD IN RESET

F2	PHASE DETECTOR POLARITY
0	NEGATIVE
1	POSITIVE

F3	CHARGE PUMP OUTPUT
0	NORMAL
1	THREE-STATE

F4	F5	FASTLOCK MODE
0	X	FASTLOCK DISABLED
1	0	FASTLOCK MODE 1
1	1	FASTLOCK MODE 2

TC4	TC3	TC2	TC1	TIMEOUT (PFD CYCLES)
0	0	0	0	3
0	0	0	1	7
0	0	1	0	11
0	0	1	1	15
0	1	0	0	19
0	1	0	1	23
0	1	1	0	27
0	1	1	1	31
1	0	0	0	35
1	0	0	1	39
1	0	1	0	43
1	0	1	1	47
1	1	0	0	51
1	1	0	1	55
1	1	1	0	59
1	1	1	1	63

SEE FUNCTION LATCH, TIMER COUNTER CONTROL SECTION

M3	M2	M1	OUTPUT
0	0	0	THREE-STATE OUTPUT
0	0	1	DIGITAL LOCK DETECT (ACTIVE HIGH)
0	1	0	N DIVIDER OUTPUT
0	1	1	DV_{DD}
1	0	0	R DIVIDER OUTPUT
1	0	1	ANALOG LOCK DETECT (N-CHANNEL OPEN-DRAIN)
1	1	0	SERIAL DATA OUTPUT
1	1	1	DGND

CPI6	CPI5	CPI4	I_{CP} (mA)		
CPI3	CPI2	CPI1	2.7kΩ	4.7kΩ	10kΩ
0	0	0	1.09	0.63	0.29
0	0	1	2.18	1.25	0.59
0	1	0	3.26	1.88	0.88
0	1	1	4.35	2.50	1.76
1	0	0	5.44	3.13	1.47
1	0	1	6.53	3.75	1.76
1	1	0	7.62	4.38	2.06
1	1	1	8.70	5.00	2.35

CE PIN	PD2	PD1	MODE
0	X	X	ASYNCHRONOUS POWER-DOWN
1	X	0	NORMAL OPERATION
1	0	1	ASYNCHRONOUS POWER-DOWN
1	1	1	SYNCHRONOUS POWER-DOWN

P2	P1	PRESCALER VALUE
0	0	8/9
0	1	16/17
1	0	32/33
1	1	64/65

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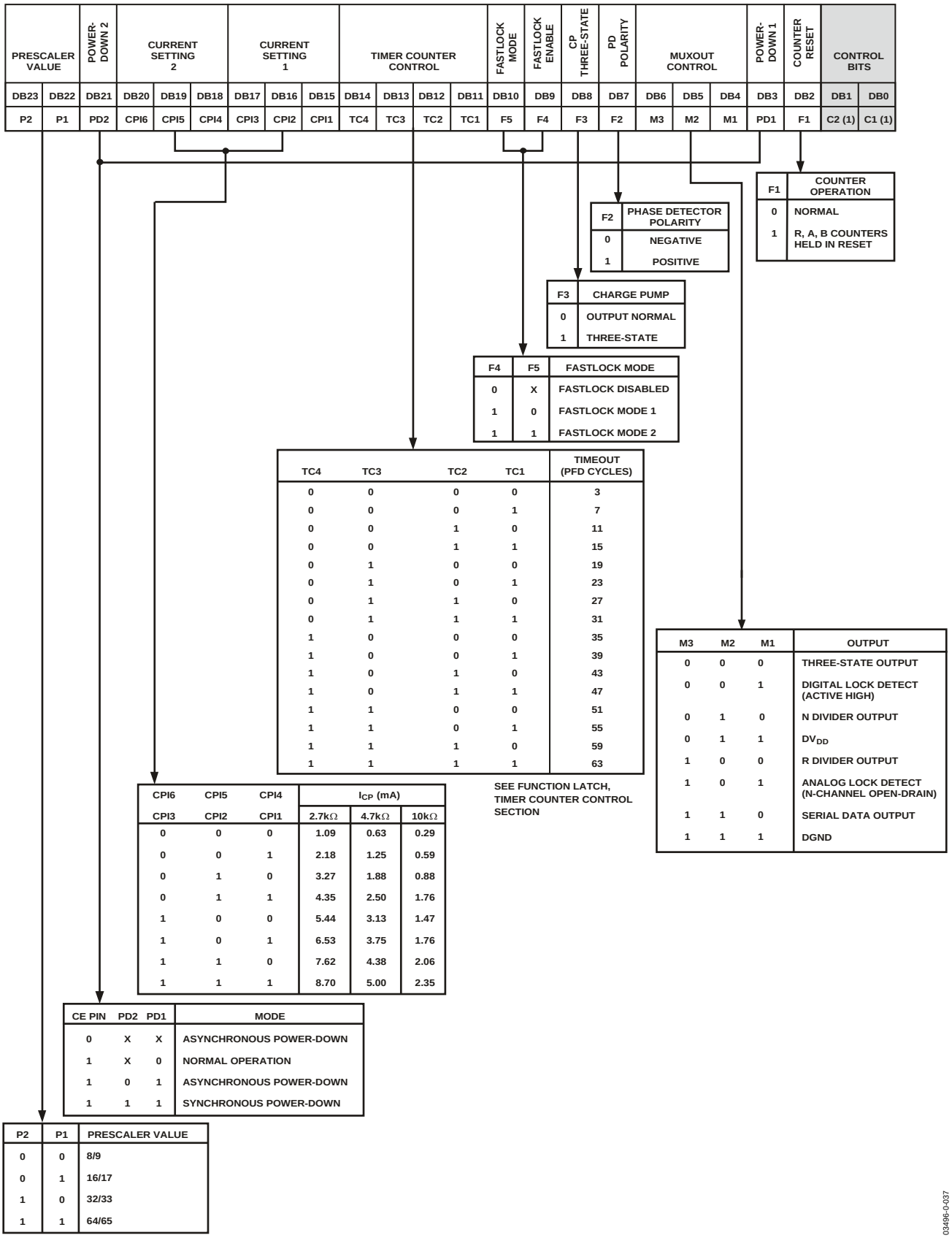
Table 10. Initialization Latch Map



FUNCTION LATCH

The on-chip function latch is programmed with C2, C1 set to 1. Table 9 shows the input data format for programming the function latch.

Counter Reset

DB2 (F1) is the counter reset bit. When DB2 is 1, the R counter and the AB counters are reset. For normal operation, this bit should be 0. Upon powering up, the F1 bit must be disabled, and the N counter resumes counting in "close" alignment with the R counter. (The maximum error is one prescaler cycle.)

Power-Down

DB3 (PD1) and DB21 (PD2) on the ADF411x provide program-mable power-down modes. They are enabled by the CE pin.

When the CE pin is low, the device is immediately disabled regardless of the states of PD2, PD1.

In the programmed asynchronous power-down, the device powers down immediately after latching a 1 into Bit PD1, provided PD2 has been loaded with a 0.

In the programmed synchronous power-down, the device power-down is gated by the charge pump to prevent unwanted frequency jumps. Once power-down is enabled by writing a 1 into Bit PD1 (provided a 1 has also been loaded to PD2), the device goes into power-down on the next charge pump event.

When a power-down is activated (either synchronous or asynchronous mode including CE pin activated power-down), the following events occur:

- All active dc current paths are removed.
- The R, N, and timeout counters are forced to their load state conditions.
- The charge pump is forced into three-state mode.
- The digital clock detect circuitry is reset.
- The RFIN input is debiased.
- The reference input buffer circuitry is disabled.
- The input register remains active and capable of loading and latching data.

MUXOUT Control

The on-chip multiplexer is controlled by M3, M2, and M1 on the ADF4110 family. Table 9 shows the truth table.

Fastlock Enable Bit

DB9 of the function latch is the fastlock enable bit. Fastlock is enables only when this is 1.

Fastlock Mode Bit

DB10 of the function latch is the fastlock enable bit. When fastlock is enabled, this bit determines which fastlock mode is used. If the fastlock mode bit is 0, fastlock mode 1 is selected; if the fastlock mode bit is 1, fastlock mode 2 is selected.

Fastlock Mode 1

The charge pump current is switched to the contents of Current Setting 2.

The device enters fastlock by having a 1 written to the CP gain bit in the AB counter latch. The device exits fastlock by having a 0 written to the CP gain bit in the AB counter latch.

Fastlock Mode 2

The charge pump current is switched to the contents of Current Setting 2. The device enters fastlock by having a 1 written to the CP gain bit in the AB counter latch. The device exits fastlock under the control of the timer counter. After the timeout period determined by the value in TC4 through TC1, the CP gain bit in the AB counter latch is automatically reset to 0 and the device reverts to normal mode instead of fastlock. See Table 9 for the timeout periods.

Timer Counter Control

The user has the option of programming two charge pump currents. Current Setting 1 is meant to be used when the RF output is stable and the system is in a static state. Current Setting 2 is meant to be used when the system is dynamic and in a state of change (i.e., when a new output frequency is programmed).

The normal sequence of events is as follows:

The user initially decides what the preferred charge pump currents are going to be. For example, they may choose 2.5 mA as Current Setting 1 and 5 mA as Current Setting 2.

At the same time, they must also decide how long they want the secondary current to stay active before reverting to the primary current. This is controlled by the timer counter control bits, DB14 through DB11 (TC4 through TC1) in the function latch. The truth table is given in Table 10.

A user can program a new output frequency simply by programming the AB counter latch with new values for A and B. At the same time, the CP gain bit can be set to 1, which sets the charge pump with the value in CPI6–CPI4 for a period determined by TC4 through TC1. When this time is up, the charge pump current reverts to the value set by CPI3–CPI1. At the same time, the CP gain bit in the AB counter latch is reset to 0 and is ready for the next time the user wishes to change the frequency.

Note that there is an enable feature on the timer counter. It is enabled when Fastlock Mode 2 is chosen by setting the fastlock mode bit (DB10) in the function latch to 1.

Charge Pump Currents

CPI3, CPI2, and CPI1 program Current Setting 1 for the charge pump. CPI6, CPI5, and CPI4 program Current Setting 2 for the charge pump. The truth table is given in Table 10.

Prescaler Value

P2 and P1 in the function latch set the prescaler values. The prescaler value should be chosen so that the prescaler output frequency is always less than or equal to 200 MHz. Thus, with an RF frequency of 2 GHz, a prescaler value of 16/17 is valid but a value of 8/9 is not.

PD Polarity

This bit sets the phase detector polarity bit. See Table 10.

CP Three-State

This bit controls the CP output pin. With the bit set high, the CP output is put into three-state. With the bit set low, the CP output is enabled.

INITIALIZATION LATCH

When C2, C1 = 1, 1, the initialization latch is programmed. This is essentially the same as the function latch (programmed when C2, C1 = 1, 0).

However, when the initialization latch is programmed, an additional internal reset pulse is applied to the R and AB counters. This pulse ensures that the AB counter is at load point when the AB counter data is latched, and the device begins counting in close phase alignment.

If the latch is programmed for synchronous power-down (CE pin high; PD1 bit high; PD2 bit low), the internal pulse also triggers this power-down. The prescaler reference and the oscillator input buffer are unaffected by the internal reset pulse, so close phase alignment is maintained when counting resumes.

When the first AB counter data is latched after initialization, the internal reset pulse is again activated. However, successive AB counter loads after this will not trigger the internal reset pulse.

DEVICE PROGRAMMING AFTER INITIAL POWER-UP

After initial power-up of the device, there are three ways to program the device.

Initialization Latch Method

Apply V_{DD}. Program the initialization latch (11 in 2 LSBs of input word). Make sure the F1 bit is programmed to 0. Then, do an R load (00 in 2 LSBs). Then do an AB load (01 in 2 LSBs).

When the initialization latch is loaded, the following occurs:

1. The function latch contents are loaded.
2. An internal pulse resets the R, A, B, and timeout counters to load state conditions and three-states the charge pump. Note that the prescaler band gap reference and the oscillator input buffer are unaffected by the internal reset pulse, allowing close phase alignment when counting resumes.
3. Latching the first AB counter data after the initialization word activates the same internal reset pulse. Successive AB loads do not trigger the internal reset pulse unless there is another initialization.

CE Pin Method

1. Apply V_{DD}.
2. Bring CE low to put the device into power-down. This is an asynchronous power-down in that it happens immediately.
3. Program the function latch (10). Program the R counter latch (00). Program the AB counter latch (01).
4. Bring CE high to take the device out of power-down. The R and AB counters now resume counting in close alignment.

After CE goes high, a duration of 1 μs may be required for the prescaler band gap voltage and oscillator input buffer bias to reach steady state.

CE can be used to power the device up and down in order to check for channel activity. The input register does not need to be reprogrammed each time the device is disabled and enabled as long as it has been programmed at least once after V_{DD} was initially applied.

Counter Reset Method

1. Apply V_{DD}.
2. Do a function latch load (10 in 2 LSBs). As part of this, load 1 to the F1 bit. This enables the counter reset.
3. Do an R counter load (00 in 2 LSBs). Do an AB counter load (01 in 2 LSBs). Do a function latch load (10 in 2 LSBs). As part of this, load 0 to the F1 bit. This disables the counter reset.

This sequence provides the same close alignment as the initialization method. It offers direct control over the internal reset. Note that counter reset holds the counters at load point and three states the charge pump but does not trigger synchronous power-down. The counter reset method requires an extra function latch load compared to the initialization latch method.

RESYNCHRONIZING THE PRESCALER OUTPUT

Table 7 (the Reference Counter Latch Map) shows two bits, DB22 and DB21, which are labeled DLY and SYNC, respectively. These bits affect the operation of the prescaler.

With SYNC = 1, the prescaler output is resynchronized with the RF input. This has the effect of reducing jitter due to the prescaler and can lead to an overall improvement in synthesizer phase noise performance. Typically, a 1 dB to 2 dB improvement is seen in the ADF4113. The lower bandwidth devices can show an even greater improvement. For example, the ADF4110 phase noise is typically improved by 3 dB when SYNC is enabled.

With DLY = 1, the prescaler output is resynchronized with a delayed version of the RF input.

If the SYNC feature is used on the synthesizer, some care must be taken. At some point, (at certain temperatures and output frequencies), the delay through the prescaler coincides with the active edge on RF input; this causes the SYNC feature to break down. It is important to be aware of this when using the SYNC feature. Adding a delay to the RF signal, by programming DLY = 1, extends the operating frequency and temperature somewhat. Using the SYNC feature also increases the value of the AI_{DD} for the device. With a 900 MHz output, the ADF4113 AI_{DD} increases by about 1.3 mA when SYNC is enabled and by an additional 0.3 mA if DLY is enabled.

All the typical performance plots in this data sheet, except for Figure 8, apply for DLY and SYNC = 0, i.e., no resynchronization or delay enabled.

APPLICATIONS

LOCAL OSCILLATOR FOR GSM BASE STATION TRANSMITTER

Figure 33 shows the ADF4111/ADF4112/ADF4113 being used with a VCO to produce the LO for a GSM base station transmitter.

The reference input signal is applied to the circuit at $FREF_{IN}$ and, in this case, is terminated in 50 Ω. A typical GSM system would have a 13 MHz TCXO driving the reference input without any 50 Ω termination. In order to have channel spacing of 200 kHz (GSM standard), the reference input must be divided by 65, using the on-chip reference divider of the ADF4111/ADF4112/ADF4113.

The charge pump output of the ADF4111/ADF4112/ADF4113 (Pin 2) drives the loop filter. In calculating the loop filter component values, a number of items need to be considered. In this example, the loop filter was designed so that the overall phase margin for the system would be 45 degrees. Other PLL system specifications are

K_D = 5 mA
K_V = 12 MHz/V
Loop Bandwidth = 20 kHz
F_{REF} = 200 kHz
N = 4500
Extra Reference Spur Attenuation = 10 dB

All of these specifications are needed and used to come up with the loop filter component values shown in Figure 33.

The loop filter output drives the VCO, which in turn is fed back to the RF input of the PLL synthesizer. It also drives the RF output terminal. A T-circuit configuration provides 50 Ω matching between the VCO output, the RF output, and the RF_{IN} terminal of the synthesizer.

In a PLL system, it is important to know when the system is in lock. In Figure 33, this is accomplished by using the MUXOUT signal from the synthesizer. The MUXOUT pin can be programmed to monitor various internal signals in the synthesizer. One of these is the LD or lock-detect signal.

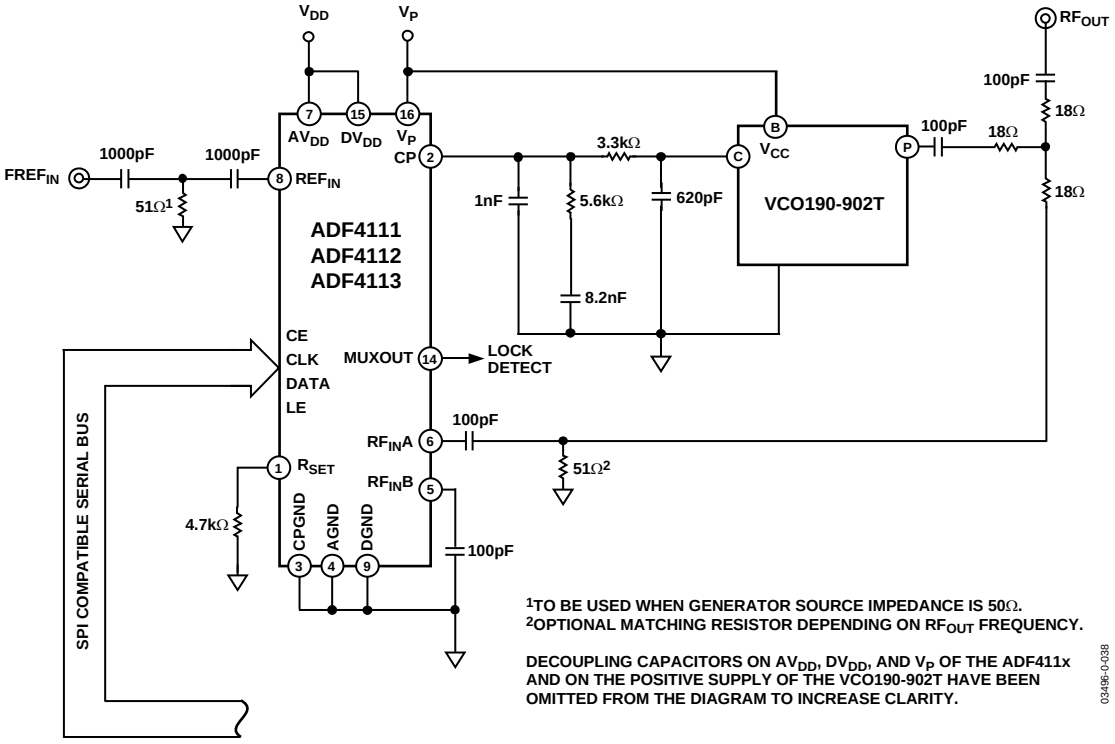


Figure 33. Local Oscillator for GSM Base Station

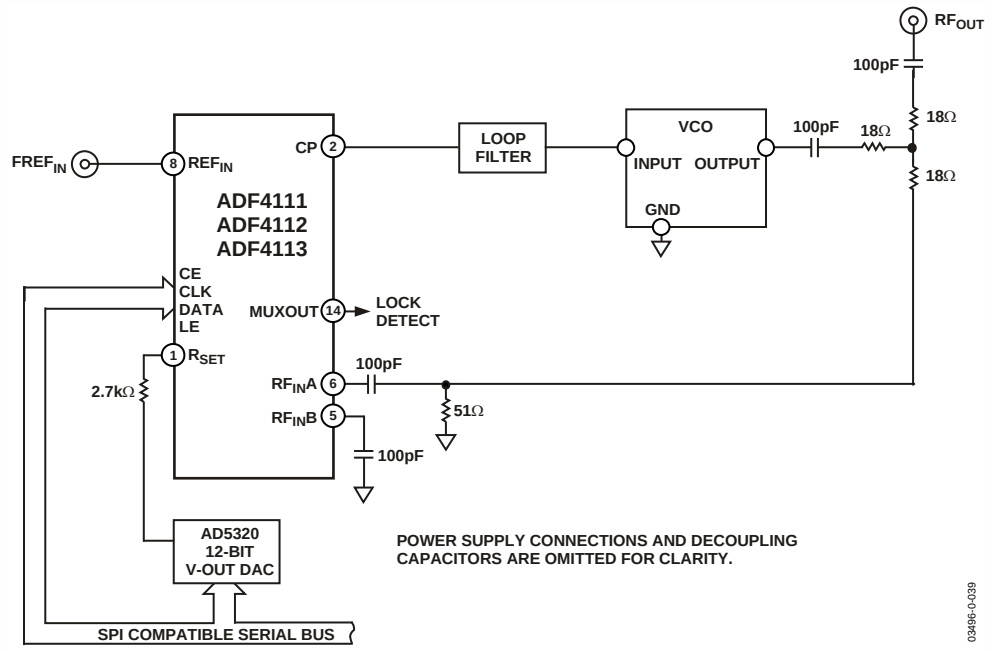


Figure 34. Driving the R_{SET} Pin with a D/A Converter

USING A D/A CONVERTER TO DRIVE THE R_{SET} PIN

A D/A converter can be used to drive the R_{SET} pin of the ADF4110 family, thus increasing the level of control over the charge pump current, I_{CP}. This can be advantageous in wide-band applications where the sensitivity of the VCO varies over the tuning range. To compensate for this, the I_{CP} may be varied to maintain good phase margin and ensure loop stability. See Figure 34.

SHUTDOWN CIRCUIT

The attached circuit in Figure 35 shows how to shut down both the ADF4110 family and the accompanying VCO. The ADG701 switch goes closed circuit when a Logic 1 is applied to the IN input. The low cost switch is available in both SOT-23 and MSOP packages.

WIDEBAND PLL

Many of the wireless applications for synthesizers and VCOs in PLLs are narrow band in nature. These applications include the various wireless standards like GSM, DSC1800, CDMA, and WCDMA. In each of these cases, the total tuning range for the local oscillator is less than 100 MHz. However, there are also wideband applications for which the local oscillator could have a tuning range as wide as an octave. For example, cable TV tuners have a total range of about 400 MHz. Figure 36 shows an application where the ADF4113 is used to control and program the Micronetics M3500-2235. The loop filter was designed for an RF output of 2900 MHz, a loop bandwidth of 40 kHz, a PFD frequency of 1 MHz, I_{CP} of 10 mA (2.5 mA synthesizer I_{CP} multiplied by the gain factor of 4), VCO K_D of 90 MHz/V (sensitivity of the M3500-2235 at an output of 2900 MHz), and a phase margin of 45°C.

In narrow-band applications, there is generally a small variation in output frequency (generally less than 10%) and a small variation in VCO sensitivity over the range (typically 10% to 15%). However, in wideband applications, both of these parameters have a much greater variation. In Figure 36, for example, there is a −25% and +17% variation in the RF output from the nominal 2.9 GHz. The sensitivity of the VCO can vary from 120 MHz/V at 2750 MHz to 75 MHz/V at 3400 MHz (+33%, −17%). Variations in these parameters change the loop bandwidth. This in turn can affect stability and lock time. By changing the programmable I_{CP}, it is possible to get compensation for these varying loop conditions and ensure that the loop is always operating close to optimal conditions.

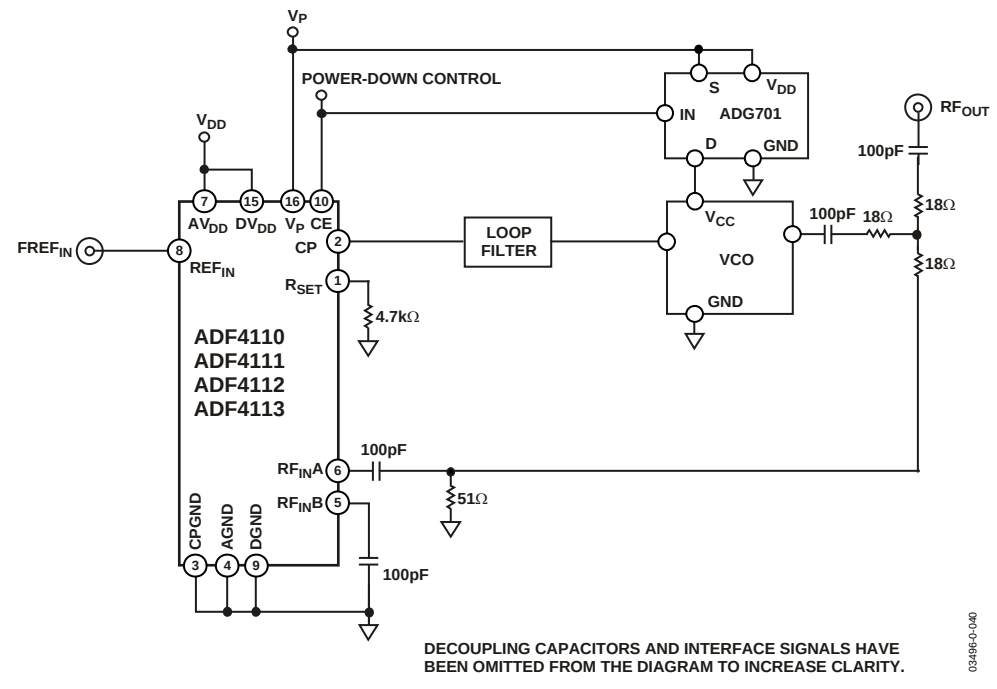


Figure 35. Local Oscillator Shutdown Circuit

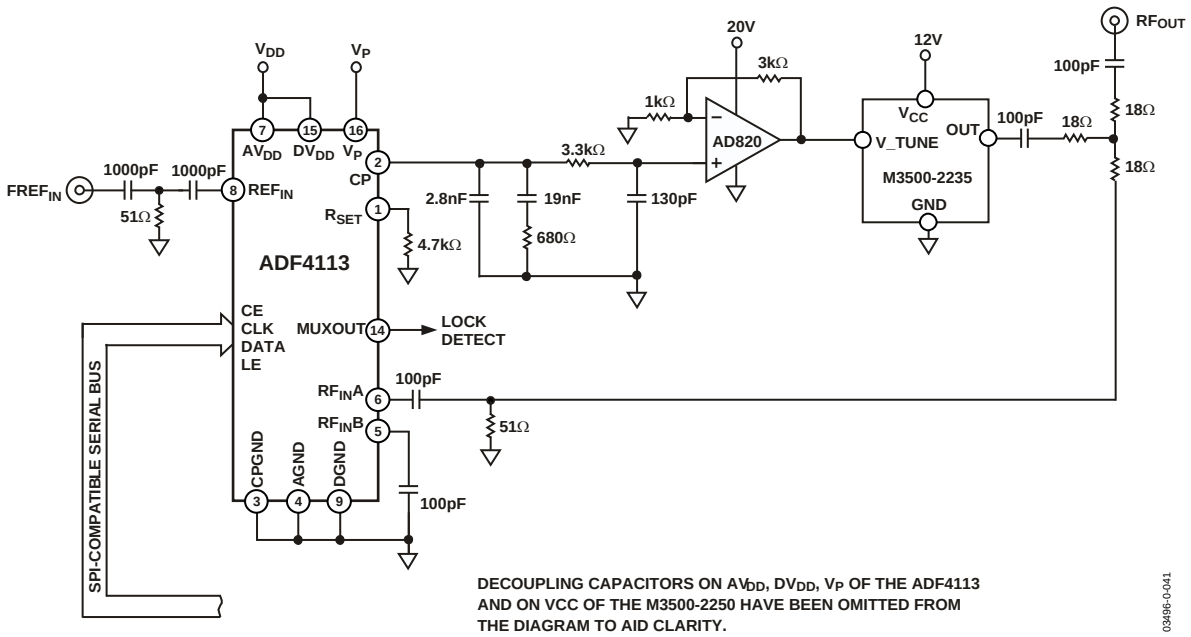


Figure 36. Wideband Phase-Locked Loop

DIRECT CONVERSION MODULATOR

In some applications, a direct conversion architecture can be used in base station transmitters. Figure 37 shows the combination available from ADI to implement this solution.

The circuit diagram shows the AD9761 being used with the AD8346. The use of dual integrated DACs such as the AD9761 with specified ±0.02 dB and ±0.004 dB gain and offset matching characteristics ensures minimum error contribution (over temperature) from this portion of the signal chain.

The local oscillator (LO) is implemented using the ADF4113. In this case, the OSC 3B1-13M0 provides the stable 13 MHz reference frequency. The system is designed for a 200 kHz channel spacing and an output center frequency of 1960 MHz. The target application is a WCDMA base station transmitter.

Typical phase noise performance from this LO is −85 dBc/Hz at a 1 kHz offset.

The LO port of the AD8346 is driven in single-ended fashion. LOIN is ac-coupled to ground with the 100 pF capacitor; LOIP is driven through the ac coupling capacitor from a 50 Ω source. An LO drive level of between −6 dBm and −12 dBm is required. The circuit of Figure 37 gives a typical level of −8 dBm.

The RF output is designed to drive a 50 Ω load but must be ac-coupled as shown in Figure 37. If the I and Q inputs are driven in quadrature by 2 V p-p signals, the resulting output power is around −10 dBm.

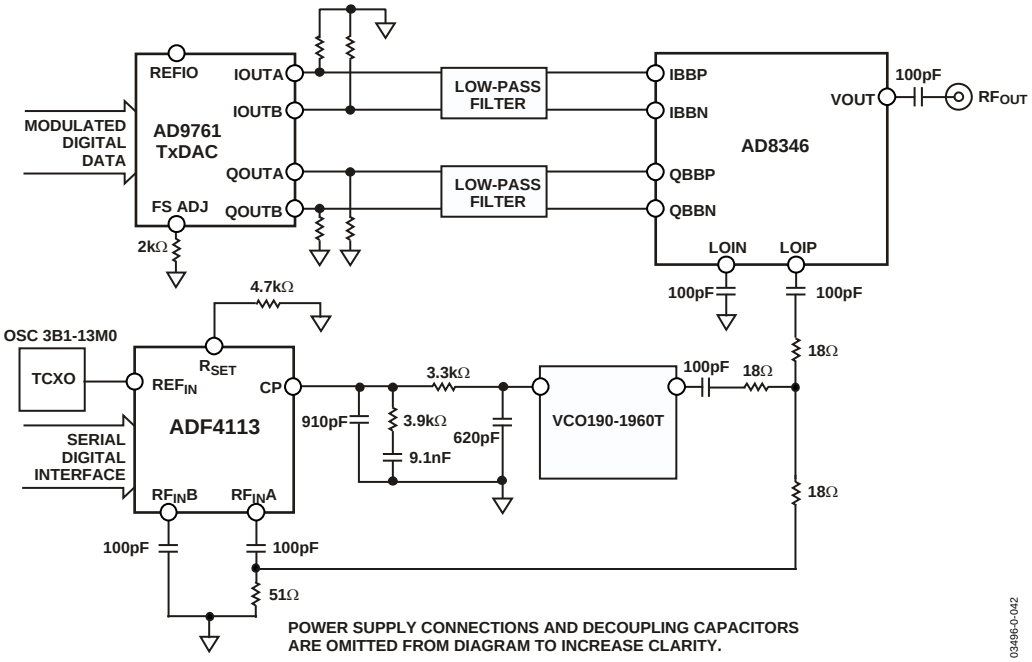


Figure 37. Direct Conversion Transmitter Solution

INTERFACING

The ADF4110 family has a simple SPI® compatible serial interface for writing to the device. SCLK, SDATA, and LE control the data transfer. When latch enable (LE) goes high, the 24 bits that have been clocked into the input register on each rising edge of SCLK get transferred to the appropriate latch. See Figure 2 for the timing diagram and Table 5 for the latch truth table.

The maximum allowable serial clock rate is 20 MHz. This means that the maximum update rate possible for the device is 833 kHz, or one update every 1.2 µs. This is certainly more than adequate for systems that have typical lock times in the hundreds of microseconds.

ADuC812 Interface

Figure 38 shows the interface between the ADF4110 family and the ADuC812 MicroConverter®. Since the ADuC812 is based on an 8051 core, this interface can be used with any 8051 based microcontroller. The MicroConverter is set up for SPI master mode with CPHA = 0. To initiate the operation, the I/O port driving LE is brought low. Each latch of the ADF4110 family needs a 24-bit word. This is accomplished by writing three 8-bit bytes from the MicroConverter to the device. When the third byte has been written, the LE input should be brought high to complete the transfer.

When power is first applied to the ADF4110 family, three writes are needed (one each to the R counter latch, N counter latch, and initialization latch) for the output to become active.

I/O port lines on the ADuC812 are also used to control power-down (CE input), and to detect lock (MUXOUT configured as lock detect and polled by the port input).

When the ADuC812 is operating in the mode described above, the maximum SCLOCK rate of the ADuC812 is 4 MHz. This means that the maximum rate at which the output frequency can be changed is 166 kHz.

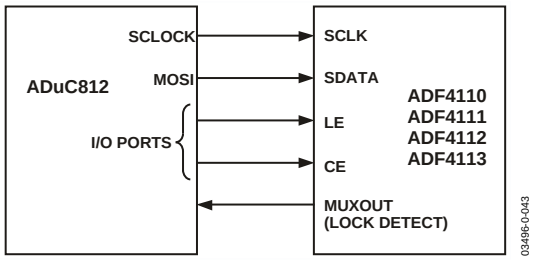


Figure 38. ADuC812 to ADF4110 Family Interface

ADSP-2181 Interface

Figure 39 shows the interface between the ADF4110 family and the ADSP-21xx digital signal processor. The ADF4110 family needs a 24-bit serial word for each latch write. The easiest way to accomplish this using the ADSP-21xx family is to use the auto buffered transmit mode of operation with alternate framing. This provides a means for transmitting an entire block of serial data before an interrupt is generated.

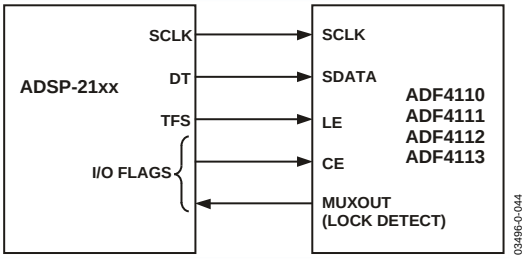


Figure 39. ADSP-21xx to ADF4110 Family Interface

Set up the word length for 8 bits and use three memory locations for each 24-bit word. To program each 24-bit latch, store the three 8-bit bytes, enable the auto buffered mode, and then write to the transmit register of the DSP. This last operation initiates the autobuffer transfer.

PCB DESIGN GUIDELINES FOR CHIP SCALE PACKAGE

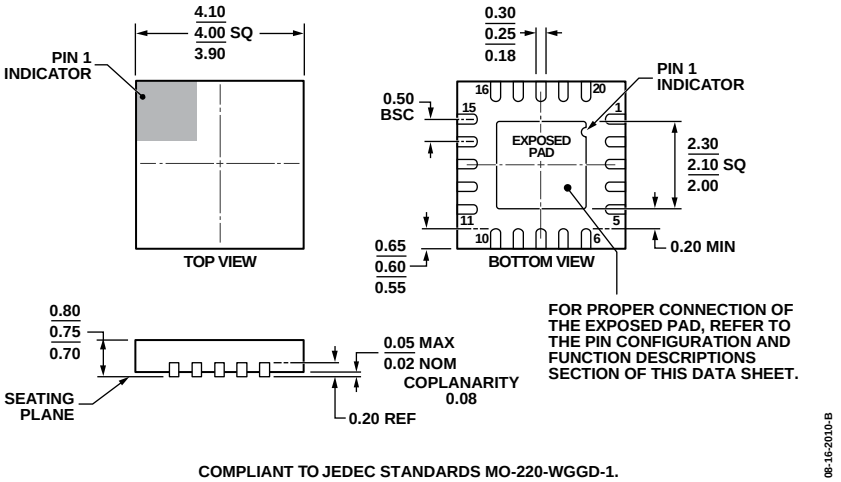
The lands on the chip scale package (CP-20) are rectangular. The printed circuit board pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land should be centered on the pad. This ensures that the solder joint size is maximized.

The bottom of the chip scale package has a central thermal pad. The thermal pad on the printed circuit board should be at least as large as this exposed pad. On the printed circuit board, there should be a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern. This ensures that shorting is avoided.

Thermal vias may be used on the printed circuit board thermal pad to improve thermal performance of the package. If vias are used, they should be incorporated in the thermal pad at 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm, and the via barrel should be plated with 1 oz. copper to plug the via.

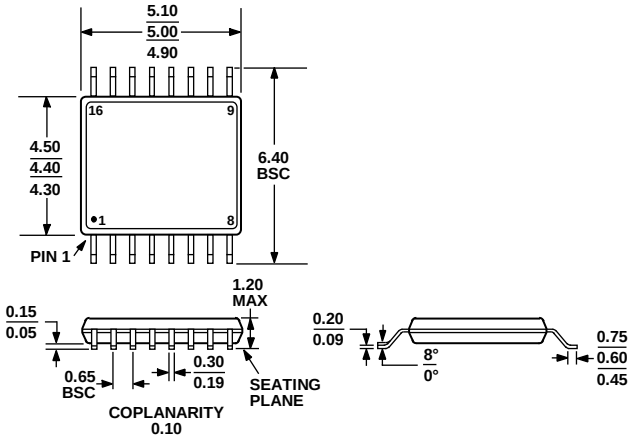
The user should connect the printed circuit board thermal pad to AGND.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-1.

Figure 40. 20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-20-6)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 41. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option[2]
ADF4110BCPZ	–40°C to +85°C	20-Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6
ADF4110BCPZ-RL	–40°C to +85°C	20-Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6
ADF4110BCPZ-RL7	–40°C to +85°C	20-Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6
ADF4110BRU	–40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4110BRU-REEL	–40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4110BRU-REEL7	-40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4110BRUZ	–40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4110BRUZ-RL	–40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4110BRUZ-RL7	–40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4111BCPZ	–40°C to +85°C	20-Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6
ADF4111BCPZ-RL	–40°C to +85°C	20-Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6
ADF4111BCPZ-RL7	–40°C to +85°C	20-Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6
ADF4111BRU	–40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4111BRUZ	–40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4111BRUZ-RL	–40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4111BRUZ-RL7	–40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4112BCPZ	–40°C to +85°C	20-Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6
ADF4112BCPZ-RL	–40°C to +85°C	20-Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6
ADF4112BCPZ-RL7	–40°C to +85°C	20-Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6
ADF4112BRU	–40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4112BRU-REEL7	–40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4112BRUZ	–40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4112BRUZ-REEL	–40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4112BRUZ-REEL7	–40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4113BCPZ	–40°C to +85°C	20-Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6
ADF4113BCPZ-RL	–40°C to +85°C	20-Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6
ADF4113BCPZ-RL7	–40°C to +85°C	20-Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6
ADF4113BRU	–40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4113BRU-REEL7	–40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4113BRUZ	–40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4113BRUZ-REEL	–40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4113BRUZ-REEL7	–40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4113BCHIPS	–40°C to +85°C	DIE	
EVAL-ADF4113EBZ1		Evaluation Board	
EVAL-ADF4113EBZ2		Evaluation Board	
EV-ADF411XSD1Z		Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] CP-20-6 package was formerly CP-20-1 package.

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