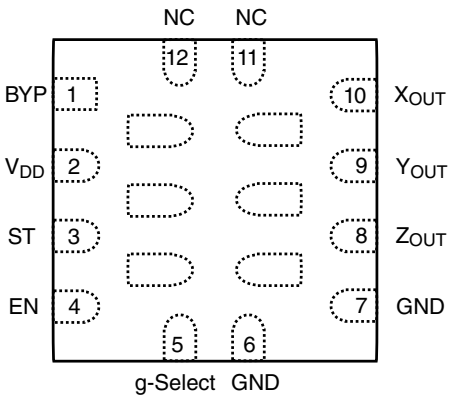
Xtrinsic FXLN83xxQ 3-Axis Low-Power Analog-Output Accelerometer

FXLN83xxQ

12-pin QFN
3 mm x 3 mm x 1 mm
Case 2300-01



Pin Connections

FXLN83xxQ is a family of 3-axis, low-power, low-*g*, analog-output accelerometers that consist of an acceleration sensor along with a CMOS signal conditioning and control ASIC in a 3x3x1mm QFN package. The analog outputs for the X, Y, and Z axes are internally compensated for zero-*g* offset and sensitivity, and then buffered to the output pads. The outputs have a fixed zero-*g* offset of 0.75V, irrespective of the V_{DD} supply voltage. The bandwidth of the output signal for each axis may be independently adjusted using external capacitors. The host can place the FXLN83xxQ into a low-current shutdown mode to conserve power.

Features

- Supply voltage (V_{DD}) from 1.71 V to 3.6 V
- Accelerometer operating ranges selectable
  - ±2 *g* or ±8 *g* (FXLN83x1Q)
  - ±4 *g* or ±16 *g* (FXLN83x2Q)
- Low current consumption of 180 µA (typical)
- Output Bandwidth Options
  - High bandwidth, 2.7 kHz (XY axes), 600 Hz (Z axis), (FXLN837XQ)
  - Low bandwidth, 1.1 kHz (XY axes), 600 Hz (Z axis), (FXLN836XQ)
- 3 x 3 x 1 mm, 12-pin QFN package (0.65 mm lead pitch)
- Robust design with high shock survivability (10,000 *g*)
- Operating temperature from –40 °C to +105 °C
- MSL 1 compliant

Typical Applications

- Tamper detection
- White goods: tilt, vibration, and shake detection
- Motion sensing in robotics applications
- Inclinometer, vibrometer
- Activity monitoring in sports and medical devices

Ordering Information

Part Number	Operating Range	Bandwidth	Temperature Range	Package Description	Shipping
FXLN8361QR1	±2/8 *g*	Low	–40 °C to +105 °C	QFN-12	Tape and reel (1 k)
FXLN8362QR1	±4/16 *g*	Low	–40 °C to +105 °C	QFN-12	Tape and reel (1 k)
FXLN8371QR1	±2/8 *g*	High	–40 °C to +105 °C	QFN-12	Tape and reel (1 k)
FXLN8372QR1	±4/16 *g*	High	–40 °C to +105 °C	QFN-12	Tape and reel (1 k)

Related Documentation

The FXLN83xxQ device features and operations are described in a variety of reference manuals, user guides, and application notes. To find the most-current versions of these documents:

1. Go to the Freescale homepage at freescale.com.
2. In the **Keyword** search box at the top of the page, enter the device number FXLN83xxQ.
3. In the **Refine Your Result** pane on the left, click on the **Documentation** link.

Table of Contents

1 General Description

1.1 Block Diagram

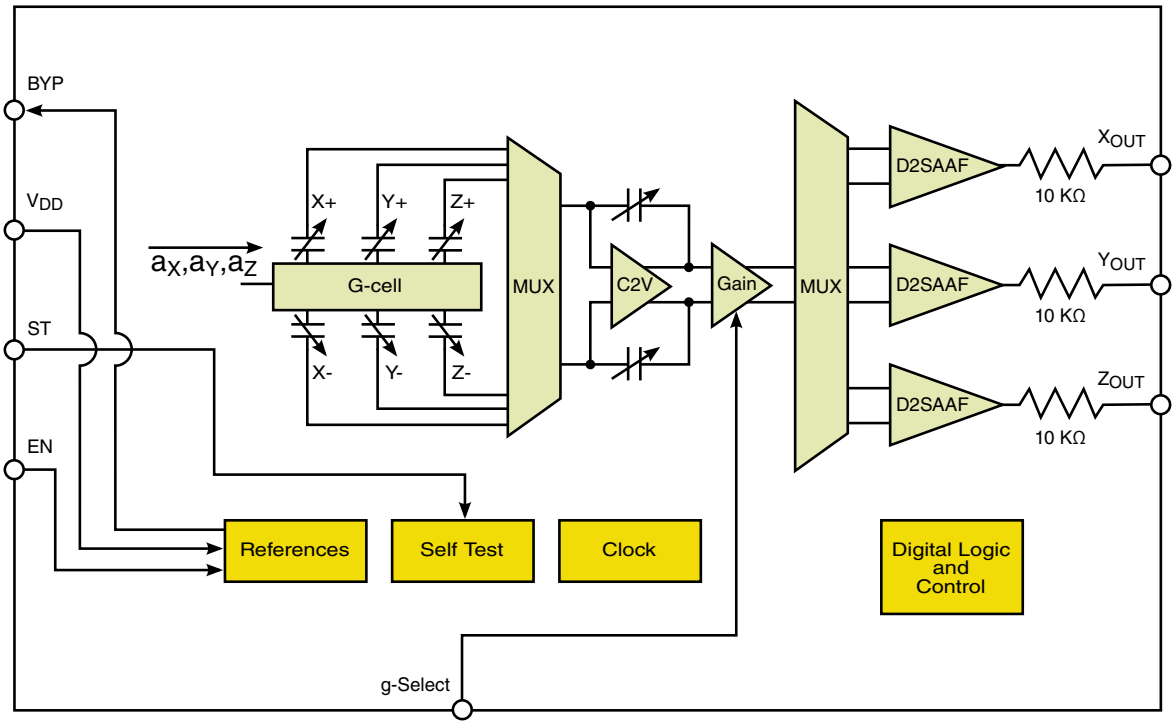


Figure 1. FXLN83xxQ block diagram

1.2 Pin Descriptions

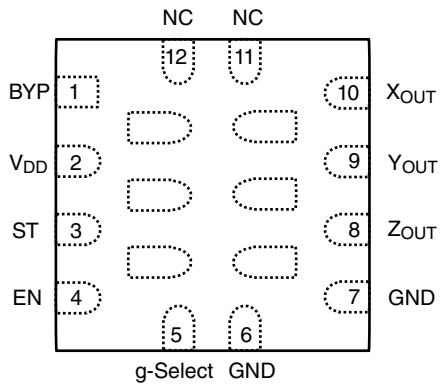


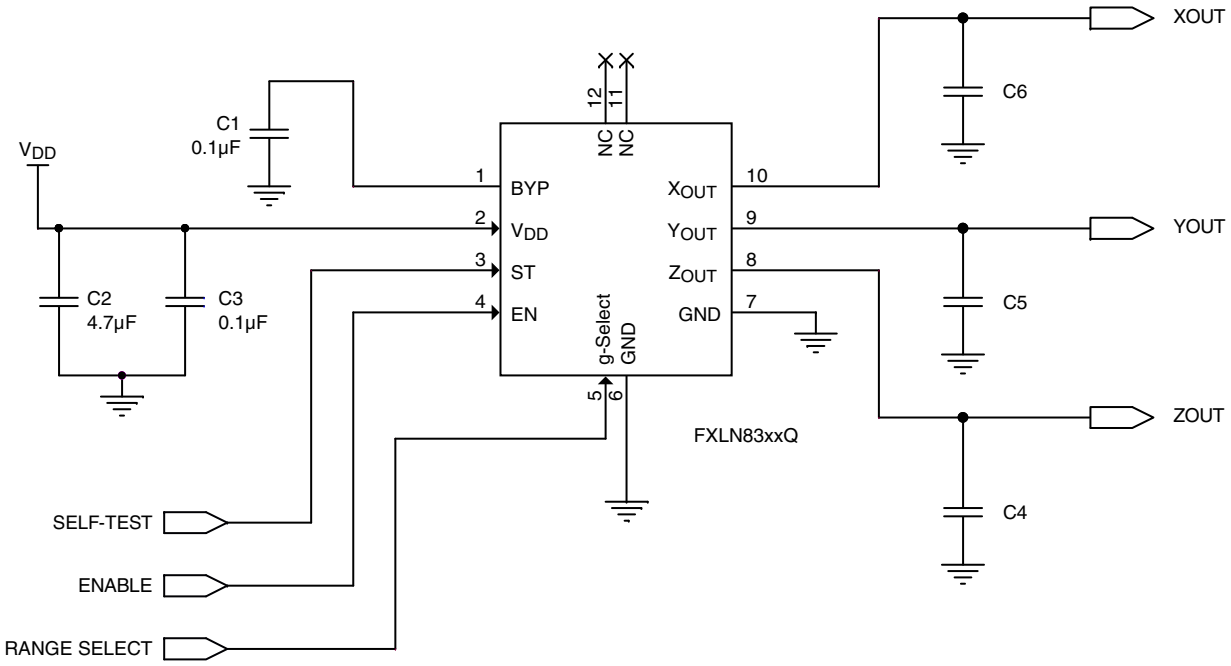
Figure 2. Pin locations

Table 1. Pin descriptions

Pin	Name	Description	I/O
1	BYP	Internal voltage regulator output capacitor connection	Output
2	V_{DD}	Supply voltage	Power
3	ST[1]	Self-Test • When ST pin is logic high, the accelerometer is put into self-test mode. • When ST pin is logic low, the accelerometer is put into normal operating mode.	Input
4	EN	Power enable pin • When the EN pin is logic low, the accelerometer is shut down, minimizing current consumption. • When the EN pin is logic high, the accelerometer is fully functional.	Input
5	g-Select	Full Scale Range selection: **For part numbers FXLN8361QR1 & FXLN8371QR1:** • When the g-select pin is logic low, the accelerometer is in ±8 *g* mode • When the g-select pin is logic high, the accelerometer is in ±2 *g* mode **For part numbers FXLN8362QR1 & FXLN8372QR1:** • When the g-select pin is logic low, the accelerometer is in ±16 *g* mode • When the g-select pin is logic high, the accelerometer is in ±4 *g* mode	Input
6	GND	Ground	Ground
7	GND	Ground	Ground
8	Z_{OUT}	Z-axis analog output	Output
9	Y_{OUT}	Y-axis analog output	Output
10	X_{OUT}	X-axis analog output	Output
11	NC	No internal connection, may be left floating or connected to GND	—
12	NC	No internal connection, may be left floating or connected to GND	—
EP	DNC	Center pads should not be soldered, refer to Printed Circuit Board Layout and Device Mounting	—

1. The Self-Test function verifies the correct functioning of the sensor and signal path without the need to apply a mechanical stimulus. When Self-Test is activated, an electrostatic actuation force is applied to the sensor, simulating a small acceleration.

1.3 Typical Application Circuit

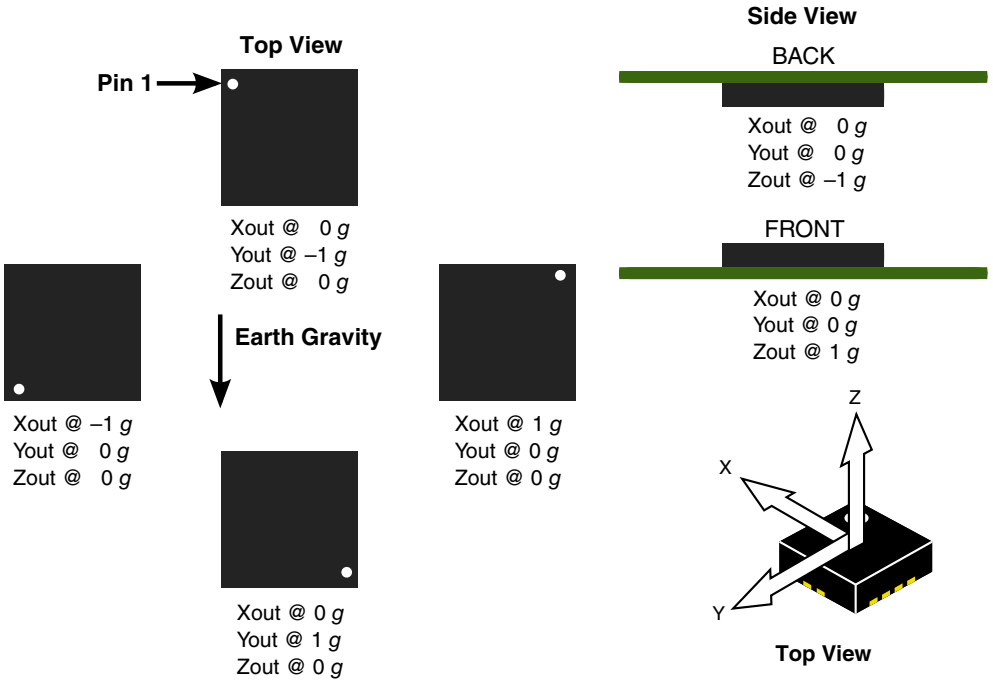


Notes:
1. Position the decoupling capacitors (C2, C3) as near as possible to the V_{DD} pin (common practice to filter out undesired noise from the power supply).
2. C1 is required to stabilize the output of the internal voltage regulator.
3. Connecting the EN pin to the V_{DD} pin is not a supported configuration and may prevent the part from starting up. Do not set the EN pin high until V_{DD} > 1.71 V.

Recommended Minimum Capacitance Specifications				
Part Number	**Bandwidth**	**C4 (pF)**	**C5 (pF)**	**C6 (pF)**
FXLN8361Q	Low	9100	9100	9100
FXLN8362Q	Low	9100	9100	9100
FXLN8371Q	High	8200	3300	3300
FXLN8372Q	High	8200	3300	3300

Figure 3. Electrical Connections

1.4 Sensing Direction and Output Response



Part Number	Mode	XYZ Output Voltage		
		–1 *g*	0 *g*	+1 *g*
FXLN8361Q, FXLN8371Q	±2 *g* ±8 *g*	0.521 0.693	0.750 0.750	0.979 0.807
FXLN8362Q, FXLN8372Q	±4 *g* ±16 *g*	0.636 0.722	0.750 0.750	0.865 0.779

Figure 4. Sensitive Axes Orientation and Response to Gravity Stimulus

2 Device Characteristics

2.1 Absolute Maximum Ratings

Absolute maximum ratings are the limits the device can be exposed to without permanently damaging it. Absolute maximum ratings are stress ratings only; functional operation at these ratings is not guaranteed. Exposure to absolute maximum ratings conditions for extended periods may affect reliability.

This device contains circuitry to protect against damage due to high static voltage or electrical fields. It is advised, however, that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit.

Table 2. Absolute maximum ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +3.6	V
Drop-test height, component	D_{drop}	1.8	m
Operating temperature range	T_{OP}	–40 to +105	°C
Storage temperature range	T_{STG}	–40 to +125	°C

Table 3. ESD and latch-up protection characteristics

Rating	Symbol	Value	Unit
Human body model (HBM)	V_{HBM}	±2000	V
Machine model (MM)	V_{MM}	±200	V
Charge device model (CDM)	V_{CDM}	±500	V
Latch-up current at T = 85 °C	I_{LU}	±100	mA

Caution
This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

Caution
This is an ESD sensitive device, improper handling can cause permanent damage to the part.

2.2 Mechanical Specifications

Table 4. Mechanical characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Full scale range (FXLN83X1)	FSR	±2 *g* mode	—	±2	—	*g*
		±8 *g* mode	—	±8	—	
Full scale range (FXLN83X2)		±4 *g* mode	—	±4	—	
		±16 *g* mode	—	±16	—	
Nominal sensitivity	SEN	±2 *g* range	—	229.0	—	mV/*g*
		±4*g* range	—	114.5	—	
		±8 *g* range	—	57.25	—	
		±16 *g* range	—	28.62	—	
Calibrated sensitivity	SEN_{CAL}	±2 *g*	V_{BYP}/(3.276*gRange)			V/*g*
		±4 *g*				
		±8 *g*				
		±16 *g*				
Calibrated sensitivity error	SEN_{ERR}	±2 *g* range	–5	—	+5	%
		±4 *g* range	–6	—	+6	
Sensitivity change vs. temperature[1]	TCS	—	–0.07	—	+0.07	%/°C
Cross-axis sensitivity[1]	CAS	—	–4.2	—	+4.2	%
Self-test output change[1]	STOC	—	35(XY) 300(Z)	—	—	m*g*
Zero-*g* level offset	V_{OFF}	±2 *g* range	0.705	0.75	0.795	V
		±4 *g* range	0.7125	0.75	0.7875	
		±8 *g* range				
		±16 *g* range				
Zero-*g* level change vs. temperature[1]	TCO	±2 *g* range	–1.2	—	+1.2	m*g*/°C
		±4 *g* range	–2.0	—	+2.0	
Zero-*g* level offset, post board mount[1]	OFF_{PBM}	1 mm (overall thickness), 2-layer, FR4-based PCB	–200	—	+200	m*g*
Noise Density[1, 2]	N_D	FXLN8371QR1, FXLN8372QR1	—	200(XY) 280(Z)	—	µ*g*/√Hz
		FXLN8361QR1, FXLN8362QR1	—	130(XY) 200(Z)	—	µ*g*/√Hz
Operating temperature range[1]	T_{OP}	—	–40	—	+105	°C
Notes:						
Test conditions (unless otherwise noted): • V_{DD} = 2.8 V, unless otherwise noted • T = 25 °C, ±2 *g* range (for ±2/8 *g* product), ±4 *g* range (for ±4/16 *g* product)						

Table 4. Mechanical characteristics

• Analog acceleration output pin loading = 3.3 nF capacitors on X and Y axes, with 8.2 nF capacitor on Z axis (HBW configuration) • Analog acceleration output pin loading = 9.1 nF capacitors on X, Y and Z axes (LBW configuration) • No analog acceleration output pin loading other than external BW setting capacitor • No BYP pin loading other than bypass capacitor and 150 µA DC current draw through resistive divider.

1. Limits verified by characterization only.
2. High and Low Bandwidth modes are configured in non-volatile Memory (NVM) at the factory

2.3 Electrical Specifications

Table 5. Electrical characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply voltage[1]	V_{DD}	—	1.71	2.8	3.6	V
Active supply current	I_{DD}	—	—	180	—	µA
Shutdown supply current	$I_{DD–SD}$	—	—	30	—	nA
Voltage supplied at BYP pin[1]	V_{BYP}	$I_{BYP} \leq 150$ µA	1.45	1.5	1.55	V
Output impedance (XYZ outputs)[1]	R_O	—	8	10	12	kΩ
Bandwidth[1, 2, 3]	BW	High BW device	—	2700(XY) 600(Z)	—	Hz
		Low BW device	—	1100(XY) 600(Z)	—	
BYP output capacitor value	C_{BYP}	External capacitor	70	100	500	nF
Logic high input level on EN, g-Select, ST pins[1]	VIH	—	0.75 * V_{DD}	—	V_{DD}	V
Logic low input level on EN, g-Select, ST pins[1]	VIL	—	0	—	0.3 * V_{DD}	V
Turn-on time[1, 2, 4]	T_{ON}		—	660	—	µs
g-Select transition delay[3]	$T_{g\text{-}Select}$		—	340	—	µs
Operating temperature range[1]	T_{OP}	—	–40	—	+105	°C
Notes:						
Test conditions (unless otherwise noted): • V_{DD} = 2.8 V • Output load = 3.3 nF capacitors on X and Y axes, with 8.2 nF capacitor on Z axis (HBW configuration) • Output load = 9.1 nF capacitors on X, Y and Z axes (LBW configuration) • Output loading other than external capacitor: high impedance • No electrical loading on BYP pin other than output capacitor and 150 µA (max) • DC output current for ADC reference input • T = 25°C, ±2 *g* range (for ±2/8 *g* product), ±4 *g* range (for ±4/16 *g* product)						

1. Limits verified by characterization only.
2. Apply VDD first. Then, Turn-on time is defined by the delay between when the EN pin is set to high and the time at which a pin's output value reaches 90% of its final value.
3. g-Select pin transition from high to low. Time for output value to reach 90% of final value.

4. BYP pin is not connected

3 Printed Circuit Board Layout and Device Mounting

Printed Circuit Board (PCB) layout and device mounting are critical to the overall performance of the design. The footprint for the surface mount packages must be the correct size as a base for a proper solder connection between the PCB and the package. This, along with the recommended soldering materials and techniques, will optimize assembly and minimize the stress on the package after board mounting.

Freescale application note AN1902, "Assembly Guidelines for QFN and DFN Packages" discusses the QFN package used by the FXLN83xxQ.

3.1 Printed Circuit Board Layout

The following recommendations are a guide to an effective PCB layout. See Figure 5 for footprint dimensions.

- The PCB land should be designed with Non-Solder Mask Defined (NSMD) as shown in Figure 5.
- No additional via pattern underneath package.
- No components or vias should be placed at a distance less than 2 mm from the package land area. This may cause additional package stress if it is too close to the package land area.
- Signal traces connected to pads should be as symmetric as possible. Put dummy traces on the NC pads in order to have same length of exposed trace for all pads.
- No copper traces should be on the top layer of the PCB under the package. This will cause planarity issues with board mount. Freescale QFN sensors are compliant with Restrictions on Hazardous Substances (RoHS), having halide-free molding compound (green) and lead-free terminations. These terminations are compatible with tin-lead (Sn-Pb) as well as tin-silver-copper (Sn-Ag-Cu) solder paste soldering processes. Reflow profiles applicable to those processes can be used successfully for soldering the devices.

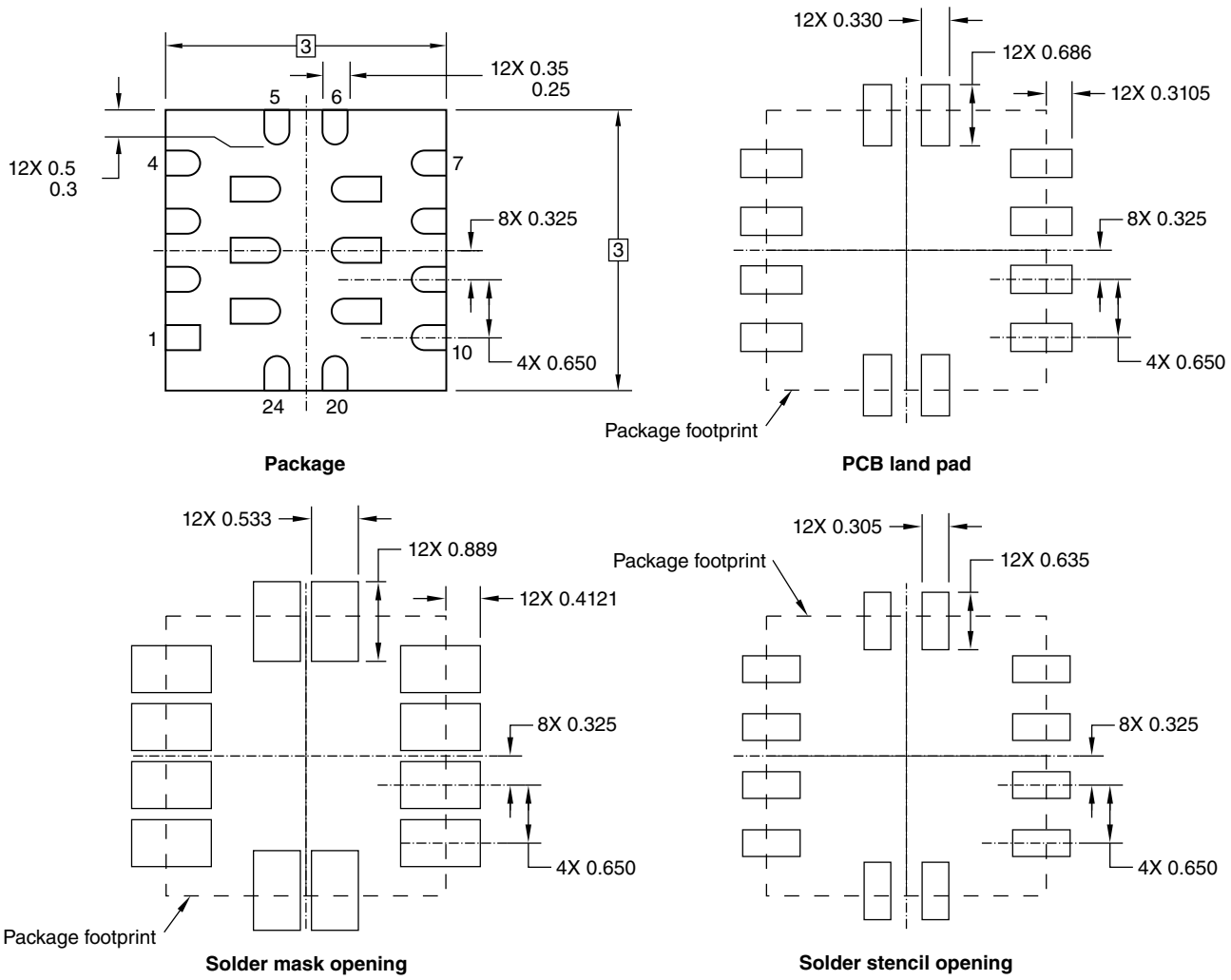


Figure 5. Footprint

3.2 Overview of Soldering Considerations

The information provided here is based on experiments executed on QFN devices. These experiments cannot represent exact conditions present at a customer site. Therefore, information herein should be used for guidance purposes only. Process and design optimizations are recommended to develop an application-specific solution. With the proper PCB footprint and solder stencil designs, the package will self-align during the solder reflow process.

- Stencil thickness should be 100 or 125 µm.
- The PCB should be rated for the multiple lead-free reflow condition with a maximum 260 °C temperature.

- Use a standard pick-and-place process and equipment. Do not use a hand soldering process.
- Do not use a screw-down or stacking to mount the PCB into an enclosure. These methods could bend the PCB, which would put stress on the package.

3.3 Halogen Content

This package is designed to be Halogen Free, exceeding most industry and customer standards. Halogen Free means that no homogeneous material within the assembly package shall contain chlorine (Cl) in excess of 700 ppm or 0.07% weight/weight or bromine (Br) in excess of 900 ppm or 0.09% weight/weight.

4 Package Information

The FXLN83xxQ device uses a 12-lead QFN package, case number 2300-01.

4.1 Device Marking

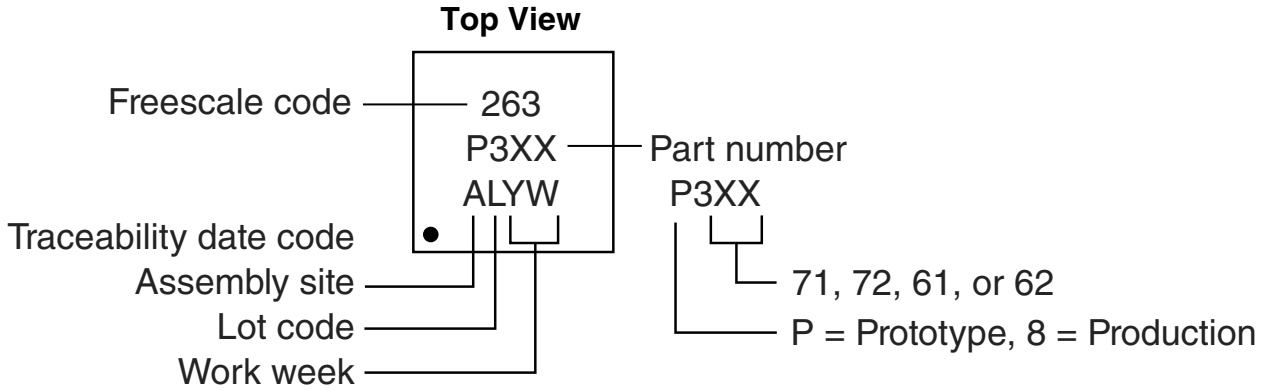
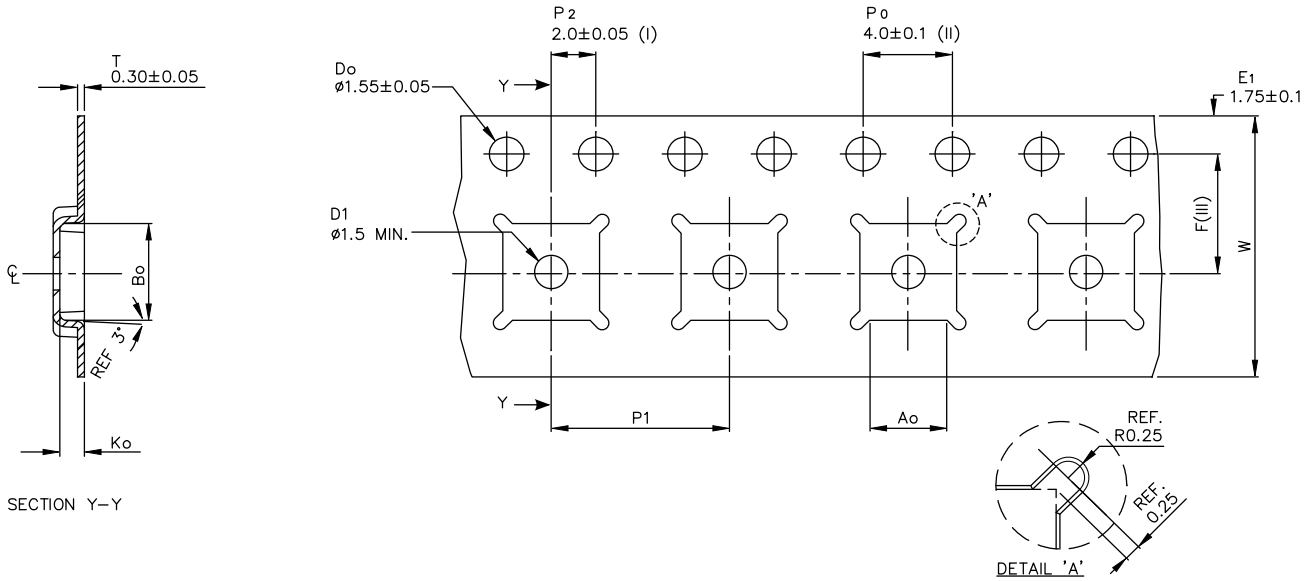


Figure 6. Device Marking Description

4.2 Tape and Reel Information



Ao	4.35 +/– 0.1
Bo	4.35 +/– 0.1
Ko	1.10 +/– 0.1
F	5.50 +/– 0.05
P1	8.00 +/– 0.1
W	12.00 +/– 0.3

(I) Measured from centerline of sprocket hole to centerline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centerline of sprocket hole to centerline of pocket.
(IV) Other material available.
(V) Typical SR value Max 10^9 OHM/SQ
ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE STATED.

Figure 7. Tape dimensions

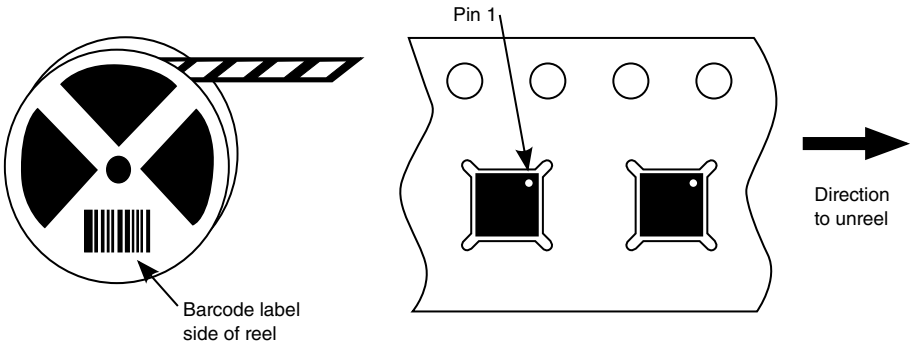
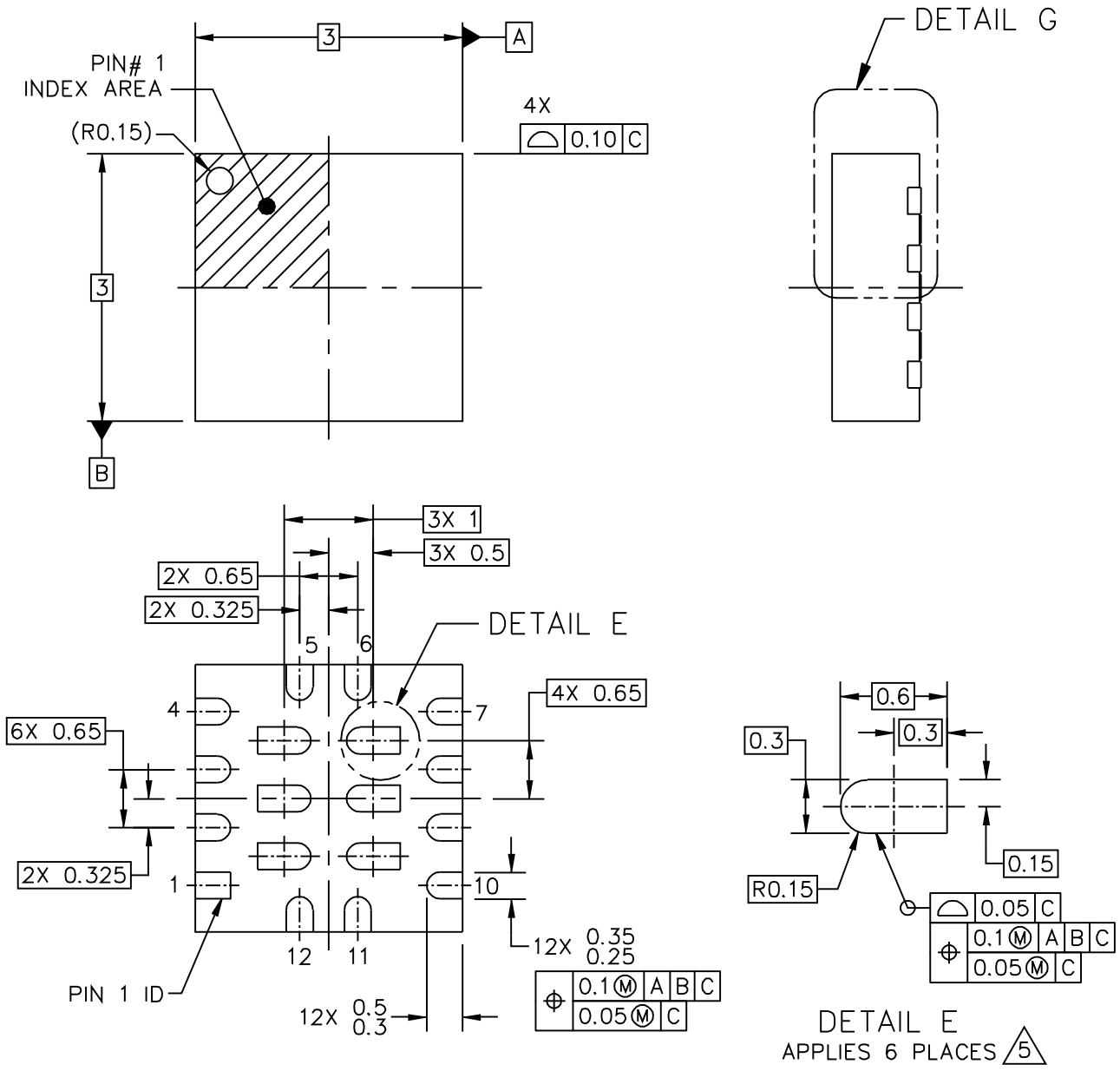


Figure 8. Tape and reel orientation

4.3 Package Description



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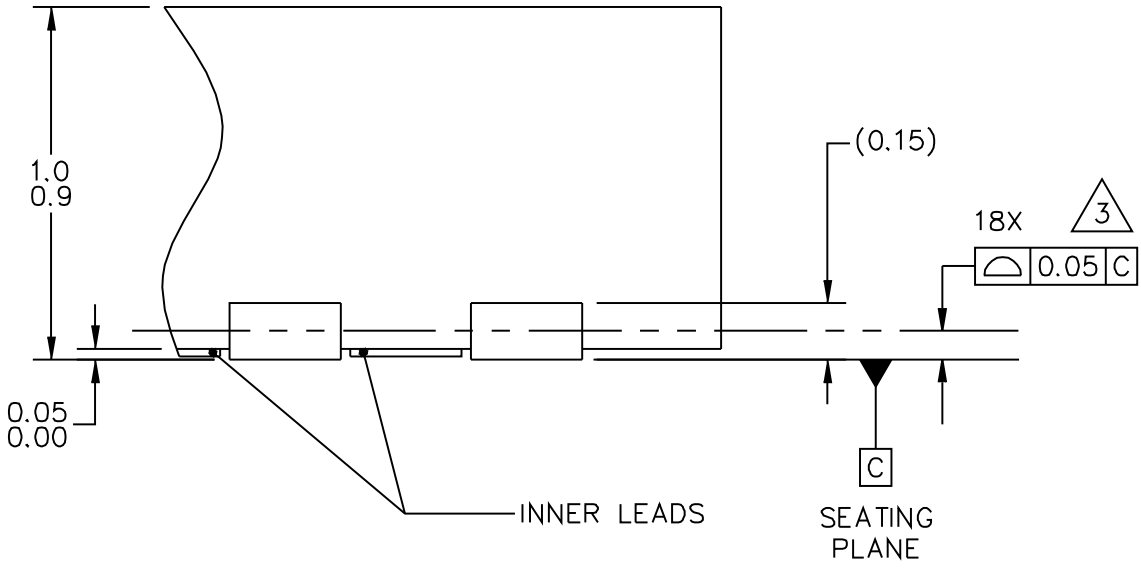
TITLE: QFN-COL, 3 X 3 X 1, 0.65 PITCH, 12 TERMINAL	DOCUMENT NO: 98ASA00480D	REV: O
	CASE NUMBER: 2300-01	26 JUL 2012
	STANDARD: NON-JEDEC	



DETAIL G
VIEW ROTATED 90° CW

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. COPLANARITY APPLIES TO LEADS.
4. MIN. METAL GAP SHOULD BE 0.2 MM.
5. CENTER TERMINALS ARE NOT SOLDERABLE.

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TITLE: QFN–COL, 3 X 3 X 1, 0.65 PITCH, 12 TERMINAL	DOCUMENT NO: 98ASA00480D	REV: O	
	CASE NUMBER: 2300–01	26 JUL 2012	
	STANDARD: NON–JEDEC		

This drawing is located at freescale.com.

5 Revision History

Revision number	Revision date	Description
1.0	11/2013	Initial release.
1.1	7/2014	Revised to match current Freescale standard Figure 3, added note #3
2.0	7/2014	Changed document type from Advance Information to Technical Data

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Revision 2.0, 7/2014