Programmable Fanout Buffer

5P1103

DATASHEET

Description

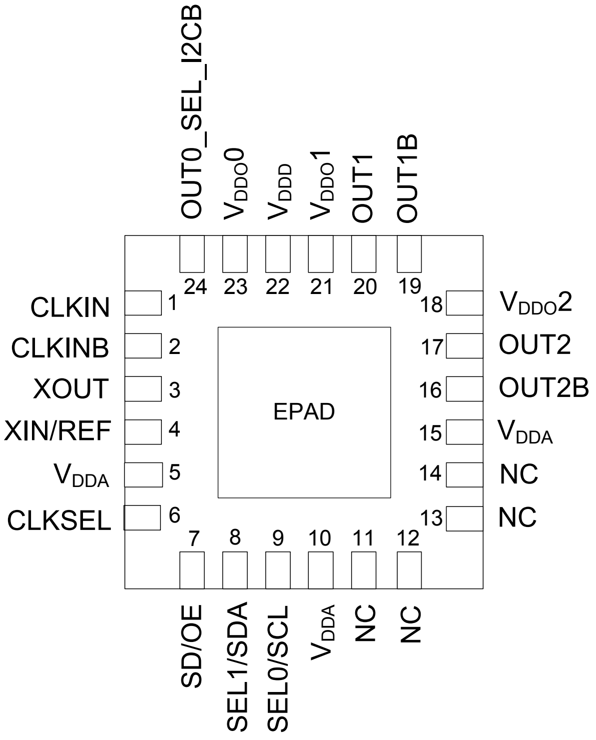
The 5P1103 is a programmable fanout buffer intended for high performance consumer, networking, industrial, computing, and data-communications applications. Configurations may be stored in on-chip One-Time Programmable (OTP) memory or changed using I^2C interface.

The outputs are generated from a single reference clock. The input reference can be crystal, external single-ended or differential clock. The reference clock can come from one of the two redundant clock inputs and is selected by CLKSEL pin. A glitchless manual switchover function allows one of the redundant clocks to be selected during normal operation. See reference clock input section for details.

Two select pins allow up to 4 different configurations to be programmed and accessible using processor GPIOs or bootstrapping. The different selections may be used for different operating modes (full function, partial function, partial power-down), regional standards (US, Japan, Europe) or system production margin testing.

The device may be configured to use one of two I^2C addresses to allow multiple devices to be used in a system.

Pin Assignment

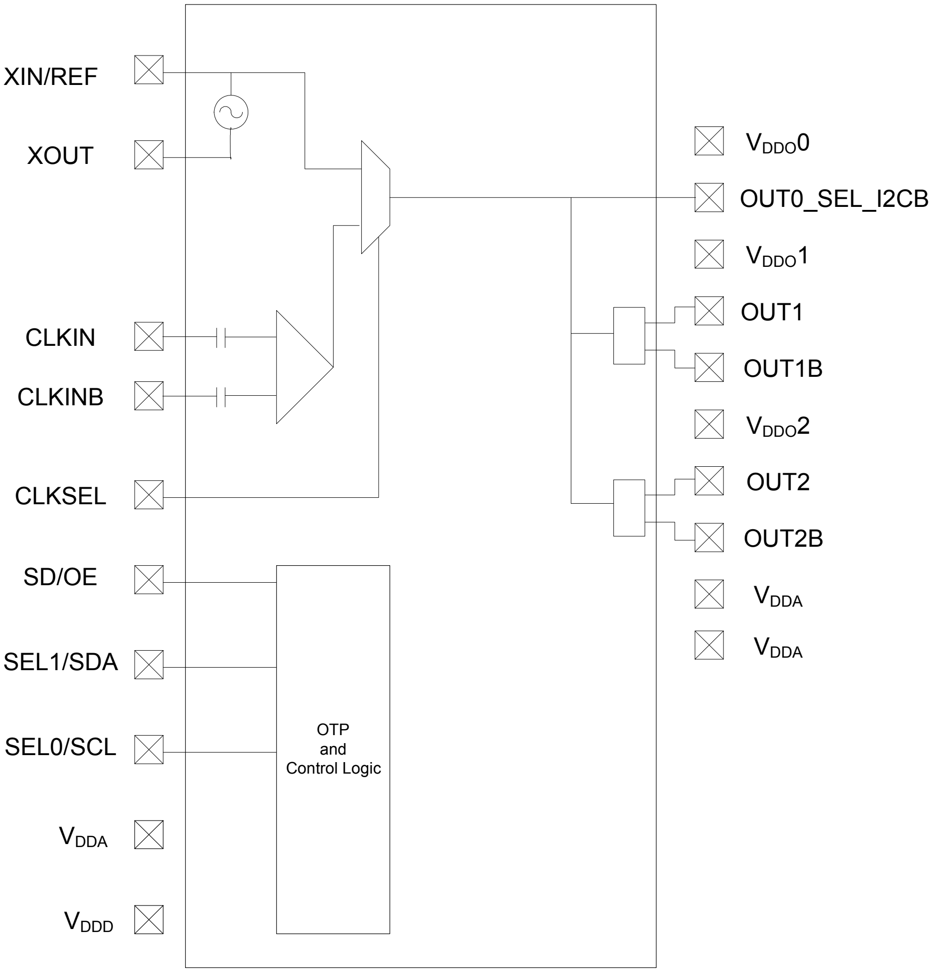


24-pin VFQFPN

Features

- Up to two high performance universal differential output pairs
  - Low RMS additive phase jitter: 0.2ps
- Four banks of internal non-volatile in-system programmable or factory programmable OTP memory
- I^2C serial programming interface
- One additional LVCMOS output clock
- Two universal output pairs:
  - Each configurable as one differential output pair or two LVCMOS outputs
- I/O Standards:
  - Single-ended I/Os: 1.8V to 3.3V LVCMOS
  - Differential I/Os - LVPECL, LVDS and HCSL
- Input frequency ranges:
  - LVCMOS Reference Clock Input (XIN/REF) – 1MHz to 200MHz
  - LVDS, LVPECL, HCSL Differential Clock Input (CLKIN, CLKINB) – 1MHz to 350MHz
  - Crystal frequency range: 8MHz to 40MHz
- Individually selectable output voltage (1.8V, 2.5V, 3.3V) for each output pair
- Redundant clock inputs with manual switchover
- Programmable crystal load capacitance
- Individual output enable/disable
- Power-down mode
- 1.8V, 2.5V or 3.3V core V_{DDD}, V_{DDA}
- Available in 24-pin VFQFPN 4mm x 4mm package
- -40° to +85°C industrial temperature operation

Functional Block Diagram



Applications

- Ethernet switch/router
- PCI Express 1.0/2.0/3.0
- Broadcast video/audio timing
- Multi-function printer
- Processor and FPGA clocking
- MSAN/DSLAM/PON
- Fiber Channel, SAN
- Telecom line cards
- 1 GbE and 10 GbE

Table 1:Pin Descriptions

Number	Name	Type		Description
1	CLKIN	Input	Pull-down	Differential clock input. Weak 100kohms internal pull-down.
2	CLKINB	Input	Pull-down	Complementary differential clock input. Weak 100kohms internal pull-down.
3	XOUT	Input		Crystal Oscillator interface output.
4	XIN/REF	Input		Crystal Oscillator interface input, or single-ended LVCMOS clock input. Ensure that the input voltage is 1.2V max. Refer to the section “Overdriving the XIN/REF Interface”.
5	VDDA	Power		Analog functions power supply pin. Connect to 1.8V to 3.3V. VDDA and VDDD should have the same voltage applied.
6	CLKSEL	Input	Pull-down	Input clock select. Selects the active input reference source, when in Manual switchover mode. 0 = XIN/REF, XOUT (default) 1 = CLKIN, CLKINB CLKSEL Polarity can be changed by I2C programming as shown in Table 4.
7	SD/OE	Input	Pull-down	Enables/disables the outputs (OE) or powers down the chip (SD). The SH bit controls the configuration of the SD/OE pin. The SH bit needs to be high for SD/OE pin to be configured as SD. The SP bit (0x02) controls the polarity of the signal to be either active HIGH or LOW only when pin is configured as OE (Default is active LOW.) Weak internal pull down resistor. When configured as SD, device is shut down, differential outputs are driven high/low, and the single-ended LVCMOS outputs are driven low. When configured as OE, and outputs are disabled, the outputs can be selected to be tri-stated or driven high/low, depending on the programming bits as shown in the SD/OE Pin Function Truth table.
8	SEL1/SDA	Input	Pull-down	Configuration select pin, or I2C SDA input as selected by OUT0_SEL_I2CB. Weak internal pull down resistor.
9	SEL0/SCL	Input	Pull-down	Configuration select pin, or I2C SCL input as selected by OUT0_SEL_I2CB. Weak internal pull down resistor.
10	VDDA	Power		Analog functions power supply pin. Connect to 1.8V to 3.3V. VDDA and VDDD should have the same voltage applied.
11	NC			No connect.
12	NC			No connect.
13	NC			No connect.
14	NC			No connect.
15	VDDA	Power		Analog functions power supply pin. Connect to 1.8V to 3.3V. VDDA and VDDD should have the same voltage applied.
16	OUT2B	Output		Complementary Output Clock 2. Please refer to the Output Drivers section for more details.
17	OUT2	Output		Output Clock 2. Please refer to the Output Drivers section for more details.
18	VDDO2	Power		Output power supply. Connect to 1.8 to 3.3V. Sets output voltage levels for OUT2/OUT2B.
19	OUT1B	Output		Complementary Output Clock 1. Please refer to the Output Drivers section for more details.
20	OUT1	Output		Output Clock 1. Please refer to the Output Drivers section for more details.
21	VDDO1	Power		Output power supply. Connect to 1.8 to 3.3V. Sets output voltage levels for OUT1/OUT1B.
22	VDDD	Power		Digital functions power supply pin. Connect to 1.8 to 3.3V. VDDA and VDDB should have the same voltage applied.
23	VDDO0	Power		Power supply pin for OUT0_SEL_I2CB. Connect to 1.8 to 3.3V. Sets output voltage levels for OUT0.
24	OUT0_SELB_I2C	Input/Output	Pull-down	Latched input/LVCMOS Output. At power up, the voltage at the pin OUT0_SEL_I2CB is latched by the part and used to select the state of pins 8 and 9. If a weak pull up (10Kohms) is placed on OUT0_SEL_I2CB, pins 8 and 9 will be configured as hardware select pins, SEL1 and SEL0. If a weak pull down (10Kohms) is placed on OUT0_SEL_I2CB or it is left floating, pins 8 and 9 will act as the SDA and SCL pins of an I2C interface. After power up, the pin acts as a LVCMOS reference output.
ePAD	VEE	Power		Connect to ground pad.

Configuration and Input Descriptions

Table 2: Configuration Table

This table shows the SEL1, SEL0 settings to select the configuration stored in OTP. Four configurations can be stored in OTP. These can be factory programmed or user programmed.

OUT0_SEL_I2CB @ POR	SEL1	SEL0	I^2C Access	REG0:7	Config
1	0	0	No	0	0
1	0	1	No	0	1
1	1	0	No	0	2
1	1	1	No	0	3
0	X	X	Yes	1	I2C defaults
0	X	X	Yes	0	0

At power up time, the SEL0 and SEL1 pins must be tied to either the VDDD/VDDA power supply so that they ramp with that supply or are tied low (this is the same as floating the pins). This will cause the register configuration to be loaded that is selected according to Table 3 above. Providing that OUT0_SEL_I2CB was 1 at POR and OTP register 0:7=0, after the first 10mS of operation the levels of the SELx pins can be changed, either to low or to the same level as VDDD/VDDA. The SELx pins must be driven with a digital signal of < 300nS Rise/Fall time and only a single pin can be changed at a time. After a pin level change, the device must not be interrupted for at least 1ms so that the new values have time to load and take effect.

If OUT0_SEL_I2CB was 0 at POR, alternate configurations can only be loaded via the I2C interface.

Table 3: Input Clock Select

Input clock select. Selects the active input reference source in manual switchover mode.
0 = XIN/REF, XOUT (default)
1 = CLKIN, CLKINB
CLKSEL Polarity can be changed by I^2C programming as shown in Table 4.

PRIMSRC	CLKSEL	Source
0	0	XIN/REF
0	1	CLKIN, CLKINB
1	0	CLKIN, CLKINB
1	1	XIN/REF

PRIMSRC is bit 1 of Register 0x13.

Reference Clock Input Pins and Selection

The 5P1103 supports up to two clock inputs. One input supports a crystal between XIN and XOUT. XIN can also be driven from a single ended reference clock. XIN can accept small amplitude signals like from TCXO or one channel of a differential clock.

The second clock input (CLKIN, CLKINB) is a fully differential input that only accepts a reference clock. The differential input accepts differential clocks from all the differential logic types and can also be driven from a single ended clock on one of the input pins.

The CLKSEL pin selects the input clock between either XTAL/REF or (CLKIN, CLKINB).

Either clock input can be set as the primary clock. The primary clock designation is to establish which is the main reference clock. The non-primary clock is designated as the secondary clock in case the primary clock goes absent and a backup is needed. The PRIMSRC bit determines which clock input will be selected as primary clock. When PRIMSRC bit is “0”, XIN/REF is selected as the primary clock, and when “1”, (CLKIN, CLKINB) as the primary clock.

The two external reference clocks can be manually selected using the CLKSEL pin. The SM bits must be set to “0x” for manual switchover which is detailed in Manual Switchover Mode section.

Crystal Input (XIN/REF)

The crystal used should be a fundamental mode quartz crystal; overtone crystals should not be used.

A crystal manufacturer will calibrate its crystals to the nominal frequency with a certain load capacitance value. When the oscillator load capacitance matches the crystal load capacitance, the oscillation frequency will be accurate. When the oscillator load capacitance is lower than the crystal load capacitance, the oscillation frequency will be higher than nominal and vice versa so for an accurate oscillation frequency you need to make sure to match the oscillator load capacitance with the crystal load capacitance.

To set the oscillator load capacitance there are two tuning capacitors in the IC, one at XIN and one at XOUT. They can be adjusted independently but commonly the same value is used for both capacitors. The value of each capacitor is composed of a fixed capacitance amount plus a variable capacitance amount set with the XTAL[5:0] register. Adjustment of the crystal tuning capacitors allows for maximum flexibility to accommodate crystals from various manufacturers. The range of tuning capacitor values available are in accordance with the following table.

XTAL[5:0] Tuning Capacitor Characteristics

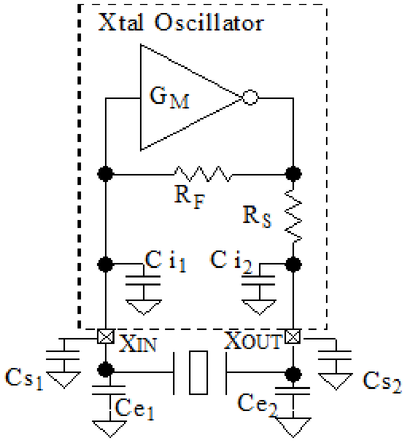
Parameter	Bits	Step (pF)	Min (pF)	Max (pF)
XTAL	6	0.5	9	25

The capacitance at each crystal pin inside the chip starts at 9pF with setting 000000b and can be increased up to 25pF with setting 111111b. The step per bit is 0.5pF.

You can write the following equation for this capacitance:

$$Ci = 9pF + 0.5pF \times XTAL[5:0]$$

The PCB where the IC and the crystal will be assembled adds some stray capacitance to each crystal pin and more capacitance can be added to each crystal pin with additional external capacitors.



You can write the following equations for the total capacitance at each crystal pin:

$$C_{XIN} = Ci_1 + Cs_1 + Ce_1$$
$$C_{XOUT} = Ci_2 + Cs_2 + Ce_2$$

Ci_1 and Ci_2 are the internal, tunable capacitors. Ci_1 and Cs_2 are stray capacitances at each crystal pin and typical values are between 1pF and 3pF.

Ce_1 and Ce_2 are additional external capacitors that can be added to increase the crystal load capacitance beyond the tuning range of the internal capacitors. However, increasing the load capacitance reduces the oscillator gain so please consult the factory when adding Ce_1 and/or Ce_2 to avoid crystal startup issues. Ce_1 and Ce_2 can also be used to adjust for unpredictable stray capacitance in the PCB.

The final load capacitance of the crystal:

$$CL = C_{XIN} \times C_{XOUT} / (C_{XIN} + C_{XOUT})$$

For most cases it is recommended to set the value for capacitors the same at each crystal pin:

$$C_{XIN} = C_{XOUT} = Cx \longrightarrow CL = Cx / 2$$

The complete formula when the capacitance at both crystal pins is the same:

$$CL = (9pF + 0.5pF \times XTAL[5:0] + Cs + Ce) / 2$$

Example 1: The crystal load capacitance is specified as 8pF and the stray capacitance at each crystal pin is Cs=1.5pF. Assuming equal capacitance value at XIN and XOUT, the equation is as follows:

8pF = (9pF + 0.5pF × XTAL[5:0] + 1.5pF) / 2 ⟶
0.5pF × XTAL[5:0] = 5.5pF ⟶ XTAL[5:0] = 11 (decimal)

Example 2: The crystal load capacitance is specified as 12pF and the stray capacitance Cs is unknown. Footprints for external capacitors Ce are added and a worst case Cs of 5pF is used. For now we use Cs + Ce = 5pF and the right value for Ce can be determined later to make 5pF together with Cs.

12pF = (9pF + 0.5pF × XTAL[5:0] + 5pF) / 2 ⟶
XTAL[5:0] = 20 (decimal)

Manual Switchover Mode

When SM[1:0] is “0x”, the redundant inputs are in manual switchover mode. In this mode, CLKSEL pin is used to switch between the primary and secondary clock sources. The primary and secondary clock source setting is determined by the PRIMSRC bit. During the switchover, no glitches will occur at the output of the device, although there may be frequency and phase drift, depending on the exact phase and frequency relationship between the primary and secondary clocks.

OTP Interface

The 5P1103 can also store its configuration in an internal OTP. The contents of the device's internal programming registers can be saved to the OTP by setting burn_start (W114[3]) to high and can be loaded back to the internal programming registers by setting usr_rd_start(W114[0]) to high.

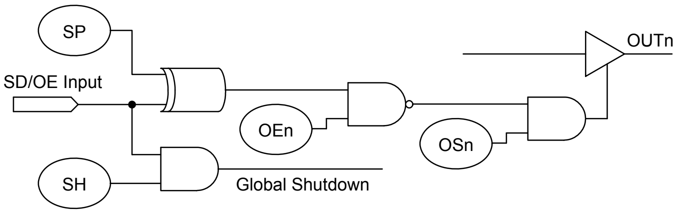
To initiate a save or restore using I^2C, only two bytes are transferred. The Device Address is issued with the read/write bit set to “0”, followed by the appropriate command code. The save or restore instruction executes after the STOP condition is issued by the Master, during which time the 5P1103 will not generate Acknowledge bits. The 5P1103 will acknowledge the instructions after it has completed execution of them. During that time, the I^2C bus should be interpreted as busy by all other users of the bus.

On power-up of the 5P1103, an automatic restore is performed to load the OTP contents into the internal programming registers. The 5P1103 will be ready to accept a programming instruction once it acknowledges its 7-bit I^2C address.

Availability of Primary and Secondary I^2C addresses to allow programming for multiple devices in a system. The I^2C slave address can be changed from the default 0xD4 to 0xD0 by programming the I2C_ADDR bit D0. *VersaClock 5 Programming Guide* provides detailed I^2C programming guidelines and register map.

SD/OE Pin Function

The polarity of the SD/OE signal pin can be programmed to be either active HIGH or LOW with the SP bit (W16[1]). When SP is “0” (default), the pin becomes active LOW and when SP is “1”, the pin becomes active HIGH. The SD/OE pin can be configured as either to shutdown the PLL or to enable/disable the outputs. The SH bit controls the configuration of the SD/OE pin The SH bit needs to be high for SD/OE pin to be configured as SD.



When configured as SD, device is shut down, differential outputs are driven High/low, and the single-ended LVCMOS outputs are driven low. When configured as OE, and outputs are disabled, the outputs are driven high/low.

Table 4: SD/OE Pin Function Truth Table

SH bit	SP bit	OSn bit	OEn bit	SD/OE	OUTn
0	0	0	x	x	Tri-state[2]
0	0	1	0	x	Output active
0	0	1	1	0	Output active
0	0	1	1	1	Output driven High Low
0	1	0	x	x	Tri-state[2]
0	1	1	0	x	Output active
0	1	1	1	0	Output driven High Low
0	1	1	1	1	Output active
1	0	0	x	0	Tri-state[2]
1	0	1	0	0	Output active
1	0	1	1	0	Output active
1	1	0	x	0	Tri-state[2]
1	1	1	0	0	Output active
1	1	1	1	0	Output driven High Low
1	x	x	x	1	Output driven High Low [1]

Note 1 : Global Shutdown
Note 2 : Tri-state regardless of OEn bits

Output Skew

Rising edges of all outputs are automatically phase aligned.

Output Drivers

The OUT1 to OUT2 clock outputs are provided with register-controlled output drivers. By selecting the output drive type in the appropriate register, any of these outputs can support LVCMOS, LVPECL, HCSL or LVDS logic levels

The operating voltage ranges of each output is determined by its independent output power pin (V_{DDO}) and thus each can have different output voltage levels. Output voltage levels of 2.5V or 3.3V are supported for differential HCSL, LVPECL operation, and 1. 8V, 2.5V, or 3.3V are supported for LVCMOS and differential LVDS operation.

Each output may be enabled or disabled by register bits. When disabled an output will be in a logic 0 state as determined by the programming bit table shown on page 6.

LVCMOS Operation

When a given output is configured to provide LVCMOS levels, then both the OUTx and OUTxB outputs will toggle at the selected output frequency. All the previously described configuration and control apply equally to both outputs. Frequency, phase alignment, voltage levels and enable / disable status apply to both the OUTx and OUTxB pins. The OUTx and OUTxB outputs can be selected to be phase-aligned with each other or inverted relative to one another by register programming bits. Selection of phase-alignment may have negative effects on the phase noise performance of any part of the device due to increased simultaneous switching noise within the device.

Device Hardware Configuration

The 5P1103 supports an internal One-Time Programmable (OTP) memory that can be pre-programmed at the factory with up to 4 complete device configuration.

These configurations can be over-written using the serial interface once reset is complete. Any configuration written via the programming interface needs to be re-written after any power cycle or reset. Please contact IDT if a specific factory-programmed configuration is desired.

Device Start-up & Reset Behavior

The 5P1103 has an internal power-up reset (POR) circuit. The POR circuit will remain active for a maximum of 10ms after device power-up.

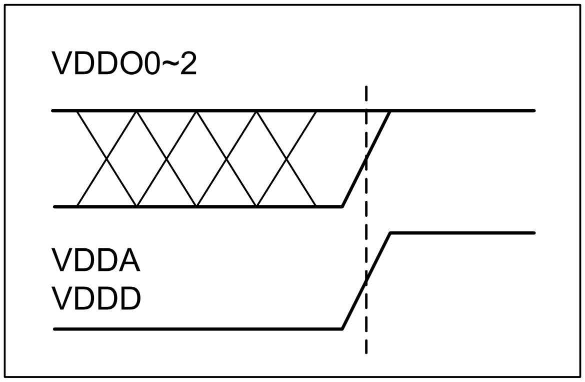
Upon internal POR circuit expiring, the device will exit reset and begin self-configuration.

The device will load internal registers using the configuration stored in the internal One-Time Programmable (OTP) memory.

Once the full configuration has been loaded, the device will respond to accesses on the serial port and will attempt to begin operation.

Power Up Ramp Sequence

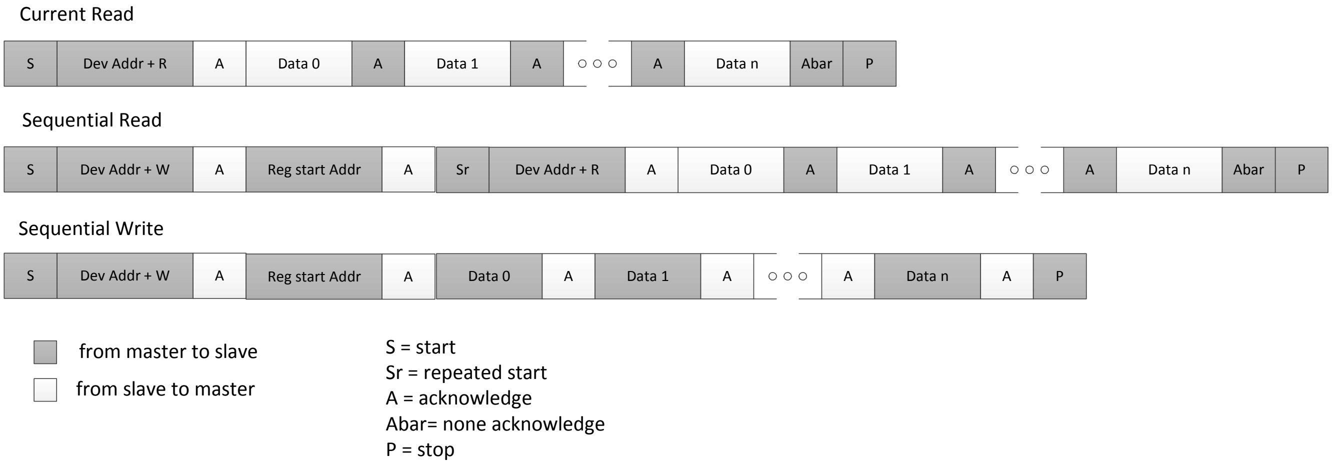
VDDA and VDDD must ramp up together. VDDO0~2 must ramp up before, or concurrently with, VDDA and VDDD. All power supply pins must be connected to a power rail even if the output is unused. All power supplies must ramp in a linear fashion and ramp monotonically.



I^{2}C Mode Operation

The device acts as a slave device on the I^{2}C bus using one of the two I^{2}C addresses (0xD0 or 0xD4) to allow multiple devices to be used in the system. The interface accepts byte-oriented block write and block read operations. Two address bytes specify the register address of the byte position of the first register to write or read. Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first). Read and write block transfers can be stopped after any complete byte transfer. During a write operation, data will not be moved into the registers until the STOP bit is received, at which point, all data received in the block write will be written simultaneously.

For full electrical I^{2}C compliance, it is recommended to use external pull-up resistors for SDATA and SCLK. The internal pull-down resistors have a size of 100kΩ typical.



I^{2}C Slave Read and Write Cycle Sequencing

Table 5: I^{2}C Bus DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	Input HIGH Level	For SEL1/SDA pin and SEL0/SCL pin.	0.7xV_{DDD}		5.5 [2]	V
V_{IL}	Input LOW Level	For SEL1/SDA pin and SEL0/SCL pin.	GND-0.3		0.3xV_{DDD}	V
V_{HYS}	Hysteresis of Inputs		0.05xV_{DDD}			V
I_{IN}	Input Leakage Current		-1		30	µA
V_{OL}	Output LOW Voltage	I_{OL} = 3 mA			0.4	V

Table 6: I^{2}C Bus AC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
F_{SCLK}	Serial Clock Frequency (SCL)	10		400	kHz
t_{BUF}	Bus free time between STOP and START	1.3			µs
$t_{SU:START}$	Setup Time, START	0.6			µs
$t_{HD:START}$	Hold Time, START	0.6			µs
$t_{SU:DATA}$	Setup Time, data input (SDA)	100			ns
$t_{HD:DATA}$	Hold Time, data input (SDA) [1]	0			µs
t_{OVD}	Output data valid from clock			0.9	µs
C_B	Capacitive Load for Each Bus Line			400	pF
t_R	Rise Time, data and clock (SDA, SCL)	20 + 0.1xC_B		300	ns
t_F	Fall Time, data and clock (SDA, SCL)	20 + 0.1xC_B		300	ns
t_{HIGH}	HIGH Time, clock (SCL)	0.6			µs
t_{LOW}	LOW Time, clock (SCL)	1.3			µs
$t_{SU:STOP}$	Setup Time, STOP	0.6			µs

Note 1: A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH}(MIN) of the SCL signal) to bridge the undefined region of the falling edge of SCL.
Note 2: I2C inputs are 5V tolerant.

Table 7: Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 5P1103. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, $V_{DDA,}$ $V_{DDD,}$ V_{DDO}	3.465V
Inputs XIN/REF CLKIN, CLKINB Other inputs	 0V to 1.2V voltage swing 0V to 1.2V voltage swing single-ended -0.5V to V_{DDD}
Outputs, V_{DDO} (LVCMOS)	-0.5V to V_{DDO}+ 0.5V
Outputs, I_O (SDA)	10mA
Package Thermal Impedance, θ_{JA}	42°C/W (0 mps)
Package Thermal Impedance, θ_{JC}	41.8°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C
ESD Human Body Model	2000V
Junction Temperature	125°C

Table 8: Recommended Operation Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DDOX}	Power supply voltage for supporting 1.8V outputs	1.71	1.8	1.89	V
V_{DDOX}	Power supply voltage for supporting 2.5V outputs	2.375	2.5	2.625	V
V_{DDOX}	Power supply voltage for supporting 3.3V outputs	3.135	3.3	3.465	V
V_{DDD}	Power supply voltage for core logic functions	1.71		3.465	V
V_{DDA}	Analog power supply voltage. Use filtered analog power supply.	1.71		3.465	V
T_A	Operating temperature, ambient	-40		+85	°C
C_{LOAD_OUT}	Maximum load capacitance (3.3V LVCMOS only)			15	pF
F_{IN}	External reference crystal	8		40	MHz
	External reference clock CLKIN, CLKINB	1		350	
t_{PU}	Power up time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic)	0.05		5	ms

Note: V_{DDO}1 and V_{DDO}2 must be powered on either before or simultaneously with V_{DDD}, V_{DDA} and V_{DDO}0.

Table 9: Input Capacitance, LVCMOS Output Impedance, and Internal Pull-down Resistance (T_A = +25 °C)

Symbol	Parameter	Min	Typ	Max	Unit
CIN	Input Capacitance (SD/OE, SEL1/SDA, SEL0/SCL)		3	7	pF
Pull-down Resistor		100		300	kΩ
ROUT	LVCMOS Output Driver Impedance (VDDO = 1.8V, 2.5V, 3.3V)		17		Ω
XIN/REF	Programmable capacitance at XIN/REF	9		25	pF
XOUT	Programmable capacitance at XOUT	9		25	pF

Table 10: Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		8	25	40	MHz
Equivalent Series Resistance (ESR)			10	100	Ω
Shunt Capacitance				7	pF
Load Capacitance (CL) @ <=25 MHz		6	8	12	pF
Load Capacitance (CL) >25M to 40M		6		8	pF
Maximum Crystal Drive Level				100	μW

Note: Typical crystal used is IDT 603-25-150 or FOX 603-25-150. For different reference crystal options please go to www.foxonline.com.

Table 11: DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Iddcore[3]	Core Supply Current	100 MHz on all outputs, 25 MHz REFCLK		4	5	mA
Iddox	Output Buffer Supply Current	LVPECL, 350 MHz, 3.3V VDDOx		35	37	mA
		LVPECL, 350 MHz, 2.5V VDDOx		33	35	mA
		LVDS, 350 MHz, 3.3V VDDOx		8	9	mA
		LVDS, 350 MHz, 2.5V VDDOx		7	8	mA
		LVDS, 350 MHz, 1.8V VDDOx		6	7	mA
		HCSL, 250 MHz, 3.3V VDDOx, 2 pF load		22	23	mA
		HCSL, 250 MHz, 2.5V VDDOx, 2 pF load		20	22	mA
		LVCMOS, 50 MHz, 3.3V, VDDOx [1,2]		5	6	mA
		LVCMOS, 50 MHz, 2.5V, VDDOx [1,2]		4	5	mA
		LVCMOS, 50 MHz, 1.8V, VDDOx [1,2]		3	4	mA
		LVCMOS, 200 MHz, 3.3V VDDOx[1]		17	18	mA
		LVCMOS, 200 MHz, 2.5V VDDOx[1,2]		12	13	mA
		LVCMOS, 200 MHz, 1.8V VDDOx[1,2]		9	10	mA
Iddpd	Power Down Current	SD asserted, I2C Programming		5	6	mA

1. Single CMOS driver active.
2. Measured into a 5” 50 Ohm trace with 2 pF load.
3. Iddcore = IddA + IddD, no loads.

Table 12: Electrical Characteristics – Differential Clock Input Parameters [1,2] (Supply Voltage V_{DDA}, V_{DDD}, $V_{DDO}0$ = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, TA = -40°C to +85°C)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IH}	Input HIGH Voltage–CLKIN, CLKINB	Single-ended input	0.55		1.7	V
V_{IL}	Input LOW Voltage–CLKIN, CLKINB	Single-ended input	GND - 0.3		0.4	V
V_{SWING}	Input Amplitude - CLKIN, CLKINB	Peak to Peak value, single-ended	200		1200	mV
dv/dt	Input Slew Rate - CLKIN, CLKINB	Measured differentially	0.4		8	V/ns
I_{IL}	Input Leakage Low Current	V_{IN} = GND	-5		5	μA
I_{IH}	Input Leakage High Current	V_{IN} = 1.7V			20	μA
d_{TIN}	Input Duty Cycle	Measurement from differential waveform	45		55	%

1. Guaranteed by design and characterization, not 100% tested in production.
2. Slew rate measured through ±75mV window centered around differential zero.

Table 13: DC Electrical Characteristics for 3.3V LVCMOS (V_{DDO} = 3.3V±5%, TA = -40°C to +85°C) [1]

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
VOH	Output HIGH Voltage	IOH = -15mA	2.4		VDDO	V
VOL	Output LOW Voltage	IOL = 15mA			0.4	V
IOZDD	Output Leakage Current (OUT1~4)	Tri-state outputs, VDDO = 3.465V			5	μA
IOZDD	Output Leakage Current (OUT0)	Tri-state outputs, VDDO = 3.465V			30	μA
VIH	Input HIGH Voltage	Single-ended inputs - CLKSEL, SD/OE	0.7xVDDD		VDDD + 0.3	V
VIL	Input LOW Voltage	Single-ended inputs - CLKSEL, SD/OE	GND - 0.3		0.3xVDDD	V
VIH	Input HIGH Voltage	Single-ended input OUT0_SEL_I2CB	2		VDDO0 + 0.3	V
VIL	Input LOW Voltage	Single-ended input OUT0_SEL_I2CB	GND - 0.3		0.4	V
VIH	Input HIGH Voltage	Single-ended input - XIN/REF	0.8		1.2	V
VIL	Input LOW Voltage	Single-ended input - XIN/REF	GND - 0.3		0.4	V
TR/TF	Input Rise/Fall Time	CLKSEL, SD/OE, SEL1/SDA, SEL0/SCL			300	nS

1. See “Recommended Operating Conditions” table.

Table 14: DC Electrical Characteristics for 2.5V LVCMOS (V_{DDO} = 2.5V±5%, TA = -40°C to +85°C)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
VOH	Output HIGH Voltage	IOH = -12mA	0.7xVDDO		VDDD + 0.3	V
VOL	Output LOW Voltage	IOL = 12mA			0.4	V
IOZDD	Output Leakage Current	Tri-state outputs, VDDO = 2.625V			5	µA
VOH	Output HIGH Voltage	IOH = -12mA, OUT0	0.6 xVDDO		VDDD + 0.3	V
VOL	Output LOW Voltage	IOL = 12mA, OUT0			0.4	V
IOZDD	Output Leakage Current	Tri-state outputs, VDDO = 2.625V, OUT0			30	µA
VIH	Input HIGH Voltage	Single-ended inputs - CLKSEL, SD/OE	0.7xVDDD		VDDD + 0.3	V
VIL	Input LOW Voltage	Single-ended inputs - CLKSEL, SD/OE	GND - 0.3		0.3xVDDD	V
VIH	Input HIGH Voltage	Single-ended input OUT0_SEL_I2CB	1.7		VDDO0 + 0.35	V
VIL	Input LOW Voltage	Single-ended input OUT0_SEL_I2CB	GND - 0.3		0.4	V
VIH	Input HIGH Voltage	Single-ended input - XIN/REF	0.8		1.2	V
VIL	Input LOW Voltage	Single-ended input - XIN/REF	GND - 0.3		0.4	V
TR/TF	Input Rise/Fall Time	CLKSEL, SD/OE, SEL1/SDA, SEL0/SCL			300	nS

Table 15: DC Electrical Characteristics for 1.8V LVCMOS (V_{DDO} = 1.8V±5%, TA = -40°C to +85°C)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
VOH	Output HIGH Voltage	IOH = -8mA	0.7 xVDDO		VDDO	V
VOL	Output LOW Voltage	IOL = 8mA			0.25 x VDDO	V
IOZDD	Output Leakage Current	Tri-state outputs, VDDO = 3.465V			5	µA
VOH	Output HIGH Voltage	IOH = -8mA, OUT0	0.6 xVDDO		VDDO	V
VOL	Output LOW Voltage	IOL = 8mA, OUT0			0.25 x VDDO	V
IOZDD	Output Leakage Current	Tri-state outputs, VDDO = 3.465V, OUT0			30	µA
VIH	Input HIGH Voltage	Single-ended inputs - CLKSEL, SD/OE	0.7 * VDDD		VDDD + 0.3	V
VIL	Input LOW Voltage	Single-ended inputs - CLKSEL, SD/OE	GND - 0.3		0.3 * VDDD	V
VIH	Input HIGH Voltage	Single-ended input OUT0_SEL_I2CB	0.65 * VDDO0		VDDD0 + 0.3	V
VIL	Input LOW Voltage	Single-ended input OUT0_SEL_I2CB	GND - 0.3		0.4	V
VIH	Input HIGH Voltage	Single-ended input - XIN/REF	0.8		1.2	V
VIL	Input LOW Voltage	Single-ended input - XIN/REF	GND - 0.3		0.4	V
TR/TF	Input Rise/Fall Time	CLKSEL, SD/OE, SEL1/SDA, SEL0/SCL			300	nS

Table 16: DC Electrical Characteristics for LVDS(V_{DDO} = 3.3V±5% or 2.5V±5%, TA = -40°C to +85°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{OT} (+)	Differential Output Voltage for the TRUE binary state	247		454	mV
V_{OT} (-)	Differential Output Voltage for the FALSE binary state	-247		-454	mV
$\triangle V_{OT}$	Change in V_{OT} between Complimentary Output States			50	mV
V_{OS}	Output Common Mode Voltage (Offset Voltage)	1.125	1.25	1.375	V
$\triangle V_{OS}$	Change in V_{OS} between Complimentary Output States			50	mV
I_{OS}	Outputs Short Circuit Current, V_{OUT}+ or V_{OUT} - = 0V or V_{DDO}		9	24	mA
I_{OSD}	Differential Outputs Short Circuit Current, V_{OUT}+ = V_{OUT} -		6	12	mA

Table 17: DC Electrical Characteristics for LVDS (V_{DDO} = 1.8V±5%, TA = -40°C to +85°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{OT} (+)	Differential Output Voltage for the TRUE binary state	247		454	mV
V_{OT} (-)	Differential Output Voltage for the FALSE binary state	-247		-454	mV
$\triangle V_{OT}$	Change in V_{OT} between Complimentary Output States			50	mV
V_{OS}	Output Common Mode Voltage (Offset Voltage)	0.8	0.875	0.95	V
$\triangle V_{OS}$	Change in V_{OS} between Complimentary Output States			50	mV
I_{OS}	Outputs Short Circuit Current, V_{OUT}+ or V_{OUT} - = 0V or V_{DDO}		9	24	mA
I_{OSD}	Differential Outputs Short Circuit Current, V_{OUT}+ = V_{OUT} -		6	12	mA

Table 18: DC Electrical Characteristics for LVPECL (V_{DDO} = 3.3V±5% or 2.5V±5%, TA = -40°C to +85°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{OH}	Output Voltage HIGH, terminated through 50Ω tied to V_{DD} - 2 V	V_{DDO} - 1.19		V_{DDO} - 0.69	V
V_{OL}	Output Voltage LOW, terminated through 50Ω tied to V_{DD} - 2 V	V_{DDO} - 1.94		V_{DDO} - 1.4	V
V_{SWING}	Peak-to-Peak Output Voltage Swing	0.55		0.993	V

Table 19: Electrical Characteristics – DIF 0.7V Low Power HCSL Differential Outputs
(V_{DDO} = 3.3V±5%, 2.5V±5%, TA = -40°C to +85°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Notes
dV/dt	Slew Rate	Scope averaging on	1		4	V/ns	1,2,3
V_{HIGH}	Voltage High	Statistical measurement on single-ended signal using oscilloscope math function (Scope averaging ON)	660		850	mV	1,6,7
V_{LOW}	Voltage Low		-150		150	mV	1,6
V_{MAX}	Maximum Voltage	Measurement on single-ended signal using absolute value (Scope averaging off)			1150	mV	1
V_{MIN}	Minimum Voltage		-300			mV	1
V_{SWING}	Voltage Swing	Scope averaging off	300			mV	1,2,6
V_{CROSS}	Crossing Voltage Value	Scope averaging off	250		550	mV	1,4,6
ΔV_{CROSS}	Crossing Voltage Variation	Scope averaging off			140	mV	1,5

1. Guaranteed by design and characterization. Not 100% tested in production
2. Measured from differential waveform.
3. Slew rate is measured through the V_{SWING} voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.
4. V_{CROSS} is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).
5. The total variation of all V_{CROSS} measurements in any particular system. Note that this is a subset of V_{CROSS} min/max (V_{CROSS} absolute) allowed. The intent is to limit V_{CROSS} induced modulation by setting ΔV_{CROSS} to be smaller than V_{CROSS} absolute.
6. Measured from single-ended waveform.
7. Measured with scope averaging off, using statistics function. Variation is difference between min. and max.

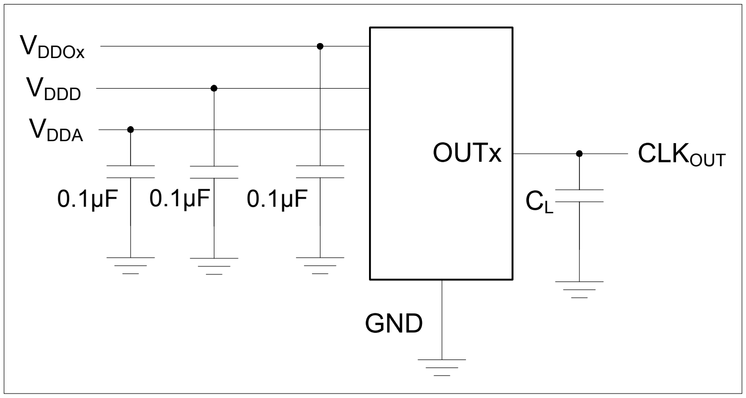
Table 20: AC Timing Electrical Characteristics

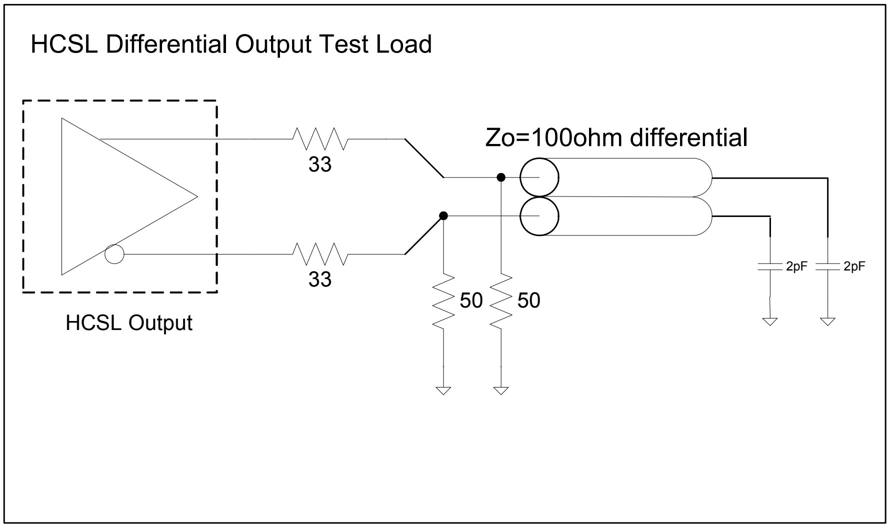
(V_{DDO} = 3.3V+5% or 2.5V+5% or 1.8V ±5%, TA = -40°C to +85°C)

(Spread Spectrum Generation = OFF)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
fIN	Input Frequency	Input frequency limit (XIN)	8		40	MHz
		Input frequency limit (REF)	1		200	MHz
		Input frequency limit (CLKIN, CLKINB)	1		350	MHz
fOUT	Output Frequency	Single ended clock output limit (LVCMOS)	1		200	MHz
		Differential cock output limit (LVPECL/ LVDS/HCSL)	1		350	
t2	Input Duty Cycle	Duty Cycle	45	50	55	%
t3	Output Duty Cycle Distortion	LVPECL Output Duty Cycle Distortion	-5		5	%
		LVPECL Output Duty Cycle Distortion	-5		5	%
		HCSL Output Duty Cycle Distortion	-5		5	%
		LVCMOS Output Duty Cycle Distortion @ 2.5V and 3.3V	-5		5	%
		LVCMOS Output Duty Cycle Distortion @ 1.8 V, f <100MHz	-5		5	%
		LVCMOS Output Duty Cycle Distortion @ 1.8 V, f >=100MHz	-10		10	%
t4	Slew Rate, SLEW[1:0] = 11	Single-ended 3.3V LVCMOS output clock rise and fall time, @ 125MHz 25% to 75% of VDDO (Output Load = 5 pF)	1.7	2.7	4.1	V/ns
	Slew Rate, SLEW[1:0] = 10	Single-ended 3.3V LVCMOS output clock rise and fall time, @ 125MHz 25% to 75% of VDDO (Output Load = 5 pF)	1.4	2.4	3.8	V/ns
	Slew Rate, SLEW[1:0] = 01	Single-ended 3.3V LVCMOS output clock rise and fall time, @ 125MHz 25% to 75% of VDDO (Output Load = 5 pF)	1.3	2.3	3.7	V/ns
	Slew Rate, SLEW[1:0] = 00	Single-ended 3.3V LVCMOS output clock rise and fall time, @ 125MHz 25% to 75% of VDDO (Output Load = 5 pF)	1.1	2.1	3.6	V/ns
	Slew Rate, SLEW[1:0] = 11	Single-ended 2.5V LVCMOS output clock rise and fall time, @ 125MHz 25% to 75% of VDDO (Output Load = 5 pF)	0.9	1.7	2.6	V/ns
	Slew Rate, SLEW[1:0] = 10	Single-ended 2.5V LVCMOS output clock rise and fall time, @ 125MHz 25% to 75% of VDDO (Output Load = 5 pF)	0.6	1.4	2.3	V/ns
	Slew Rate, SLEW[1:0] = 01	Single-ended 2.5V LVCMOS output clock rise and fall time, @ 125MHz 25% to 75% of VDDO (Output Load = 5 pF)	0.6	1.3	2.2	V/ns
	Slew Rate, SLEW[1:0] = 00	Single-ended 2.5V LVCMOS output clock rise and fall time, @ 125MHz 25% to 75% of VDDO (Output Load = 5 pF)	0.6	1.2	2.1	V/ns
	Slew Rate, SLEW[1:0] = 11	Single-ended 1.8V LVCMOS output clock rise and fall time, @ 125MHz 25% to 75% of VDDO (Output Load = 5 pF)	0.7	1.2	2.1	V/ns
	Slew Rate, SLEW[1:0] = 10	Single-ended 1.8V LVCMOS output clock rise and fall time, @ 125MHz 25% to 75% of VDDO (Output Load = 5 pF)	0.4	0.9	1.7	V/ns
	Slew Rate, SLEW[1:0] = 01	Single-ended 1.8V LVCMOS output clock rise and fall time, @ 125MHz 25% to 75% of VDDO (Output Load = 5 pF)	0.4	0.8	1.6	V/ns
	Slew Rate, SLEW[1:0] = 00	Single-ended 1.8V LVCMOS output clock rise and fall time, @ 125MHz 25% to 75% of VDDO (Output Load = 5 pF)	0.3	0.7	1.4	V/ns
t5	Rise Times	LVDS, 20% to 80%, single-ended		300		ps
	Fall Times	LVDS, 80% to 20%, single-ended		300		
	Rise Times	LVPECL, 20% to 80%, single-ended		400		
	Fall Times	LVPECL, 80% to 20%, single-ended		400		
t6	Buffer Additive Phase Jitter, RMS	fREF=125MHz, LVCMOS, Vpp=1V, Integration range: 12kHz–20MHz		0.2		ps
t7	Output Skew	Skew between the same frequencies, with outputs using the same driver format and phase delay set to 0 ns.		35		ps
	Input to Output Skew	Skew from input to output		3		ns

Test Circuits and Loads





Test Circuits and Loads for Outputs

5P1103 Application Schematic

The following figure shows an example of 5P1103 application schematic. Input and output terminations shown are intended as examples only and may not represent the exact user configuration. In this example, the device is operated at $V_{DDD,}$ V_{DDA} = 3.3V. The decoupling capacitors should be located as close as possible to the power pin. A 12pF parallel resonant 8MHz to 40MHz crystal is used in this example. Different crystal frequencies may be used. The C1 = C2 = 5pF are recommended for frequency accuracy. If different crystal types are used, please consult IDT for recommendations. For different board layout, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy.

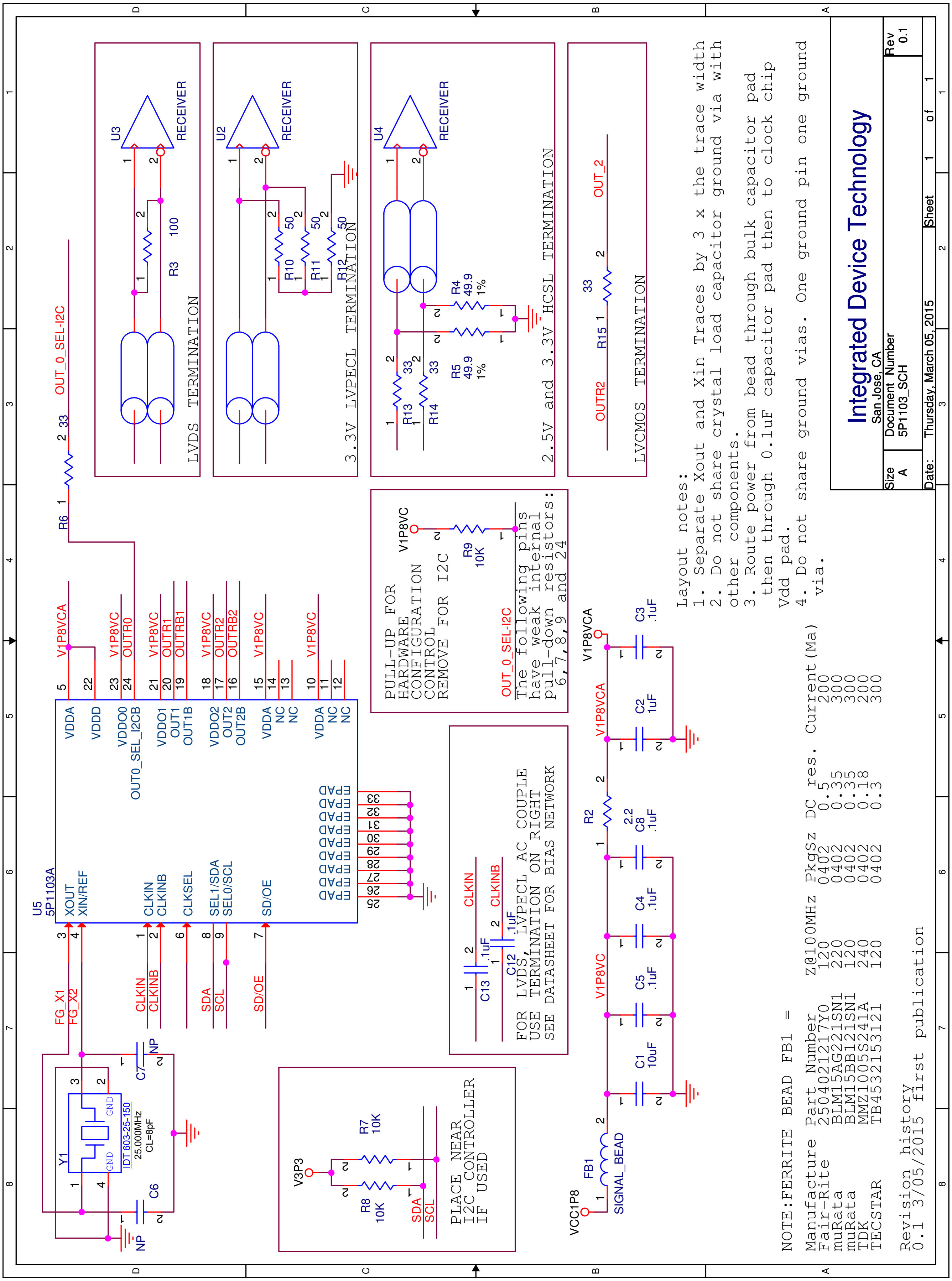
As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. 5P1103 provides separate power supplies to isolate any high switching noise from coupling into the part.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uf capacitor in each power pin filter should be placed on the device side. The other components can be on the opposite side of the PCB.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10 kHz. If a specific frequency noise component is known, such as switching power supply frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set.

5P1103 Reference Schematic



PULL-UP FOR HARDWARE CONFIGURATION CONTROL REMOVE FOR I2C

The following pins have weak internal pull-down resistors: 6,7,8,9 and 24

FOR LVDS, LVPECL AC COUPLE USE TERMINATION ON RIGHT SEE DATASHEET FOR BIAS NETWORK

PLACE NEAR I2C CONTROLLER IF USED

Layout notes:
1. Separate Xout and Xin Traces by 3 x the trace width
2. Do not share crystal load capacitor ground via with other components.
3. Route power from bead through bulk capacitor pad then through 0.1uF capacitor pad then to clock chip Vdd pad.
4. Do not share ground vias. One ground pin one ground via.

NOTE:FERRITE BEAD FB1 =

Manufacture	Part Number	Z@100MHz	PkgSz	DC res.	Current(Ma)
Fair-Rite	2504021217Y0	120	0402	0.5	200
muRata	BLM15AG221SN1	220	0402	0.35	300
muRata	BLM15BB121SN1	120	0402	0.35	300
TDK	MMZ1005S241A	240	0402	0.18	200
TECSTAR	TB4532153121	120	0402	0.3	300

Revision history
0.1 3/05/2015 first publication

Integrated Device Technology
San Jose, CA

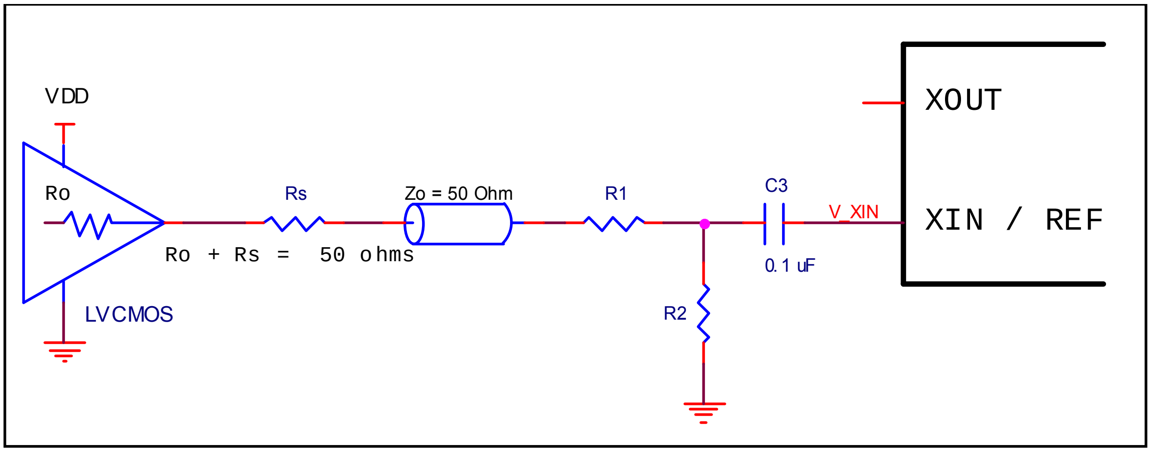
Size A	Document Number 5P1103_SCH	Rev 0.1
Date: Thursday, March 05, 2015	Sheet 1 of 1	

Overdriving the XIN/REF Interface

LVCMOS Driver

The XIN/REF input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XOUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.2V and the slew rate should not be less than 0.2V/ns. Figure General Diagram for LVCMOS Driver to XTAL Input Interface shows an example of the interface diagram for a LVCMOS driver.

This configuration has three properties; the total output impedance of Ro and Rs matches the 50 ohm transmission line impedance, the Vrx voltage is generated at the CLKIN inputs which maintains the LVCMOS driver voltage level across the transmission line for best S/N and the R1-R2 voltage divider values ensure that the clock level at XIN is less than the maximum value of 1.2V.



General Diagram for LVCMOS Driver to XTAL Input Interface

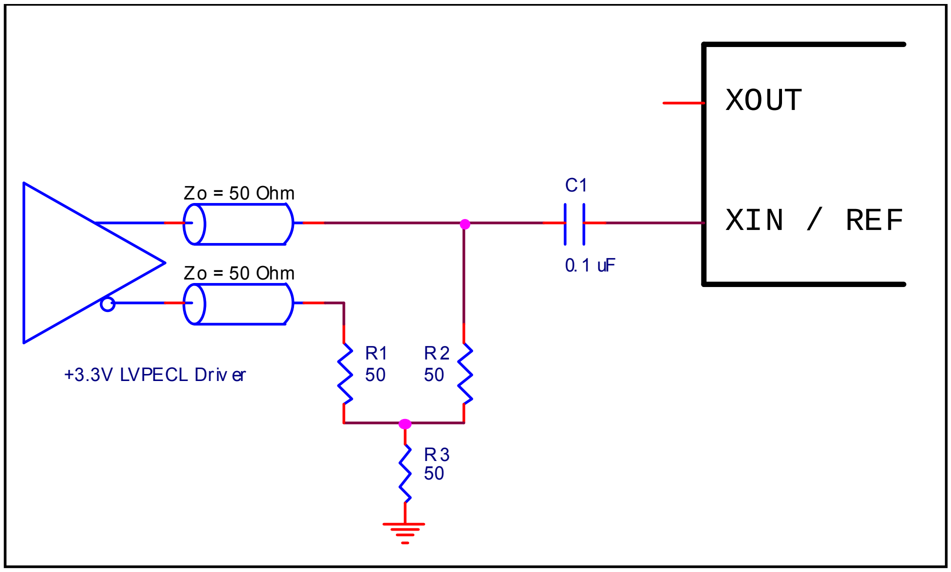
Table 21 *Nominal Voltage Divider Values vs LVCMOS VDD for XIN* shows resistor values that ensure the maximum drive level for the XIN/REF port is not exceeded for all combinations of 5% tolerance on the driver VDD, the VDDA and 5% resistor tolerances. The values of the resistors can be adjusted to reduce the loading for slower and weaker LVCMOS driver by increasing the voltage divider attenuation as long as the minimum drive level is maintained over all tolerances. To assist this assessment, the total load on the driver is included in the table.

Table 21:Nominal Voltage Divider Values vs LVCMOS VDD for XIN

LVCMOS Driver VDD	Ro+Rs	R1	R2	V_XIN (peak)	Ro+Rs+R1+R2
3.3	50.0	130	75	0.97	255
2.5	50.0	100	100	1.00	250
1.8	50.0	62	130	0.97	242

LVPECL Driver

Figure General Diagram for LVPECL Driver to XTAL Input Interface shows an example of the interface diagram for a +3.3V LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XIN/REF input. It is recommended that all components in the schematics be placed in the layout; though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input. If the driver is 2.5V LVPECL, the only change necessary is to use the appropriate value of R3.

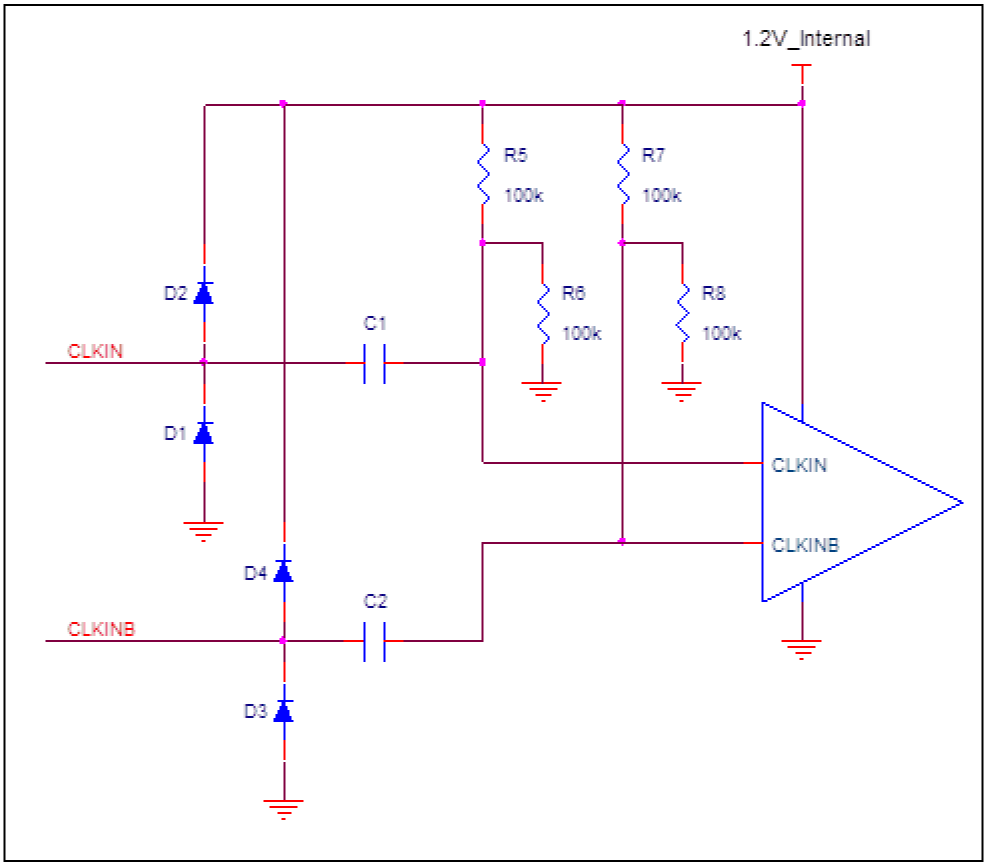


General Diagram for +3.3V LVPECL Driver to XTAL Input Interface

CLKIN Equivalent Schematic

Figure *CLKIN Equivalent Schematic* below shows the basis of the requirements on VIH max, VIL min and the 1200 mV p-p single ended Vswing maximum.

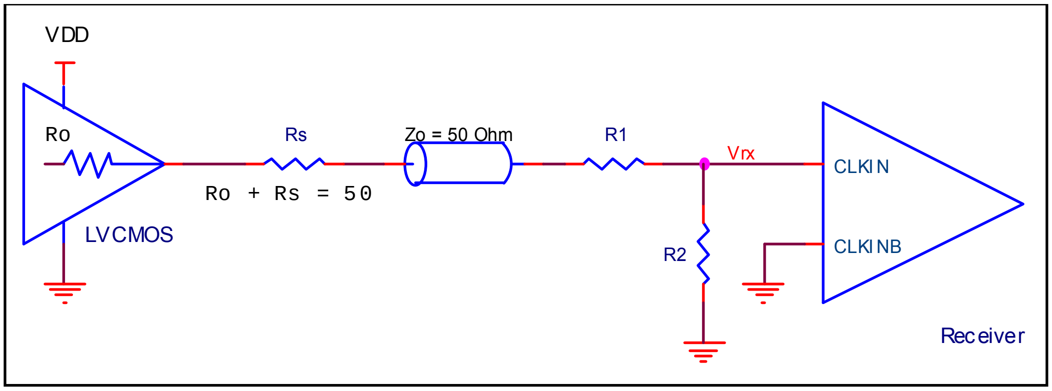
- The CLKIN and CLKINB Vih max spec comes from the cathode voltage on the input ESD diodes D2 and D4, which are referenced to the internal 1.2V supply. CLKIN or CLKINB voltages greater than 1.2V + 0.5V =1.7V will be clamped by these diodes. CLKIN and CLKINB input voltages less than -0.3V will be clamped by diodes D1 and D3.
- The 1.2V p-p maximum Vswing input requirement is determined by the internally regulated 1.2V supply for the actual clock receiver. This is the basis of the Vswing spec in Table 13.



CLKIN Equivalent Schematic

Wiring the Differential Input to Accept Single-Ended Levels

Figure *Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels* shows how a differential input can be wired to accept single ended levels. This configuration has three properties; the total output impedance of Ro and Rs matches the 50 ohm transmission line impedance, the Vrx voltage is generated at the CLKIN inputs which maintains the LVCMOS driver voltage level across the transmission line for best S/N and the R1-R2 voltage divider values ensure that Vrx p-p at CLKIN is less than the maximum value of 1.2V.



Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

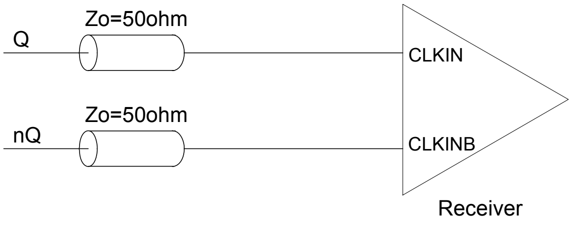
Table 22 *Nominal Voltage Divider Values vs Driver VDD* shows resistor values that ensure the maximum drive level for the CLKIN port is not exceeded for all combinations of 5% tolerance on the driver VDD, the Vddo_0 and 5% resistor tolerances. The values of the resistors can be adjusted to reduce the loading for slower and weaker LVCMOS driver by increasing the impedance of the R1-R2 divider. To assist this assessment, the total load on the driver is included in the table.

Table 22:Nominal Voltage Divider Values vs Driver VDD

LVCMOS Driver VDD	Ro+Rs	R1	R2	Vrx (peak)	Ro+Rs+R1+R2
3.3	50.0	130	75	0.97	255
2.5	50.0	100	100	1.00	250
1.8	50.0	62	130	0.97	242

HCSL Differential Clock Input Interface

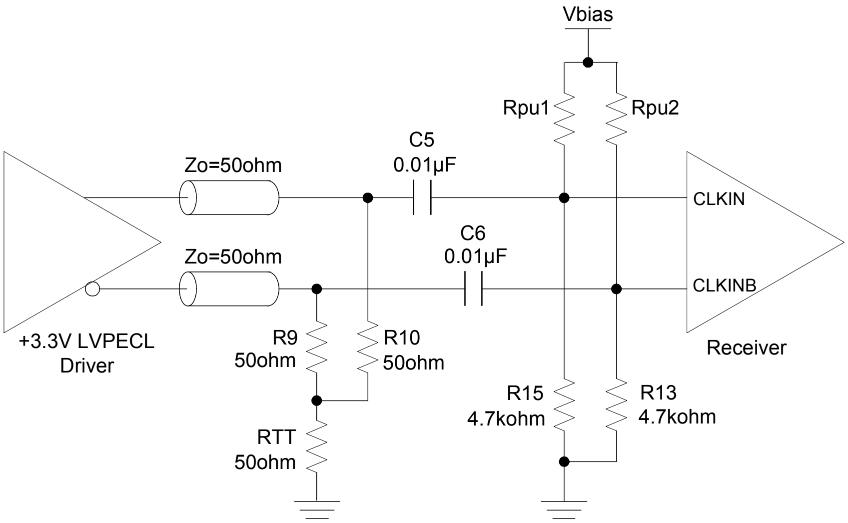
CLKIN/CLKINB will accept DC coupled HCSL signals.



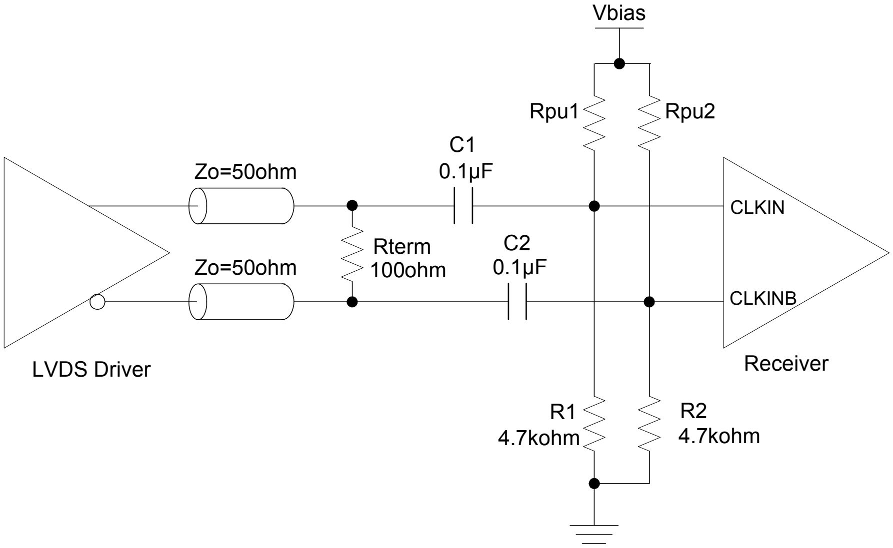
CLKIN, CLKINB Input Driven by an HCSL Driver

3.3V Differential LVPECL Clock Input Interface

The logic levels of 3.3V LVPECL and LVDS can exceed VIH max for the CLKIN/B pins. Therefore the LVPECL levels must be AC coupled to the differential input and the DC bias restored with external voltage dividers. A single table of bias resistor values is provided below for both for 3.3V LVPECL and LVDS. Vbias can be VDDD, V_{DDOX} or any other available voltage at the receiver that is most conveniently accessible in layout.



CLKIN, CLKINB Input Driven by a 3.3V LVPECL Driver



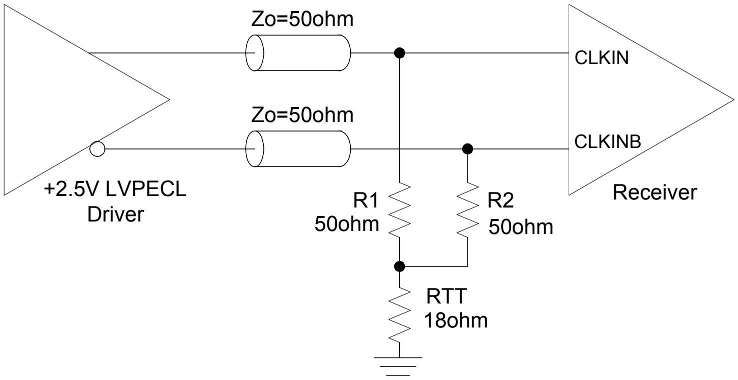
CLKIN, CLKINB Input Driven by an LVDS Driver

Table 23:Bias Resistors for 3.3V LVPECL and LVDS Drive to CLKIN/B

Vbias (V)	Rpu1/2 (kohm)	CLKIN/B Bias Voltage (V)
3.3	22	0.58
2.5	15	0.60
1.8	10	0.58

2.5V Differential LVPECL Clock Input Interface

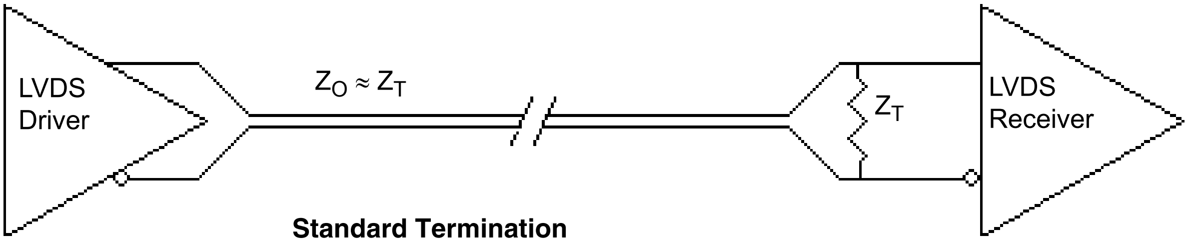
The maximum DC 2.5V LVPECL voltage meets the VIH max CLKIN requirement. Therefore 2.5V LVPECL can be connected directly to the CLKIN terminals without AC coupling



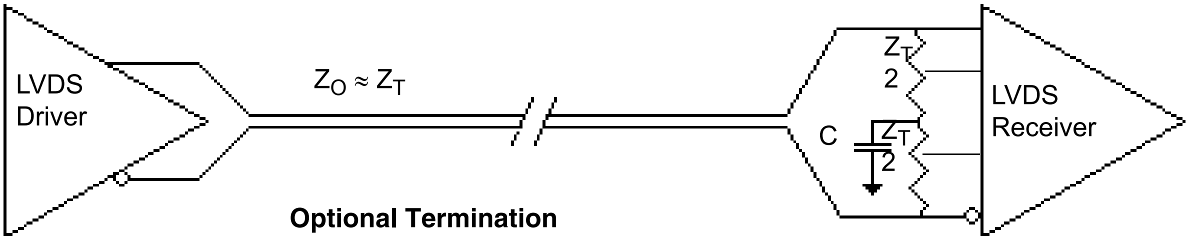
CLKIN, CLKINB Input Driven by a 2.5V LVPECL Driver

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω. and 132Ω. The actual value should be selected to match the differential impedance (Zo) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω. differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. The standard termination schematic as shown in figure *Standard Termination* or the termination of figure *Optional Termination* can be used, which uses a center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the IDT LVDS output. If using a non-standard termination, it is recommended to contact IDT and confirm that the termination will function as intended. For example, the LVDS outputs cannot be AC coupled by placing capacitors between the LVDS outputs and the 100 ohm shunt load. If AC coupling is required, the coupling caps must be placed between the 100 ohm shunt termination and the receiver. In this manner the termination of the LVDS output remains DC coupled



Standard Termination

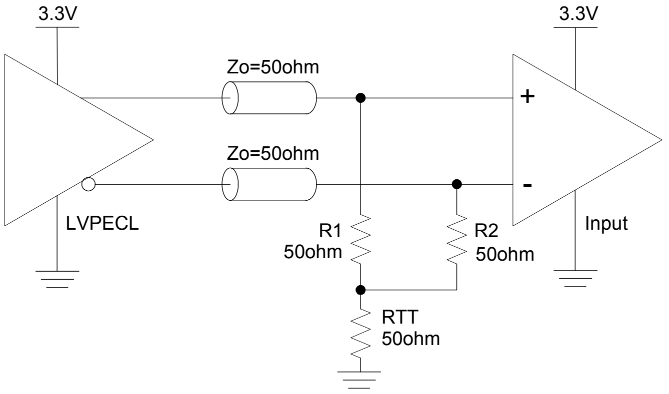


Optional Termination

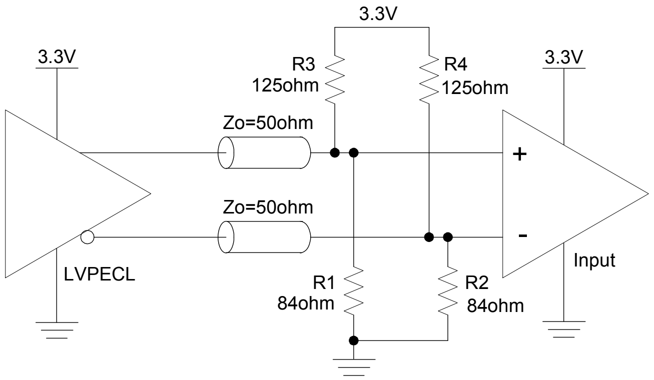
Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. The figure below show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.



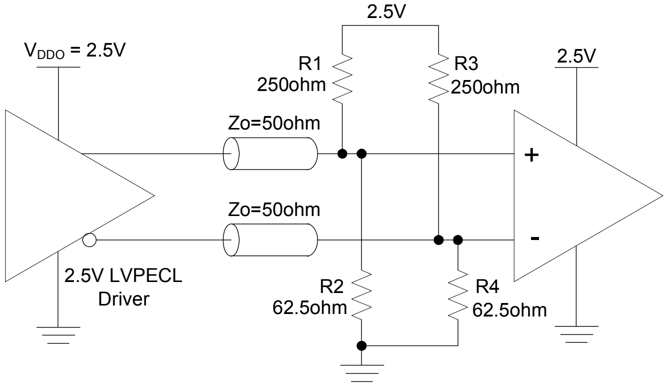
3.3V LVPECL Output Termination (1)



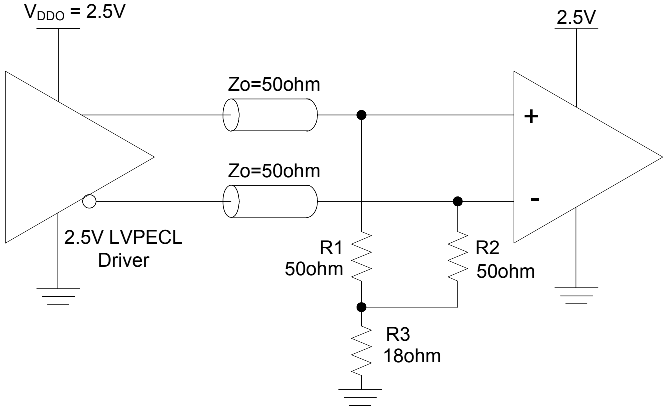
3.3V LVPECL Output Termination (2)

Termination for 2.5V LVPECL Outputs

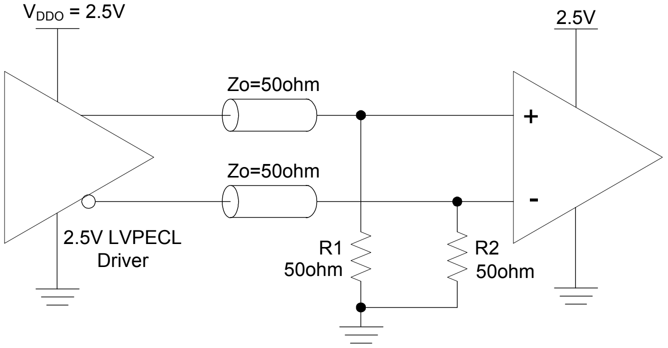
Figures *2.5V LVPECL Driver Termination Example (1) and (2)* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{DDO} – 2V. For V_{DDO} = 2.5V, the V_{DDO} – 2V is very close to ground level. The R3 in Figure *2.5V LVPECL Driver Termination Example (3)* can be eliminated and the termination is shown in example (2).



2.5V LVPECL Driver Termination Example (1)



2.5V LVPECL Driver Termination Example (3)



2.5V LVPECL Driver Termination Example (2)

PCI Express Application Note

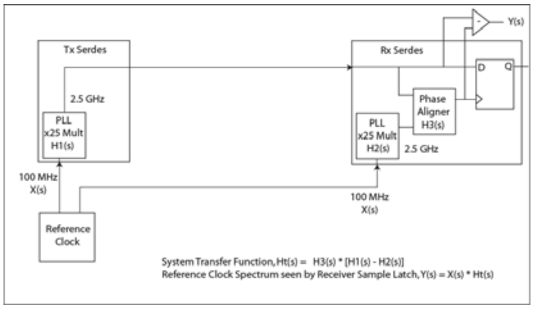
PCI Express jitter analysis methodology models the system response to reference clock jitter. The block diagram below shows the most frequently used Common Clock Architecture in which a copy of the reference clock is provided to both ends of the PCI Express Link. In the jitter analysis, the transmit (Tx) and receive (Rx) serdes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is:

$$\mathrm{Ht}(s) = \mathrm{H3}(s) \times [\mathrm{H1}(s) - \mathrm{H2}(s)]$$

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum X(s) and is:

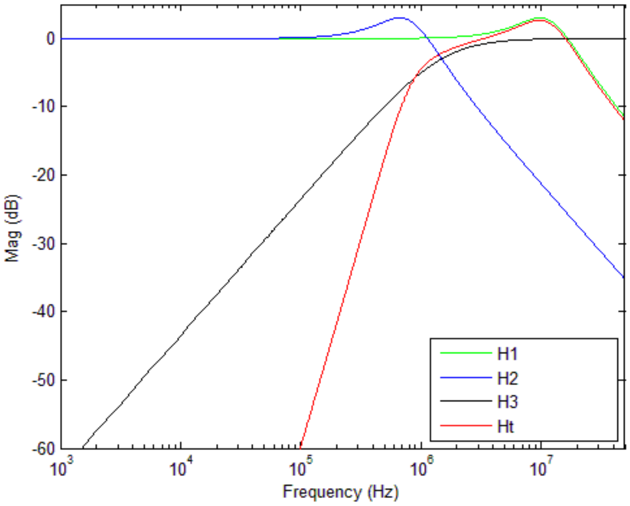
$$\mathrm{Y}(s) = \mathrm{X}(s) \times \mathrm{H3}(s) \times [\mathrm{H1}(s) - \mathrm{H2}(s)]$$

In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on X(s)*H3(s) * [H1(s) - H2(s)].



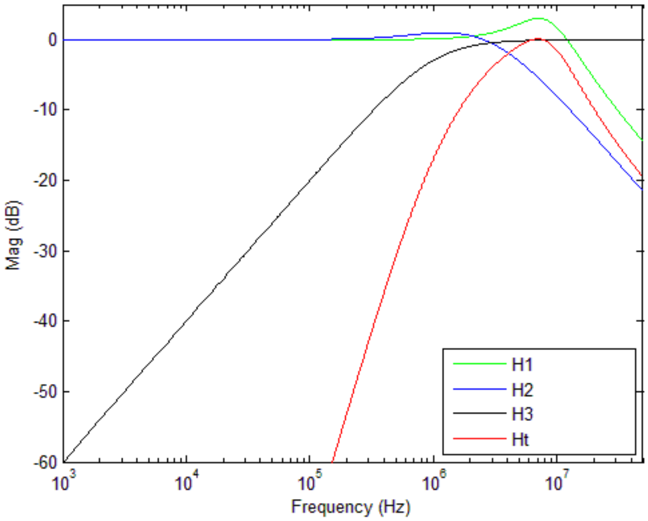
PCI Express Common Clock Architecture

For PCI Express Gen 1, one transfer function is defined and the evaluation is performed over the entire spectrum: DC to Nyquist (e.g for a 100MHz reference clock: 0Hz – 50MHz) and the jitter result is reported in peak-peak.

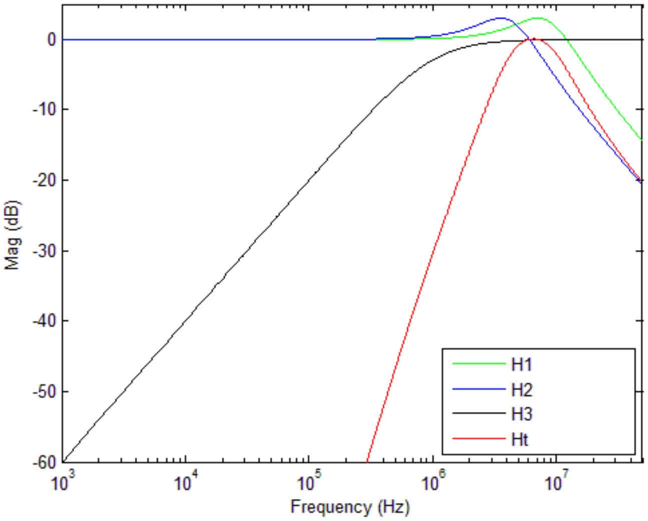


PCIe Gen1 Magnitude of Transfer Function

For PCI Express Gen2, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in RMS. The two evaluation ranges for PCI Express Gen 2 are 10kHz – 1.5MHz (Low Band) and 1.5MHz – Nyquist (High Band). The plots show the individual transfer functions as well as the overall transfer function Ht.

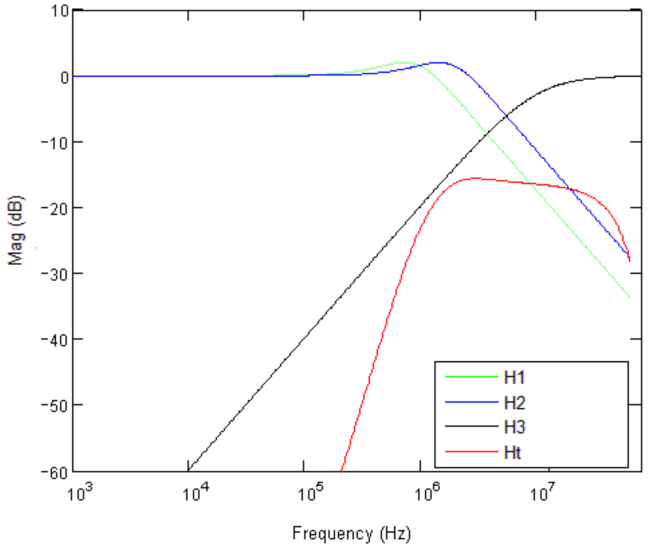


PCIe Gen2A Magnitude of Transfer Function



PCIe Gen2B Magnitude of Transfer Function

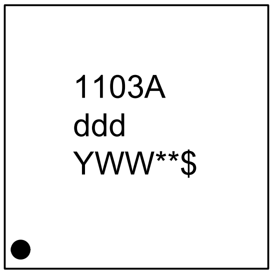
For PCI Express Gen 3, one transfer function is defined and the evaluation is performed over the entire spectrum. The transfer function parameters are different from Gen 1 and the jitter result is reported in RMS.



PCIe Gen3 Magnitude of Transfer Function

For a more thorough overview of PCI Express jitter analysis methodology, please refer to IDT Application Note PCI Express Reference Clock Requirements.

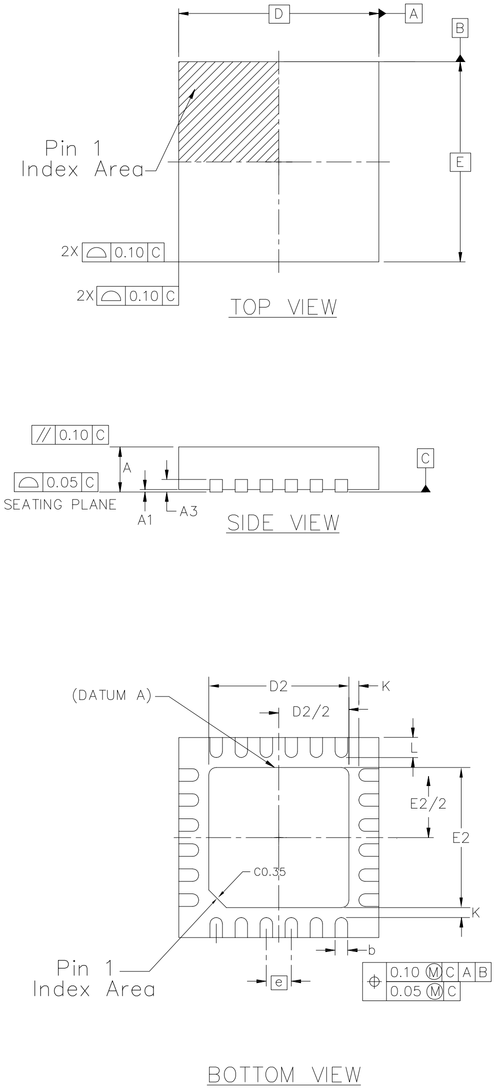
Marking Diagram



1. Line 1 is the truncated part number.
2. “ddd” denotes dash code.
3. “YWW” is the last digit of the year and week that the part was assembled.
4. “**” denotes sequential lot number.
5. “$” denotes mark code.

NLG24P2 Package Outline and Dimensions (4 x 4 mm 24-VFQFPN)

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	11/17/15	J.H
01	ADD CHAMFER	10/12/16	J.H



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.20 REF	
K		0.20	
D		4.00 BSC	
E		4.00 BSC	
D2	2.70	2.80	2.90
E2	2.70	2.80	2.90
e		0.50 BSC	
L	0.30	0.40	0.50
b	0.18	0.25	0.30

NOTES :

1. DIMENSIONING AND TOLERANCING CONFORME TO ASME Y14.5M — 1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.

TOLERANCES
UNLESS SPECIFIED
DECIMAL ANGULAR
XX± ±
XXX±
XXXX±

IDT®
www.IDT.com
6024 Silver Creek Valley Road
San Jose, CA 95138
PHONE: (408) 284-8200
FAX: (408) 284-8591

APPROVALS	DATE
DRAWN RAC	11/17/15
CHECKED	

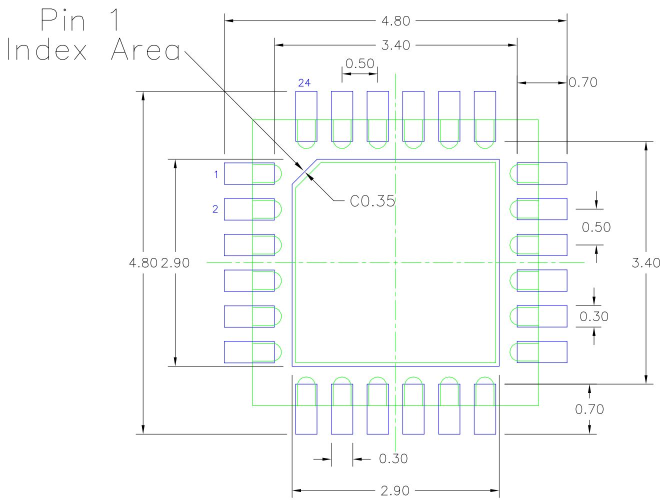
TITLE NL/NLG24 PACKAGE OUTLINE
4.0 x 4.0 mm BODY
0.5 mm PITCH QFN

SIZE	DRAWING No.	REV
C	PSC-4192-02	01

DO NOT SCALE DRAWING
SHEET 1 OF 2

NLG24P2 Package Outline and Dimensions, cont. (4 x 4 mm 24-VFQFPN)

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	11/17/15	J.H
01	ADD CHAMFER	10/12/16	J.H



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW, AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOWS FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES
UNLESS SPECIFIED
DECIMAL ANGULAR
XX± ±
XXX±
XXXX±

www.IDT.com

6024 Silver Creek Valley Road
San Jose, CA 95138
PHONE: (408) 284-8200
FAX: (408) 284-8591

APPROVALS	DATE
DRAWN RAC	11/17/15
CHECKED	

TITLE NL/NLG24 PACKAGE OUTLINE
4.0 x 4.0 mm BODY
0.5 mm PITCH QFN

SIZE	DRAWING No.	REV
C	PSC-4192-02	01

DO NOT SCALE DRAWING
SHEET 2 OF 2

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
5P1103AdddNLGI	see page 29	Trays	24-pin VFQFPN	-40° to +85°C
5P1103AdddNLGI8		Tape and Reel	24-pin VFQFPN	-40° to +85°C

Note: “ddd” denotes specific order codes.
“G” after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

Revision History

Rev.	Date	Originator	Description of Change
A	04/15/15	B. Chandhoke	Initial release.
B	04/30/15	B. Chandhoke	Replaced “clock buffer” with “fanout buffer” Removed “A” version letter from part number title header
C	06/19/15	B. Chandhoke	Removed the “Output Divides” section.
D	07/13/15	B. Chandhoke	1. Added conditions text and min/max values for VIH/VIL. 2. Updated 1.8V, 2.5V, and 3.3V VIH/VIL conditions text and min/max values for "Single-ended inputs - CLKSEL, SD/OE" 3. Added IDT and Fox crystal references.

www.IDT.com

Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138 USA
www.IDT.com

Sales
1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.IDT.com/go/sales

Tech Support
www.IDT.com/go/support

DISCLAIMER Integrated Device Technology, Inc. (IDT) and its affiliated companies (herein referred to as “IDT”) reserve the right to modify the products and/or specifications described herein at any time, without notice, at IDT’s sole discretion. Performance specifications and operating parameters of the described products are determined in an independent state and are not guaranteed to perform the same way when installed in customer products. The information contained herein is provided without representation or warranty of any kind, whether express or implied, including, but not limited to, the suitability of IDT's products for any particular purpose, an implied warranty of merchantability, or non-infringement of the intellectual property rights of others. This document is presented only as a guide and does not convey any license under intellectual property rights of IDT or any third parties.

IDT's products are not intended for use in applications involving extreme environmental conditions or in life support systems or similar devices where the failure or malfunction of an IDT product can be reasonably expected to significantly affect the health or safety of users. Anyone using an IDT product in such a manner does so at their own risk, absent an express, written agreement by IDT.

Integrated Device Technology, IDT and the IDT logo are trademarks or registered trademarks of IDT and its subsidiaries in the United States and other countries. Other trademarks used herein are the property of IDT or their respective third party owners. For datasheet type definitions and a glossary of common terms, visit www.idt.com/go/glossary. Integrated Device Technology, Inc. All rights reserved.