ISL97671A

6-Channel SMBus/I²C or PWM Dimming LED Driver with Phase Shift Control

FN7709
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The ISL97671A is a 6-Channel 45V dual dimming capable LED driver that can be used with either SMBus/I²C or PWM signal for dimming control. The ISL97671A can drive six channels of LEDs from an input of 4.5V~26.5V to an output of up to 45V. It can also operate from an input as low as 3V to an output of up to 26.5V in bootstrap configuration (refer to Figure 38 on page 26).

The ISL97671A features optional channel phase shift control to minimize the input/output ripple characteristics, and load transients to improve efficiency and eliminate audible noise.

The device can also be configured for Direct PWM Dimming with a minimum dimming duty cycle of 0.007% at 200Hz.

The ISL97671A headroom control circuit monitors the highest LED forward voltage string for output regulation, to minimize the voltage headroom and power loss in a typical multi-string operation.

The ISL97671A is offered in a compact and thermally efficient 20 Ld QFN 4mmx3mm package.

Related Literature

- For a full list of related documents, visit our website
  - ISL97671A product page

Features

- 6 x 50mA channels
- 4.5V to 26.5V input with 45V maximum output
- 3V (see Figure 38 on page 26) to 21V input with 26.5V maximum output
- PWM dimming with phase shift control
- SMBus/I²C controlled PWM or DC dimming
- Direct PWM dimming
- PWM dimming linearity
  - PWM dimming with adjustable dimming frequency and duty cycle linear from 0.4% to 100% <30kHz
  - Direct PWM dimming duty cycle linear from 0.007% to 100% at 200Hz
- Current matching ±0.7%
- 600kHz/1.2MHz selectable switching frequency
- Dynamic headroom control
- Fault protection
  - String open/short-circuit, OVP, OTP, and optional output short-circuit fault protection
- 20 Ld 4mmx3mm QFN package

Applications

- Tablet PC to notebook displays LED backlighting
- LCD monitor LED backlighting
- Field sequential RGB LED backlighting

Typical Application Circuits

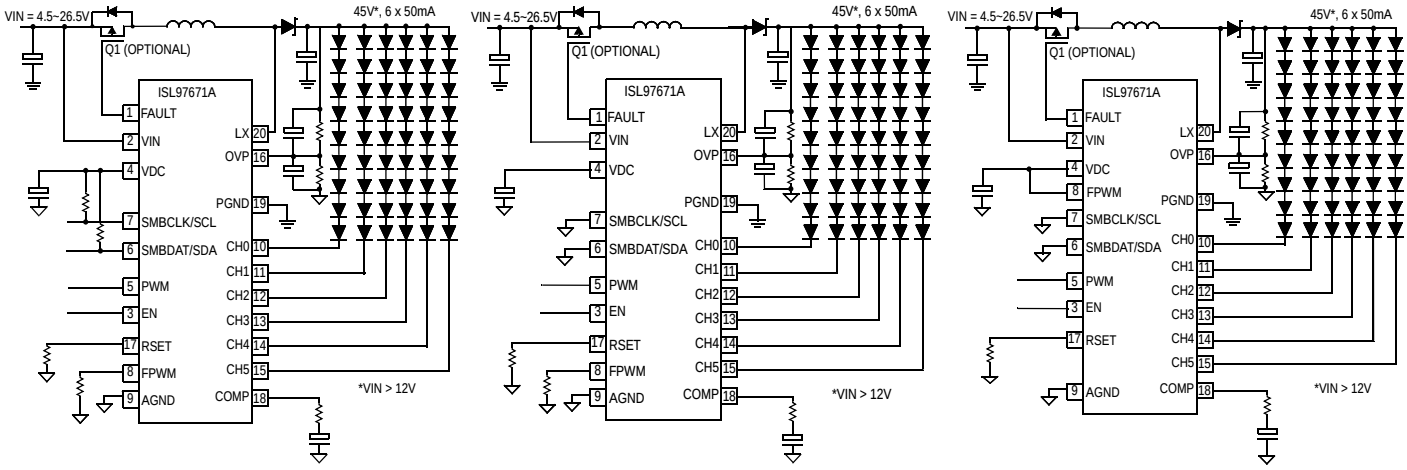

FIGURE 1A. SMBus/I²C CONTROLLED DIMMING AND ADJUSTABLE DIMMING FREQUENCY

FIGURE 1B. PWM DIMMING WITH PWM INPUT AND ADJUSTABLE DIMMING FREQUENCY

FIGURE 1C. DIRECT PWM DIMMING

FIGURE 1. ISL97671A TYPICAL APPLICATION DIAGRAMS

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Block Diagram

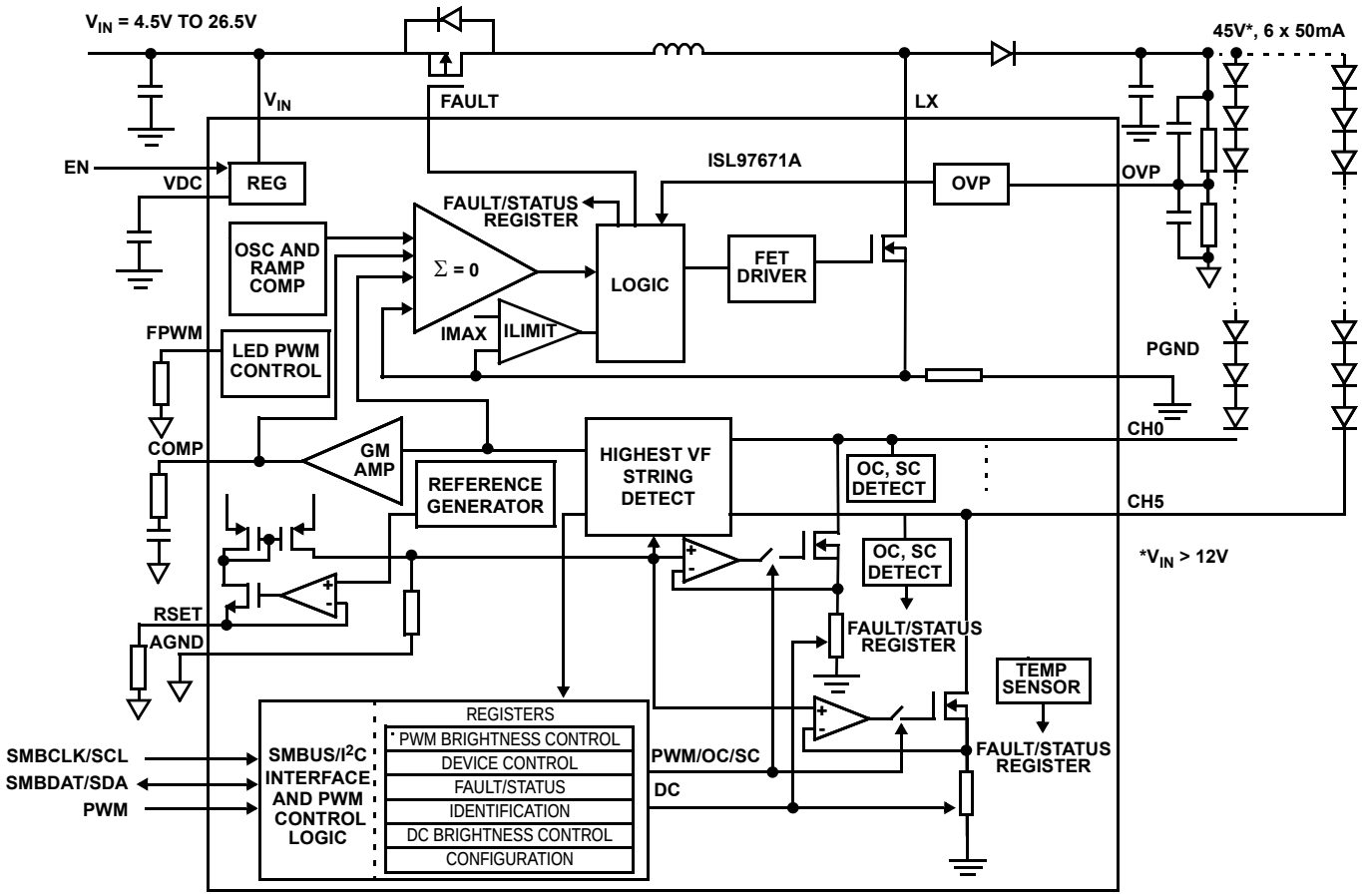


FIGURE 2. ISL97671A BLOCK DIAGRAM

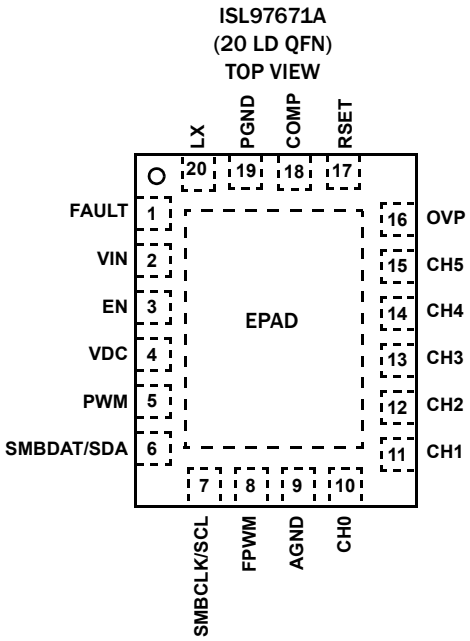
Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
ISL97671AIRZ	671A	20 Ld 3x4 QFN	L20.3x4
ISL97671AIRZ-EVALZ	Evaluation Board		

NOTES:

1. Add -T" suffix for 6k unit or "-TK" suffix for 1k unit tape and reel options. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), refer to the ISL97671A device information page. For more information about MSL, refer to TB363.

Pin Configuration



Pin Descriptions (I = Input, O = Output, S = Supply)

PIN NAME	PIN #	TYPE	DESCRIPTION
FAULT	1	O	Fault disconnect switch gate control.
VIN	2	S	Input voltage for the device and LED power.
EN	3	I	Enable input. The device needs 4ms for the initial power-up enable. It will be disabled if it is not biased for longer than 30.5ms.
VDC	4	S	Internal LDO output. Connect a decoupling capacitor to ground.
PWM	5	I	PWM brightness control pin or DPST control input.
SMBDAT/SDA	6	I/O	SMBus/I^2C serial data input and output. When Pins 6 and 7 are grounded or in logic 0's for longer than 60ms, the drivers will be controlled by the external PWM signal.
SMBCLK/SCL	7	I	SMBus/I^2C serial clock input. When Pins 6 and 7 are grounded or in logic 0's for longer than 60ms, the drivers will be controlled by external PWM signal.
FPWM	8	I	Sets the PWM dimming frequency by connecting a resistor between this pin and ground. When FPWM is tied to VDC and SMBCLK/SMBDAT is tied to ground, the device will be in Direct PWM Dimming where the output follows the input frequency and duty cycle without any digitization.
AGND	9	S	Analog ground for precision circuits.
CH0, CH1 CH2, CH3 CH4, CH5	10, 11, 12, 13, 14, 15	I	Current source and channel monitoring input for Channels 0-5.
OVP	16	I	Overvoltage protection input.
RSET	17	I	Resistor connection for setting LED current, (see Equation 1 to calculate the $I_{LED(peak)}$).
COMP	18	O	Boost compensation pin.
PGND	19	S	Power ground.
LX	20	O	Boost switch node.
EPAD			No electrical connection, but should be used to connect PGND and AGND. For example, use the top plane as PGND and the bottom plane as AGND with vias on EPAD to allow heat dissipation and minimum noise coupling from PGND to AGND operation.

Absolute Maximum Ratings (T_A = +25°C)

VIN, EN . . . . . -0.3V to 28V
FAULT . . . . . VIN - 8.5V to VIN + 0.3V
VDC, COMP, RSET . . . . . -0.3V to 5.5V
SMBCLK/SCL, SMBDAT/SDA, FPWM, PWM . . . . . -0.3V to 5.5V
OVP . . . . . -0.3V to 5.5V
CH0 - CH5, LX . . . . . -0.3V to 45V
PGND . . . . . -0.3V to +0.3V
Above voltage ratings are all with respect to AGND pin
ESD Rating
Human Body Model (Tested per JESD22-A114E) 3kV
Machine Model (Tested per JESD22-A115-A) 300V
Charged Device Model 1kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
20 Ld QFN Package (Notes 4, 5, 7)	40	2.5

Thermal Characterization (Typical)	PSI_{JT} (°C/W)
20 Ld QFN Package (Note 6)	1

Maximum Continuous Junction Temperature . . . . . +125°C
Storage Temperature . . . . . -65°C to +150°C

Operating Conditions

Temperature Range . . . . . -40°C to +85°C

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. Refer to TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
6. PSI_{JT} is the PSI junction-to-top thermal characterization parameter. If the package top temperature can be measured with this rating, then the die junction temperature can be estimated more accurately than the θ_{JC} and θ_{JC} thermal resistance ratings.
7. Refer to JESD51-7 high effective thermal conductivity board layout for proper via and plane designs.

Electrical Specifications

V_{IN} = 12V, EN = 5V, R_{SET} = 20.1kΩ, unless otherwise noted. **Boldface limits apply across the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	CONDITION	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
GENERAL						
Backlight Supply Voltage	V_{IN} (Note 9)	≤13 LEDs per channel (3.2V/20mA type)	**4.5**		**26.5**	V
V_{IN} Shutdown Current	I_{VIN_STBY}	T_A = +25°C			5	µA
V_{IN} Active Current	I_{VIN}	EN = 5V		5		mA
Output Voltage	V_{OUT}	4.5V < V_{IN} ≤ 26V, f_{SW} = 600kHz			**45**	V
		8.55V < V_{IN} ≤ 26V, f_{SW} = 1.2MHz			**45**	V
		4.5V < V_{IN} ≤ 8.55V, f_{SW} = 1.2MHz			**V_{IN}/0.19**	V
Undervoltage Lockout Threshold	V_{UVLO}		**2.1**		**2.6**	V
Undervoltage Lockout Hysteresis	V_{UVLO_HYS}			200		mV
REGULATOR						
LDO Output Voltage	V_{DC}	V_{IN} ≥ 6V	**4.55**	4.8	**5**	V
Standby Current	I_{VDC_STBY}	EN = 0V			**5**	µA
VDC LDO Droop Voltage	V_{LDO}	V_{IN} > 5.5V, 20mA		20	**200**	mV
Guaranteed Range for EN Input Low Voltage	EN_{LOW}				**0.5**	V
Guaranteed Range for EN Input High Voltage	EN_{HI}		**1.8**			V
EN Low Time Before Shut-down	t_{ENLow}			30.5		ms

Electrical Specifications V_{IN} = 12V, EN = 5V, R_{SET} = 20.1kΩ, unless otherwise noted. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	CONDITION	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
BOOST						
Boost FET Current Limit	SW_{ILimit}		**1.5**	2.0	2.7	A
Internal Boost Switch ON-resistance	$r_{DS(ON)}$	T_A = +25°C		235	300	mΩ
Soft-Start	SS	100% LED Duty Cycle		7		ms
Peak Efficiency	Eff_peak	V_{IN} = 12V, 72 LEDs, 20mA each, L = 10µH with DCR 101mΩ, T_A = +25°C		92.9		**%**
		V_{IN} = 12V, 60 LEDs, 20mA each, L = 10µH with DCR 101mΩ, T_A = +25°C		90.8		**%**
Line Regulation	$\Delta I_{OUT}/\Delta V_{IN}$			0.1		**%**
Boost Maximum Duty Cycle	D_{MAX}	f_{SW} = 1, 600kHz	**90**			**%**
		f_{SW} = 0, 1.2MHz	**81**			
Boost Minimum Duty Cycle	D_{MIN}	f_{SW} = 1, 600kHz			9.5	**%**
		f_{SW} = 0, 1.2MHz			**17**	
Lx Frequency High	f_{OSC_hi}	f_{SW} = 1, 600kHz	**475**	600	**640**	kHz
Lx Frequency Low	f_{OSC_lo}	f_{SW} = 0, 1.2MHz	**0.97**	1.14	**1.31**	MHz
LX Pin Leakage Current	$I_{LX\_leakage}$	LX = 45V, EN = 0V			**10**	µA
REFERENCE						
FAULT DETECTION						
Short Circuit Threshold Accuracy	V_{SC}		**7.5**	8.2		V
Temperature Shutdown Threshold	Temp_shtdwn			150		°C
Temperature Shutdown Hysteresis	Temp_Hyst			23		°C
Overvoltage Limit on OVP Pin	V_{OVPlo}		**1.199**		**1.24**	V
CURRENT SOURCES						
DC Channel-to-Channel Current Matching	I_{MATCH}	R_{SET} = 20.1kΩ, Reg0x00 = 0xFF, (I_{OUT} = 20mA)		±0.7	**±1.0**	**%**
Current Accuracy	I_{ACC}		**-1.5**		**+1.5**	**%**
Dominant Channel Current Sink Headroom Range at CHx Pin	$V_{HEADROOM}$	I_{LED} = 20mA T_A = +25°C		500 (Note 10)		mV
Dominant Channel Current Sink Headroom Range at CHx Pin	$V_{HEADROOM\_RANGE}$	I_{LED} = 20mA T_A = +25°C		90		mV
Voltage at RSET Pin	V_{RSET}	R_{SET} = 20.1kΩ	**1.2**	1.22	**1.24**	V
Maximum LED Current per Channel	$I_{LED(max)}$	V_{IN} = 12V, V_{OUT} = 45V, f_{SW} = 1.2MHz, T_A = +25°C		50		mA
PWM GENERATOR						
Guaranteed Range for PWM Input Low Voltage	V_{IL}				**0.8**	V
Guaranteed Range for PWM Input High Voltage	V_{IH}		**1.5**		**VDD**	V
PWM Input Frequency Range	F_{PWMI}		**200**		**30,000**	Hz
PWM Dimming Accuracy (Except Direct PWM Dimming)	PWMACC			8		bits
Direct PWM Minimum On Time	$t_{DIRECTPWM}$	Direct PWM Mode	**250**		**350**	ns
PWM Dimming Frequency Range	F_{PWM}		100		30,000	Hz

Electrical Specifications V_{IN} = 12V, EN = 5V, R_{SET} = 20.1kΩ, unless otherwise noted. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	CONDITION	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
FAULT PIN						
Fault Pull-down Current	I_{FAULT}	V_{IN} = 12V	**12**	21	**30**	µA
Fault Clamp Voltage with Respect to V_{IN}	V_{FAULT}	V_{IN} = 12, V_{IN} - V_{FAULT}	**6**	7	**8.3**	V
LX Start-up Threshold	LXstart_thres		**0.9**		**1.2**	V
LX Start-up Current	ILXStart-up		**1**	3.5	**5**	mA
SMBus/I²C INTERFACE						
Guaranteed Range for Data, Clock Input Low Voltage	V_{IL}				**0.8**	V
Guaranteed Range for Data, Clock Input High Voltage	V_{IH}		**1.5**		**VDD**	V
SMBus/I²C Data line Logic Low Voltage	V_{OL}	I_{PULLUP} = 4mA			**0.17**	V
Input Leakage On SMBData/SMBClk	I_{LEAK}	Measured at 4.8V	**-10**		**10**	µA
SMBus/I²C TIMING SPECIFICATIONS						
Minimum Time Between EN high and SMBus/I²C Enabled	t_{EN}-SMB/I²C	1µF capacitor on VDC	2			ms
Pulse Width Suppression on SMBCLK/SMBDAT	PWS		0.15		0.45	µs
SMBus/I²C Clock Frequency	f_{SMB}				400	kHz
Bus Free Time Between Stop and Start Condition	t_{BUF}		1.3			µs
Hold Time After (Repeated) START Condition. After this Period, the First Clock is Generated	$t_{HD:STA}$		0.6			µs
Repeated Start Condition Setup Time	$t_{SU:STA}$		0.6			µs
Stop Condition Setup Time	$t_{SU:STO}$		0.6			µs
Data Hold Time	$t_{HD:DAT}$		300			ns
Data Setup Time	$t_{SU:DAT}$		100			ns
Clock Low Period	t_{LOW}		1.3			µs
Clock High Period	t_{HIGH}		0.6			µs
Clock/data Fall Time	t_F				300	ns
Clock/data Rise Time	t_R				300	ns

NOTES:

8. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
9. At maximum V_{IN} of 26.5V, minimum V_{OUT} is limited 28V.
10. Varies within range specified by $V_{HEADROOM\_RANGE}$.

Typical Performance Curves

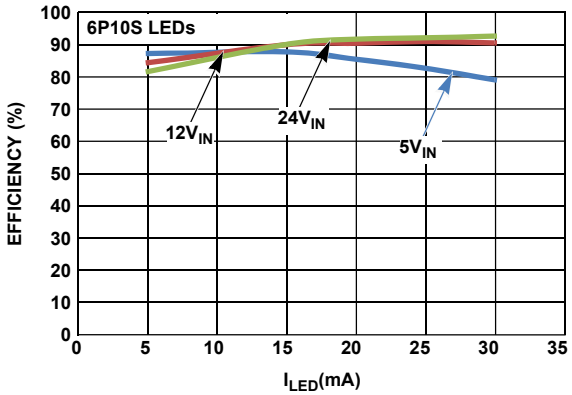


FIGURE 3. EFFICIENCY vs UP TO 30mA LED CURRENT (100% LED DUTY CYCLE) vs V_{IN}

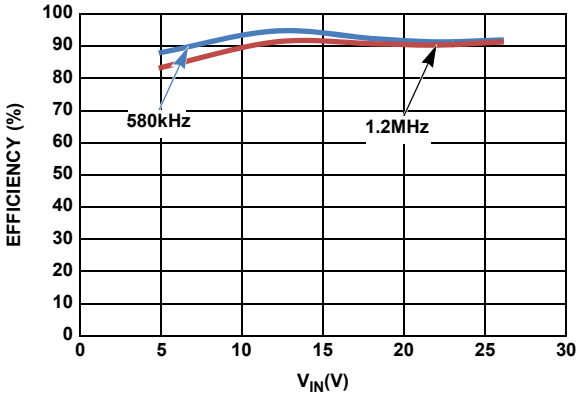


FIGURE 4. EFFICIENCY vs V_{IN} vs SWITCHING FREQUENCY AT 20mA (100% LED DUTY CYCLE)

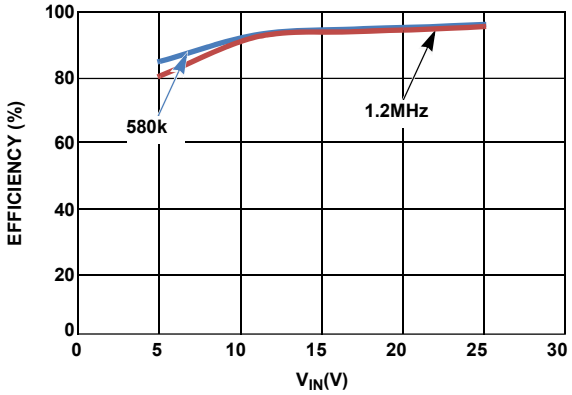


FIGURE 5. EFFICIENCY vs V_{IN} vs SWITCHING FREQUENCY AT 30mA (100% LED DUTY CYCLE)

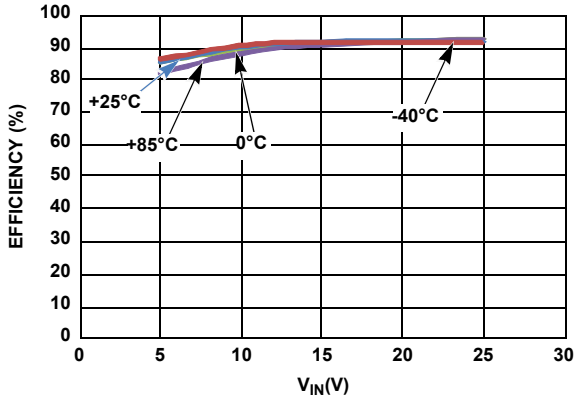


FIGURE 6. EFFICIENCY vs V_{IN} vs TEMPERATURE AT 20mA (100% LED DUTY CYCLE)

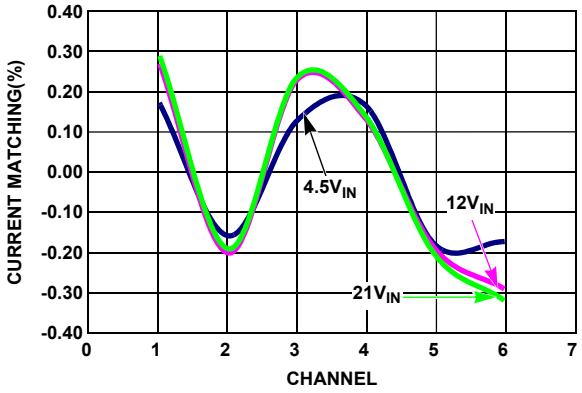


FIGURE 7. CHANNEL-TO-CHANNEL CURRENT MATCHING

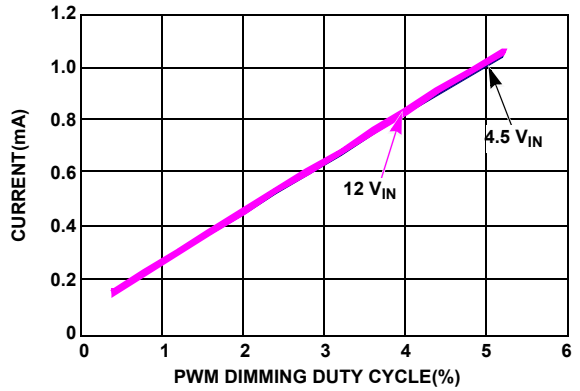


FIGURE 8. CURRENT LINEARITY vs LOW LEVEL PWM DIMMING DUTY CYCLE vs V_{IN}

Typical Performance Curves (Continued)

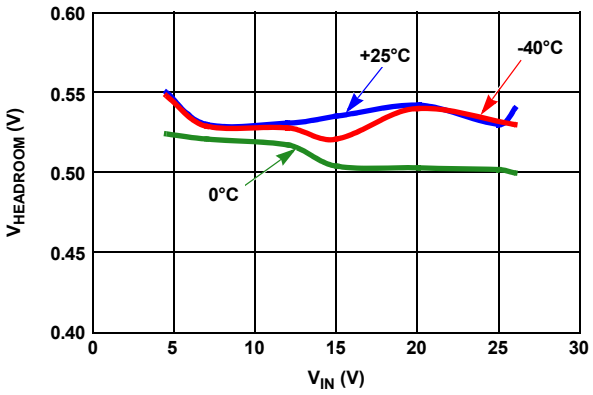


FIGURE 9. $V_{HEADROOM}$ vs V_{IN} vs TEMPERATURE AT 20mA

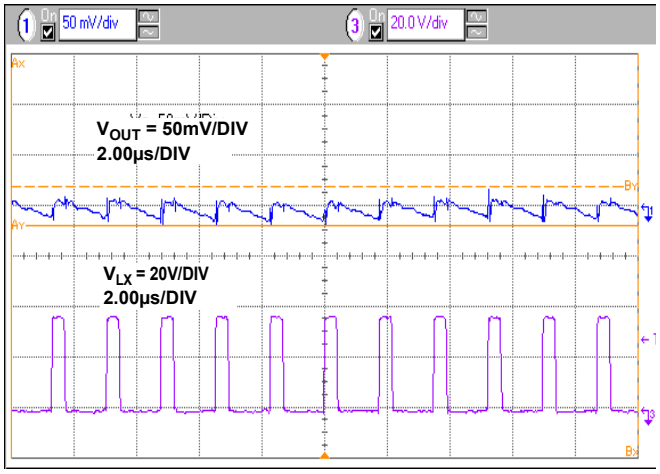


FIGURE 10. V_{OUT} RIPPLE VOLTAGE, V_{IN} = 12V, 6P12S AT 20mA/CHANNEL

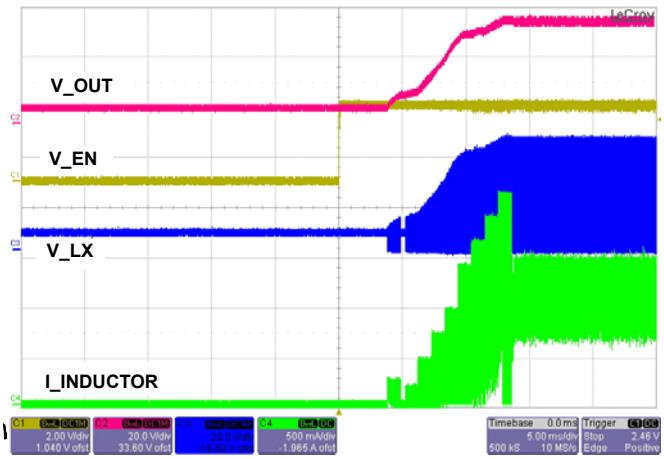


FIGURE 11. SOFT-START INDUCTOR CURRENT AT V_{IN} = 6V FOR 6P12S AT 20mA/CHANNEL

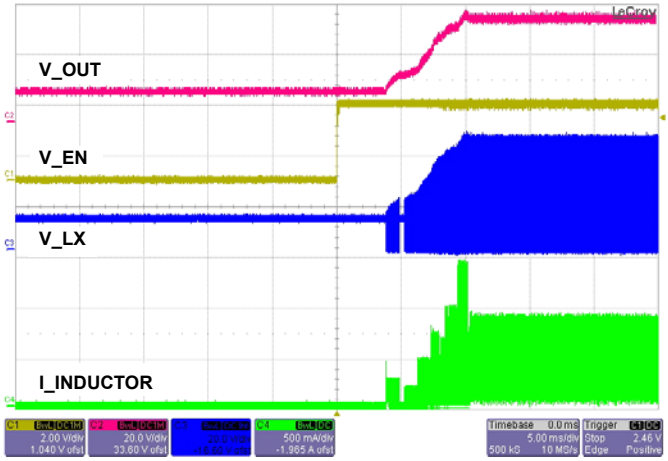


FIGURE 12. SOFT-START INDUCTOR CURRENT AT V_{IN} = 12V FOR 6P12S AT 20mA/CHANNEL

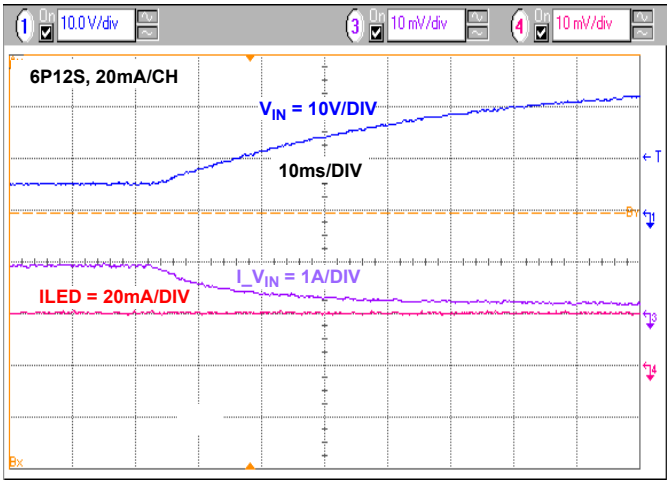


FIGURE 13. LINE REGULATION WITH V_{IN} CHANGE FROM 6V TO 26V, 6P12S AT 20mA/CHANNEL

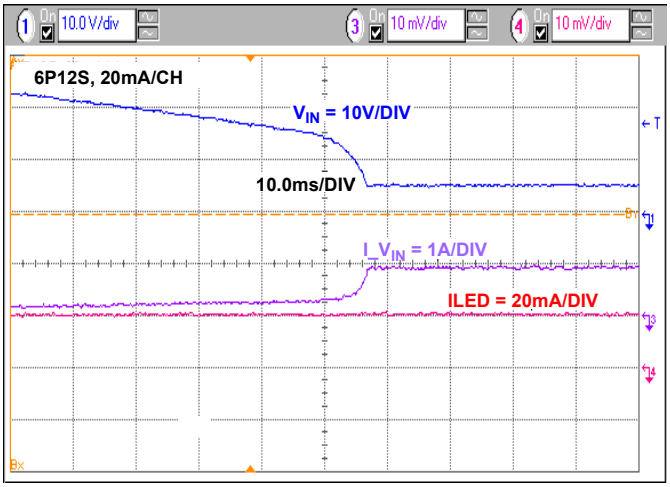


FIGURE 14. LINE REGULATION WITH V_{IN} CHANGE FROM 26V TO 6V FOR 6P12S AT 20mA/CHANNEL

Typical Performance Curves (Continued)

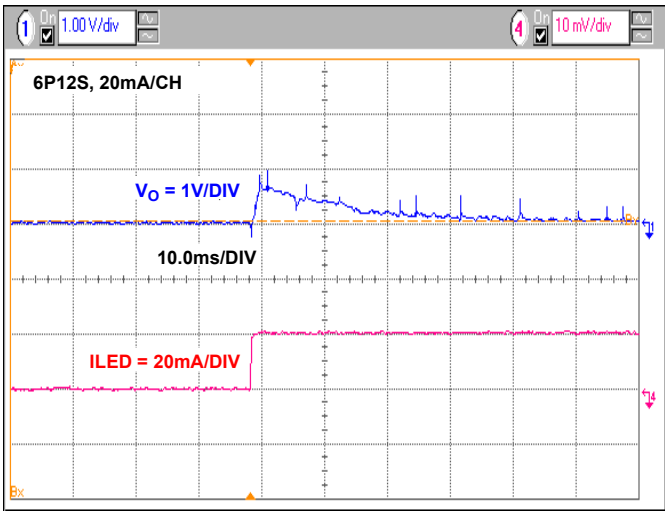


FIGURE 15. BOOST OUTPUT VOLTAGE WITH BRIGHTNESS CHANGE FROM 0% TO 100%, V_{IN} = 12V, 6P12S AT 20mA/CHANNEL

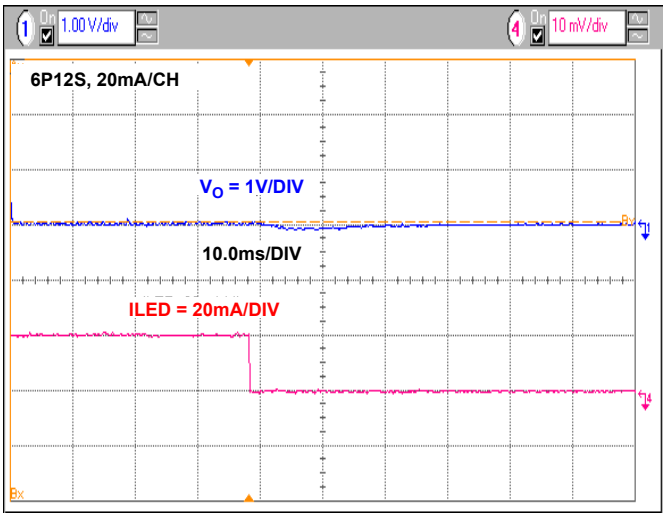


FIGURE 16. BOOST OUTPUT VOLTAGE WITH BRIGHTNESS CHANGE FROM 100% TO 0%, V_{IN} = 12V, 6P12S AT 20mA/CHANNEL

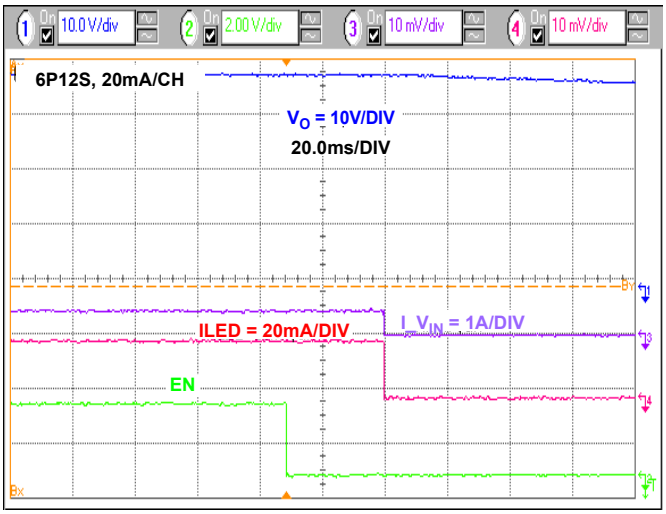


FIGURE 17. ISL97671A SHUTS DOWN AND STOPS SWITCHING ~30ms AFTER EN GOES LOW

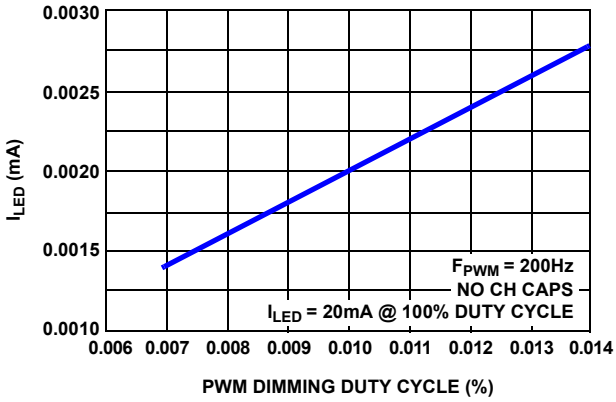


FIGURE 18. DIRECT PWM DIMMING LINEARITY AT VERY LOW DUTY CYCLE

Theory of Operation

PWM Boost Converter

The current mode PWM boost converter produces the minimal voltage needed to enable the LED stack with the highest forward voltage drop to run at the programmed current. The ISL97671A employs current mode control boost architecture that has a fast current sense loop and a slow voltage feedback loop. Such architecture achieves a fast transient response that is essential for notebook backlight applications in which drained batteries can be instantly changed to an AC/DC adapter without noticeable visual disturbance. The number of LEDs that can be driven by ISL97671A depends on the type of LED chosen in the application. The ISL97671A is capable of boosting up to 45V and typically driving 13 LEDs in series for each of the 6 channels, enabling a total of 78 pieces of the 3.2V/20mA type of LEDs.

Enable

The EN pin enables or disables the ISL97671A operation. It is a high voltage pin that can be tied directly to V_{IN} up to 26.5V. If EN is pulled low for longer than 30ms, the device will shut down.

Current Matching and Current Accuracy

Each channel of the LED current is regulated by the current source circuit, as shown in Figure 19.

The LED peak current is set by translating the R_{SET} current to the output with a scaling factor of $410.5/R_{SET}$. The source terminals of the current source MOSFETs are designed to operate within a range at about 500mV to optimize power loss versus accuracy requirements. The sources of the channel-to-channel current matching errors come from the op amp offset, internal layout, reference, and current source resistors. These parameters are optimized for current matching and absolute current accuracy. On the other hand, the absolute accuracy is additionally determined by the external R_{SET}, and therefore, additional tolerance will be contributed by the current setting resistor. A 1% tolerance resistor is therefore recommended.

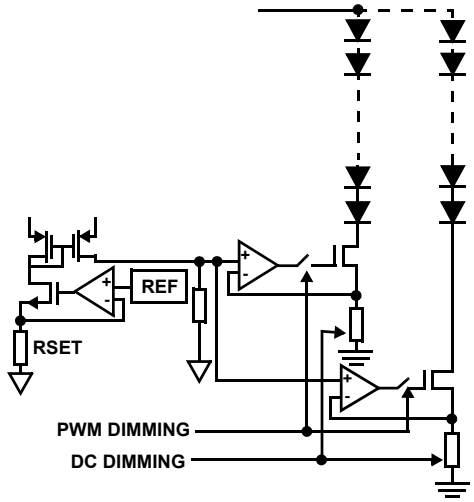


FIGURE 19. SIMPLIFIED CURRENT SOURCE CIRCUIT

Dynamic Headroom Control

The ISL97671A features a proprietary Dynamic Headroom Control circuit that detects the highest forward voltage string or effectively the lowest voltage from any of the CH0-CH5 pins. When this lowest channel voltage is lower than the short-circuit threshold, V_{SC}, such voltage will be used as the feedback signal for the boost regulator. The boost makes the output to the correct level such that the lowest channel pin is at the target headroom voltage. Since all LED stacks are connected to the same output voltage, the other channel pins will have a higher voltage, but the regulated current source circuit on each channel will ensure that each channel has the same programmed current. The output voltage will regulate cycle-by-cycle and is always referenced to the highest forward voltage string in the architecture.

MAXIMUM DC CURRENT SETTING

Set the initial brightness by choosing an appropriate value for R_{SET}. This should be chosen to fix the maximum possible LED current:

$$I_{LEDmax} = \frac{410.5}{R_{SET}} \quad \text{(EQ. 1)}$$

Once R_{SET} is fixed, the LED DC current can be adjusted through Register 0x07 (BRTDC) as follows:

$$I_{LED} = 1.61x(BRTDC/R_{SET}) \quad \text{(EQ. 2)}$$

BRTDC can be programmed from 0 to 255 in decimal and defaults to 255 (0xFF). If left at the default value, the LED current will be fixed at I_{LEDmax}. BRTDC can be adjusted dynamically on the fly during operation. BRTDC = 0 disconnects all channels.

For example, if the maximum required LED current ($I_{LED(max)}$) is 20mA, rearranging Equation 1 yields Equation 3:

$$R_{SET} = 410.5/0.02 = 20.52k\Omega \quad \text{(EQ. 3)}$$

If BRTDC is set to 200, then:

$$I_{LED} = 1.61 \bullet 200/20100 = 16.02mA \quad \text{(EQ. 4)}$$

PWM DIMMING CONTROL

The ISL97671A provides multiple PWM dimming methods, as described in the following. Table Figure 1 on page 12 summarizes the dimming mode selection. Each of these methods results in PWM chopping of the current in the LEDs for all 6 channels to provide a lower average LED current. During the On periods, the LED current will be defined by the value of R_{SET} and BRTDC, as described in Equations 1 and 2. The source of the PWM signal can be described as follows:

1. **Internally generated** - 256 step duty cycle BRT register programmed through the SMBus/I^2C.
2. **External** - Signal from PWM.
3. **DPST mode -** Internally generated signal with duty cycle defined by the product of the PWM input duty cycle and SMBus/I^2C programmed BRT register.
4. **Direct PWM mode -** The output duty cycle and dimming frequency follow the input PWM signal.

The default PWM dimming mode is in DPST. In all of the methods, the average LED channel current is controlled by I_{LED} and the PWM duty cycle in percent, as shown in Equation 5:

$$I_{LED(ave)} = I_{LED} \times PWM \quad \text{(EQ. 5)}$$

Method 1 (SMBus/I²C Controlled Dimming)

The average LED channel current is controlled by the internally generated PWM signal, as shown in Equation 6:

$$I_{LED(ave)} = I_{LED} \times (BRT/255) \quad \text{(EQ. 6)}$$

where BRT is the PWM brightness level programmed in the Register 0x00. BRT ranges from 0 to 255 in decimal and defaults to 255 (0xFF). BRT = 0 disconnects all channels.

To use only the SMBus/I²C controlled PWM brightness control, set Register 0x01 to 0x05. Alternatively, the same operation can be obtained by leaving Register 0x01 at its default value of 0x01 (DPST mode) and connecting the PWM input to VDC, so that the dimming level depends only on the BRT register.

The PWM dimming frequency is adjusted by a resistor at the FPWM pin.

Method 2 (PWM Controlled Dimming with Settable Dimming Frequency)

The average LED channel current can also be controlled by the duty cycle of the external PWM signal, as shown in Equation 7:

$$I_{LILED(ave)} = I_{LED} \times PWMI \quad \text{(EQ. 7)}$$

The PWM dimming frequency is adjusted by a resistor at the FPWM pin. The PWM input cannot be low for more than 30.5ms or else the driver will enter shutdown.

To use the externally applied PWM signal only for brightness control, set Register 0x01 to 0x03. Alternatively, the same operation can be obtained by leaving Register 0x01 at its default value of 0x01 (DPST mode), and not programming Register BRT, so that it contains its default value of 0xFF. A third way to obtain this mode of operation is to tie both SCL and SDA to ground.

Method 3 (DPST Mode)

The average LED channel current can also be controlled by the product of the SMBus/I²C controlled PWM and the external PWM signals as:

$$I_{LED(ave)} = I_{LED} x PWM_{DPST} \quad \text{(EQ. 8)}$$

where:

$$PPWM_{DPST} = BRT/255 \times PWMI \quad \text{(EQ. 9)}$$

therefore:

$$I_{LED(ave)} = I_{LED} \times BRT/255 \times PWMI \quad \text{(EQ. 10)}$$

where BRT is the value held in Register 0x00 (default setting 0xFF) controlled by SMBus/I²C and PWMI is the duty cycle of the incoming PWM signal. In this way, users can change the PWM current in a ratiometric manner to achieve DPST compliant backlight dimming. To use the DPST mode, set Register 0x01 to 0x01. The PWM dimming frequency is adjusted by a resistor at the FPWM pin.

For example, if the SMBus/I²C controlled PWM duty is 80% dimming at 200Hz (see Equation 11) and the external PWM duty cycle is 60% dimming at 1kHz, the resultant PWM duty cycle is 48% dimming at 200Hz.

In DPST mode, the ISL97671A features 8-bit dimming resolution; it calculates the dimming level by taking the eight most significant bits of the product of the PWMI duty cycle (digitized with 8-bit resolution) and of the BRT I²C register.

Method 4 (Direct PWM Mode)

Direct PWM Dimming mode is selected when f_{PWM} is tied to V_{DC} and SMBCLK/SMBDAT are grounded. The current of the six channels will follow the incoming PWM signal's frequency and duty cycle. The minimum duty cycle can be as low as 0.007% at 200Hz (or an equivalent pulse width of 350ns). This ultra low duty cycle dimming performance can be achieved if no channel capacitor is present. Additionally, the Phase Shift function is disabled in Direct PWM Dimming mode.

TABLE 1. DIMMING MODE SELECTION

SMBCLK/ SCL PIN SIGNAL	SMBDAT/ SDA PIN SIGNAL	FPWM PIN	0x01 REGISTER	DIMMING METHOD SELECTION
SMBUS /I2C clock	SMBUS /I2C data	Resistor to ground	Set to 0x05, or set to 0x01 and connect PWM to VDC	Method 1 (SMBUS/I2C controlled dimming)
SMBUS /I2C clock	SMBUS /I2C data	Resistor to ground	Set to 0x03, or set to 0x01 and not program register 0x00	Method 2 (PWM controlled with settable dimming frequency)
Grounded	Grounded	Resistor to ground	N/A	Method 2 (PWM controlled with settable dimming frequency)
SMBUS /I2C clock	SMBUS /I2C data	Resistor to ground	Set to 0x01	Method 3 (DPST mode)
Grounded	Grounded	Tie to VDC	N/A	Method 4 (Direct PWM dimming)

PWM Dimming Frequency Adjustment

For dimming methods 1-3, the PWM dimming frequency is set by an external resistor at the FPWM pin as:

$$F_{PWM} = \frac{6.66 \times 10^7}{RFPWM} \quad \text{(EQ. 11)}$$

where f_{PWM} is the PWM dimming frequency and R_{FPWM} is the setting resistor.

The maximum PWM dimming frequency is 30kHz when the duty cycle is from 0.4% to 100%.

Phase Shift Control

For dimming methods 1-3, the ISL97671A is capable of delaying the phase of each current source to minimize load transients. By default, phase shifting is disabled as shown in Figure 20 where the channels PWM currents are switching at the same time.

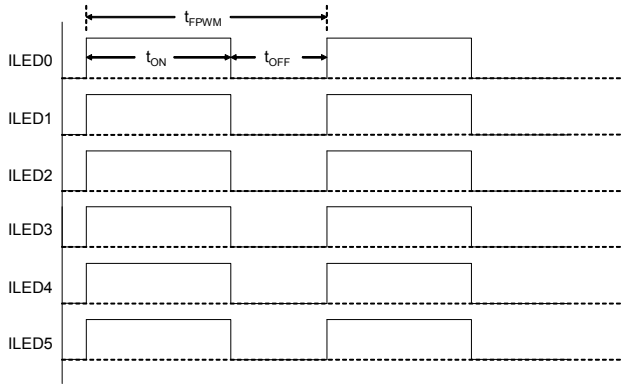


FIGURE 20. NO DELAY (DEFAULT PHASE SHIFT DISABLED)

When EqualPhase = 1 (Register 0x0A, Bit 7), the phase shift evenly spreads the channels switching across the PWM cycle, depending on how many channels are enabled, as shown in Figures 21 and 22. Equal phase means fixed delays occur between channels. Such delay can be calculated using Equation 12 and Figures 21 and 22.

$$t_{D1} = \frac{t_{FPWM}}{255} x \left(\frac{255}{N}\right) \quad \text{(EQ. 12)}$$

Equation 13 shows the phase delay between the last channel of the current duty cycle and the first channel of the next duty cycle in Figures 21 and 22.

$$t_{D2} = \frac{t_{FPWM}}{255} x \left(255 - (N-1)\left(\frac{255}{N}\right)\right) \quad \text{(EQ. 13)}$$

where (255/N) is rounded down to the nearest integer. For example, if N = 6, (255/N) = 42, leading to:

$t_{D1} = t_{FPWM} \times 42/255$

$t_{D2} = t_{FPWM} \times 45/255$

where t_{FPWM} is the sum of t_{ON} and t_{OFF}. N is the number of LED channels. The ISL97671A will detect the number of operating channels automatically.

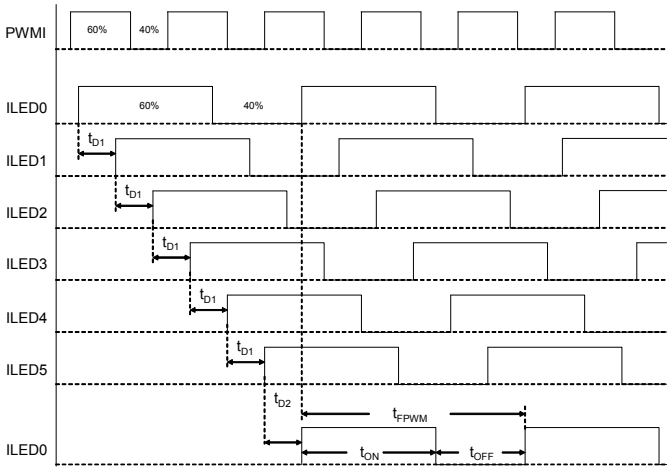


FIGURE 21. 6 EQUAL PHASE CHANNELS PHASE SHIFT ILLUSTRATION

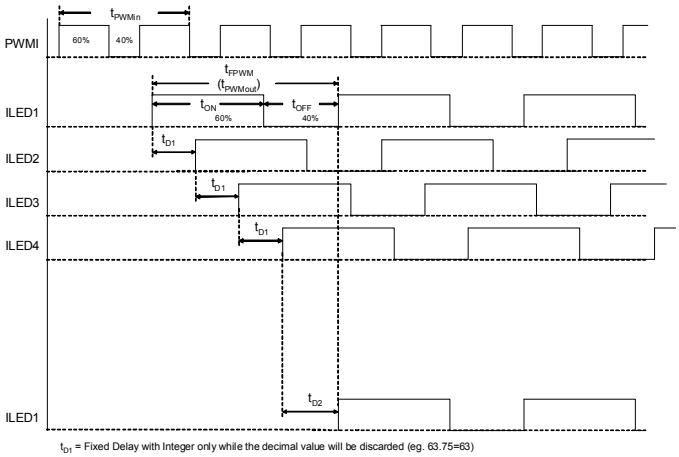


FIGURE 22. 4 EQUAL PHASE CHANNELS PHASE SHIFT ILLUSTRATION

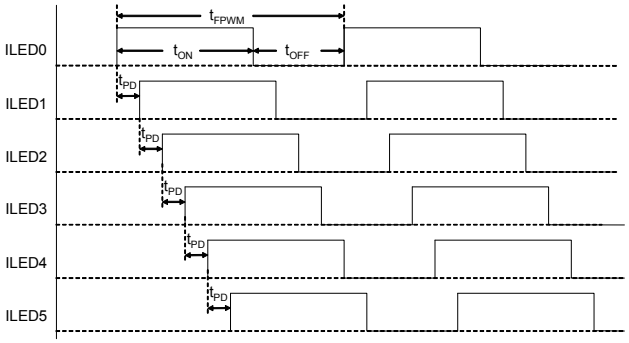


FIGURE 23. PHASE SHIFT WITH 7-BIT PROGRAMMABLE DELAY

The ISL97671A allows the user to program the amount of phase shift degree with 7-bit resolution, as shown in Figure 23. To enable programmable phase shifting, write to the Phase Shift Control register with EqualPhase = 0 and the desirable phase shift value of PhaseShift[6:0]. The delay between CH5 and the repeated CH0 is the rest of the PWM cycle.

Switching Frequency

The default switching frequency is 600kHz but it can be selected from 600kHz or 1.2MHz if the SMBus/I²C communications is used. The switching frequency select bit is accessible in the SMBus/I²C Configuration Register 0x08 Bit 2.

5V Low Dropout Regulator

An internal 5V low dropout (LDO) regulator develops the necessary low-voltage supply, which is used by the chip's internal control circuitry. VDC is the output of this LDO regulator, which requires a bypass capacitor of 1µF or more for the regulation. The VDC pin can be used as a coarse reference as long as it is sourcing only a few milliamps.

IC Protection Features and Fault Management

ISL97671A has several protection and fault management features that improve system reliability. The following sections describe them in more detail.

Inrush Control and Soft-Start

The ISL97671A has separate, built-in, independent inrush control and soft-start functions. The inrush control function is built around an external short-circuit protection P-channel FET in series with V_{IN}. At start-up, the fault protection FET is turned on slowly due to a 21µA pull-down current output from the FAULT pin. This discharges the fault FET's gate-source capacitance, turning on the FET in a controlled fashion. As this happens, the output capacitor is charged slowly through the low-current FET before it becomes fully enhanced. This results in a low inrush current. This current can be further reduced by adding a capacitor (in the 1nF to 5nF range) across the gate source terminals of the FET.

Once the chip detects that the fault protection FET is turned on fully, it assumes that inrush is complete. At this point, the boost regulator begins to switch, and the current in the inductor ramps up. The current in the boost power switch is monitored, and switching is terminated in any cycle in which the current exceeds the current limit. The ISL97671A includes a soft-start feature in which this current limit starts at a low value (275mA). This value is stepped up to the final 2.2A current limit in seven additional steps of 275mA each. These steps happen over at least 8ms and are extended at low LED PWM frequencies if the LED duty cycle is low. This extension allows the output capacitor to charge to the required value at a low current limit and prevents high input current for systems that have only a low to medium output current requirement.

For systems with no master fault protection FET, the inrush current flows towards C_{OUT} when V_{IN} is applied. The inrush current is determined by the ramp rate of V_{IN} and the values of C_{OUT} and L.

Fault Protection and Monitoring

The ISL97671A features extensive protection functions to cover all perceivable failure conditions.

The failure mode of an LED can be either an open circuit or a short. The behavior of an open-circuited LED can additionally take the form of either infinite resistance or, for some LEDs, a Zener diode, which is integrated into the device in parallel with the now-opened LED.

For basic LEDs (which do not have built-in Zener diodes), an open-circuit failure of an LED results only in the loss of one channel of LEDs, without affecting other channels. Similarly, a short-circuit condition on a channel that results in that channel being turned off does not affect other channels unless a similar fault is occurring.

Due to the lag in boost response to any load change at its output, certain transient events (such as LED current steps or significant step changes in LED duty cycle) can transiently look like LED fault modes. The ISL97671A uses feedback from the LEDs to determine when it is in a stable operating region and prevents apparent faults during these transient events from allowing any of the LED stacks to fault out. Refer to Table 2 on page 16 for details.

A fault condition that results in an input current that exceeds the device's electrical limits will result in a shutdown of all output channels.

All LED faults are reported via the SMBus/I^{2}C interface to Register 0x02 (Fault/Status register). The controller is able to determine which channels have failed via Register 0x09 (Output Masking register). The controller can also choose to use Register 0x09 to disable faulty channels at start-up, resulting in only further faulty channels being reported by Register 0x02.

Short-Circuit Protection (SCP)

The short-circuit detection circuit monitors the voltage on each channel and disables faulty channels that are above approximately 7.5V. This action is described in Table 2 on page 16.

Open-Circuit Protection (OCP)

When one of the LEDs becomes an open circuit, it can behave as either an infinite resistance or as a gradually increasing finite resistance. The ISL97671A monitors the current in each channel such that any string that reaches the intended output current is considered "good." Should the current subsequently fall below the target, the channel is considered an "open circuit." Furthermore, should the boost output of the ISL97671A reach the OVP limit, or should the lower over-temperature threshold be reached, all channels that are not good are immediately considered to be open circuit. Detection of an open circuit channel results in a time-out before the affected channel is disabled. This time-out is sped up when the device is above the lower over-temperature threshold, in an attempt to prevent the upper over-temperature trip point from being reached.

Some users employ special types of LEDs that have a Zener diode structure in parallel with the LED. This configuration provides ESD enhancement and enables open-circuit operation. When this type of LED is open circuited, the effect is as if the LED forward voltage has increased but the lighting level has not increased. Any affected string will not be disabled, unless the failure results in the boost OVP limit being reached, which allows all other LEDs in the string to remain functional. In this case, ensure that the boost OVP limit and SCP limit are set properly, so that multiple failures on one string do not cause all other good channels to fault out. This condition could arise if the increased forward voltage of the faulty channel makes all other channels look as if they have LED shorts. Refer to Table 2 on page 16 for details about responses to fault conditions.

OVP and V_{OUT}

The Overvoltage Protection (OVP) pin sets the overvoltage trip level and limits the V_{OUT} regulation range.

The ISL97671A OVP threshold is set by R_{UPPER} and R_{LOWER} such that:

$$V_{OUT\_OVP} = 1.22V \times \frac{(R_{UPPER} + R_{LOWER})}{R_{LOWER}} \quad \text{(EQ. 14)}$$

and the output voltage V_{OUT} can regulate between 64% and 100% of the V_{OUT_OVP} such that:

Allowable V_{OUT} = 64% to 100% of V_{OUT_OVP}

If R_1 and R_2 are chosen such that the OVP level is set at 40V, then V_{OUT} is allowed to operate between 25.6V and 40V. If the V_{OUT} requirement is changed to an application of six LEDs of 21V,

then the OVP level must be reduced. Follow the V_{OUT} = (64% ~100%) OVP level requirement, otherwise the headroom control will be disturbed such that the channel voltage can be much higher than expected. This can sometimes prevent the driver from operating properly.

The resistances should be large to minimize power loss. For example, a 1MΩ R_{UPPER} and a 30kΩ R_{LOWER} sets OVP to 41.9V. Large OVP resistors also allow C_{OUT} to discharge slowly during the PWM Off time. Parallel capacitors should also be placed across the OVP resistors such that $R_{UPPER}/R_{LOWER} = C_{LOWER}/C_{UPPER}$. Using a C_{UPPER} value of 30pF is recommended. These capacitors reduce the AC impedance of the OVP node, which is important when using high-value resistors. For example, if R_{UPPER}/R_{LOWER} = 33/1, then C_{UPPER}/C_{LOWER} = 1/33 with C_{UPPER} = 100pF and C_{LOWER} = 3.3nF

Undervoltage Lock-out

If the input voltage falls below the UVLO level, the device stops switching and is reset. Operation restarts only when V_{IN} returns to the normal operating range.

Input Overcurrent Protection

During a normal switching operation, the current through the internal boost power FET is monitored. If the current exceeds the current limit, the internal switch is turned off. Monitoring occurs on a cycle-by-cycle basis in a self-protecting way. Additionally, the ISL97671A monitors the voltage at the LX and OVP pins. At start-up, the LX pins inject a fixed current into the output capacitor. The device does not start unless the voltage at LX exceeds 1.2V. The OVP pin is also monitored such that if it rises above and subsequently falls below 20% of the target OVP level, the input protection FET is also switched off.

Over-Temperature Protection (OTP)

The ISL97671A includes two over-temperature thresholds. The lower threshold is set to +130°C. When this threshold is reached, any channel that is outputting current at a level significantly below the regulation target is treated as “open circuit” and is disabled after a time-out period. This time-out period is 800µs when it is above the lower threshold. The lower threshold isolates and disables bad channels before they cause enough power dissipation (as a result of other channels having large voltages across them) to hit the upper temperature threshold.

The upper threshold is set to +150°C. Each time this threshold is reached, the boost stops switching, and the output current sources switch off. Once the device has cooled to approximately +100°C, the device restarts, with the DC LED current level reduced to 75% of the initial setting. If dissipation persists, subsequent hitting of the limit causes identical behavior, with the current reduced in steps to 50% and finally 25%. Unless disabled via the EN pin, the device stays in an active state throughout.

For complete details about fault protection conditions, refer to Figure 24 and Table 2.

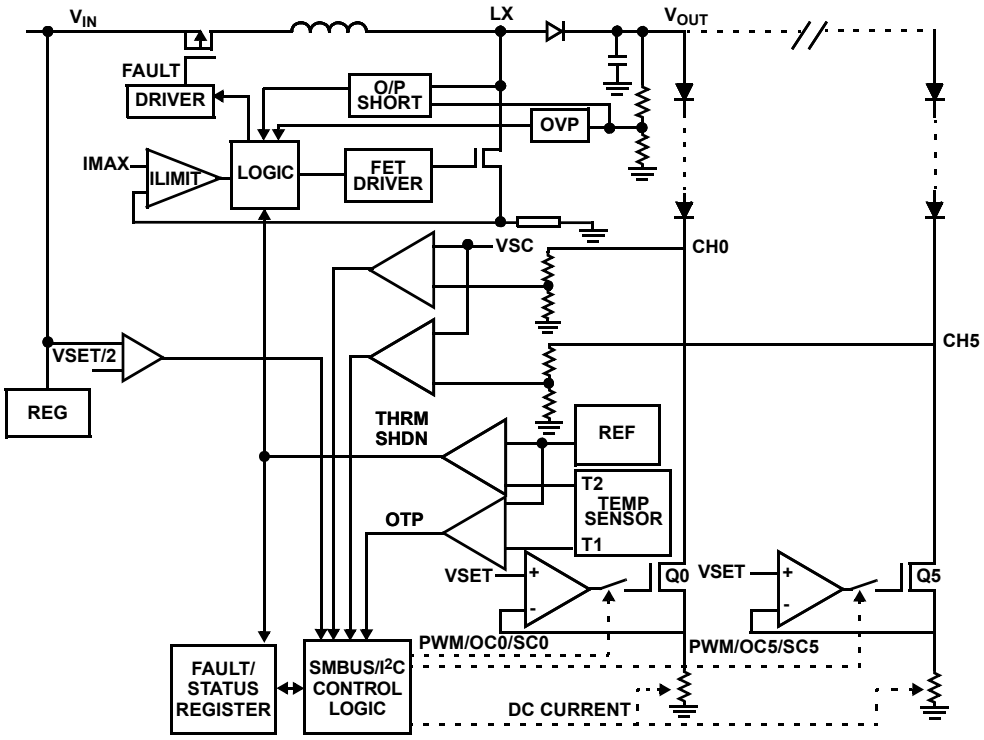
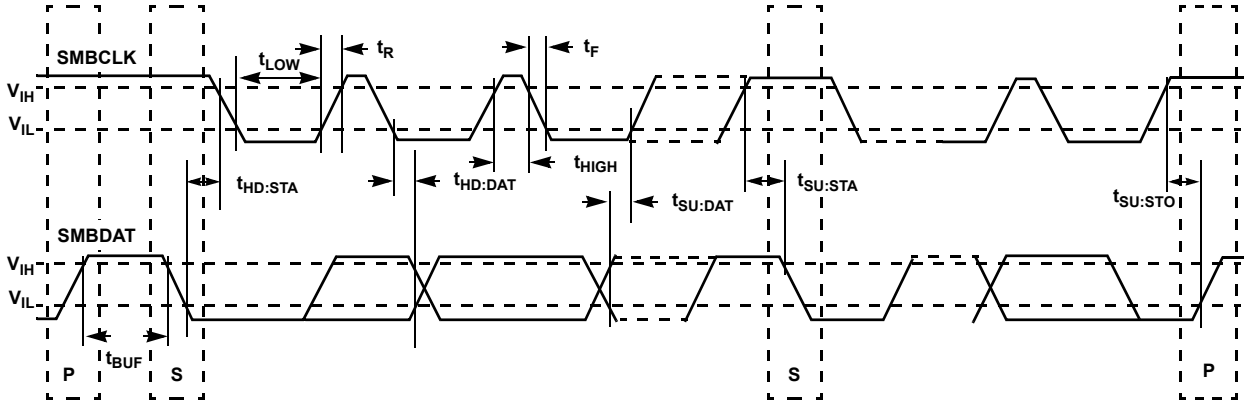


FIGURE 24. SIMPLIFIED FAULT PROTECTIONS

TABLE 2. PROTECTIONS TABLE

CASE	FAILURE MODE	DETECTION MODE	FAILED CHANNEL ACTION	GOOD CHANNELS ACTION	V_{OUT} REGULATED BY
1	CHx Short-Circuit	Upper Over-Temperature Protection limit (OTP) not triggered and CHx < 7.5V	CHx ON and burns power.	Remaining channels normal	Highest VF of all channels
2	CHx Short-Circuit	Upper OTP triggered but CHx < 7.5V	All channels turn off until chip cooled, then turn back on with current reduced to 76%. Subsequent OTP triggers will reduce I_{OUT} further.	Same as CHx	Highest VF of remaining channels
3	CHx Short-Circuit	Upper OTP not triggered but CHx > 7.5V	CHx disabled after 6 PWM cycle time-outs.	Remaining channels normal	Highest VF of remaining channels
4	CHx Open Circuit with infinite resistance	Upper OTP not triggered and CHx < 7.5V	V_{OUT} will ramp to OVP. CHx will time-out after 6 PWM cycles and switch off. V_{OUT} will drop to normal level.	Remaining channels normal	Highest VF of remaining channels
5	CHx LED Open Circuit but has paralleled Zener	Upper OTP not triggered and CHx < 7.5V	CHx remains ON and has highest VF, thus V_{OUT} increases.	Remaining channels ON, remaining channel FETs burn power	VF of CHX
6	CHx LED Open Circuit but has paralleled Zener	Upper OTP triggered but CHx < 7.5V	All channels turn off until chip cooled, then turn back on with current reduced to 76%. Subsequent OTP triggers will reduce I_{OUT} further.	Same as CHx	VF of CHx
7	CHx LED Open Circuit but has paralleled Zener	Upper OTP not triggered but CHx > 7.5V	CHx remains ON and has highest VF, thus V_{OUT} increases.	V_{OUT} increases, then CH-X switches OFF after 6 PWM cycles. This is an unwanted shut off and can be prevented by setting OVP at an appropriate level.	VF of CHx
8	Channel-to-Channel ΔVF too high	Lower OTP triggered but CHx < 7.5V	Any channel below the target current will fault out after 6 PWM cycles. Remaining channels driven with normal current.		Highest VF of remaining channels
9	Channel-to-Channel ΔVF too high	Upper OTP triggered but CHx < 7.5V	All channels go off until chip cools and then come back on with current reduced to 76%. Subsequent OTP triggers will reduce I_{OUT} further.		Boost switch OFF
10	Output LED stack voltage too high	V_{OUT} > VOVP	Any channel that is below the target current will time-out after 6 PWM cycles, and V_{OUT} will return to the normal regulation voltage required for other channels.		Highest VF of remaining channels
11	V_{OUT}/LX shorted to GND at start-up or V_{OUT} shorted in operation	LX current and timing are monitored. OVP pins monitored for excursions below 20% of OVP threshold.	The chip is permanently shutdown 31ms after power-up if V_{OUT}/Lx is shorted to GND.		



NOTES:

SMBus/I²C Description

S = start condition

P = stop condition

A = acknowledge

$\overline{A}$ = not acknowledge

R/$\overline{W}$ = read enable at high; write enable at low

FIGURE 25. SMBUS/I²C INTERFACE

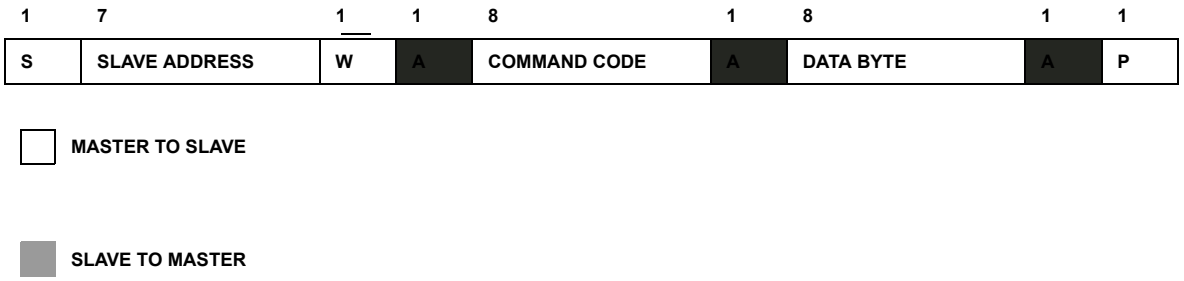


FIGURE 26. WRITE BYTE PROTOCOL

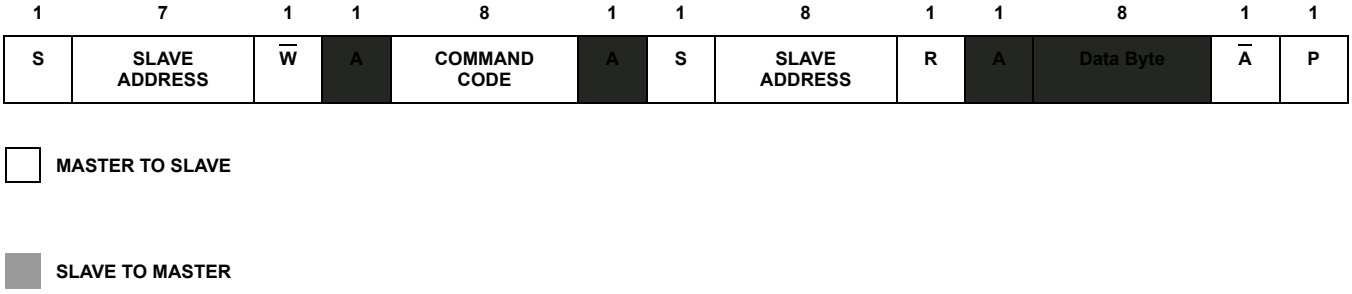


FIGURE 27. READ BYTE PROTOCOL

SMBus/I²C Communications

The ISL97671A can be controlled by the SMBus/I²C for PWM or DC dimming. The LEDs are off by default and the user must use the SMBus/I²C interface to turn them on, except when both the SDA and SCL input pins are tied to ground. When both SDA and SCL are shorted to ground, the LEDs turn on by default when the IC is turned on, and the customer can use the ISL97671A without having to control the SMBus/I²C interface. The switching frequency is fixed at 600kHz if SMBus/I²C is not used.

Write Byte

The Write Byte protocol is only three bytes long. The first byte starts with the slave address followed by the “command code,” which translates to the “register index” being written. The third byte contains the data byte that must be written into the register selected by the “command code”. A shaded label is used on cycles during which the slaved backlight controller “owns” or “drives” the Data line. All other cycles are driven by the “host master.”

Read Byte

Figure 27 on page 17 shows that the four byte long Read Byte protocol starts out with the slave address followed by the “command code” which translates to the “register index.” Subsequently, the bus direction turns around with the re-broadcast of the slave address with Bit 0 indicating a read (“R”) cycle. The fourth byte contains the data being returned by the backlight controller. That byte value in the data byte reflects the value of the register being queried at the “command code” index. Note the bus directions, which are highlighted by the shaded label that is used on cycles during which the slaved backlight controller “owns” or “drives” the Data line. All other cycles are driven by the “host master.”

Slave Device Address

The slave address contains seven MSB plus one LSB as a R/W bit, but these eight bits are usually called Slave Address bytes. Figure 28 shows that the high nibble of the Slave Address byte is 0x5 or 0101b to denote the “backlight controller class.” Bit 3 in the lower nibble of the Slave Address byte is 1. Bit 0 is always the R/W bit, as specified by the SMBus/I²C protocol.

Note: In this document, the device address will always be expressed as a full 8-bit address instead of the shorter 7-bit address typically used in other backlight controller specifications to avoid confusion. Therefore, if the device is in the write mode where Bit 0 is 0, the slave address byte is 0x58 or 01011000b. If the device is in the read mode where Bit 0 is 1, the slave address byte is 0x59 or 01011001b.

SMBus/I²C Register Definitions

The backlight controller registers are a byte wide and accessible via the SMBus/I²C Read/Write Byte protocols. Their bit assignments are provided in the following sections with reserved bits containing a default value of “0”.

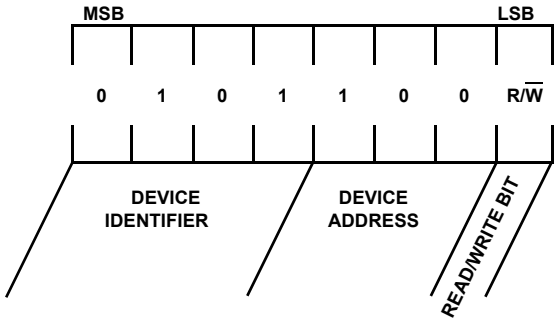


FIGURE 28. SLAVE ADDRESS BYTE DEFINITION

TABLE 3A. ISL97671A REGISTER LISTING

ADDRESS	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	DEFAULT VALUE	SMBUS/I²C PROTOCOL
0x00	PWM Brightness Control Register	BRT7	BRT6	BRT5	BRT4	BRT3	BRT2	BRT1	BRT0	0xFF	Read and Write
0x01	Device Control Register	Reserved	Reserved	Reserved	Reserved	Reserved	PWM_MD	PWM_SEL	BL_CTL	0x00	Read and Write
0x02	Fault/Status Register	Reserved	Reserved	2_CH_SD	1_CH_SD	BL_STAT	OV_CURR	THRM_SHDN	FAULT	0x00	Read Only
0x03	Identification Register	LED PANEL	MFG3	MFG2	MFG1	MFG0	REV2	REV1	REV0	0xC8	Read Only
0x07	DC Brightness Control Register	BRTDC7	BRTDC6	BRTDC5	BRTDC4	BRTDC3	BRTDC2	BRTDC1	BRTDC0	0xFF	Read and Write
0x08	Configuration Register	Reserved	Reserved	Reserved	BstSlew Rate1	BstSlew Rate0	FSW	Reserved	VSC	0x1F	Read and Write
0x09	Output Channel Register	Reserved	Reserved	CH5	CH4	CH3	CH2	CH1	CH0	0x3F	Read and Write
0x0A	Phase Shift Deg	Equal Phase	Phase Shift6	Phase Shift5	Phase Shift4	Phase Shift3	Phase Shift2	Phase Shift1	Phase Shift0	0x00	Read and Write

TABLE 3B. DATA BIT DESCRIPTIONS

ADDRESS	REGISTER	DATA BIT DESCRIPTIONS
0x00	PWM Brightness Control Register	BRT[7..0] = 256 steps of DPWM duty cycle brightness control
0x01	Device Control Register	PWM_MD, PWM_SEL: select the dimming method. Refer to Table 4 for more details. Default = 00 BL_CTL = BL On/Off (1 = On, 0 = Off), default = 0
0x02	Fault/Status Register	2_CH_SD = Two LED output channels are shutdown (1 = Shutdown, 0 = OK) 1_CH_SD = One LED output channel is shutdown (1 = Shutdown, 0 = OK) BL_STAT = BL status (1 = BL On, 0 = BL Off) OV_CURR = Input overcurrent (1 = Overcurrent condition, 0 = Current OK) THRM_SHDN = Thermal Shutdown (1 = Thermal fault, 0 = Thermal OK) FAULT = Fault occurred (Logic “OR” of all of the fault conditions)
0x03	Identification Register	LED PANEL = 1 MFG[3..0] = Manufacturer ID (16 vendors available. Intersil is vendor ID 9) REV[2..0] = Silicon rev (Rev 0 through Rev 7 allowed for silicon spins)
0x07	DC Brightness Control Register	BRTDC[7..0] = 256 steps of DC brightness control
0x08	Configuration Register	BstSlewRate[1..0] = Controls strength of FET driver. 00 - 25% drive strength, 01 - 50% drive strength, 10 - 75% drive strength, 11 - 100% drive strength. f_{SW} = Switching frequencies selection, f_{SW} = 0 = 1.2MHz. f_{SW} = 1 = 600kHz VSC[0] = Short-circuit thresholds selection, 0 = disabled, 1 = 7.2V minimum
0x09	Output Channel Mask/Fault Readout Register	CH[5..0] = Output Channel Read and Write. In Write, 1 = Channel Enabled, 0 = Channel Disabled. In Read, 1 = Channel OK, 0 = Channel Not OK/Channel disabled
0x0A	Phase Shift Degree	EqualPhase = Controls phase shift mode. When 1, phase shift is 360/N (where N is the number of channels enabled). When 0, phase shift is defined by PhaseShift<6:0>. PS[6..0] = 7-bit Phase shift setting - phase shift between each channel is PhaseShift<6:0>/(255*PWMFreq). In direct PWM modes, phase shift between each channel is PhaseShift<6:0>/12.8MHz.

PWM Brightness Control Register (0x00)

The Brightness control resolution has 256 steps of PWM duty cycle adjustment. Figure 29 shows the bit assignment. All of the bits in this Brightness Control Register can be read or written. Step 0 corresponds to the minimum step where the current is less than 10µA. Steps 1 to 255 represent the linear steps between 0.39% and 100% duty cycle with approximately 0.39% duty cycle adjustment per step.

- An SMBus/I^{2}C Write Byte cycle to Register 0x00 sets the PWM brightness level only if the backlight controller is in SMBus/I^{2}C mode (see Table 4). Operating Modes are selected by Device Control Register Bits 1 and 2.
- An SMBus/I^{2}C Read Byte cycle to Register 0x00 returns the programmed PWM brightness level.
- An SMBus/I^{2}C setting of 0xFF for Register 0x00 sets the backlight controller to the maximum brightness.
- An SMBus/I^{2}C setting of 0x00 for Register 0x00 sets the backlight controller to the minimum brightness output.
- The default value for Register 0x00 is 0xFF.

Device Control Register (0x01)

This register has two bits that control either SMBus/I^{2}C controlled or external PWM controlled PWM dimming and a single bit that controls the backlight ON/OFF state. The remaining bits are reserved. The bit assignment is shown in Figure 30. All other bits in the Device Control Register will read as low unless otherwise written.

- All reserved bits have no functional effect when written.
- All defined control bits return their current, latched value when read.

A value of 1 written to BL_CTL turns on the backlight in 4ms or less after the write cycle completes. The backlight is deemed to be on when Bit 3 BL_STAT of Register 0x02 is 1 and Register 0x09 is not 0.

A value of 0 written to BL_CTL immediately turns off the BL. The BL is deemed to be off when Bit 3 BL_STAT of Register 0x02 is 0 and Register 0x09 is 0.

The default value for Register 0x01 is 0x00.

REGISTER 0x00	PWM BRIGHTNESS CONTROL REGISTER

BRT7	BRT6	BRT5	BRT4	BRT3	BRT2	BRT1	BRT0
Bit 7 (R/W)	Bit 6 (R/W)	Bit 5 (R/W)	Bit 4 (R/W)	Bit 3 (R/W)	Bit 2 (R/W)	Bit 1 (R/W)	Bit 0 (R/W)

BIT ASSIGNMENT	BIT FIELD DEFINITIONS
BRT[7..0]	= 256 steps of PWM brightness levels

FIGURE 29. DESCRIPTIONS OF BRIGHTNESS CONTROL REGISTER

REGISTER 0x01	DEVICE CONTROL REGISTER

RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	PWM_MD	PWM_SEL	BL_CTL
Bit 7 (R/W)	Bit 6 (R/W)	Bit 5 (R/W)	Bit 4 (R/W)	Bit 3 (R/W)	Bit 2 (R/W)	Bit 1 (R/W)	Bit 0 (R/W)

PWM_MD	PWM_SEL	BL_CTL	MODE
X	X	0	Backlight Off
0	0	1	SMBus/I^{2}C and PWM input controlled (DPST) dimming (Method 3)
1	0	1	SMBus/I^{2}C controlled PWM dimming (Method 1)
X	1	1	PWM input controlled PWM dimming (Method 2)

FIGURE 30. DESCRIPTIONS OF DEVICE CONTROL REGISTER

TABLE 4. OPERATING MODES SELECTED BY DEVICE CONTROL REGISTER BITS 1 AND 2

PWM_MD	PWM_SEL	MODE
0	0	SMBus/I²C and PWM input controlled (DPST) dimming (Method 3)
1	0	SMBus/I²C controlled PWM dimming (Method 1)
X	1	PWM input controlled PWM dimming (Method 2)

The PWM_SEL bit determines whether the SMBus/I²C or PWM input should drive the output brightness in terms of PWM dimming. When PWM_SEL bit is 1, the PWM input only drives the output brightness regardless of what the PWM_MD is.

When the PWM_SEL bit is 0, the PWM_MD bit selects the manner in which the PWM dimming is to be interpreted. When this bit is 1, the PWM dimming is based on the SMBus/I²C brightness setting only. When this bit is 0, the PWM dimming reflects a percentage change in the current brightness programmed in the SMBus/I²C Register 0x00, i.e., DPST (Display Power Saving Technology) mode as:

$$\text{DSPT Brightness} = \text{Cbt} \times \text{PWM} \quad \text{(EQ. 15)}$$

where:

Cbt = Current brightness setting from SMBus/I²C Register 0x00 without influence from the PWM

PWM = is the percent duty cycle of the PWM

For example, the Cbt = 50% duty cycle programmed in the SMBus/I²C Register 0x00 and the PWM frequency is tuned to be 200Hz with an appropriate capacitor at the FPWM pin. On the other hand, PWM is fed with a 1kHz 30% high PWM signal. When PWM_SEL = 0 and PWM_MD = 0, the device is in DPST operation where DPST brightness = 15% PWM dimming at 200Hz.

Fault/Status Register (0x02)

This register has six status bits that allow monitoring of the backlight controller's operating state. Not all of the bits in this register are fault related (Bit 3 is a simple BL status indicator). The remaining bits are reserved and return a "0" when read and ignore the bit value when written. All of the bits in this register are read-only, with the exception of Bit 0, which can be cleared by writing to it.

- BL_STAT indicates the current backlight on/off status in BL_STAT (1 if the BL is on, 0 if the BL is off).
- FAULT is the logical OR of THRM_SHDN, OV_CURR, 2_CH_SD, and 1_CH_SD should these events occur.
- 1_CH_SD returns a 1 if one or more channels have faulted out.
- 2_CH_SD returns a 1 if two or more channels have faulted out.
- When FAULT is set to 1, it will remain at 1 even if the signal which sets it goes away. FAULT will be cleared when the BL_CTL bit of the Device Control Register is toggled or when a 0 is written into the FAULT bit. At that time, if the fault condition is still present or reoccurs, FAULT will be set to 1 again. BL_STAT will not cause FAULT to be set.
- The default value for Register 0x02 is 0x00.

REGISTER 0x02	FAULT/STATUS REGISTER

RESERVED	RESERVED	2_CH_SD	1_CH_SD	BL_STAT	OV_CURR	THRM_SHDN	FAULT
Bit 7 (R)	Bit 6 (R)	Bit 5 (R)	Bit 4 (R)	Bit 3 (R)	Bit 2 (R)	Bit 1 (R)	Bit 0 (R)

BIT	BIT ASSIGNMENT	BIT FIELD DEFINITIONS
Bit 5	2_CH_SD	Two LED output channels are shutdown (1 = shutdown, 0 = OK)
Bit 4	1_CH_SD	One LED output channel is shutdown (1 = shutdown, 0 = OK)
Bit 3	BL_STAT	BL Status (1 = BL On, 0 = BL Off)
Bit 2	OV_CURR	Input Overcurrent (1 = Overcurrent condition, 0 = Current OK)
Bit 1	THRM_SHDN	Thermal Shutdown (1 = Thermal Fault, 0 = Thermal OK)
Bit 0	FAULT	Fault occurred (Logic "OR" of all of the fault conditions)

FIGURE 31. DESCRIPTIONS OF FAULT/STATUS REGISTER

Identification Register (0x03)

The ID register contains three bit fields to denote the LED driver (always set to 1), manufacturer, and the silicon revision of the controller IC. The bit field widths allow up to 16 vendors with up to eight silicon revisions each. All of the bits in this register are read-only.

- Vendor ID 9 represents Intersil Corporation.
- The default value for Register 0x03 is 0xC8.

The initial value of REV is 0. Subsequent values of REV will increment by 1.

DC Brightness Control Register (0x07)

The DC Brightness Control Register 0x07 sets the LED current level between 0% and 100% of the level set using the RSET pin. When PWM dimming, the level set is the current during the on time. This register allows additional dimming flexibility by:

1. Effectively achieving 16-bits of dimming control when DC dimming is combined with PWM dimming
2. Achieving visual or audio noise free 8-bit DC dimming over potentially noisy PWM dimming.

The bit assignment is shown in Figure 33. All of the bits in this register can be read or written. Steps 0 to 255 represent the linear steps of current adjustment in DC on-the-fly.

- An SMBus/I^2C Write Byte cycle to Register 0x07 sets the DC LED current level.
- An SMBus/I^2C Read Byte cycle to Register 0x07 returns the DC LED current.
- The default value for Register 0x07 is 0xFF.

REGISTER 0x03	ID REGISTER

LED PANEL	MFG3	MFG2	MFG1	MFG0	REV2	REV1	REV0
Bit 7 = 1	Bit 6 (R)	Bit 5 (R)	Bit 4 (R)	Bit 3 (R)	Bit 2 (R)	Bit 1 (R)	Bit 0 (R)

BIT ASSIGNMENT	BIT FIELD DEFINITIONS
MFG[3..0]	= Manufacturer ID. Refer to "Identification Register (0x03)" on page 21. data 0 to 8 in decimal correspond to other vendors data 9 in decimal represents Intersil ID data 10 to 14 in decimal are reserved data 15 in decimal Manufacturer ID is not implemented
REV[2..0]	= Silicon rev (Rev 0 through Rev 7 allowed for silicon spins)

FIGURE 32. DESCRIPTIONS OF ID REGISTER

REGISTER 0x07	DC BRIGHTNESS CONTROL REGISTER

BRTDC7	BRTDC6	BRTDC5	BRTDC4	BRTDC3	BRTDC2	BRTDC1	BRTDC0
Bit 7 (R/W)	Bit 6 (R/W)	Bit 5 (R/W)	Bit 4 (R/W)	Bit 3 (R/W)	Bit 2 (R/W)	Bit 1 (R/W)	Bit 0 (R/W)

BIT ASSIGNMENT	BIT FIELD DEFINITIONS
BRTDC[7..0]	= 256 steps of DC brightness levels

FIGURE 33. DESCRIPTIONS OF DC BRIGHTNESS CONTROL REGISTER

Configuration Register (0x08)

The Configuration Register provides many extra functions that can optimize the driver performance at a given application.

A BstSlewRate bit allows users to control the boost FET slew rate (the rates of turn-on and turn-off). The slew rate can be selected to four relative strengths when driving the internal boost FET. This allows users to experiment with the slew rate with respect to EMI effect in the system. In general, the slower the slew rate is, the lower the EMI interference to the surrounding circuits. However, the switching loss of the boost FET is also increased.

The FSW bit allows users to set the boost converter switching frequency between 1.2MHz and 600kHz. The VSC bit allows users to set the LED string short-circuit threshold VSC to 7.2V or disable it.

The bit assignment is shown in Figure 34. The default value for Register 0x08 is 0x1F.

Output Channel Mask/Fault Readout Register (0x09)

This register can be read or written. It allows enabling and disabling each channel individually. The bit position corresponds to the channel. For example, Bit 0 corresponds to Ch0, Bit 5 corresponds to Ch5, and so on. A 1 bit value enables the channel of interest. When reading data from this register, any disabled channel and any faulted out channel will read as 0. This allows the user to determine which channel is faulty and optionally not enabling it in order to allow the rest of the system to continue to function. Additionally, a faulted out channel can be disabled and re-enabled in order to allow a retry for any faulty channel without having to power-down the other channels.

The bit assignment is shown in Figure 35. The default value for Register 0x09 is 0x3F.

REGISTER 0x08	CONFIGURATION REGISTER

RESERVED	RESERVED	BIT5	BIT4	BIT3	FSW	RESERVED	VSC
Bit 7 (R/W)	Bit 6 (R/W)	Bit 5 (R/W)	Bit 4 (R/W)	Bit 3 (R/W)	Bit 2 (R/W)	Bit 1 (R/W)	Bit 0 (R/W)

BIT ASSIGNMENT	BIT FIELD DEFINITIONS
BstSlewRate[1:0]	Controls strength of FET driver. 00 - 25% drive strength, 01 to 50% drive strength, 10 -75% drive strength, 11 to 100% drive strength.
FSW	Two levels of switching frequencies (0 = 1.2MHz, 1 = 600kHz)
VSC	Enable / disable short-circuit protection (0 = Disabled, 1 = 7.5V minimum)

FIGURE 34. DESCRIPTIONS OF CONFIGURATION REGISTER

REGISTER 0x09	OUTPUT CHANNEL REGISTER

RESERVED	RESERVED	CH5	CH4	CH3	CH2	CH1	CH0
Bit 7 (R/W)	Bit 6 (R/W)	Bit 5 (R/W)	Bit 4 (R/W)	Bit 3 (R/W)	Bit 2 (R/W)	Bit 1 (R/W)	Bit 0 (R/W)

BIT ASSIGNMENT	BIT FIELD DEFINITIONS
CH[5..0]	CH5 = Channel 5, CH4 = Channel 4 and so on

FIGURE 35. OUTPUT CHANNEL REGISTER

REGISTER 0x0A	PHASE SHIFT CONTROL REGISTER

EQUALPHASE	PHASESHIFT6	PHASESHIFT5	PHASESHIFT4	PHASESHIFT3	PHASESHIFT2	PHASESHIFT1	PHASESHIFT0
Bit 7 (R/W)	Bit 6 (R/W)	Bit 5 (R/W)	Bit 4 (R/W)	Bit 3 (R/W)	Bit 2 (R/W)	Bit 1 (R/W)	Bit 0 (R/W)

BIT ASSIGNMENT	BIT FIELD DEFINITIONS
EqualPhase	Controls phase shift mode - When 0, phase shift is defined by PhaseShift<6:0>. When 1, phase shift is 360/N (where N is the number of channels enabled).
PhaseShift[6..0]	7-bit Phase shift setting - phase shift between each channel is PhaseShift<6:0>/(255*PWMFreq)

FIGURE 36. DESCRIPTIONS OF PHASE SHIFT CONTROL REGISTER

Phase Shift Control Register (0x0A)

The Phase Shift Control register sets phase delay between channels. When Bit 7 is set high, the phase delay is set by the number of channels enabled and the PWM frequency. Referring to Figure 3 on page 8, the delay time is defined by Equation 16:

$$t_{D1} = (t_{FPWM}/N) \quad \text{(EQ. 16)}$$

where N is the number of channels enabled, and t_{FPWM} is the period of the PWM cycle. When Bit 7 is set low, the phase delay is set by Bits 6:0 and the PWM frequency. Referencing Figure 23, the programmable delay time is defined by Equation 17:

$$t_{PD} = (PS<6,0>xt_{FPWM}/(255)) \quad \text{(EQ. 17)}$$

where PS is an integer from 0 to 127, and t_{FPWM} is the period of the PWM cycle. By default, all the register bits are set low, which sets zero delay between each channel.

Note: Do not program the register to have more than one period of the PWM cycle delay between the first and last enabled channels.

Component Selections

According to the inductor Voltage-Second Balance principle, the change of inductor current during the switching regulator On time is equal to the change of inductor current during the switching regulator Off time. As shown in Equations 18 and 19, since the voltage across an inductor is:

$$\Delta I_L = \frac{V_L}{L} x \Delta t \quad \text{(EQ. 18)}$$

and ΔI_L at On = ΔI_L at Off, therefore:

$$(V_I - 0)/L \times D \times t_S = (V_O - V_D - V_I)/L \times (1 - D) \times t_S \quad \text{(EQ. 19)}$$

where D is the switching duty cycle defined by the turn-on time over the switching period. V_D is a Schottky diode forward voltage that can be neglected for approximation.

Rearranging the terms without accounting for V_D gives the boost ratio and duty cycle, respectively, as shown in Equations 20 and 21:

$$V_O/V_I = 1/(1 - D) \quad \text{(EQ. 20)}$$

$$D = (V_O - V_I)/V_O \quad \text{(EQ. 21)}$$

Input Capacitor

Switching regulators require input capacitors to deliver peak charging current and to reduce the impedance of the input supply. The capacitors reduce interaction between the regulator and input supply, thus improving system stability. The high switching frequency of the loop causes almost all ripple current to flow into the input capacitor, which must be rated accordingly.

A capacitor with low internal series resistance should be chosen to minimize heating effects and to improve system efficiency. The X5R and X7R ceramic capacitors offer small size and a lower value for temperature and voltage coefficient compared to other ceramic capacitors.

An input capacitor of 10µF is recommended. Ensure that the voltage rating of the input capacitor is able to handle the full supply range.

Inductor

Inductor selection should be based on its maximum current (I_{SAT}) characteristics, power dissipation (DCR), EMI susceptibility (shielded vs unshielded), and size. Inductor type and value influence many key parameters, including ripple current, current limit, efficiency, transient performance, and stability.

Inductor maximum current capability must be adequate to handle the peak current in the worst-case condition. If an inductor core with too low a current rating is chosen, saturation in the core will cause the effective inductor value to fall, leading to an increase in peak-to-average current level, poor efficiency, and overheating in the core. The series resistance, DCR, within the inductor causes conduction loss and heat dissipation. A shielded inductor is usually more suitable for EMI-susceptible applications such as LED backlighting.

The peak current can be derived from the voltage across the inductor during the Off period, as shown in Equation 22:

$$IL_{peak} = (V_O \times I_O)/(85\% \times V_I) + 1/2[V_I \times (V_O - V_I)/(L \times V_O \times f_S)] \quad \text{(EQ. 22)}$$

The value of 85% is an average term for the efficiency approximation. The first term is average current that is inversely proportional to the input voltage. The second term is inductor current change that is inversely proportional to L and f_S. As a result, for a given switching frequency and minimum input voltage at which the system operates, the inductor I_{SAT} must be chosen carefully.

Output Capacitors

The output capacitor smooths the output voltage and supplies load current directly during the conduction phase of the power switch. Output ripple voltage consists of discharge and charge of the output capacitor during FET On and OFF time and the voltage drop due to flow through the ESR of the output capacitor. The ripple voltage can be shown as Equation 23:

$$\Delta V_{C_O} = (I_O / C_O \times D / f_S) + (I_O \times ESR) \quad \text{(EQ. 23)}$$

The conservation of charge principle shown in Equation 21 also indicates that, during the boost switch Off period, the output capacitor is charged with the inductor ripple current, minus a relatively small output current in boost topology. As a result, the user must select an output capacitor with low ESR and adequate input ripple current capability.

Note: Capacitors have a voltage coefficient that makes their effective capacitance drop as the voltage across them increases. C_O in Equation 23 assumes the effective value of the capacitor at a particular voltage and not the manufacturer's stated value, measured at 0V.

The value of ΔVC_O can be reduced by increasing C_O or f_S, or by using small ESR capacitors. In general, ceramic capacitors are the best choice for output capacitors in small- to medium-sized LCD backlight applications, due to their cost, form factor, and low ESR.

A larger output capacitor also eases driver response during the PWM dimming Off period, due to the longer sample and hold effect of the output drooping. The driver does not need to boost harder in the next On period that minimizes transient current.

The output capacitor is also needed for compensation, and in general, 2x4.7µF/50V ceramic capacitors are suitable for notebook display backlight applications.

Output Ripple

ΔVC_O can be reduced by increasing C_O or f_{SW}, or by using small ESR capacitors. In general, ceramic capacitors are the best choice for output capacitors in small to medium sized LCD backlight applications due to their cost, form factor, and low ESR.

A larger output capacitor will also ease the driver response during PWM dimming Off period due to the longer sample and hold effect of the output drooping. The driver does not need to boost harder in the next On period that minimizes transient current. The output capacitor is also needed for compensation, and, in general 2x4.7µF/50V ceramic capacitors are suitable for notebook display backlight applications.

Schottky Diode

A high-speed rectifier diode is necessary to prevent excessive voltage overshoot. Schottky diodes are recommended because of their fast recovery time, low forward voltage, and reverse leakage current, which minimize losses. The reverse voltage rating of the selected Schottky diode must be higher than the maximum output voltage. Additionally, the average/peak current rating of the Schottky diode must meet the output current and peak inductor current requirements.

Applications

High-Current Applications

Each channel of the ISL97671A can support up to 30mA (50mA at V_{IN} = 12V). For applications that need higher current, multiple channels can be grouped to achieve the desired current (Figure 37). For example, the cathode of the last LED can be connected to CH0 through CH2; this configuration can be treated as a single string with 90mA current driving capability.

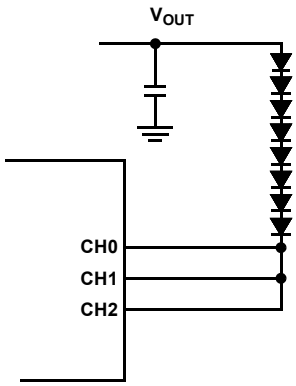


FIGURE 37. GANGING MULTIPLE CHANNELS FOR HIGH CURRENT APPLICATIONS

Low Voltage Operations

The ISL97671A VIN pin can be separately biased from the LED power input to allow low-voltage operation.

In systems that have only a single supply, VOUT can be tied to the driver VIN pin to allow initial start-up (Figure 38). The circuit works as follows: when the input voltage is available and the device is not enabled, V_{OUT} follows V_{IN} with a Schottky diode voltage drop. The V_{OUT} boot-strapped to the VIN pin allows initial start-up, once the part is enabled. Once the driver starts up with V_{OUT} regulating to the target, the VIN pin voltage also increases. As long as V_{OUT} does not exceed 26.5V and the extra power loss on V_{IN} is acceptable, this configuration can be used for input voltage as low as 3.0V. The Fault Protection FET feature cannot be used in this configuration.

In systems that have dual supplies, the VIN pin can be biased from 5V to 12V, while input voltage can be as low as 2.7V (Figure 39). In this configuration, VBIAS must be greater than or equal to VIN to use the fault FET.

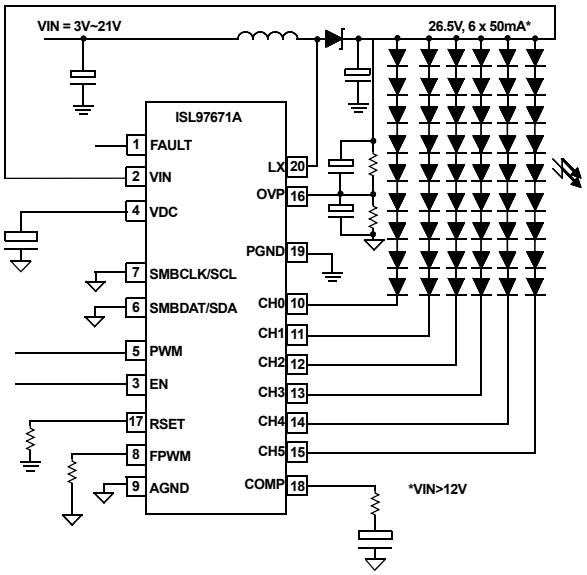


FIGURE 38. SINGLE SUPPLY 3V OPERATION

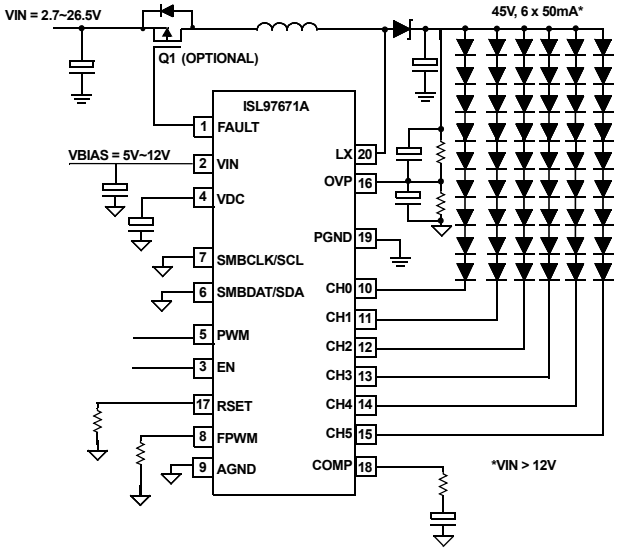


FIGURE 39. DUAL SUPPLIES 2.7V OPERATION

16-Bit Dimming

The SMBus/I^{2}C controlled PWM and DC dimmings can be combined to effectively provide 16 bits of dimming capability, which can be valuable for automotive and avionics display applications.

Field Sequential RGB LED Backlighting

The ISL97671A is able to turn each channel ON and OFF independently. In field sequential RGB LED application, it is possible to have different DC current and PWM duty cycle for different channels as long as only one channel is active at a time. This is achieved by continuously setting a new DC current and/or PWM duty cycle each time a channel is turned ON. The ISL97671A does not allow different DC currents or PWM duty cycles for channels that are ON at the same time.

Compensation

The ISL97671A incorporates a transconductance amplifier in its feedback path to allow the user to optimize boost stability and transient response. The ISL97671A uses current mode control architecture, which has a fast current sense loop and a slow voltage feedback loop. The fast current feedback loop does not require any compensation, but for stable operation, the slow voltage loop must be compensated. The compensation is a series of Rc, Cc1 network from COMP pin to ground, with an optional Cc2 capacitor connected between the COMP pin and ground. The Rc sets the high-frequency integrator gain for fast transient response, and the Cc1 sets the integrator zero to ensure loop stability. For most applications, the component values in Figure 40 can be used: Rc is 10kΩ and Cc1 is 3.3nF. Depending upon the PCB layout, for stability, a Cc2 of 390pF may be needed to create a pole to cancel the output capacitor ESR's zero effect.

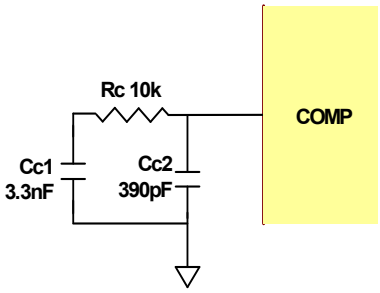


FIGURE 40. COMPENSATION CIRCUIT

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
September 14, 2017	FN7709.4	Added Related Literature section. Added $V_{HEADROOM\_RANGE}$ spec to EC table on page 6. Fixed parentheses in Equation 23. Fixed Bit Field Definitions for Bit FSW in Figure 34. Fixed FSW frequencies in Table 3B.
October 3, 2012	FN7709.3	Minor changes to improve the wording of various sections. page 5 - Thermal Information, removed Pb-Free Reflow Profile link. page 6- V_{OVPlo} in the spec table, changed to Min 1.199 and Max 1.24 from Min 1.19 and Max 1.24 page 8 - Figure 3 “EFFICIENCY vs up to 20mA LED CURRENT (100% LED DUTY CYCLE) vs VIN” removed. page 9 - Figures 11, 12 replaced to clear waveforms page 12 & page 16 respectively, Tables 1, 2 improved. page 18 - I^2C section, specified that the backlight can turns on when SDA/SCL are connected to ground. page 20 - Improved description of PWM_MD and PWM_SEL I^2C register bits. Corrected Figure 30. Removed Direct PWM and PWM-to-DC register bits from the description
July 11, 2012	FN7709.2	PWM-to-DC bit and BstSlewRate bit in the register 0x08 updated on page 19, page 22 and page 23. In “Current Matching and Current Accuracy” on page 11, changed 401.8 to 410.5. On page 11 Equation 1, changed 401.8 to 410.5.
March 24, 2011	FN7709.1	Initial Release to web.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing, and high-end consumer markets.

For the most updated datasheet, application notes, related documentation, and related parts, see the respective product information page found at www.intersil.com.

For a listing of definitions and abbreviations of common terms used in our documents, visit www.intersil.com/glossary.

You can report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support.

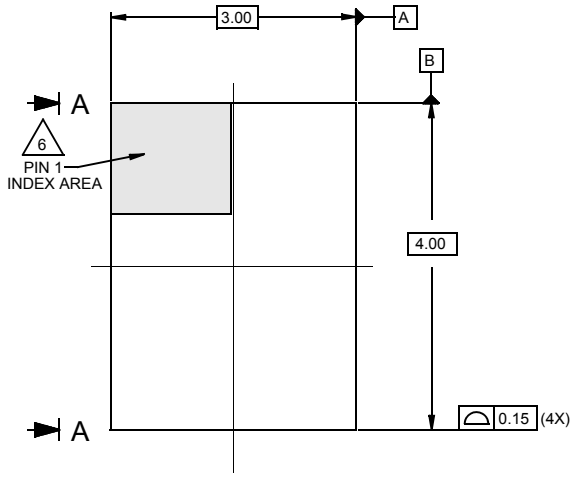
Package Outline Drawing

For the most recent package outline drawing, see L20.3x4.

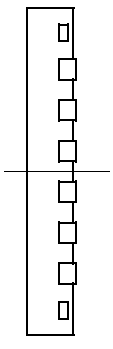
L20.3x4

20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

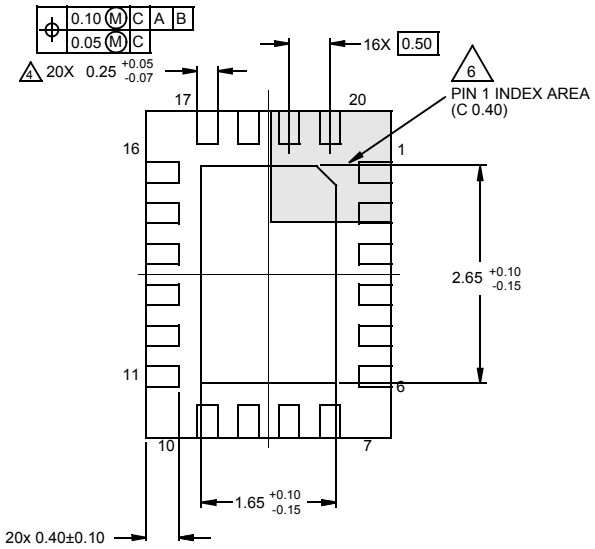
Rev 1, 3/10



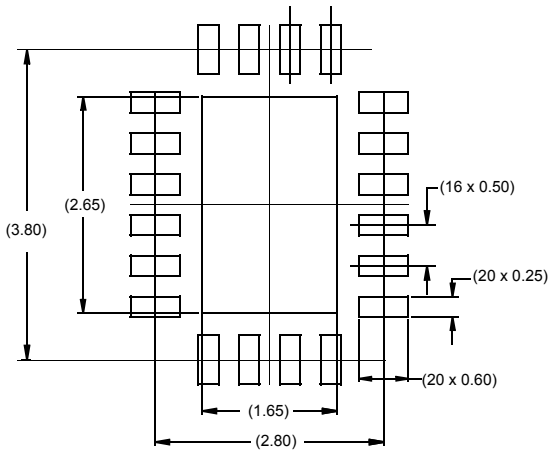
TOP VIEW



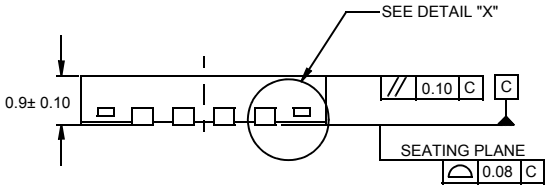
VIEW "A-A"



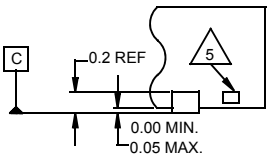
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.