Document Number: A2I25H060N
Rev. 0, 1/2016

RoHS

RF LDMOS Wideband Integrated Power Amplifiers

A2I25H060NR1
A2I25H060GNR1

2300–2690 MHz, 10.5 W AVG., 28 V AIRFAST RF LDMOS WIDEBAND INTEGRATED POWER AMPLIFIERS

The A2I25H060N wideband integrated circuit is an asymmetrical Doherty designed with on-chip matching that makes it usable from 2300 to 2690 MHz. This multi-stage structure is rated for 20 to 32 V operation and covers all typical cellular base station modulation formats.

2600 MHz

- Typical Doherty Single-Carrier W-CDMA Characterization Performance: V_{DD} = 28 Vdc, I_{DQ1A} = 26 mA, I_{DQ2A} = 163 mA, V_{GS1B} = 1.7 Vdc, V_{GS2B} = 1.3 Vdc, P_{out} = 10.5 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.(1)

Frequency	G_{ps} (dB)	PAE (%)	ACPR (dBc)
2496 MHz	27.1	40.9	–31.5
2590 MHz	27.5	40.9	–34.0
2690 MHz	27.1	39.4	–34.7

2300 MHz

- Typical Doherty Single-Carrier W-CDMA Performance: V_{DD} = 28 Vdc, I_{DQ1A} = 28 mA, I_{DQ2A} = 177 mA, V_{GS1B} = 1.8 Vdc, V_{GS2B} = 1.3 Vdc, P_{out} = 10.5 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.(1)

Frequency	G_{ps} (dB)	PAE (%)	ACPR (dBc)
2300 MHz	26.7	38.9	–33.7
2350 MHz	27.0	38.9	–34.8
2400 MHz	27.1	39.0	–34.7

TO-270WB-17
PLASTIC
A2I25H060NR1

TO-270WBG-17
PLASTIC
A2I25H060GNR1

Features

- Advanced High Performance In-Package Doherty
- On-Chip Matching (50 Ohm Input, DC Blocked)
- Integrated Quiescent Current Temperature Compensation with Enable/Disable Function (2)
- Designed for Digital Predistortion Error Correction Systems

1. All data measured in fixture with device soldered to heatsink.
2. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.nxp.com/RF and search for AN1977 or AN1987.

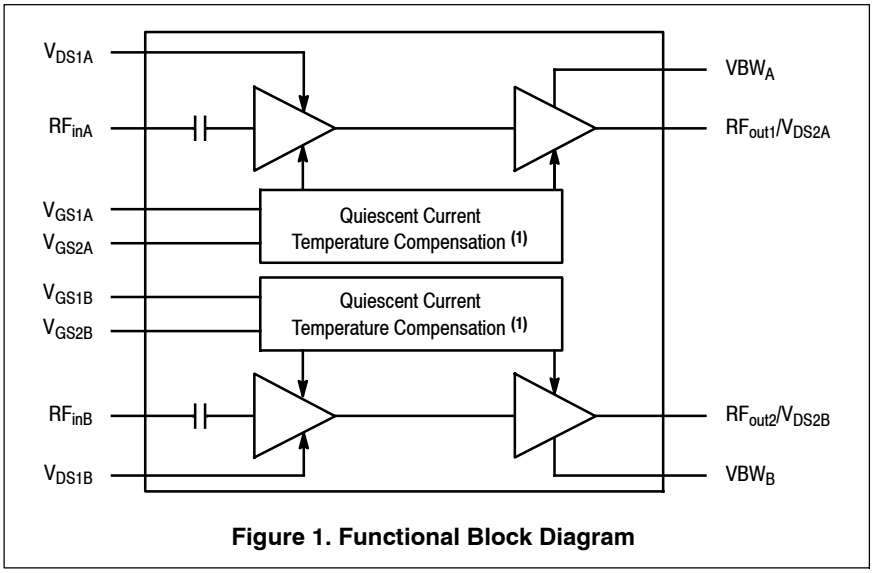
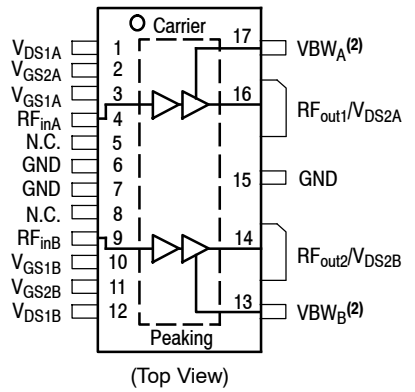


Figure 1. Functional Block Diagram



(Top View)

Note: Exposed backside of the package is the source terminal for the transistors.

Figure 2. Pin Connections

1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.nxp.com/RF and search for AN1977 or AN1987.
2. Device can operate with V_{DD} current supplied through pin 13 and pin 17.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	–0.5, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range (3,4)	T_J	–40 to +225	°C
Input Power	P_{in}	22	dBm

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (4,5)	Unit
Thermal Resistance, Junction to Case Case Temperature 77°C, 10.5 W Avg., 2590 MHz Stage 1, 28 Vdc, I_{DQ1A} = 30 mA, V_{G1A} = 3.5 Vdc, V_{G1B} = 1.7 Vdc Stage 2, 28 Vdc, I_{DQ2A} = 190 mA, V_{G2A} = 3.65 Vdc, V_{G2B} = 1.3 Vdc	$R_{\theta JC}$	 5.6 2.2	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1B
Machine Model (per EIA/JESD22-A115)	A
Charge Device Model (per JESD22-C101)	II

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

3. Continuous use at maximum temperature will affect MTTF.
4. MTTF calculator available at http://www.nxp.com/RF/calculators.
5. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Carrier Stage 1 – Off Characteristics (1)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 1.0 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Carrier Stage 1 – On Characteristics					
Gate Threshold Voltage (1) (V_{DS} = 10 Vdc, I_D = 4 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_{DQ1A} = 26 mAdc)	$V_{GS(Q)}$	—	2.0	—	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_{DQ1A} = 26 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	2.9	3.5	4.4	Vdc
Carrier Stage 2 – Off Characteristics (1)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 1.0 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Carrier Stage 2 – On Characteristics					
Gate Threshold Voltage (1) (V_{DS} = 10 Vdc, I_D = 26 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_{DQ2A} = 174 mAdc)	$V_{GS(Q)}$	—	1.7	—	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_{DQ2A} = 174 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	2.9	3.6	4.4	Vdc
Drain–Source On–Voltage (1) (V_{GS} = 10 Vdc, I_D = 350 mAdc)	$V_{DS(on)}$	0.1	0.22	1.5	Vdc

1. Each side of device measured separately.

(continued)

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Peaking Stage 1 – Off Characteristics (1)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 1.0 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Peaking Stage 1 – On Characteristics (1)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 8 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Peaking Stage 2 – Off Characteristics (1)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 1.0 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Peaking Stage 2 – On Characteristics (1)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 42 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 565 mAdc)	$V_{DS(on)}$	0.1	0.22	1.5	Vdc

1. Each side of device measured separately.

(continued)

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests [1,2,3] (In Freescale Doherty Production Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1A} = 26 mA, I_{DQ2A} = 174 mA, V_{GS1B} = 1.7 Vdc, V_{GS2B} = 1.3 Vdc, P_{out} = 10.5 W Avg., f = 2590 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	24.6	26.1	28.0	dB
Power Added Efficiency	PAE	37.5	40.4	—	%
Adjacent Channel Power Ratio	ACPR	—	–31.6	–28.0	dBc
P_{out} @ 3 dB Compression Point	P3dB	38.9	48.2	—	W
Load Mismatch [2] (In Freescale Doherty Production Test Fixture, 50 ohm system) I_{DQ1A} = 26 mA, I_{DQ2A} = 174 mA, V_{GS1B} = 1.7 Vdc, V_{GS2B} = 1.3 Vdc, f = 2590 MHz					
VSWR 10:1 at 32 Vdc, 55 W CW Output Power (3 dB Input Overdrive from 36 W CW Rated Power)	No Device Degradation				
Typical Performance [2] (In Freescale Doherty Characterization Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1A} = 26 mA, I_{DQ2A} = 163 mA, V_{GS1B} = 1.7 Vdc, V_{GS2B} = 1.3 Vdc, 2496–2690 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	52	—	W
P_{out} @ 3 dB Compression Point [4]	P3dB	—	57	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 2496–2690 MHz frequency range.)	Φ	—	–27.2	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	180	—	MHz
Quiescent Current Accuracy over Temperature [5] with 2 kΩ Gate Feed Resistors (–30 to 85°C) Stage 1 with 2 kΩ Gate Feed Resistors (–30 to 85°C) Stage 2	ΔI_{QT}	 — —	 4.76 2.33	 — —	%
Gain Flatness in 194 MHz Bandwidth @ P_{out} = 10.5 W Avg.	G_F	—	0.312	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.030	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C)	ΔP1dB	—	0.006	—	dB/°C

Table 6. Ordering Information

Device	Tape and Reel Information	Package
A2I25H060NR1	R1 Suffix = 500 Units, 44 mm Tape Width, 13-inch Reel	TO-270WB-17
A2I25H060GNR1		TO-270WBG-17

1. Part internally matched both on input and output.
2. Measurements made with device in an asymmetrical Doherty configuration.
3. Measurements made with device in straight lead configuration before any lead forming operation is applied. Lead forming is used for gull wing (GN) parts.
4. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.
5. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.nxp.com/RF and search for AN1977 or AN1987.

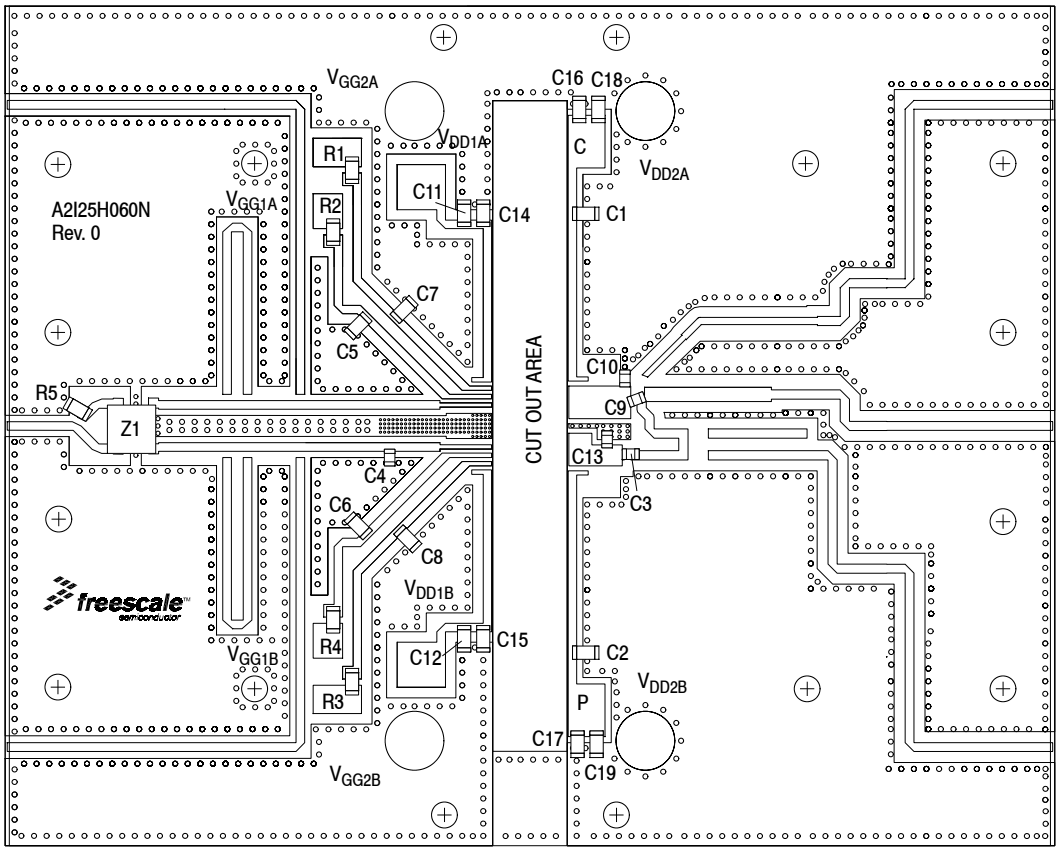
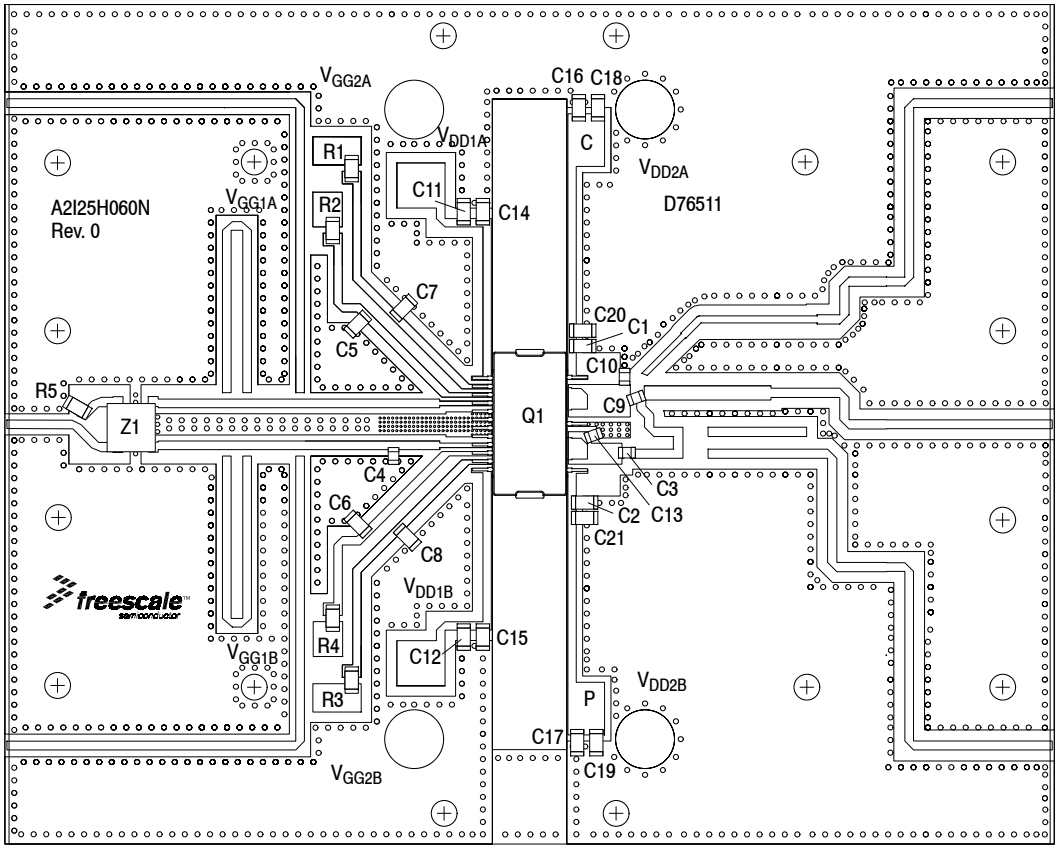


Figure 3. A2I25H060NR1 Production Test Circuit Component Layout

Table 7. A2I25H060NR1 Production Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C3	6.8 pF Chip Capacitors	ATC600F6R8BT250XT	ATC
C4	1.2 pF Chip Capacitor	ATC600F1R2BT250XT	ATC
C5, C6, C7, C8, C16, C17	4.7 μF Chip Capacitors	GRM31CR71H475KA12L	Murata
C9	4.7 pF Chip Capacitor	ATC600F4R7BT250XT	ATC
C10	0.2 pF Chip Capacitor	ATC600F0R2BT250XT	ATC
C11, C12, C18, C19	10 μF Chip Capacitors	GRM31CR61H106KA12L	Murata
C13	1 pF Chip Capacitor	ATC600F1R0BT250XT	ATC
C14, C15	1 μF Chip Capacitors	GRM31MR71H105KA88L	Murata
R1, R2, R3, R4	2 kΩ, 1/4 W Chip Resistors	SG73P2ATTD2001F	KOA Speer
R5	50 Ω, 10 W Termination	RFP-060120A25Z50-2	Anaren
Z1	2300–2700 MHz Band, 90°, 2 dB Hybrid Coupler	CMX25Q02	RN2 Technologies
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	—	MTL



Note: All data measured in fixture with device soldered to heatsink.

Figure 4. A2I25H060NR1 Characterization Test Circuit Component Layout

Table 8. A2I25H060NR1 Characterization Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C5, C6, C7, C8, C16, C17	4.7 μF Chip Capacitors	GRM31CR71H475KA12L	Murata
C3	6.8 pF Chip Capacitor	ATC600F6R8BT250XT	ATC
C4	1.2 pF Chip Capacitor	ATC600F1R2BT250XT	ATC
C9	3.6 pF Chip Capacitor	ATC600F3R6BT250XT	ATC
C10	0.2 pF Chip Capacitor	ATC600F0R2BT250XT	ATC
C11, C12, C18, C19, C20, C21	10 μF Chip Capacitors	GRM31CR61H106KA12L	Murata
C13	1.5 pF Chip Capacitor	ATC600F1R5BT250XT	ATC
C14, C15	1 μF Chip Capacitors	GRM31MR71H105KA88L	Murata
Q1	RF LDMOS Power Amplifier	A2I25H060NR1	Freescale
R1, R2, R3, R4	2 kΩ, 1/4 W Chip Resistors	SG73P2ATTD2001F	KOA Speer
R5	50 Ω, 10 W Termination	RFP-060120A25Z50-2	Anaren
Z1	2300–2700 MHz Band, 90°, 2 dB Hybrid Coupler	CMX25Q02	RN2 Technologies
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D76511	MTL

TYPICAL CHARACTERISTICS

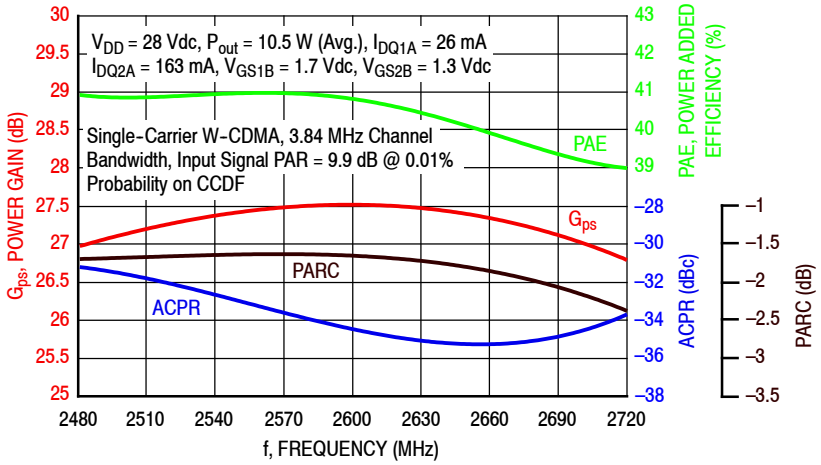


Figure 5. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 10.5 Watts Avg.

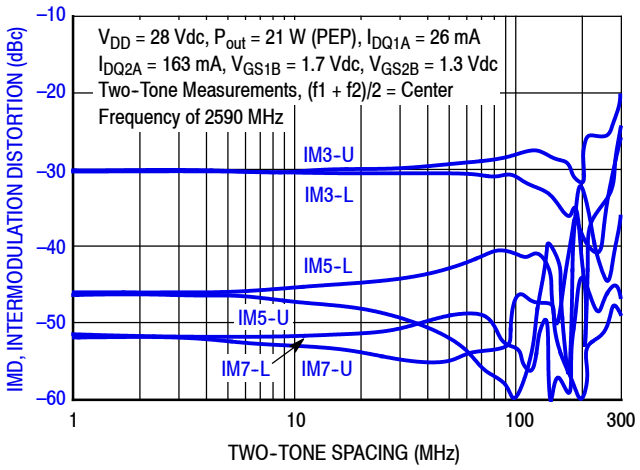


Figure 6. Intermodulation Distortion Products versus Two-Tone Spacing

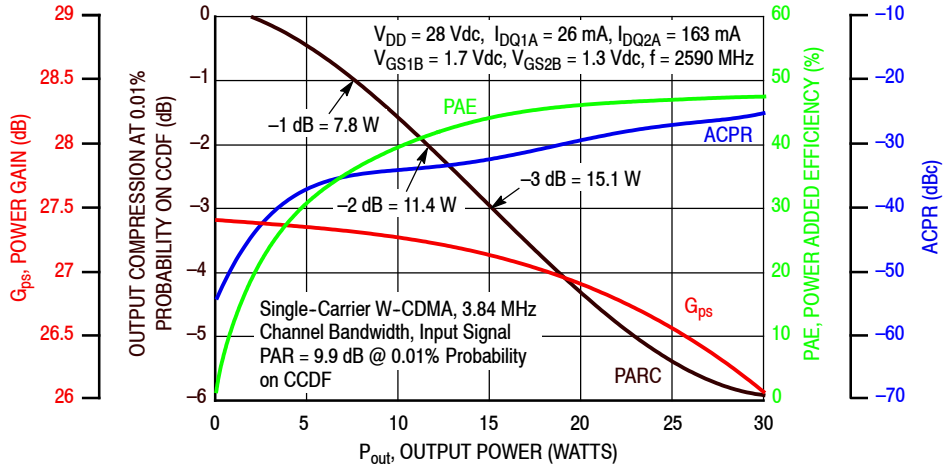


Figure 7. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS

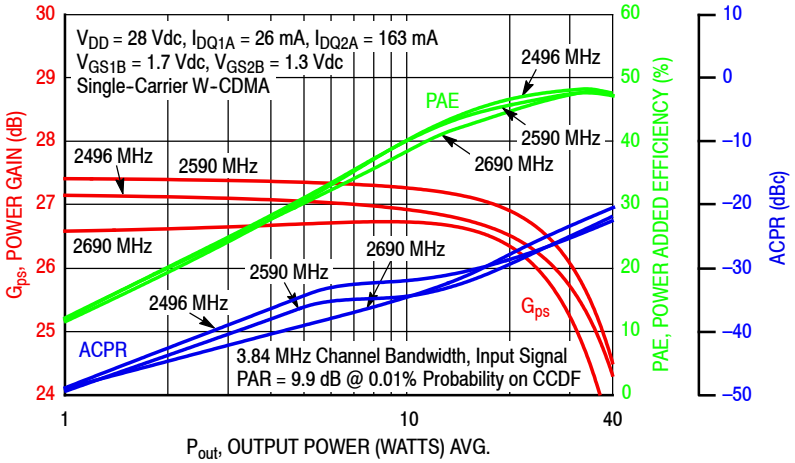


Figure 8. Single-Carrier W-CDMA Power Gain, Power Added Efficiency and ACPR versus Output Power

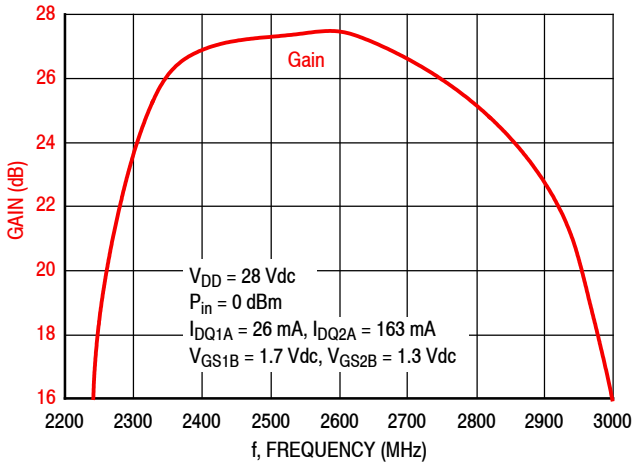


Figure 9. Broadband Frequency Response

Table 9. Carrier Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQ1A} = 28 mA, I_{DQ1B} = 182 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	60.5 – j0.96	57.6 + j1.40	10.6 – j11.1	31.9	44.5	28	53.1	–6
2590	61.5 + j10.9	57.1 – j8.84	9.99 – j10.6	32.0	44.5	28	54.9	–8
2690	60.1 + j18.7	57.9 – j11.6	8.28 – j10.5	31.6	44.1	26	52.8	–9

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	60.5 – j0.96	55.6 – j1.26	10.4 – j11.5	29.8	45.4	35	55.0	–10
2590	61.5 + j10.9	53.7 – j8.80	9.79 – j11.2	29.8	45.4	35	56.1	–14
2690	60.1 + j18.7	54.8 – j8.94	8.61 – j11.3	29.5	45.0	32	54.9	–17

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 10. Carrier Side Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 28 Vdc, I_{DQ1A} = 28 mA, I_{DQ1B} = 182 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	60.5 – j0.96	60.8 + j0.12	15.3 – j5.12	32.8	43.5	22	59.1	–8
2590	61.5 + j10.9	59.4 – j12.2	12.3 – j3.64	33.0	43.2	21	60.4	–9
2690	60.1 + j18.7	57.9 – j16.6	9.70 – j5.83	32.7	43.3	21	59.0	–9

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	60.5 – j0.96	58.6 – j1.83	14.7 – j5.71	30.8	44.5	28	60.0	–10
2590	61.5 + j10.9	56.0 – j11.9	12.1 – j4.46	30.9	44.3	27	61.5	–14
2690	60.1 + j18.7	54.7 – j14.0	9.51 – j5.64	30.7	44.1	26	60.4	–17

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

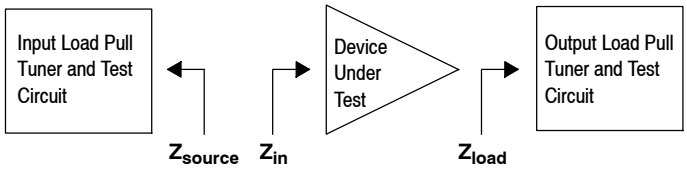


Table 11. Peaking Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, V_{GSA} = 1.0 Vdc, V_{GSB} = 1.0 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	57.3 – j1.04	47.3 – j5.57	4.76 – j7.37	23.1	47.5	57	56.2	–32
2590	61.1 + j16.3	48.1 – j12.9	4.63 – j7.34	23.5	47.5	56	57.0	–38
2690	61.5 + j21.7	52.7 – j10.3	4.21 – j7.51	23.4	47.1	52	57.6	–43

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	57.3 – j1.04	42.5 – j5.20	4.68 – j7.45	21.0	47.8	60	55.0	–44
2590	61.1 + j16.3	44.6 – j8.75	4.63 – j7.51	21.4	47.7	59	56.1	–50
2690	61.5 + j21.7	52.2 – j4.81	4.14 – j7.58	21.3	47.3	54	57.0	–54

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

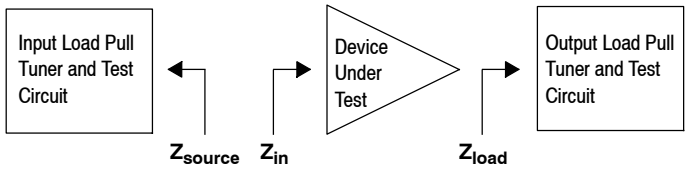
Table 12. Peaking Side Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 28 Vdc, V_{GSA} = 1.0 Vdc, V_{GSB} = 1.0 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	57.3 – j1.04	51.2 – j5.71	7.34 – j4.47	23.0	46.6	45	61.3	–35
2590	61.1 + j16.3	50.6 – j15.7	6.35 – j5.05	23.6	46.8	47	62.0	–39
2690	61.5 + j21.7	52.3 – j15.2	5.07 – j4.95	23.4	46.2	42	62.8	–46

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	57.3 – j1.04	44.4 – j6.29	6.93 – j5.75	21.1	47.2	53	59.3	–47
2590	61.1 + j16.3	45.6 – j11.3	6.12 – j4.93	21.5	47.0	50	60.5	–55
2690	61.5 + j21.7	51.0 – j7.68	5.07 – j5.45	21.4	46.6	46	61.3	–60

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB – TYPICAL CARRIER LOAD PULL CONTOURS — 2590 MHz

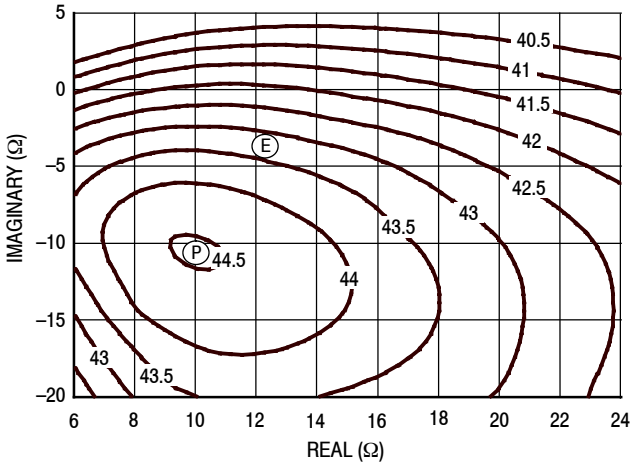


Figure 10. P1dB Load Pull Output Power Contours (dBm)

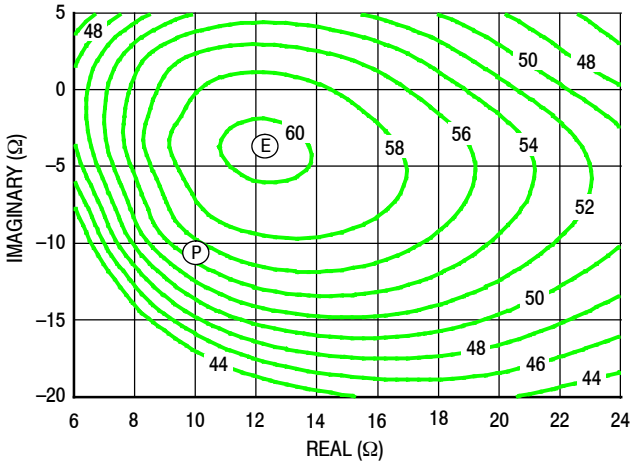


Figure 11. P1dB Load Pull Efficiency Contours (%)

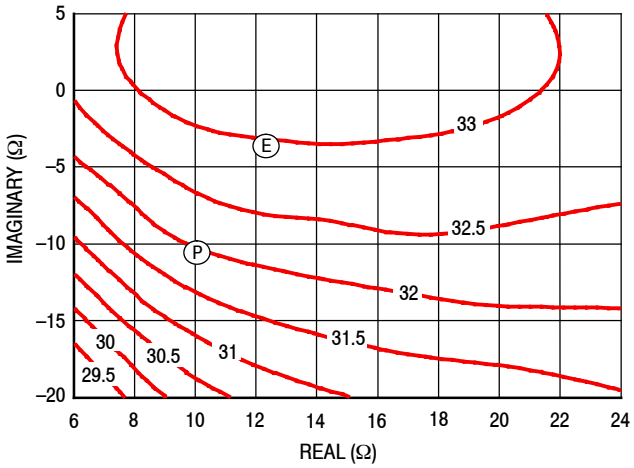


Figure 12. P1dB Load Pull Gain Contours (dB)

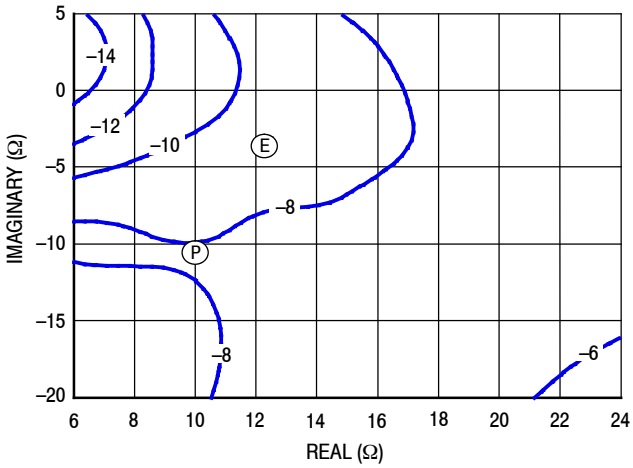


Figure 13. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL CARRIER LOAD PULL CONTOURS — 2590 MHz

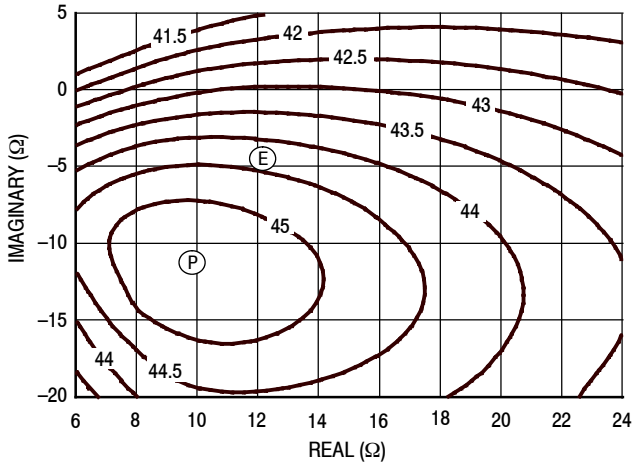


Figure 14. P3dB Load Pull Output Power Contours (dBm)

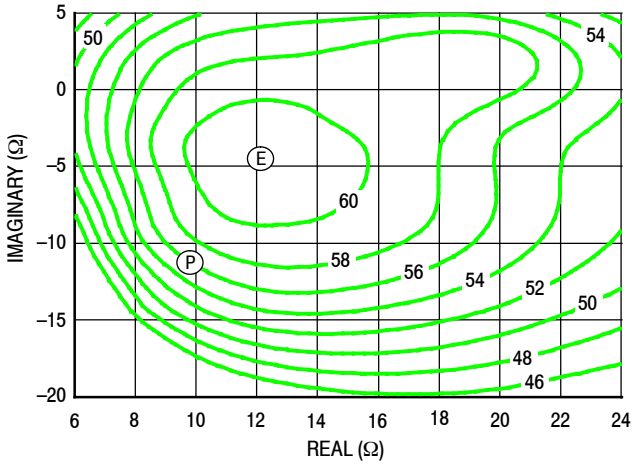


Figure 15. P3dB Load Pull Efficiency Contours (%)

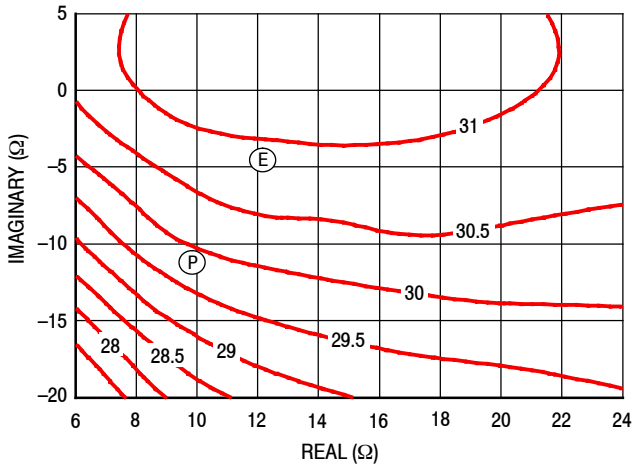


Figure 16. P3dB Load Pull Gain Contours (dB)

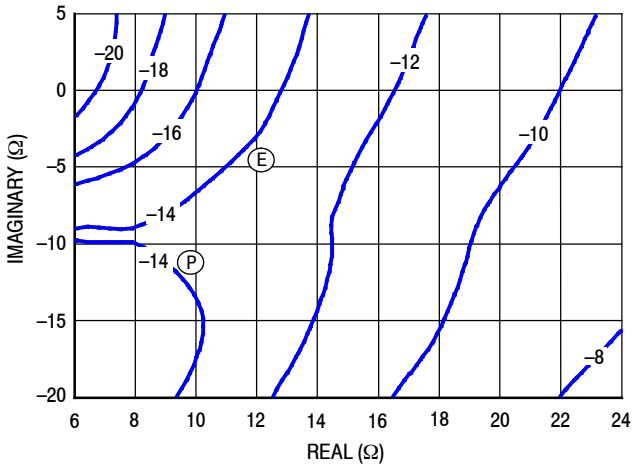


Figure 17. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power
Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

P1dB – TYPICAL PEAKING LOAD PULL CONTOURS — 2590 MHz

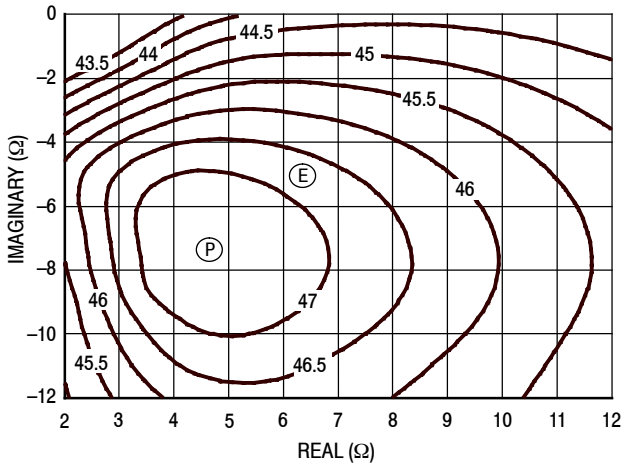


Figure 18. P1dB Load Pull Output Power Contours (dBm)

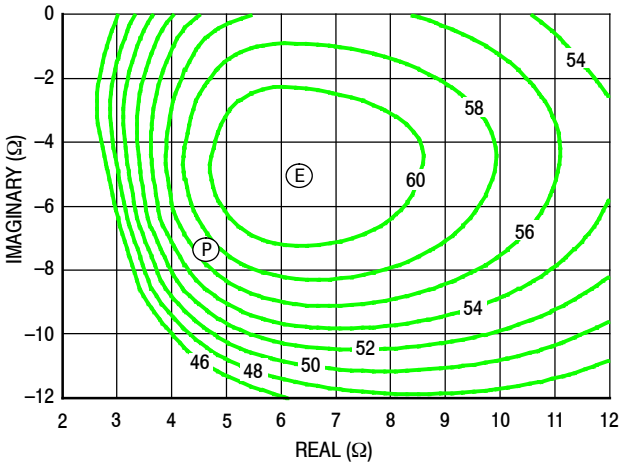


Figure 19. P1dB Load Pull Efficiency Contours (%)

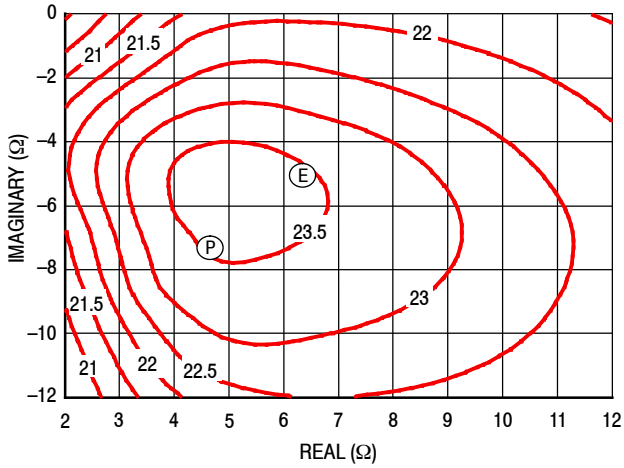


Figure 20. P1dB Load Pull Gain Contours (dB)

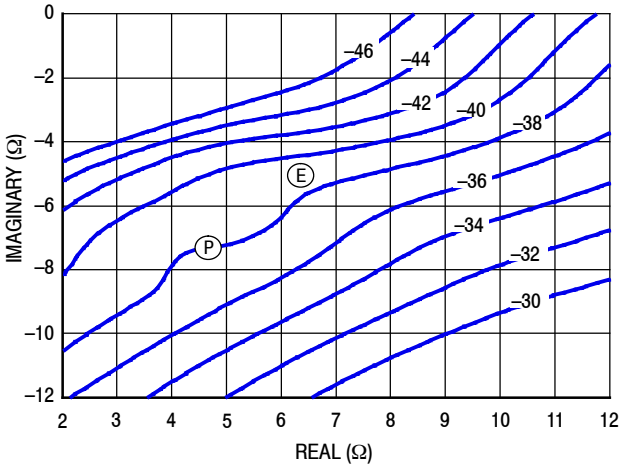


Figure 21. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL PEAKING LOAD PULL CONTOURS — 2590 MHz

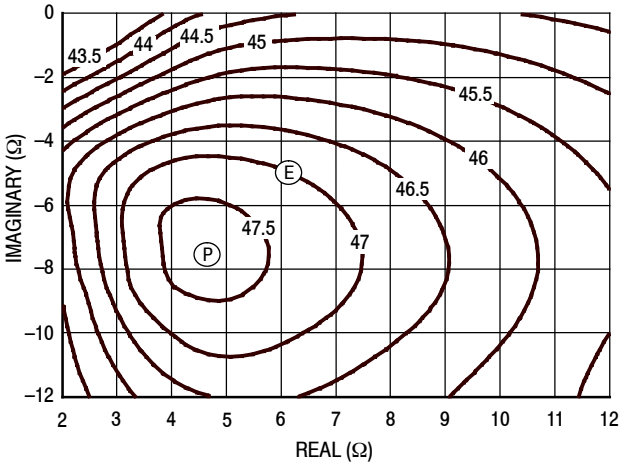


Figure 22. P3dB Load Pull Output Power Contours (dBm)

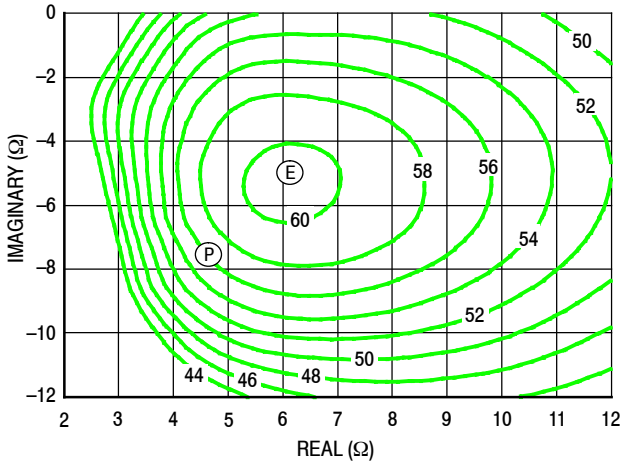


Figure 23. P3dB Load Pull Efficiency Contours (%)

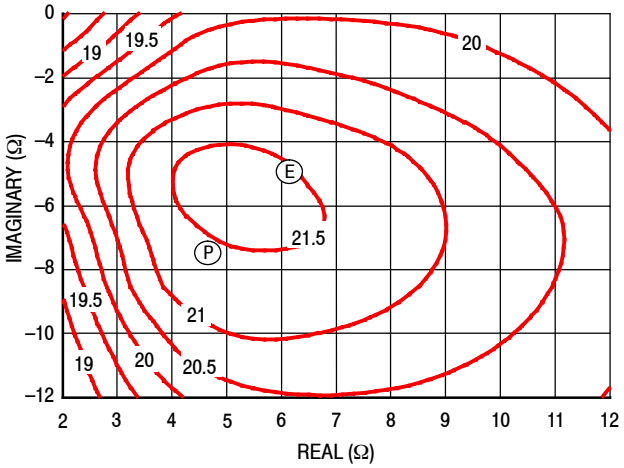


Figure 24. P3dB Load Pull Gain Contours (dB)

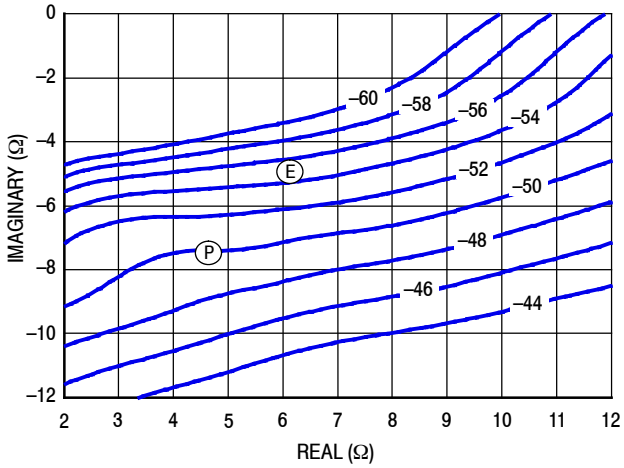


Figure 25. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

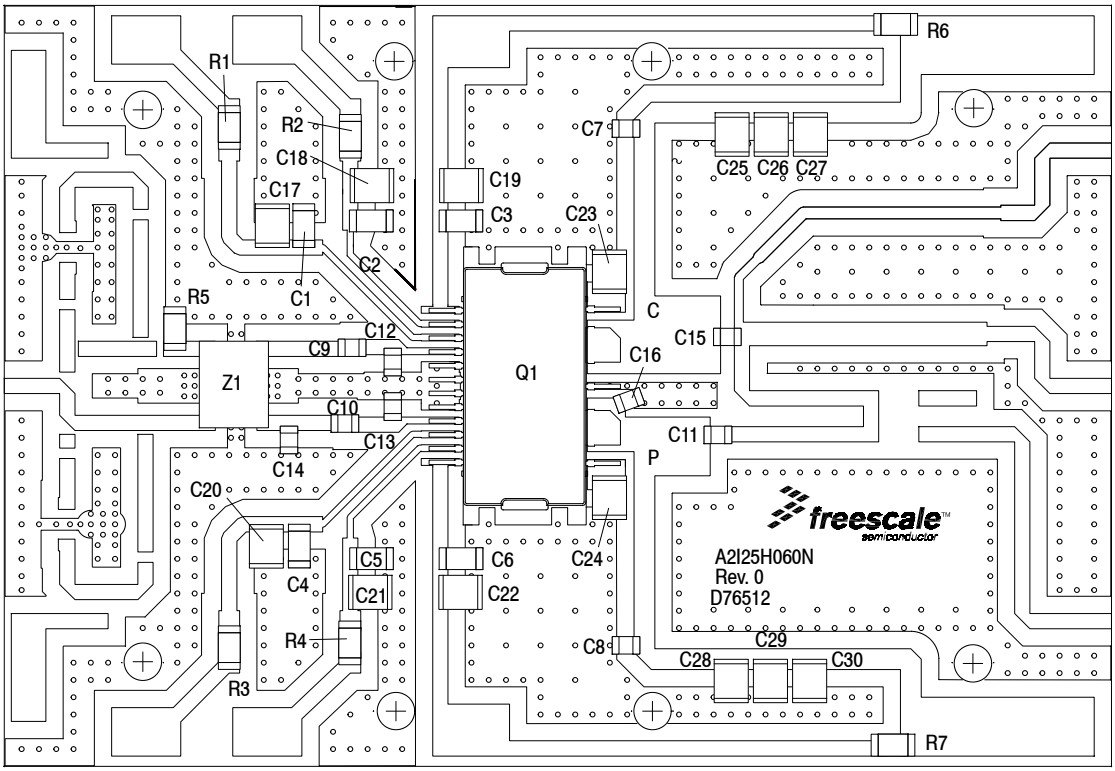
Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power



Note: All data measured in fixture with device soldered to heatsink.

Figure 26. A2I25H060NR1 Test Circuit Component Layout —2300–2400 MHz

Table 13. A2I25H060NR1 Test Circuit Component Designations and Values —2300–2400 MHz

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11	8.2 pF Chip Capacitors	ATC600F8R2BT250XT	ATC
C12, C13	0.5 pF Chip Capacitors	ATC600F0R5BT250XT	ATC
C14	0.3 pF Chip Capacitor	ATC600F0R3BT250XT	ATC
C15	12 pF Chip Capacitor	ATC600F12R0BT250XT	ATC
C16	1.5 pF Chip Capacitor	ATC600F1R5BT250XT	ATC
C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30	10 μF Chip Capacitors	GRM32ER61H106KA12L	Murata
Q1	RF LDMOS Power Amplifier	A2I25H060NR1	Freescale
R1, R2, R3, R4	2 kΩ, 1/4 W Chip Resistors	SG73P2ATTD2001F	KOA Speer
R5	50 Ω, 10 W Termination	RFP-060120A25Z50-2	Anaren
R6, R7	0 Ω, 3 A Chip Resistors	CRCW12060000Z0EA	Vishay
Z1	2300–2700 MHz Band, 90°, 2 dB Hybrid Coupler	CMX25Q02	RN2 Technologies
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D76512	MTL

TYPICAL CHARACTERISTICS — 2300–2400 MHz

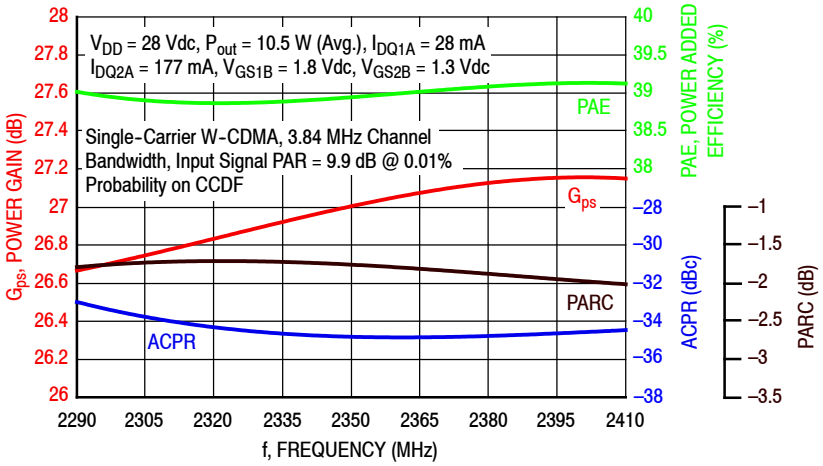


Figure 27. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 10.5 Watts Avg.

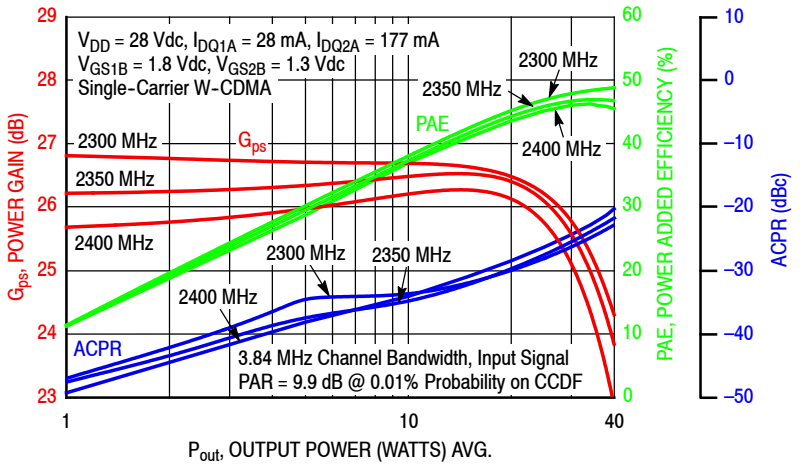


Figure 28. Single-Carrier W-CDMA Power Gain, Power Added Efficiency and ACPR versus Output Power

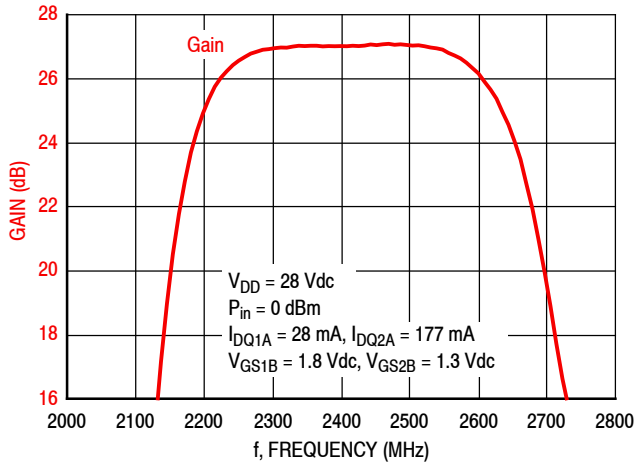


Figure 29. Broadband Frequency Response

Table 14. Carrier Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQ1A} = 28 mA, I_{DQ1B} = 182 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2300	26.5 – j9.90	26.4 + j7.78	9.63 – j12.0	30.7	44.4	28	52.7	–4
2400	44.2 – j12.0	42.3 + j9.38	10.1 – j11.7	31.1	44.3	27	51.2	–2

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2300	26.5 – j9.90	27.5 + j6.96	9.11 – j12.5	28.6	45.2	33	53.3	–6
2400	44.2 – j12.0	42.7 + j7.17	9.76 – j11.9	29.0	45.2	33	52.1	–5

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 15. Carrier Side Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 28 Vdc, I_{DQ1A} = 28 mA, I_{DQ1B} = 182 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2300	26.5 – j9.90	27.3 + j8.98	18.2 – j10.7	31.8	43.2	21	59.0	–6
2400	44.2 – j12.0	44.7 + j10.3	16.7 – j7.02	32.3	43.3	21	56.9	–4

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2300	26.5 – j9.90	28.1 + j8.20	17.0 – j10.3	29.7	44.2	26	59.2	–9
2400	44.2 – j12.0	44.7 + j8.13	17.0 – j7.71	30.3	44.1	26	57.7	–6

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

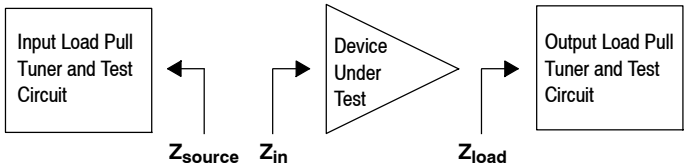


Table 16. Peaking Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, V_{GSA} = 1.0 Vdc, V_{GSB} = 1.0 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2300	23.9 + j2.41	24.2 – j4.45	4.16 – j7.89	21.4	47.4	55	54.7	–32
2400	36.1 – j2.99	35.3 – j2.41	4.57 – j7.10	22.2	47.4	54	54.2	–31

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2300	23.9 + j2.41	24.4 – j6.32	4.16 – j7.97	19.4	47.7	59	53.9	–42
2400	36.1 – j2.99	32.8 – j4.53	4.57 – j7.27	20.2	47.6	58	53.3	–42

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

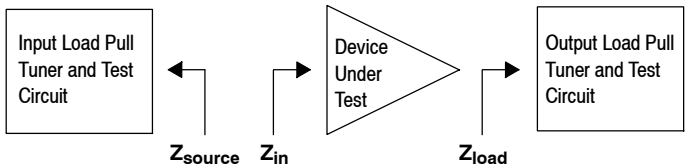
Table 17. Peaking Side Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 28 Vdc, V_{GSA} = 1.0 Vdc, V_{GSB} = 1.0 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2300	23.9 + j2.41	24.7 – j3.51	7.56 – j8.25	21.3	46.6	45	60.5	–34
2400	36.1 – j2.99	37.0 – j1.38	8.23 – j5.70	22.0	46.4	44	59.7	–34

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2300	23.9 + j2.41	24.8 – j5.77	6.68 – j8.13	19.4	47.1	52	58.0	–46
2400	36.1 – j2.99	34.2 – j4.41	7.40 – j5.84	20.1	47.0	50	57.3	–47

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 2300 MHz

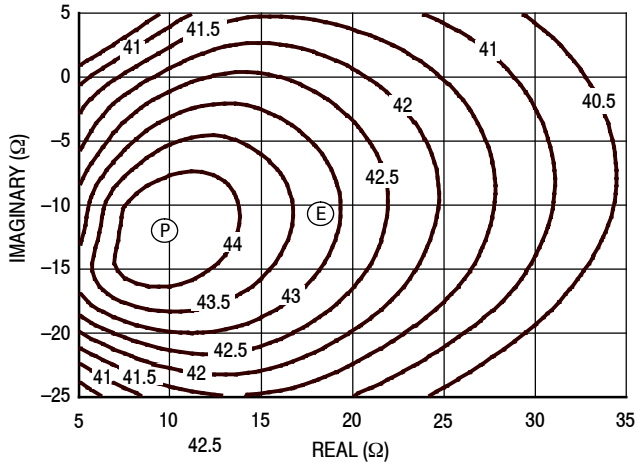


Figure 30. P1dB Load Pull Output Power Contours (dBm)

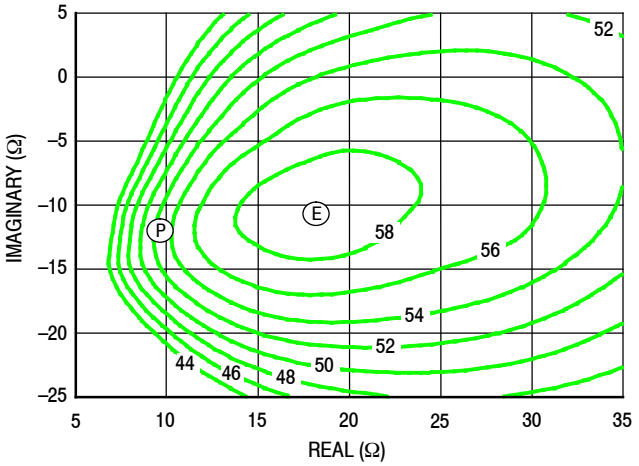


Figure 31. P1dB Load Pull Efficiency Contours (%)

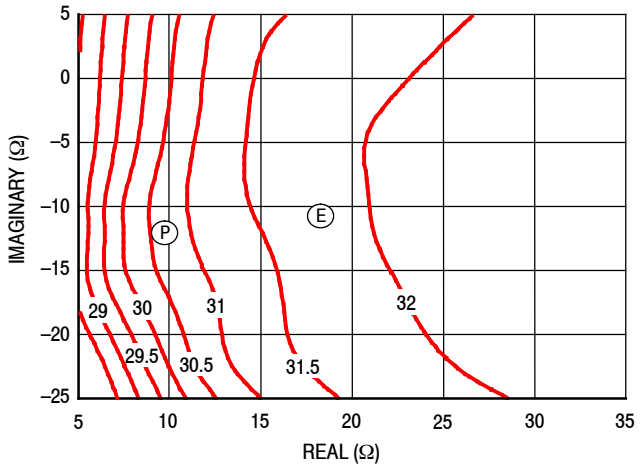


Figure 32. P1dB Load Pull Gain Contours (dB)

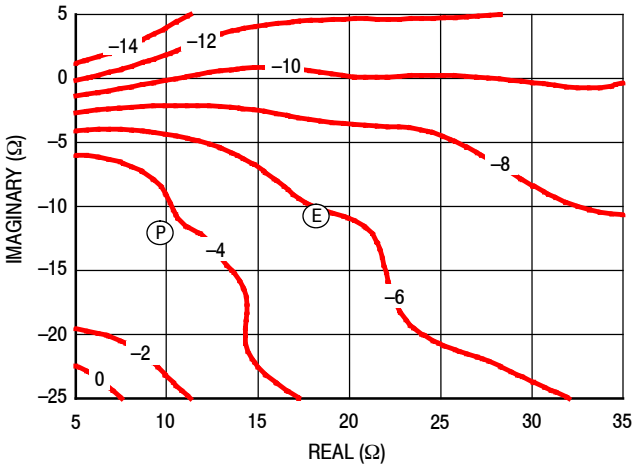


Figure 33. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power
Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

P3dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 2300 MHz

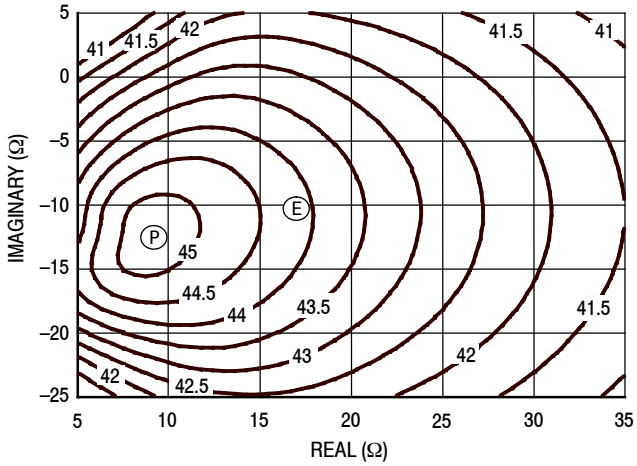


Figure 34. P3dB Load Pull Output Power Contours (dBm)

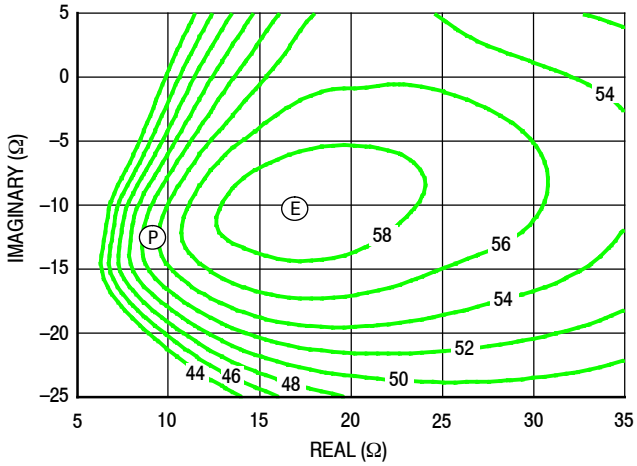


Figure 35. P3dB Load Pull Efficiency Contours (%)

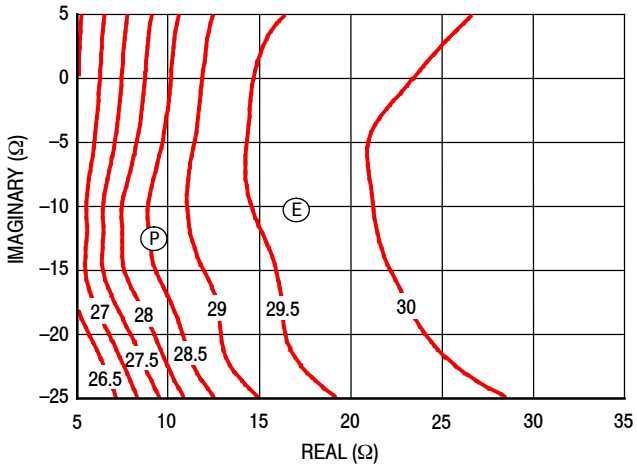


Figure 36. P3dB Load Pull Gain Contours (dB)

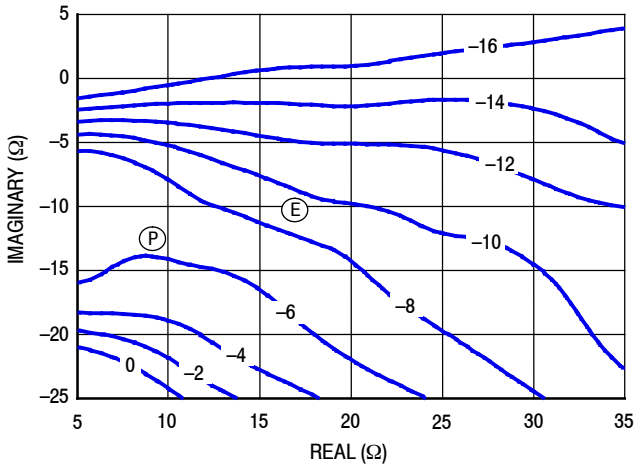


Figure 37. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power
Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

P1dB – TYPICAL PEAKING LOAD PULL CONTOURS — 2300 MHz

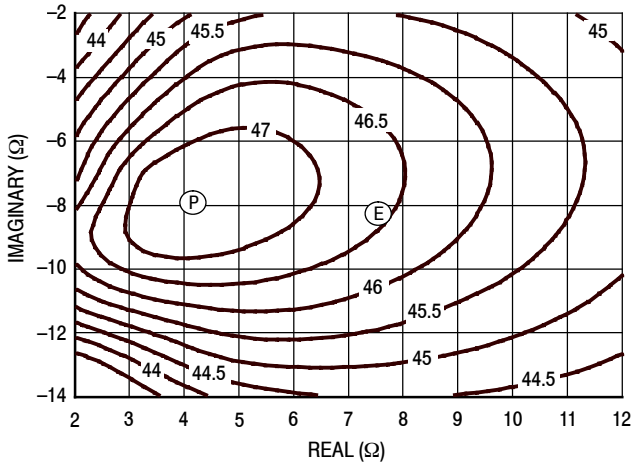


Figure 38. P1dB Load Pull Output Power Contours (dBm)

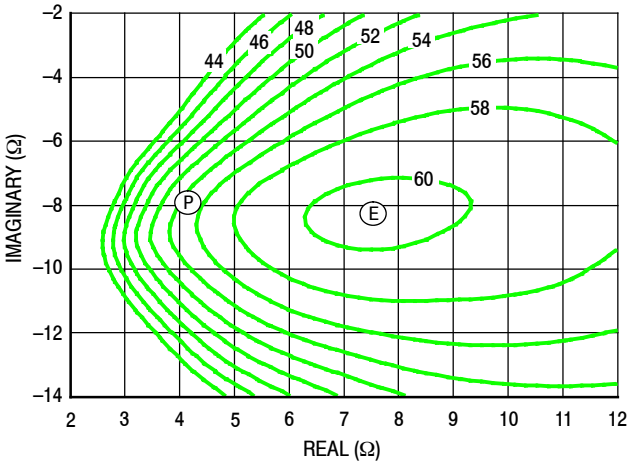


Figure 39. P1dB Load Pull Efficiency Contours (%)

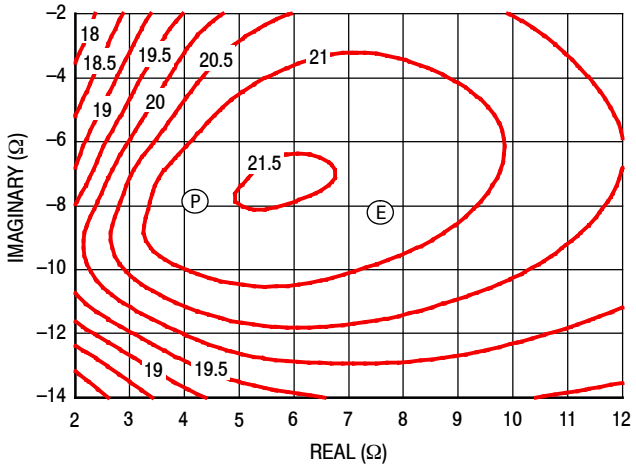


Figure 40. P1dB Load Pull Gain Contours (dB)

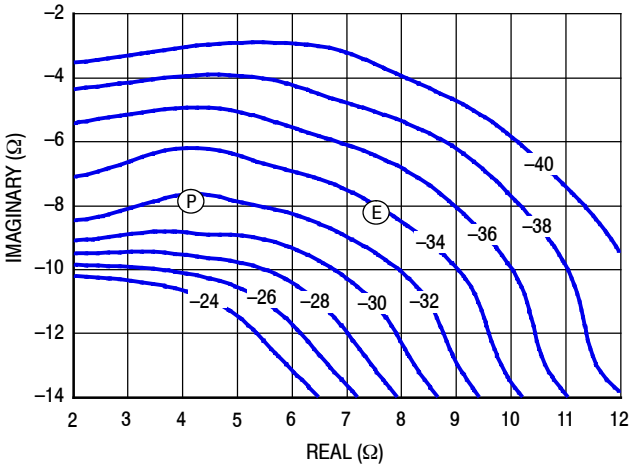


Figure 41. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power
Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

P3dB – TYPICAL PEAKING LOAD PULL CONTOURS — 2300 MHz

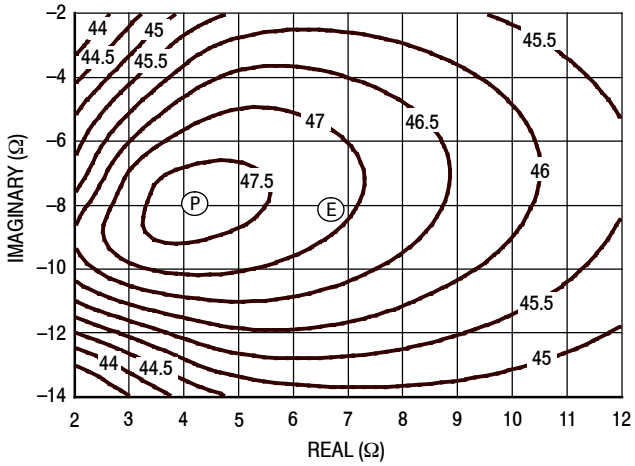


Figure 42. P3dB Load Pull Output Power Contours (dBm)

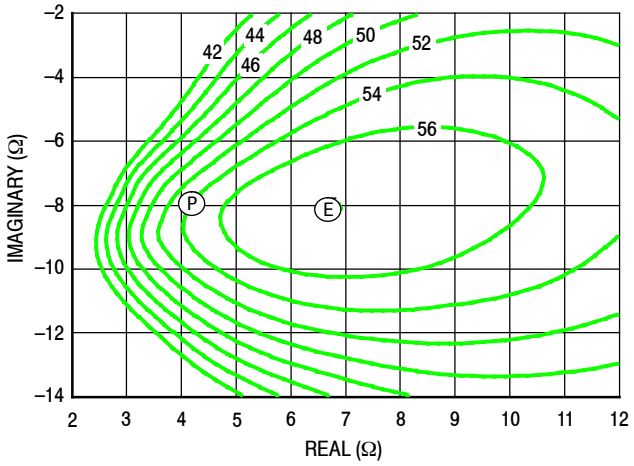


Figure 43. P3dB Load Pull Efficiency Contours (%)

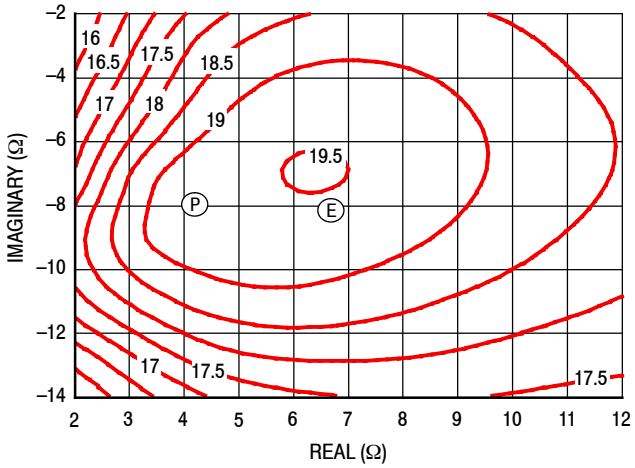


Figure 44. P3dB Load Pull Gain Contours (dB)

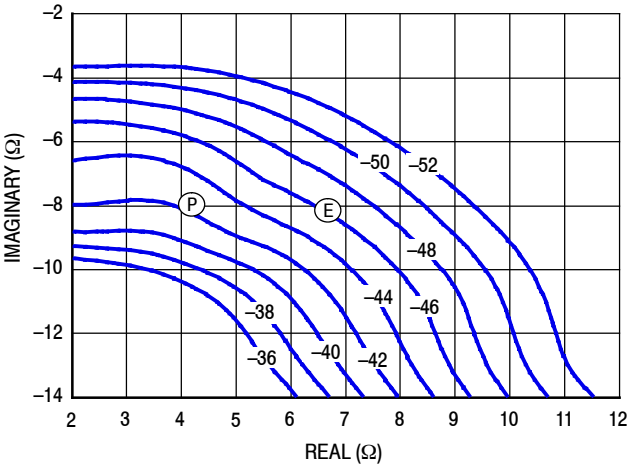
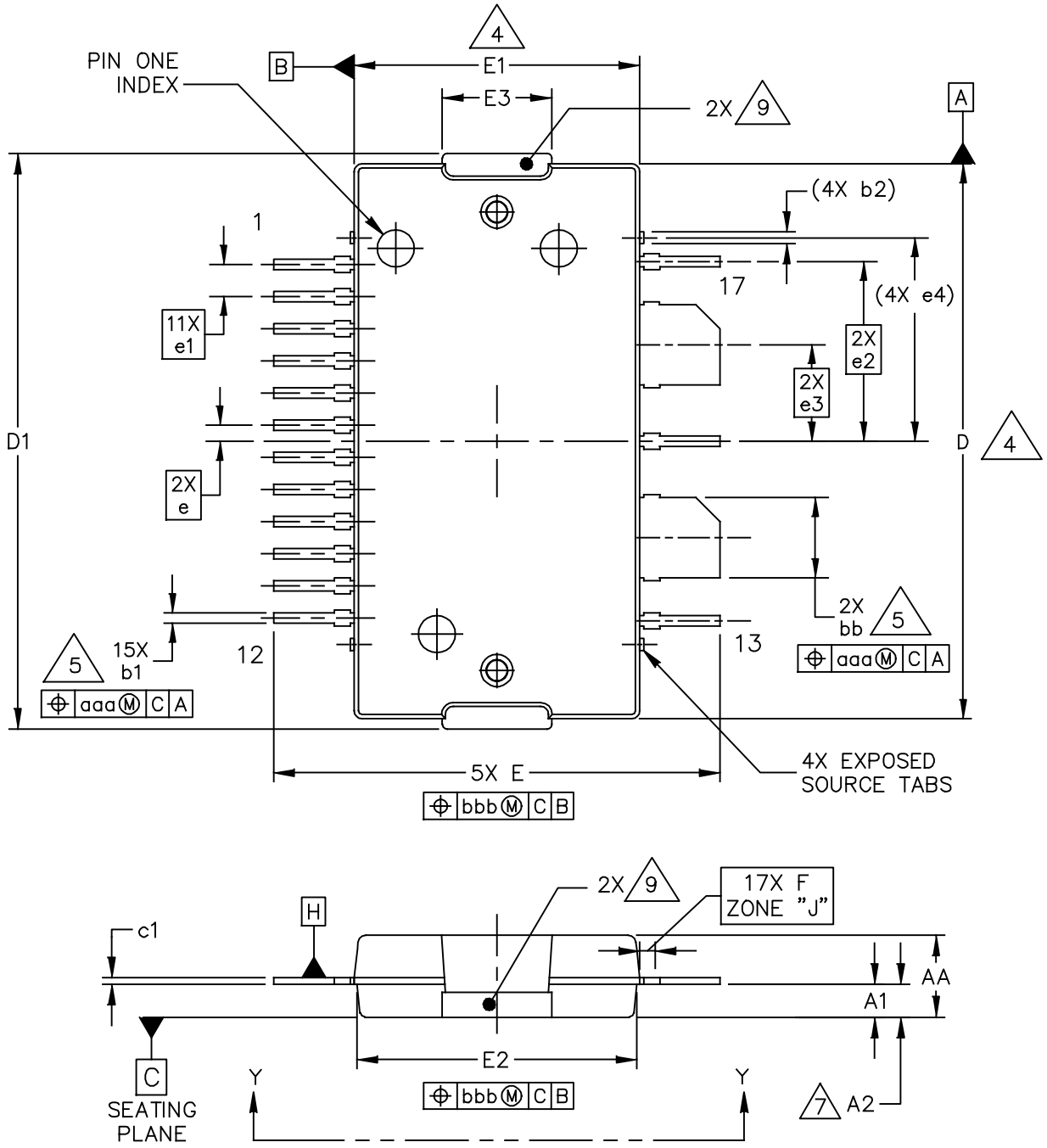


Figure 45. P3dB Load Pull AM/PM Contours (°)

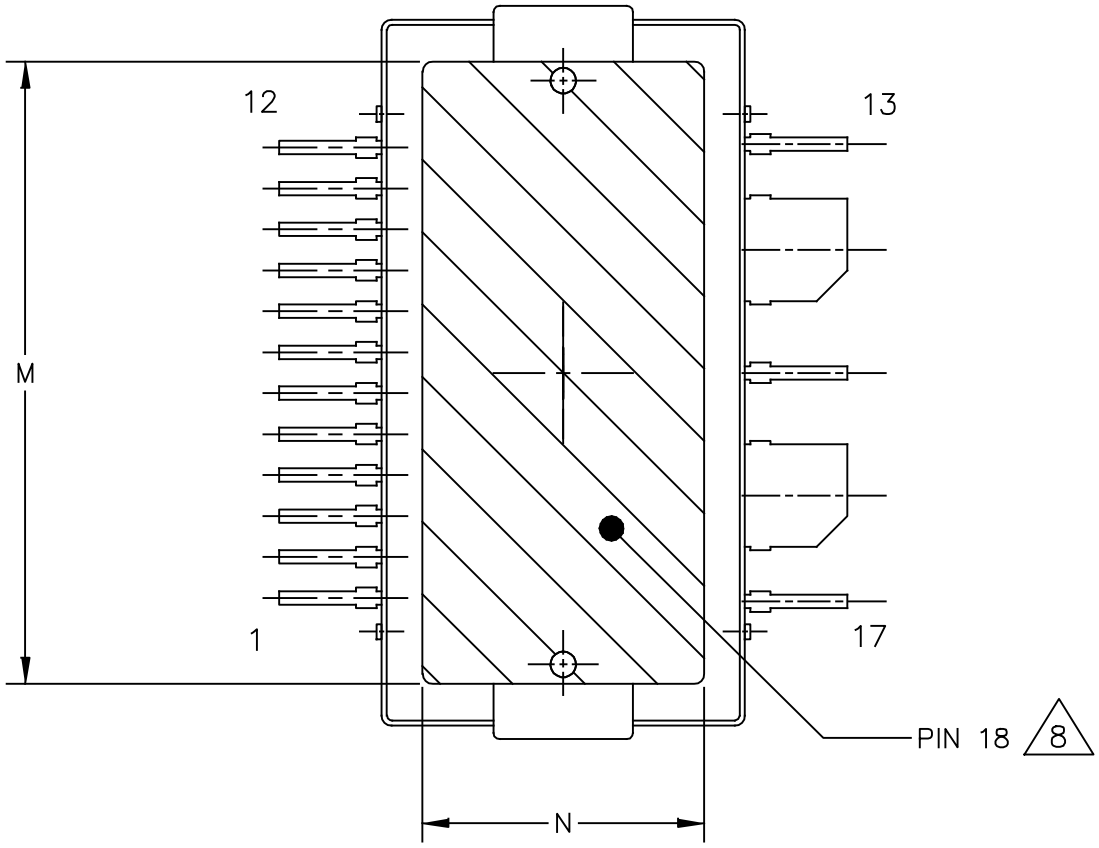
NOTE: Ⓟ = Maximum Output Power
Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

PACKAGE DIMENSIONS



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: TO−270WB−17	DOCUMENT NO: 98ASA00583D	REV: A
	STANDARD: NON−JEDEC	
	02 SEP 2014	



VIEW Y–Y

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: TO–270WB–17	DOCUMENT NO: 98ASA00583D	REV: A
	STANDARD: NON–JEDEC	
	02 SEP 2014	

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. DIMENSIONS bb AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb AND b1 DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

7. DIMENSION A2 APPLIES WITHIN ZONE J ONLY.

8. HATCHING REPRESENTS THE EXPOSED AND SOLDERABLE AREA OF THE HEAT SLUG. DIMENSIONS M AND N REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF THE HEAT SLUG.

9. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
AA	.099	.105	2.51	2.67	bb	.097	.103	2.46	2.62
A1	.039	.043	0.99	1.09	b1	.010	.016	0.25	0.41
A2	.040	.042	1.02	1.07	b2	----	.019	----	0.48
D	.688	.692	17.48	17.58	c1	.007	.011	0.18	0.28
D1	.712	.720	18.08	18.29	e	.020 BSC		0.51 BSC	
E	.551	.559	14.00	14.20	e1	.040 BSC		1.02 BSC	
E1	.353	.357	8.97	9.07	e2	.223 BSC		5.66 BSC	
E2	.346	.350	8.79	8.89	e3	.120 BSC		3.05 BSC	
E3	.132	.140	3.35	3.56	e4	.253 INFO ONLY		6.43 INFO ONLY	
F	.025 BSC		0.64 BSC		aaa	.004		0.10	
M	.600	----	15.24	----	bbb	.008		0.20	
N	.270	----	6.86	----					

MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE

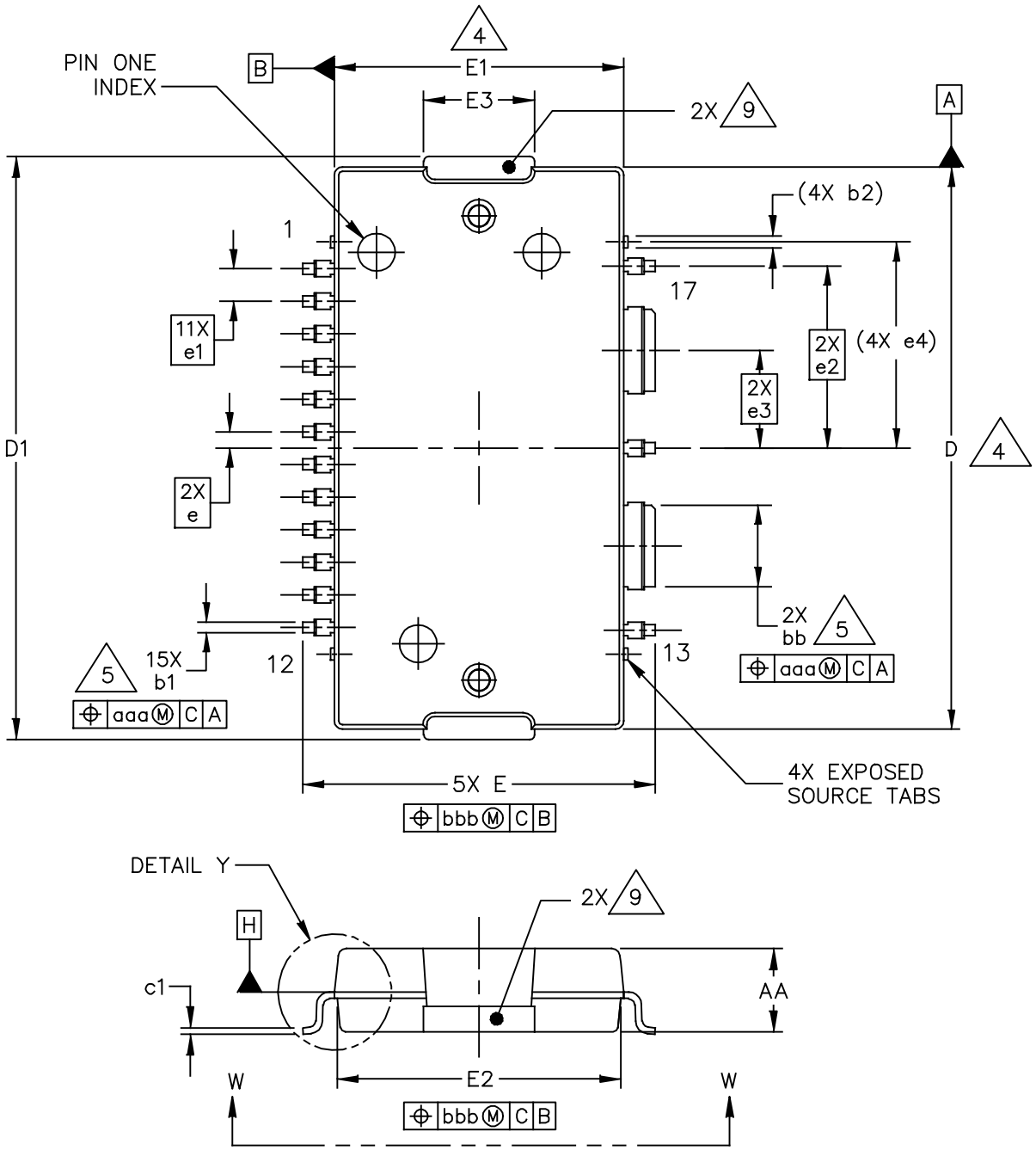
TITLE:

TO–270WB–17

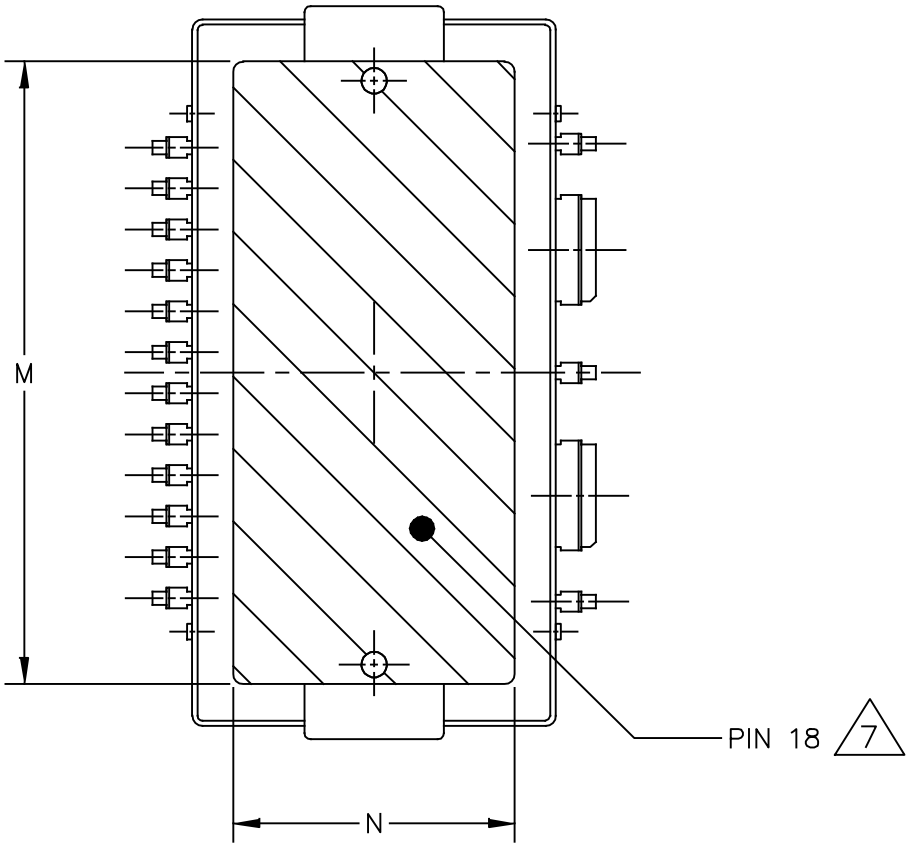
DOCUMENT NO: 98ASA00583D REV: A

STANDARD: NON–JEDEC

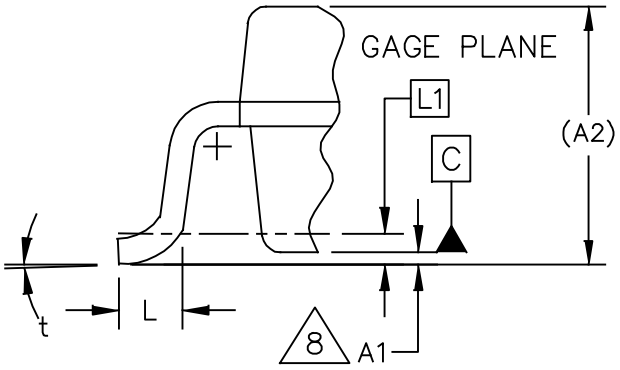
02 SEP 2014



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: TO-270WBG-17	DOCUMENT NO: 98ASA00729D	REV: A
	STANDARD: NON-JEDEC	
	02 SEP 2014	



VIEW W–W



DETAIL "Y"

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: TO–270WBG–17	DOCUMENT NO: 98ASA00729D	REV: A
	STANDARD: NON–JEDEC	
	02 SEP 2014	

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. DIMENSIONS bb AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb AND b1 DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

7. HATCHING REPRESENTS THE EXPOSED AND SOLDERABLE AREA OF THE HEAT SLUG. DIMENSIONS M AND N REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF THE HEAT SLUG.

8. DIMENSION A1 IS MEASURED WITH REFERENCE TO DATUM C. THE POSITIVE VALUE IMPLIES THAT THE BOTTOM OF THE PACKAGE IS HIGHER THAN THE BOTTOM OF THE LEAD.

9. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
AA	.099	.105	2.51	2.67	bb	.097	.103	2.46	2.62
A1	.001	.004	0.03	0.10	b1	.010	.016	0.25	0.41
A2	(.105)		(2.67)		b2	----	.019	----	0.48
D	.688	.692	17.48	17.58	c1	.007	.011	0.18	0.28
D1	.712	.720	18.08	18.29	e	.020 BSC		0.51 BSC	
E	.429	.437	10.90	11.10	e1	.040 BSC		1.02 BSC	
E1	.353	.357	8.97	9.07	e2	.223 BSC		5.66 BSC	
E2	.346	.350	8.79	8.89	e3	.120 BSC		3.05 BSC	
E3	.132	.140	3.35	3.56	e4	.253 INFO ONLY		6.43 INFO ONLY	
L	.018	.024	0.46	0.61	t	2°	8°	2°	8°
L1	.010 BSC		0.25 BSC		aaa	.004		0.10	
M	.600	----	15.24	----	bbb	.008		0.20	
N	.270	----	6.86	----					

MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE

TITLE: TO–270WBG–17

DOCUMENT NO: 98ASA00729D REV: A

STANDARD: NON–JEDEC

02 SEP 2014

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to http://www.nxp.com/RF
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Jan. 2016	• Initial release of data sheet

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Document Number: A2I25H060N
Rev. 0, 1/2016