MADC-010736

Receiver, High IIP3, SMD
40.5 - 43.5 GHz

Rev. V2

Features

- Integrates LNA, Image Reject Mixer, LO Doubler, and LO Buffer
- 3.5 dB Noise Figure
- 12 dB Conversion Gain
- 30 dBc Image Rejection
- 9 dBm Input Third Order Intercept @ 2 GHz IF
- Lead-Free 6 mm Laminate Package
- RoHS^ Compliant

Description

The MADC-010736 is an integrated USB receiver that has a noise figure of 3.5 dB and a typical conversion gain of 12 dB. The integrated mixer provides image rejection of 30 dBc. I and Q mixer outputs are provided and an external 90° hybrid is required to complete the image rejection function. The device integrates an LNA, image reject mixer and LO buffer/doubler within a 6 mm laminate package. It is ideally suited for 42 GHz band point-to-point radios.

Each device is 100% RF tested to ensure performance compliance. The part is fabricated using an efficient pHEMT process.

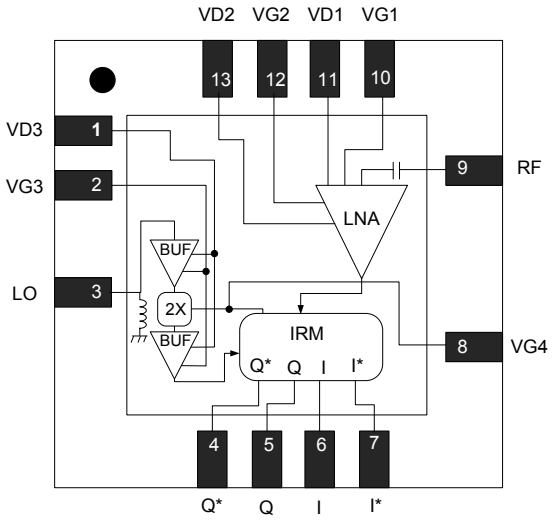
The MTTF is > 1,000,000 hours at a 150°C junction temperature.

Ordering Information[1,2]

Part Number	Package
MADC-010736-000000	Bulk Quantity
MADC-010736-TR0200	200 Piece Reel
MADC-010736-TR0500	500 Piece Reel
MADC-010736-001SMB	Sample Evaluation board

1. Reference Application Note M513 for reel size information.
2. All sample boards include 3 loose parts.

Functional Schematic



Pin Configuration[3,4]

Pin No.	Function
1	V_D3
2	V_G3
3	LO
4	Q* Input[5]
5	Q Input
6	I Input
7	I* Input[5]
8	V_G4
9	RF
10	V_G1
11	V_D1
12	V_G2
13	V_D2

3. The exposed pad centered on the package bottom must be connected to RF and DC ground.
4. MACOM recommends connecting unused package pins to ground.
5. IF pins I* and Q* may be left open (unused) for un-balanced IF operation.

^Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

Electrical Specifications[6]:

T_B = 25°C, $V_{D1,2,3}$ = 4.0 V, I_{D1} = 10 mA, I_{D2} = 100 mA, V_{G3} = -0.4 V, V_{G4} = -3 V, IF = 3.5 GHz

Parameter	Units	Min.	Typ.	Max.
Frequency Range (RF)	GHz	40.5	—	43.5
Frequency Range (LO)	GHz	18.5	—	21.75
Frequency Range (IF)	GHz	DC	—	3.5
Conversion Gain	dB	10	12	—
Image Rejection	dBc	—	30	—
Input IP3	dBm	—	6	—
Noise Figure	dB	—	3.5	5.0
LO Power	dBm	—	0	—
IF Return Loss	dB	—	15	—
RF Return Loss	dB	—	18	—
LO Return Loss	dB	—	15	—
DC Current (ID1+ID2+ID3)	mA	—	290	—

6. Apply gate voltages prior to drain voltages. Adjust VG1, VG2 and VG3 between –1.0 and –0.1 V to achieve specified drain current. Typical current, 290 mA = 10 (ID1) + 100 (ID2) + 180 (ID3). Refer to App Note [1] for biasing details.

Maximum Operating Ratings[7,8]

Parameter	Absolute Maximum
Input Power	+5 dBm
Drain Supply Voltage	+4.3 Volts
Operating Temperature	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature	-55°C to +150°C

7. Exceeding any one or combination of these limits may cause permanent damage to this device.
8. MACOM does not recommend sustained operation near these survivability limits.

Handling Procedures

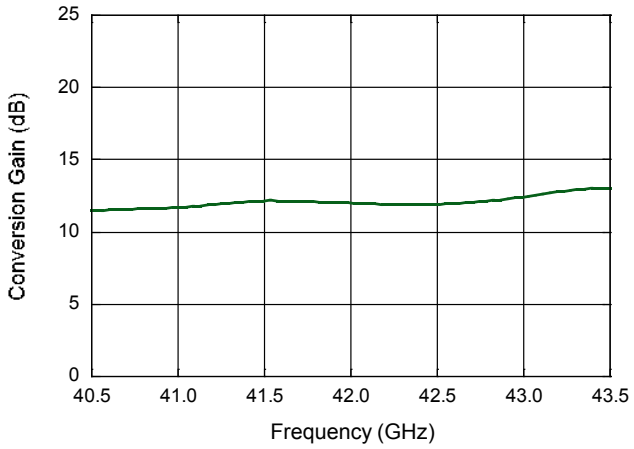
Please observe the following precautions to avoid damage:

Static Sensitivity

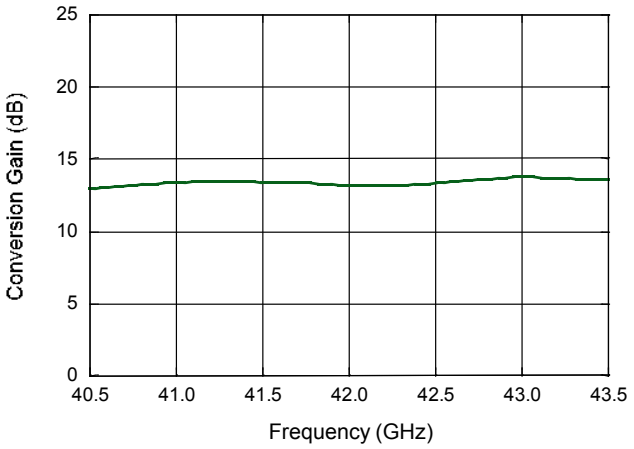
Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Typical Performance Curves: T_A = 25°C

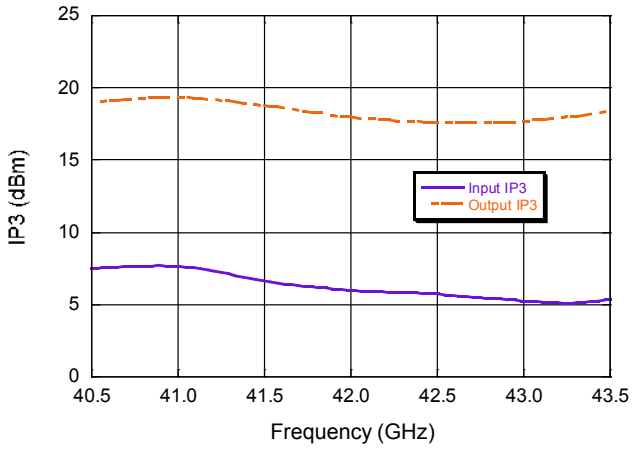
Conversion Gain @ 3.5 GHz IF



Conversion Gain @ 2.0 GHz IF



IP3 @ 3.5 GHz IF



IP3 @ 2.0 GHz IF

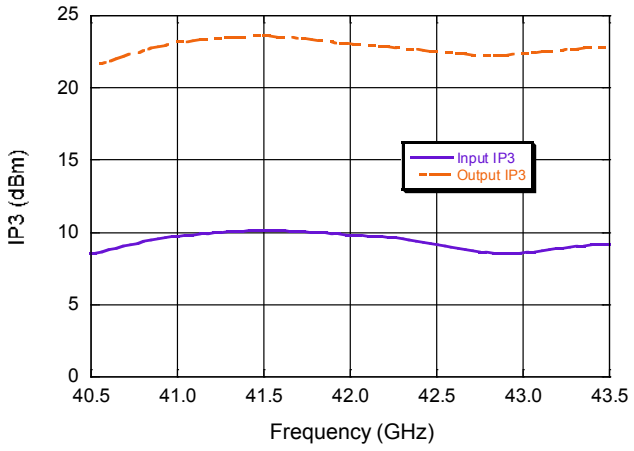


Image Rejection @ 3.5 GHz IF

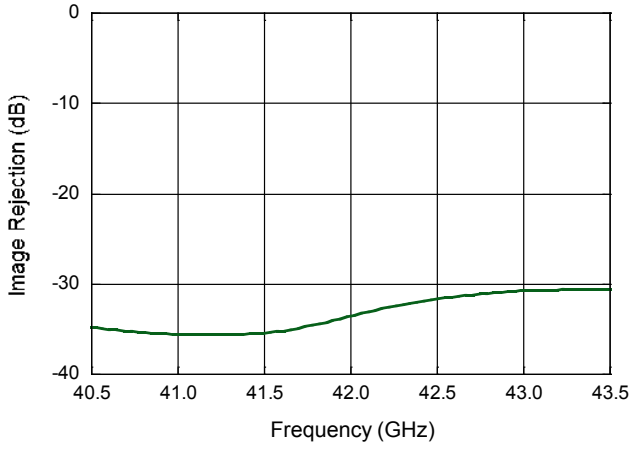
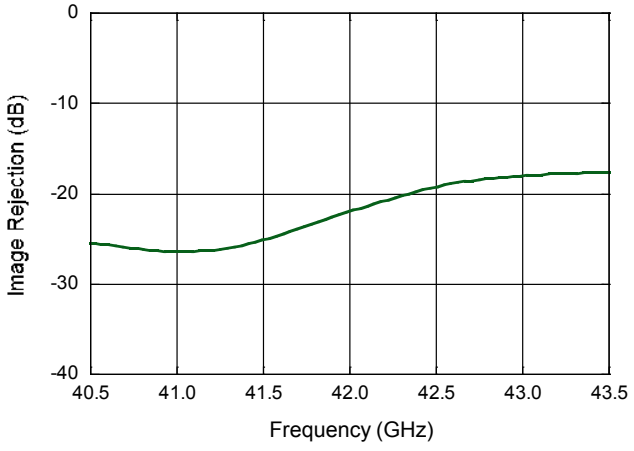
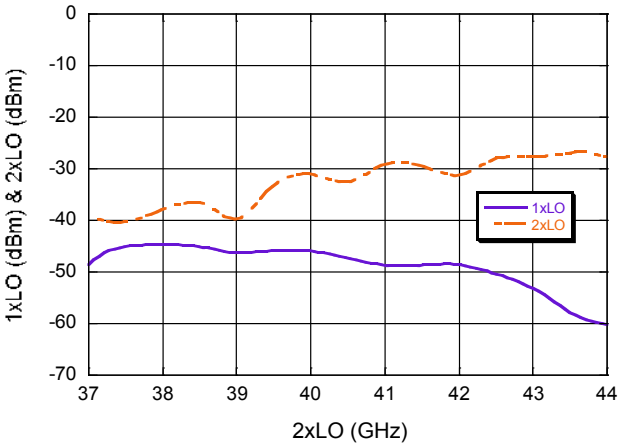


Image Rejection @ 2.0 GHz IF

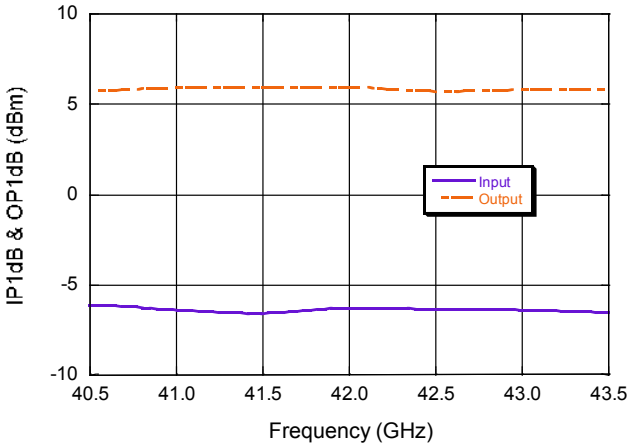


Typical Performance Curves: T_A = 25°C

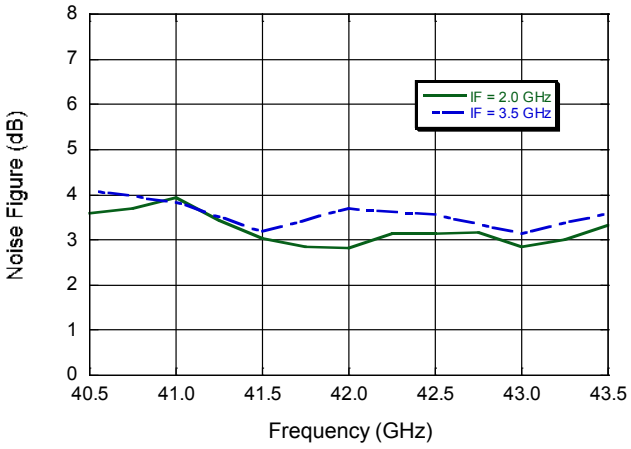
LO and 2xLO to RF Isolation



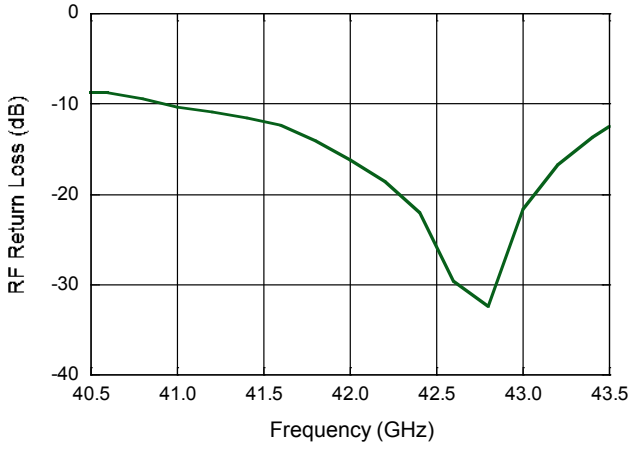
P1dB @ 2.0 GHz IF



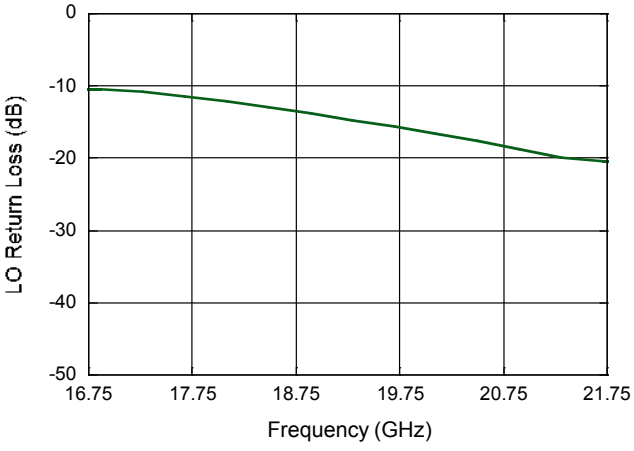
Noise Figure



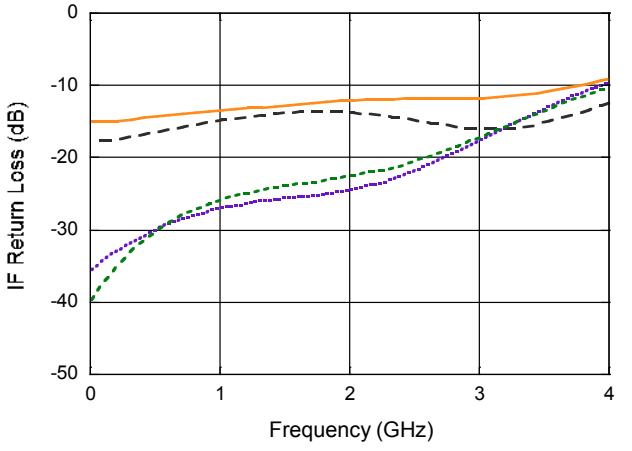
RF Return Loss



LO Return Loss



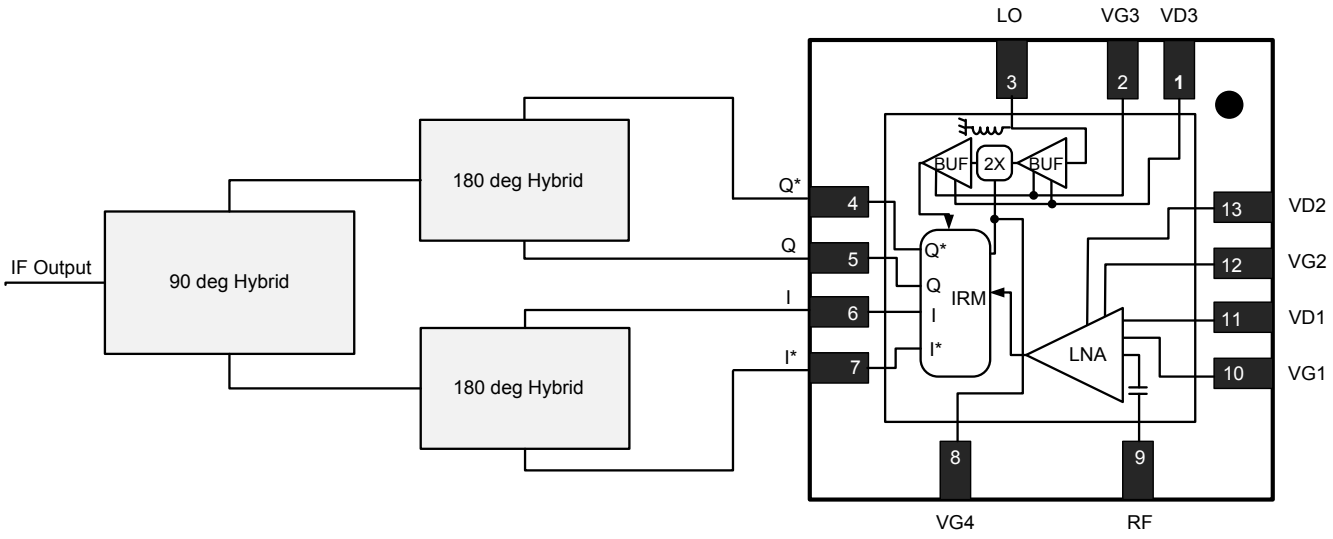
IF Return Loss



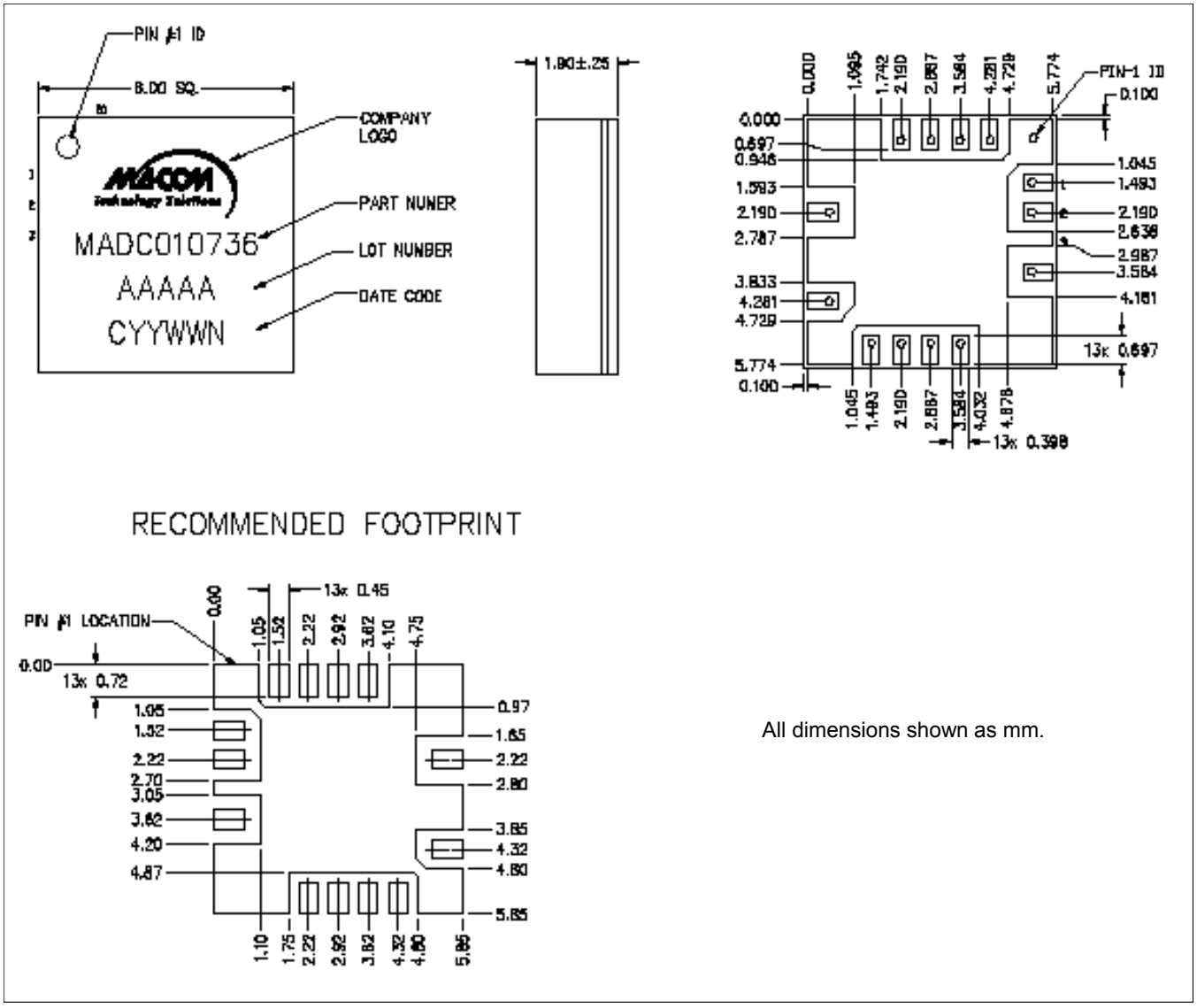
App Note [1] Biasing - The MADC-010736 is operated by biasing V_D1, V_D2, and V_D3 at 4.0 V. The corresponding drain currents are set to 10 mA, 100 mA, and 180 mA respectively. V_G4 requires a fixed voltage bias of nominally –3.0 V. It is recommended to use active bias on V_G1, V_G2, V_G3 to keep the currents in V_D1, V_D2, and V_D3 constant, in order to maintain the best performance over temperature. Depending on the supply voltages available and the power dissipation constraints, the bias circuits may include a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply to sense the current. Make sure to sequence the applied voltage to ensure negative gate bias is available before applying the positive drain supply.

App Note [2] I/Q - For highest gain, best image rejection and lowest noise figure all 4 IF ports should be used. I/I* and Q/Q* will combine through two 180 degree hybrid couplers generating inphase and quadrature phase components. Inphase and quadrature signals then need to be combined through 90 degree hybrid combiner to create IF output.

App Note [3] Board Layout - It is recommended to provide 100 pF decoupling capacitors as close to the bias pins as possible. Additional 10 nF and 1 µF on each of the bias lines are recommended placed a distance further away.



Lead-Free 6 mm Laminate Package†



All dimensions shown as mm.

† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 3 requirements.