

8-Mbit (512 K × 16) Static RAM

Features

- Very high speed: 55 ns
- Wide voltage range: 1.65 V–2.25 V
- Pin compatible with CY62157DV18 and CY62157DV20
- Ultra low standby power
 - Typical Standby current: 2 μ A
 - Maximum Standby current: 8 μ A
- Ultra low active power
 - Typical active current: 1.8 mA at $f = 1$ MHz
- Easy memory expansion with \overline{CE}_1 , CE_2 and \overline{OE} features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 48-ball very fine-pitch ball grid array (VFBGA) package

Functional Description

The CY62157EV18 is a high performance CMOS static RAM organized as 512K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power

consumption when addresses are not toggling. The device can also be put into standby mode when deselected (\overline{CE}_1 HIGH or CE_2 LOW or both BHE and BLE are HIGH). The input and output pins (I/O₀ through I/O₁₅) are placed in a high impedance state when:

- Deselected (\overline{CE}_1 HIGH or CE_2 LOW)
- Outputs are disabled (\overline{OE} HIGH)
- Both Byte High Enable and Byte Low Enable are disabled (BHE, BLE HIGH) or
- Write operation is active (\overline{CE}_1 LOW, CE_2 HIGH and \overline{WE} LOW).

Write to the device by taking Chip Enables (\overline{CE}_1 LOW and CE_2 HIGH) and Write Enable (\overline{WE}) input LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from I/O pins (I/O₀ through I/O₇), is written into the location specified on the address pins (A₀ through A₁₈). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₈).

Read from the device by taking Chip Enables (\overline{CE}_1 LOW and CE_2 HIGH) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins appear on I/O₀ to I/O₇. If Byte High Enable (BHE) is LOW, then data from memory appears on I/O₈ to I/O₁₅. See the [Truth Table on page 13](#) for a complete description of read and write modes.

For a complete list of related documentation, [click here](#).

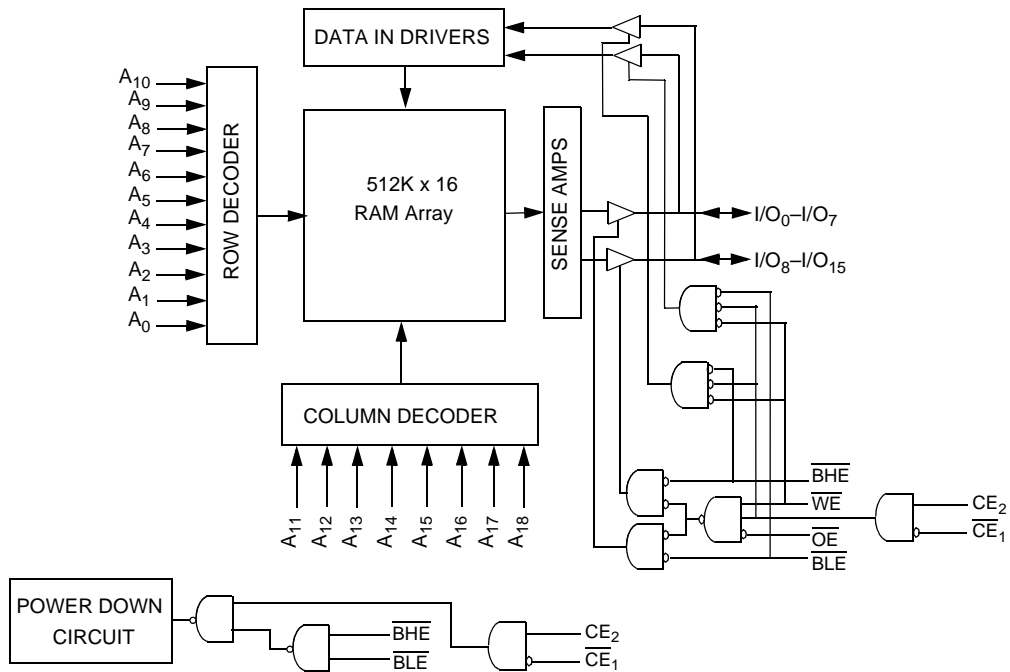
Product Portfolio

| Product | V _{CC} Range (V) | | | Speed (ns) | Power Dissipation | | | | | |
|-------------|---------------------------|--------------------|------|---------------|----------------------------------|-----|----------------------|-----|--------------------------------|-----|
| | | | | | Operating I _{CC} , (mA) | | | | Standby, I _{SB2} (μA) | |
| | | | | | f = 1MHz | | f = f _{max} | | | |
| | Min | Typ ^[1] | Max | | Typ ^[1] | Max | Typ ^[1] | Max | Typ ^[1] | Max |
| CY62157EV18 | 1.65 | 1.8 | 2.25 | 55 | 1.8 | 3 | 18 | 25 | 2 | 8 |

Note

1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.

Logic Block Diagram

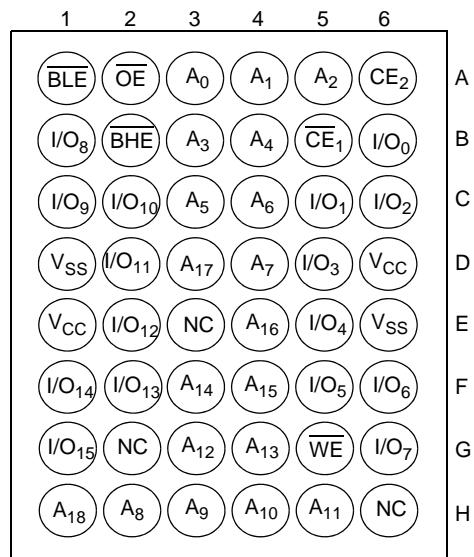


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Pin Configuration

Figure 1. 48-ball VFBGA pinout (Top View) [2]



Note

2. NC pins are not connected on the die.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature -65 °C to + 150 °C

Ambient temperature with power applied -55 °C to + 125 °C

Supply voltage to ground potential -0.2 V to 2.45 V ($V_{CCmax} + 0.2$ V)

DC voltage applied to outputs in High-Z state ^[3, 4] -0.2 V to 2.45 V ($V_{CCmax} + 0.2$ V)

DC input voltage ^[3, 4] -0.2 V to 2.45 V ($V_{CCmax} + 0.2$ V)

Output current into outputs (LOW) 20 mA

Static discharge voltage (in accordance with MIL-STD-883, Method 3015) > 2001 V

Latch-up current > 200 mA

Operating Range

| Device | Range | Ambient Temperature | V_{CC} ^[5] |
|---------------|------------|---------------------|-------------------------|
| CY62157EV18LL | Industrial | -40 °C to +85 °C | 1.65 V to 2.25 V |

Electrical Characteristics

Over the Operating Range

| Parameter | Description | Test Conditions | 55 ns | | | Unit |
|-----------------|---|---|-------|--------------------|------------------|------|
| | | | Min | Typ ^[6] | Max | |
| V_{OH} | Output HIGH voltage | $I_{OH} = -0.1$ mA $V_{CC} = 1.65$ V | 1.4 | — | — | V |
| V_{OL} | Output LOW voltage | $I_{OL} = 0.1$ mA $V_{CC} = 1.65$ V | — | — | 0.2 | V |
| V_{IH} | Input HIGH voltage | $V_{CC} = 1.65$ V to 2.25 V | 1.4 | — | $V_{CC} + 0.2$ V | V |
| V_{IL} | Input LOW voltage | $V_{CC} = 1.65$ V to 2.25 V | -0.2 | — | 0.4 | V |
| I_{IX} | Input leakage current | $GND \leq V_I \leq V_{CC}$ | -1 | — | +1 | μA |
| I_{OZ} | Output leakage current | $GND \leq V_O \leq V_{CC}$, output disabled | -1 | — | +1 | μA |
| I_{CC} | V_{CC} operating supply current | $f = f_{max} = 1/t_{RC}$ $V_{CC} = V_{CC(max)}$, $I_{OUT} = 0$ mA CMOS levels | — | 18 | 25 | mA |
| | | $f = 1$ MHz | — | 1.8 | 3 | mA |
| $I_{SB1}^{[7]}$ | Automatic CE power down current – CMOS inputs | $\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V, $V_{IN} \leq 0.2$ V, $f = f_{max}$ (address and data only), $f = 0$ (OE, WE, BHE and BLE), $V_{CC} = V_{CC(max)}$. | — | 2 | 8 | μA |
| $I_{SB2}^{[7]}$ | Automatic CE power down current – CMOS Inputs | $\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, $f = 0$, $V_{CC} = V_{CC(max)}$. | — | 2 | 8 | μA |

Notes

- $V_{IL(min)}$ = -2.0 V for pulse durations less than 20 ns.
- $V_{IH(max)}$ = $V_{CC} + 0.5$ V for pulse durations less than 20 ns.
- Full Device AC operation assumes a 100 μs ramp time from 0 to V_{CC} (min) and 200 μs wait time after V_{CC} stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25$ °C.
- Chip enable (\overline{CE}) and byte enables (\overline{BHE} and \overline{BLE}) need to be tied to CMOS levels to meet the $I_{SB1}/I_{SB2}/I_{CCDR}$ spec. Other inputs can be left floating.

Capacitance

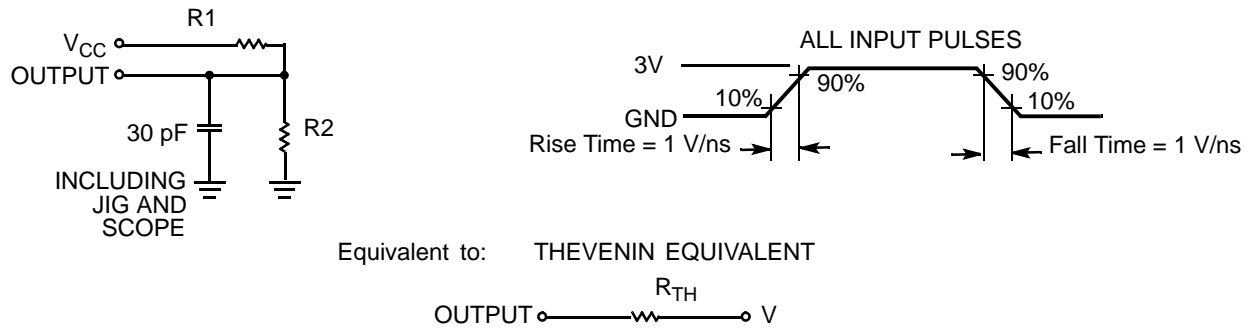
| Parameter ^[8] | Description | Test Conditions | Max | Unit |
|--------------------------|--------------------|--|-----|------|
| C_{IN} | Input capacitance | $T_A = 25\text{ }^{\circ}\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = V_{CC(typ)}$ | 10 | pF |
| C_{OUT} | Output capacitance | | 10 | pF |

Thermal Resistance

| Parameter ^[8] | Description | Test Conditions | BGA | Unit |
|--------------------------|--|---|-------|----------------------|
| Θ_{JA} | Thermal resistance (junction to ambient) | Still air, soldered on a 3 x 4.5 inch, four-layer printed circuit board | 48.34 | $^{\circ}\text{C/W}$ |
| Θ_{JC} | Thermal resistance (junction to case) | | 8.78 | $^{\circ}\text{C/W}$ |

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



| Parameters | Value | Unit |
|------------|-------|----------|
| R1 | 13500 | Ω |
| R2 | 10800 | Ω |
| R_{TH} | 6000 | Ω |
| V_{TH} | 0.80 | V |

Note

8. Tested initially and after any design or process changes that may affect these parameters.

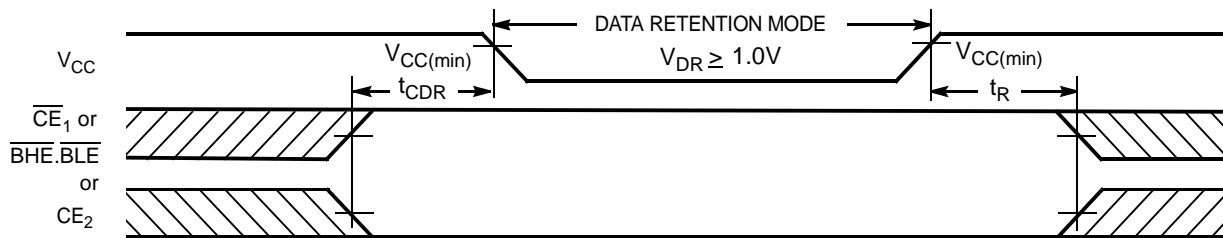
Data Retention Characteristics

Over the Operating Range

| Parameter | Description | Conditions | Min | Typ ^[9] | Max | Unit |
|----------------------------|--------------------------------------|--|-----|--------------------|-----|---------------|
| V_{DR} | V_{CC} for data retention | | 1.0 | – | – | V |
| I_{CCDR} ^[10] | Data retention current | $V_{CC} = V_{DR}$, $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$, $CE_2 \leq 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$ | – | 1 | 3 | μA |
| t_{CDR} ^[11] | Chip deselect to data retention time | | 0 | – | – | ns |
| t_R ^[12] | Operation recovery time | | 55 | – | – | ns |

Data Retention Waveform

Figure 3. Data Retention Waveform^[13]



Notes

9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25\text{ }^\circ\text{C}$.
10. Chip enable (\overline{CE}) and byte enables (\overline{BHE} and \overline{BLE}) need to be tied to CMOS levels to meet the $I_{SB1}/I_{SB2}/I_{CCDR}$ spec. Other inputs can be left floating.
11. Tested initially and after any design or process changes that may affect these parameters.
12. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100\text{ }\mu\text{s}$ or stable at $V_{CC(min)} \geq 100\text{ }\mu\text{s}$.
13. $\overline{BHE.BLE}$ is the AND of both \overline{BHE} and \overline{BLE} . Deselect the chip by either disabling chip enable signals or by disabling both \overline{BHE} and \overline{BLE} .

Switching Characteristics

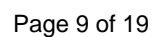
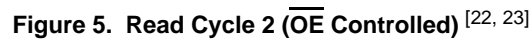
Over the Operating Range

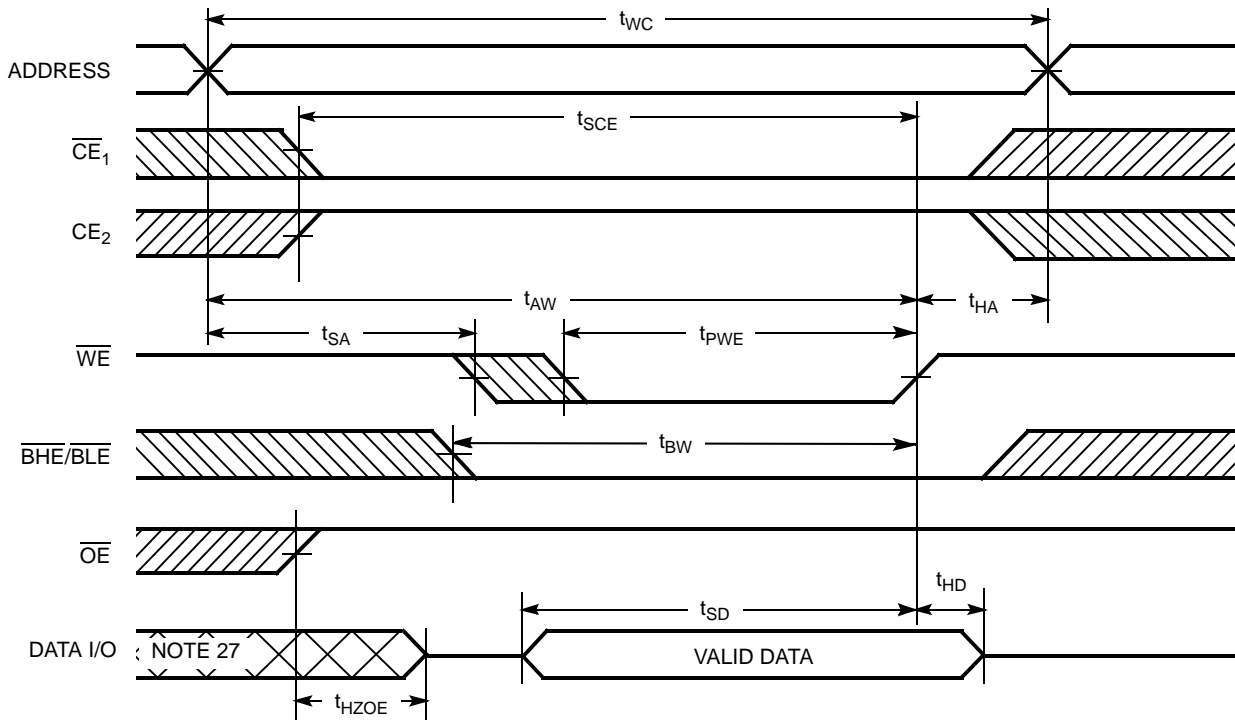
| Parameter ^[14, 15] | Description | 55 ns | | Unit |
|-----------------------------------|--|-------|-----|------|
| | | Min | Max | |
| Read Cycle | | | | |
| t _{RC} | Read cycle time | 55 | – | ns |
| t _{AA} | Address to data valid | – | 55 | ns |
| t _{OHA} | Data hold from address change | 10 | – | ns |
| t _{ACE} | \overline{CE}_1 LOW and CE ₂ HIGH to data valid | – | 55 | ns |
| t _{DOE} | \overline{OE} LOW to data valid | – | 25 | ns |
| t _{LZOE} | \overline{OE} LOW to Low-Z ^[16] | 5 | – | ns |
| t _{HZOE} | \overline{OE} HIGH to High-Z ^[16, 17] | – | 18 | ns |
| t _{LZCE} | \overline{CE}_1 LOW and CE ₂ HIGH to Low-Z ^[16] | 10 | – | ns |
| t _{HZCE} | \overline{CE}_1 HIGH and CE ₂ LOW to High-Z ^[16, 17] | – | 18 | ns |
| t _{PU} | \overline{CE}_1 LOW and CE ₂ HIGH to power up | 0 | – | ns |
| t _{PD} | \overline{CE}_1 HIGH and CE ₂ LOW to power down | – | 55 | ns |
| t _{DBE} | $\overline{BLE}/\overline{BHE}$ LOW to data valid | – | 55 | ns |
| t _{LZBE} ^[18] | $\overline{BLE}/\overline{BHE}$ LOW to Low-Z ^[16] | 10 | – | ns |
| t _{HZBE} | $\overline{BLE}/\overline{BHE}$ HIGH to High-Z ^[16, 17] | – | 18 | ns |
| Write Cycle ^[19, 20] | | | | |
| t _{WC} | Write cycle time | 45 | – | ns |
| t _{SCE} | \overline{CE}_1 LOW and CE ₂ HIGH to write end | 35 | – | ns |
| t _{AW} | Address setup to write end | 35 | – | ns |
| t _{HA} | Address hold from write end | 0 | – | ns |
| t _{SA} | Address setup to write start | 0 | – | ns |
| t _{PWE} | \overline{WE} pulse width | 35 | – | ns |
| t _{BW} | $\overline{BLE}/\overline{BHE}$ LOW to write end | 35 | – | ns |
| t _{SD} | Data setup to write end | 25 | – | ns |
| t _{HD} | Data hold from write end | 0 | – | ns |
| t _{HZWE} | \overline{WE} LOW to High-Z ^[16, 17] | – | 18 | ns |
| t _{LZWE} | \overline{WE} HIGH to Low-Z ^[16] | 10 | – | ns |

Notes

14. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1V/ns or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the [Figure 2 on page 6](#).
15. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Notes [AN13842](#) and [AN66311](#). However, the issue has been fixed and in production now, and hence, these Application Notes are no longer applicable. They are available for download on our website as they contain information on the date code of the parts, beyond which the fix has been in production.
16. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
17. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the output enters a high impedance state.
18. If both byte enables are toggled together, this value is 10 ns.
19. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$, \overline{BHE} and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
20. The minimum write cycle time for Write Cycle No. 3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .

Figure 4. Read Cycle 1 (Address Transition Controlled) ^[21, 22]



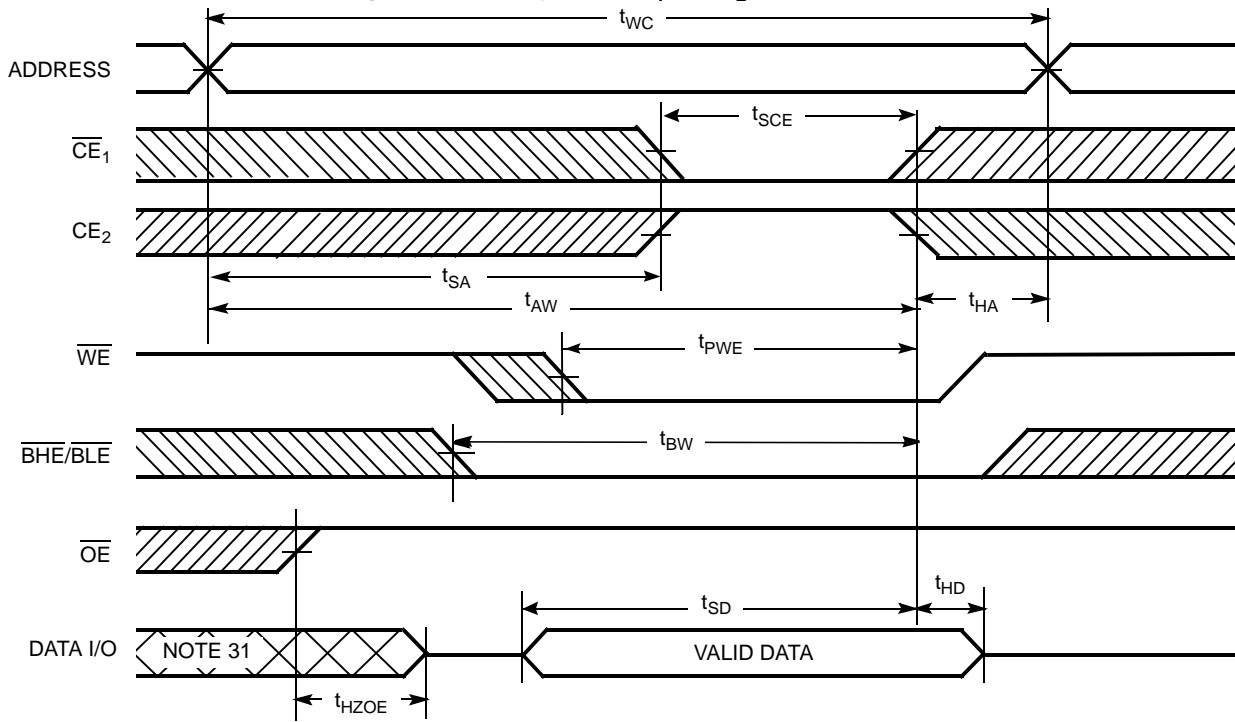
Switching Waveforms (continued)
Figure 6. Write Cycle 1 (\overline{WE} Controlled) [24, 25, 26]

Notes

24. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$, \overline{BHE} and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

25. Data I/O is high impedance if $\overline{OE} = V_{IH}$.

26. If \overline{CE}_1 goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.

27. During this period, the I/Os are in output state and input signals must not be applied.

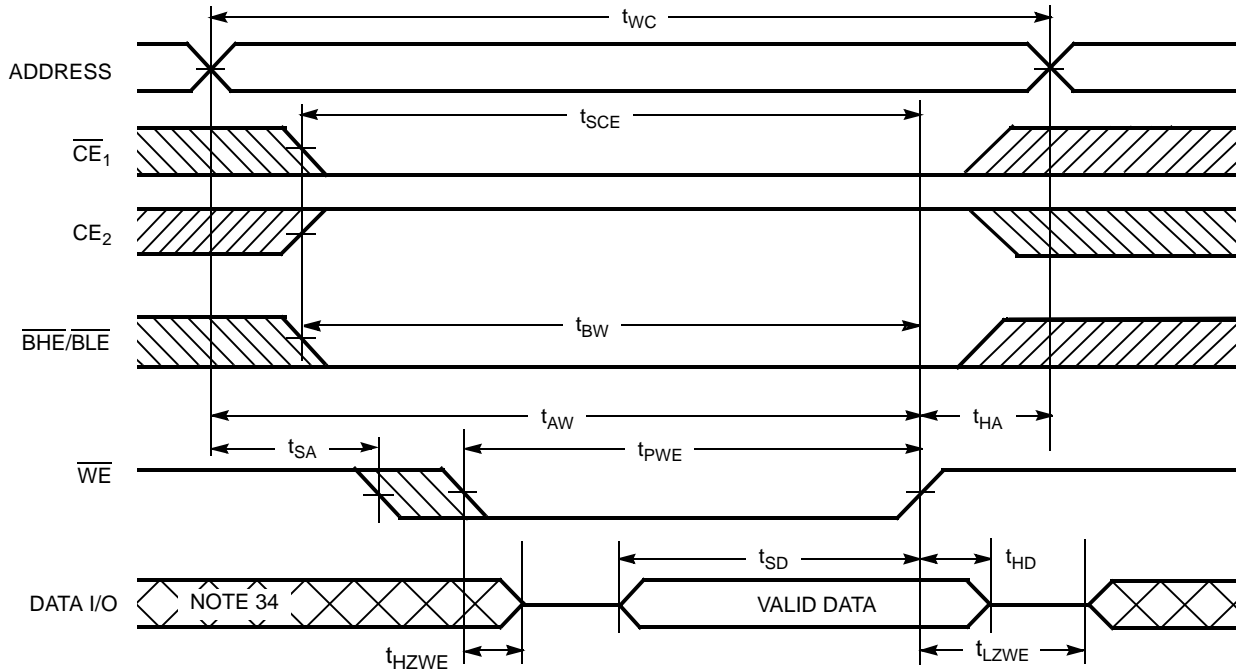
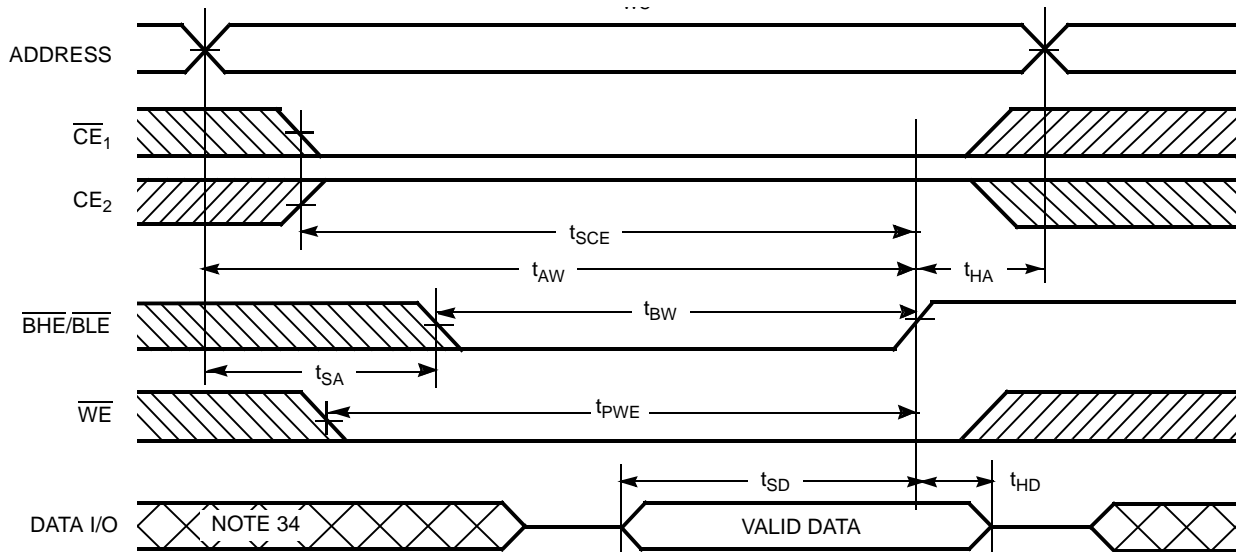
Switching Waveforms (continued)
Figure 7. Write Cycle 2 (\overline{CE}_1 or CE_2 Controlled) [28, 29, 30]

Notes

28. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$, \overline{BHE} and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

29. Data I/O is high impedance if $\overline{OE} = V_{IH}$.

30. If \overline{CE}_1 goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.

31. During this period, the I/Os are in output state and input signals must not be applied.

Switching Waveforms (continued)
Figure 8. Write Cycle 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) [32, 33]

Figure 9. Write Cycle 4 ($\overline{\text{BHE/BLER}}$ Controlled, $\overline{\text{OE}}$ LOW) [32]

Notes

32. If $\overline{\text{CE}}_1$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{\text{WE}} = V_{\text{IH}}$, the output remains in a high impedance state.

33. The minimum write cycle time for Write Cycle No. 3 ($\overline{\text{WE}}$ controlled, $\overline{\text{OE}}$ LOW) is the sum of t_{LZWE} and t_{SD} .

34. During this period, the I/Os are in output state and input signals must not be applied.

Truth Table

| \overline{CE}_1 | CE_2 | \overline{WE} | \overline{OE} | \overline{BHE} | \overline{BLE} | Inputs/Outputs | Mode | Power |
|-------------------|------------|-----------------|-----------------|------------------|------------------|--|---------------------|----------------------|
| H | $X^{[35]}$ | X | X | $X^{[35]}$ | $X^{[35]}$ | High-Z | Deselect/Power down | Standby (I_{SB}) |
| $X^{[35]}$ | L | X | X | $X^{[35]}$ | $X^{[35]}$ | High-Z | Deselect/Power down | Standby (I_{SB}) |
| $X^{[35]}$ | $X^{[35]}$ | X | X | H | H | High-Z | Deselect/Power down | Standby (I_{SB}) |
| L | H | H | L | L | L | Data out (I/O_0 – I/O_{15}) | Read | Active (I_{CC}) |
| L | H | H | L | H | L | Data out (I/O_0 – I/O_7); High-Z (I/O_8 – I/O_{15}) | Read | Active (I_{CC}) |
| L | H | H | L | L | H | High-Z (I/O_0 – I/O_7); Data out (I/O_8 – I/O_{15}) | Read | Active (I_{CC}) |
| L | H | H | H | L | H | High-Z | Output disabled | Active (I_{CC}) |
| L | H | H | H | H | L | High-Z | Output disabled | Active (I_{CC}) |
| L | H | H | H | L | L | High-Z | Output disabled | Active (I_{CC}) |
| L | H | L | X | L | L | Data in (I/O_0 – I/O_{15}) | Write | Active (I_{CC}) |
| L | H | L | X | H | L | Data in (I/O_0 – I/O_7); High-Z (I/O_8 – I/O_{15}) | Write | Active (I_{CC}) |
| L | H | L | X | L | H | High-Z (I/O_0 – I/O_7); Data in (I/O_8 – I/O_{15}) | Write | Active (I_{CC}) |

Note

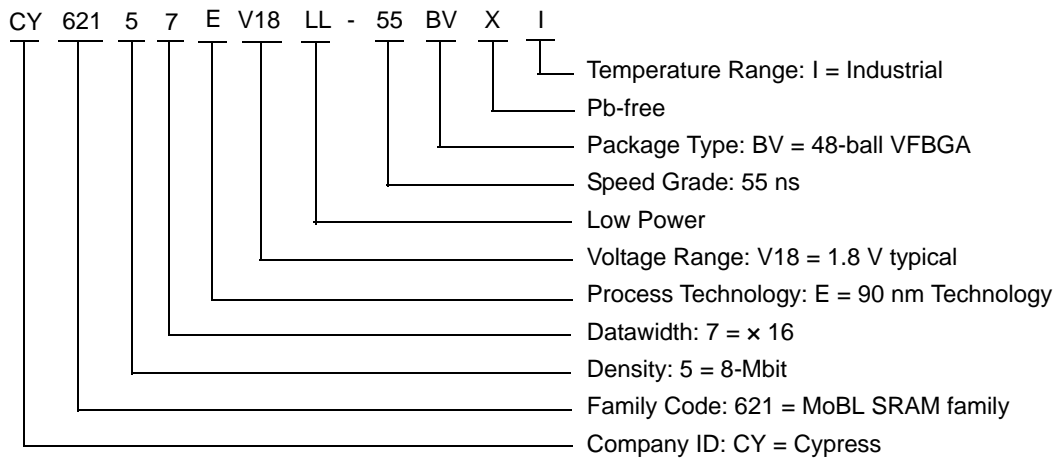
35. The 'X' (Don't care) state for the Chip enables and Byte enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|------------|----------------------|-----------------|-------------------------|-----------------|
| 55 | CY62157EV18LL-55BVXI | 51-85150 | 48-ball VFBGA (Pb-free) | Industrial |

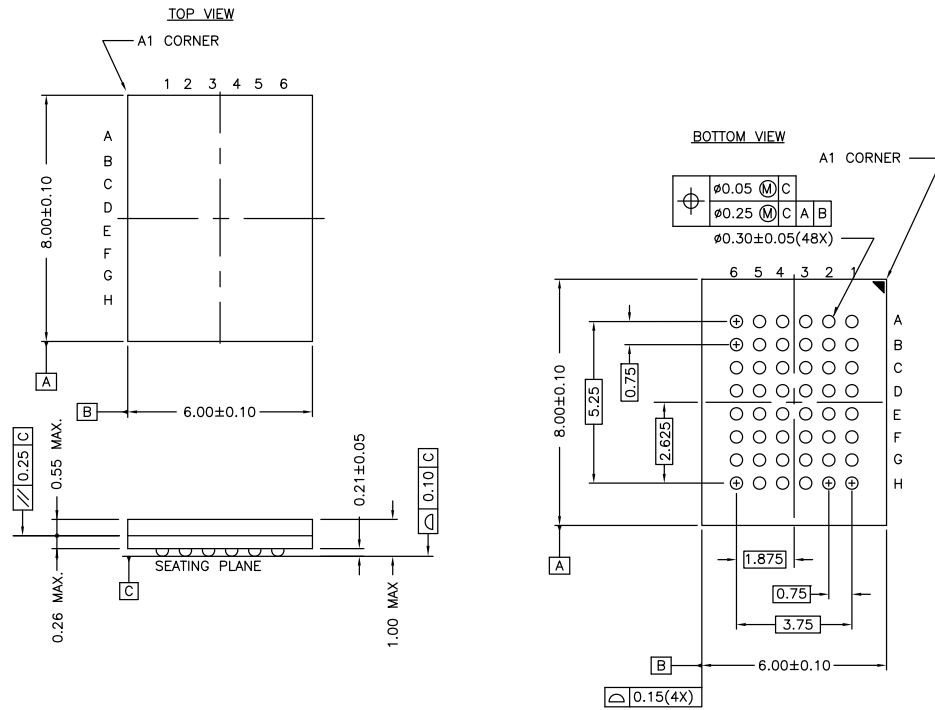
Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagram

Figure 10. 48-ball VFBGA (6 × 8 × 1 mm) BV48/BZ48 Package Outline, 51-85150



NOTE:
 PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD)
 posted on the Cypress web.

51-85150 *H

Acronyms

| Acronym | Description |
|---------|---|
| BHE | Byte High Enable |
| BLE | Byte Low Enable |
| CE | Chip Enable |
| CMOS | Complementary Metal Oxide Semiconductor |
| I/O | Input/Output |
| OE | Output Enable |
| SRAM | Static Random Access Memory |
| VFBGA | Very Fine-Pitch Ball Grid Array |
| WE | Write Enable |

Document Conventions

Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C | degrees Celsius |
| μA | microampere |
| mA | milliampere |
| MHz | megahertz |
| ns | nanosecond |
| Ω | ohm |
| pF | picofarad |
| V | volt |
| W | watt |

Document History

| Document Title: CY62157EV18 MoBL®, 8-Mbit (512 K × 16) Static RAM Document Number: 38-05490 | | | | |
|--|---------|------------|-----------------|---|
| Rev. | ECN No. | Issue Date | Orig. of Change | Description of Change |
| ** | 202862 | See ECN | AJU | New data sheet |
| *A | 291272 | See ECN | SYT | Converted from Advance Information to Preliminary Changed V_{CC} Max from 2.20 to 2.25 V Changed V_{CC} stabilization time in footnote #7 from 100 μ s to 200 μ s Changed I_{CCDR} from 4 to 4.5 μ A Changed t_{OHA} from 6 ns to 10 ns for both 35 ns and 45 ns Speed Bins Changed t_{DOE} from 15 and 22 ns to 18 and 22 ns for the 35 and 45 ns Speed Bins respectively Changed t_{HZOE} , t_{HZBE} and t_{HZWE} from 12 and 15 ns to 15 and 18 ns for the 35 and 45 ns Speed Bins respectively Changed t_{HZCE} from 12 and 15 ns to 18 and 22 ns for the 35 and 45 ns Speed Bins respectively Changed t_{SCE} , t_{AW} , and t_{BW} from 25 and 40 ns to 30 and 35 ns for the 35 and 45 ns Speed Bins respectively Changed t_{SD} from 15 and 20 ns to 18 and 22 ns for the 35 and 45 ns Speed Bins respectively Added Pb-Free Package Information |
| *B | 444306 | See ECN | NXR | Converted from Preliminary to Final Removed 35 ns speed bin and "L" bin Changed ball E3 from DNU to NC Removed redundant footnote on DNU Modified Maximum Ratings spec for Supply Voltage and DC Input Voltage from 2.4V to 2.45V Changed the I_{CC} Typ value from 16 mA to 18 mA and I_{CC} Max value from 28 mA to 25 mA for test condition $f = f_{ax} = 1/t_{RC}$ Changed the I_{CC} Max value from 2.3 mA to 3 mA for test condition $f = 1$ MHz Changed the I_{SB1} and I_{SB2} Max value from 4.5 μ A to 8 μ A and Typ value from 0.9 μ A to 2 μ A respectively Updated Thermal Resistance table Changed Test Load Capacitance from 50 pF to 30 pF Added Typ value for I_{CCDR} Changed the I_{CCDR} Max value from 4.5 μ A to 3 μ A Corrected t_R in Data Retention Characteristics from 100 μ s to t_{RC} ns Changed t_{LZOE} from 3 to 5, changed t_{LZCE} from 6 to 10, changed t_{HZCE} from 22 to 18, changed t_{LZBE} from 6 to 5, changed t_{PWE} from 30 to 35, changed t_{SD} from 22 to 25, and changed t_{LZWE} from 6 to 10 Added footnote #13 Updated the ordering Information and replaced the Package Name column with Package Diagram |
| *C | 571786 | See ECN | VKN | Replaced 45ns speed bin with 55ns |
| *D | 908120 | See ECN | VKN | Added footnote #7 related to I_{SB2} Added footnote #12 related AC timing parameters |
| *E | 2934396 | 06/03/10 | VKN | Added footnote #23 related to chip enable Updated package diagram and template |

Document History (continued)

| Document Title: CY62157EV18 MoBL®, 8-Mbit (512 K × 16) Static RAM Document Number: 38-05490 | | | | |
|--|---------|------------|-----------------|---|
| Rev. | ECN No. | Issue Date | Orig. of Change | Description of Change |
| *F | 3110053 | 12/14/2010 | PRAS | Changed Table Footnotes to Footnotes. Added Ordering Code Definitions. |
| *G | 3243545 | 04/28/2011 | RAME | Updated as per template. Added Acronyms and Units of Measure table. |
| *H | 3295175 | 06/29/2011 | RAME | Added I _{SB1} and I _{CCDR} to footnotes 7 and 11. Modified footnote 29 and referenced in Truth Table . |
| *I | 4102022 | 08/22/2013 | VINI | Updated Switching Characteristics : Updated Note 15. Updated Package Diagram : spec 51-85150 – Updated to the latest revision *H. Updated in new template. |
| *J | 4384935 | 05/20/2014 | MEMJ | Updated Switching Characteristics : Added Note 20 and referred the same note in “Write Cycle”. Updated Switching Waveforms : Added Note 33 and referred the same note in Figure 8 . Completing Sunset Review. |
| *K | 4576526 | 11/21/2014 | MEMJ | Added related documentation hyperlink in page 1. |
| *L | 5759379 | 06/01/2017 | VINI | Updated Thermal Resistance values. Updated the template. |

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