

Serial-in / Parallel-out Driver Series

# Serial-Parallel 3-input Driver



**BA823F**

No.09051EAT01

● **Description**

BA823F are an 8-bit serial-to-parallel-output driver, applicable for thermal printer heads or LED character display drivers.

● **Features**

- 1) Capable of driving a maximum of 200mA.
- 2) Non-driving current consumption can be reduced by controlling the strobe timing pulse.
- 3) Output data terminal can be used for a cascade configuration.
- 4) Digital ground and power ground are separated.
- 5) TTL and CMOS allow driving.

● **Applications**

Driver for thermal print head  
Driver for LED character display

● **Absolute maximum ratings (Ta=25°C)**

Parameter	Symbol	Limits	Unit
Power supply voltage	Vcc	7.0* <sup>1</sup>	V
Power dissipation	BA823F Pd	500* <sup>3</sup>	mW
Input voltage	VIN MAX	+0.3 to +6.0	V
Operating temperature	Topr	-20 to +75	°C
Storage temperature	Tstg	-55 to +125	°C

\*1 Voltage of  $\overline{O}_0\sim\overline{O}_7$  terminals is 34V (Max.)

\*2 Reduced by 5.5 mW/°C over 25°C.

\*3 Reduced by 5.0 mW/°C over 25°C.

● **Thermal derating curve**

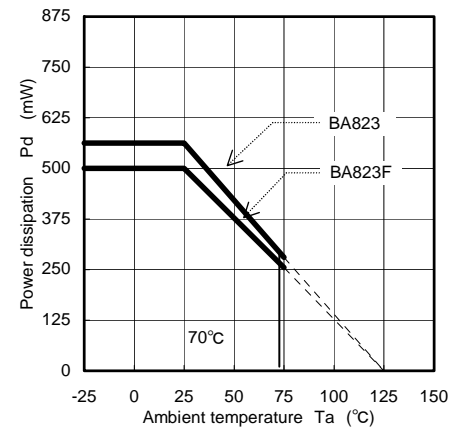


Fig.1

●Electrical characteristics (Unless otherwise specified, Ta=25°C, Vcc=+5.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Test Circuit
Power supply	VCC	4.5	5.0	5.5	V	Vcc terminal	Fig.2
Current dissipation(no load)1	IO1	-	4	6	mA	@All outputs = "0"	Fig.2
Current dissipation(no load)2	IO2	-	8	11	mA	@All outputs = "0"	Fig.2
Input low level voltage	VIL	-	-	0.8	V	-	Fig.2
Input high level voltage	VIH	2	-	-	V	-	Fig.2
Input low level current	IIL	-	-	0.4	mA	VIN=4.5V	Fig.2
Input high level current	IIH	-	-	100	μA	VIN=2.0V	Fig.3
Maximum output voltage	VO OFF	-	-	21.8	V	0 to 7, Io=10μA	Fig.3
Output saturation voltage	VO ON	-	0.8	1.3	V	@Io=100mA sink	Fig.3
Output current	IO L	-	-	207	mA	External voltage = 11.8V	Fig.3
"H" output voltage	VDOH	2.4	-	-	V	RL=10kΩ	Fig.3
"L" output voltage	VDOL	-	-	0.8	V	-	Fig.3
Minimum set up time	t1	-	-	300	ns	VIH=2.0V, VIL=0.8V	-
Minimum shift clock width	T2	-	-	1	μs	VIH=2.0V, VIL=0.8V	-
Minimum timing pulse width	T3	-	-	1	μs	VIH=2.0V, VIL=0.8V	-
Maximum transfer time	fMax	500	-	-	kHz	VIH=2.0V, VIL=0.8V	-

●Usage conditions range

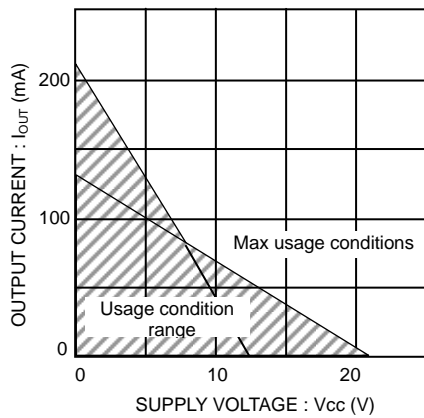
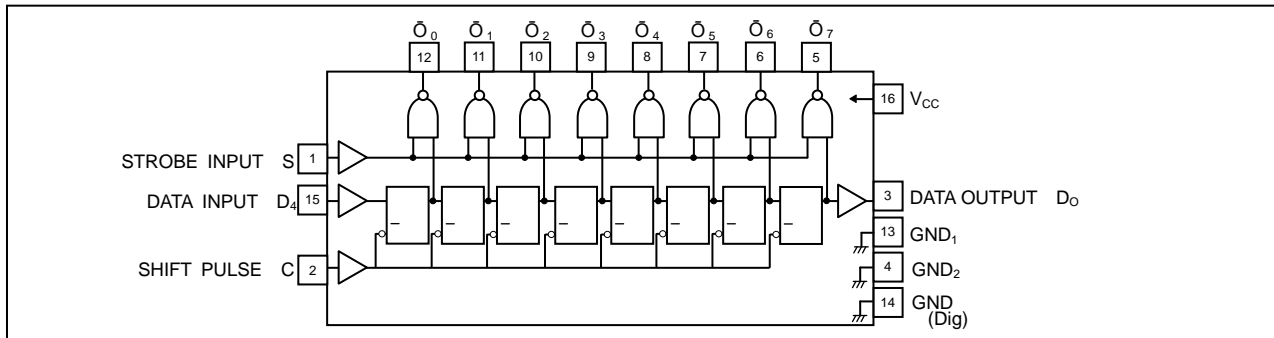


Fig.2: Conditions to use supply voltage and output current (per circuit)  
 Maximum conditions of use in the diagram to the left, show the absolute maximum supply voltage and IC output current.  
 This product should not exceed the usage conditions range.

Fig.2 Power supply voltage and current usage conditions

### ●Block diagram



### ●Pin descriptions

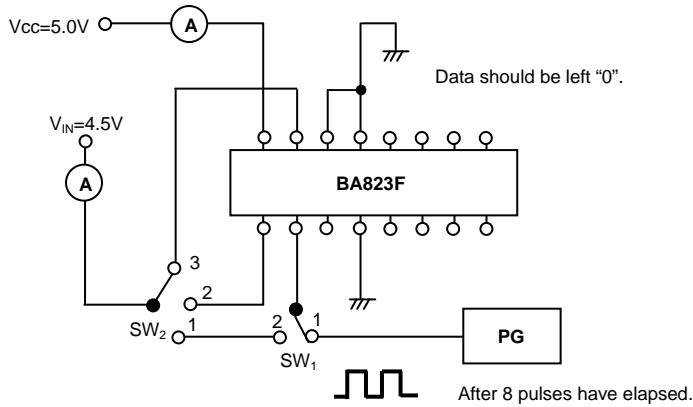
Pin No.	Pin Name	Symbol	Function
2	SHIFT PULSE	C	Shift pulse of shift register
15	DATA INPUT	D1	Data input of shift register is stored during the shift pulse rise time.
1	STROBE	S	When "1" is effective, the content of shift register is outputted.
12	OUTPUT	$\bar{O}_0$	"0" is effective when the content of register is "1" on the 1st bit is outputted.
11	OUTPUT	$\bar{O}_1$	"0" is effective when the content of register is "1" on the 2nd bit is outputted.
10	OUTPUT	$\bar{O}_2$	"0" is effective when the content of register is "1" on the 3rd bit is outputted.
9	OUTPUT	$\bar{O}_3$	"0" is effective when the content of register is "1" on the 4th bit is outputted.
8	OUTPUT	$\bar{O}_4$	"0" is effective when the content of register is "1" on the 5th bit is outputted.
7	OUTPUT	$\bar{O}_5$	"0" is effective when the content of register is "1" on the 6th bit is outputted.
6	OUTPUT	$\bar{O}_6$	"0" is effective when the content of register is "1" on the 7th bit is outputted.
5	OUTPUT	$\bar{O}_7$	"0" is effective when the content of register is "1" on the 8th bit is outputted.
3	DATA OUTPUT	D0	Data having passed through the output circuit of $\bar{O}_7$ becomes the input of the next stage
16	Vcc	Vcc	5.0V .is used normally ( $\pm 10\%$ )
13	GND	GND1	Especially, GND of the output circuit of $\bar{O}_0 \sim \bar{O}_3$
4	GND	GND2	Especially, GND of the output circuit of $\bar{O}_4 \sim \bar{O}_7$
14	GND	GND(Dig)	Especially, GND of the logic circuit

### ●Description of operation

BA823 is configured internally as shown in the block diagram. Terminals of clock C, data D1, and strobe S are used as input. Data input is synchronized with the clock, read serially during the rise time and latched at the rise time edge of the shifted shift register. The content of the set shift register appears on the output terminal of  $\bar{O}_0 \sim \bar{O}_7$  when the strobe is input, as shown in the time chart of Fig.5. Pulse width is the same as that of the strobe input pulse.

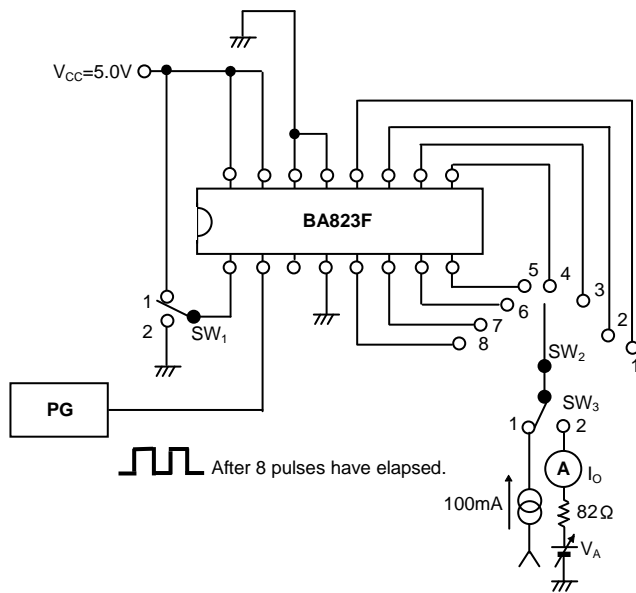
Data output terminal D0, is a terminal used for cascade connection of the IC, where the output of the final stage of the shift register has appeared, and is connected to the next data input terminal D1. In this case, when the clock and the strobe are used in conjunction, output terminal can be increased by 8 bits at a time.

●Measurement circuits



Item	SW <sub>1</sub>	SW <sub>2</sub>
I <sub>CC</sub>	1	1
I <sub>IH</sub>	2	1~3

Fig.3 Icc 1st measurement circuit



Item	SW <sub>1</sub>	SW <sub>2</sub>	SW <sub>3</sub>
VO ON	1	1~8	1
IOL	1	1~8	1
VO OFF	2	1~8	2

I<sub>O</sub> = 10μA when VO OFF is measured  
 V<sub>A</sub> = 30V when IO ON is measured

Fig.4 Vo ON, Vo OFF, IOL measurement circuit

●Input conditions

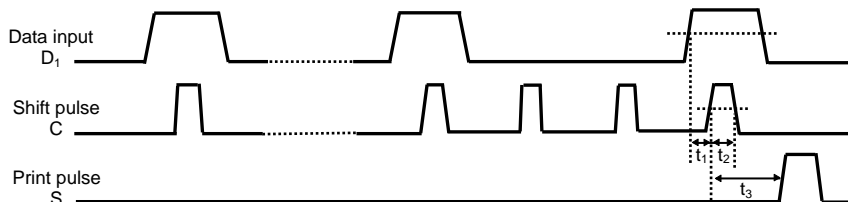


Fig.5

●Timing chart

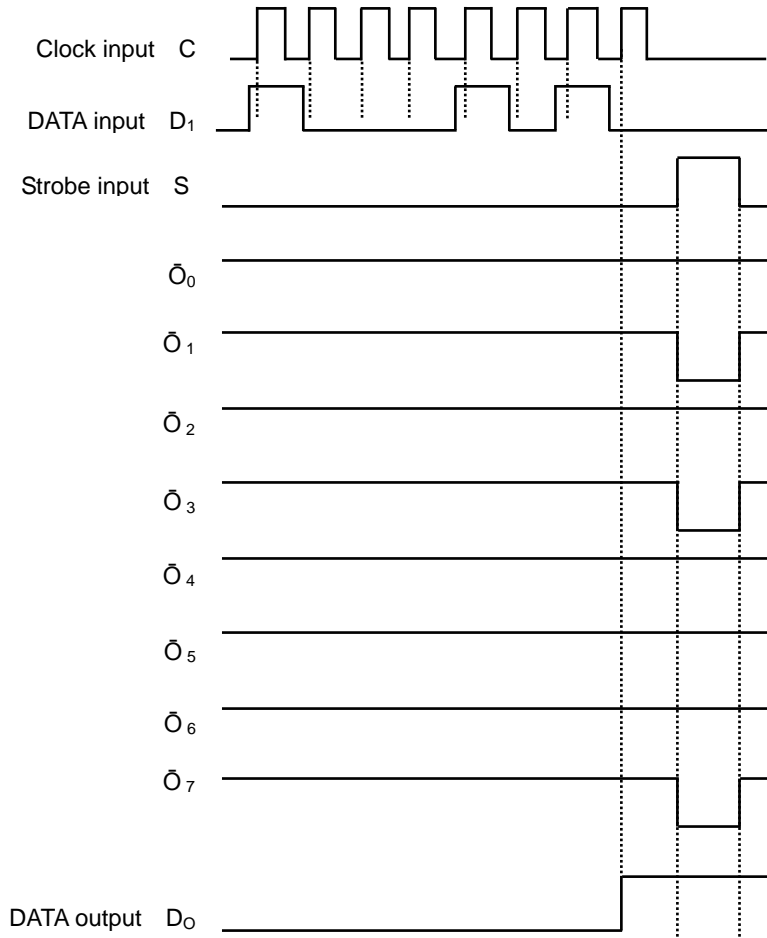


Fig.6

●Application example

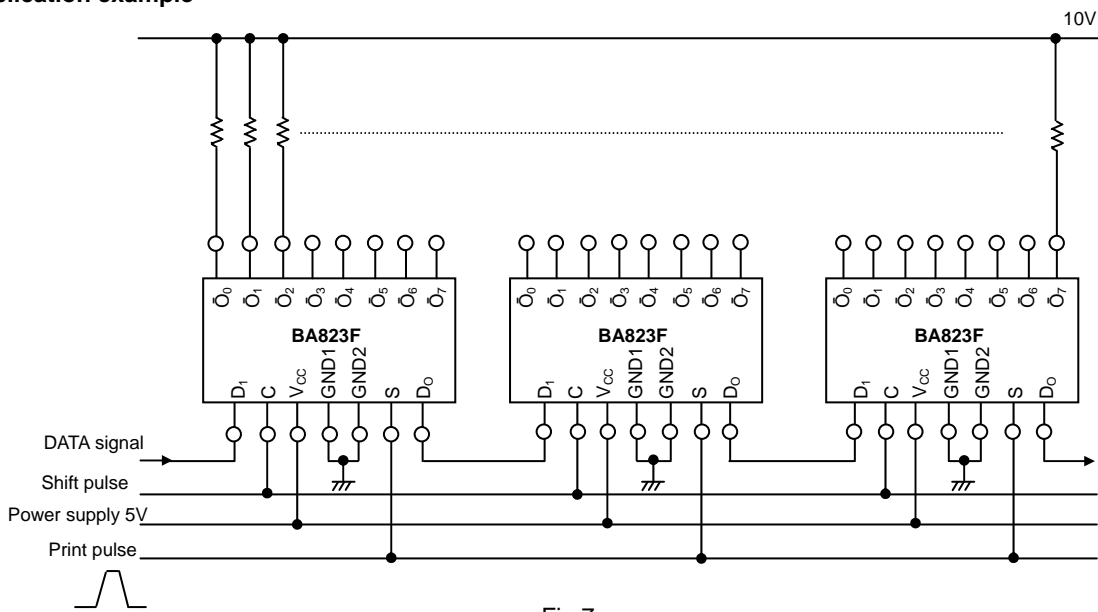


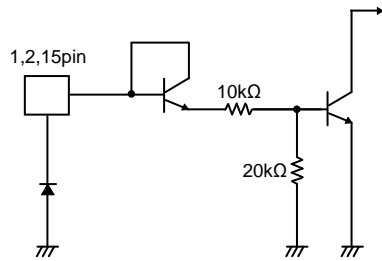
Fig.7

Example: Print head using the strobe function  
 Disabling the high current while the heating element is switched off is advantageous.

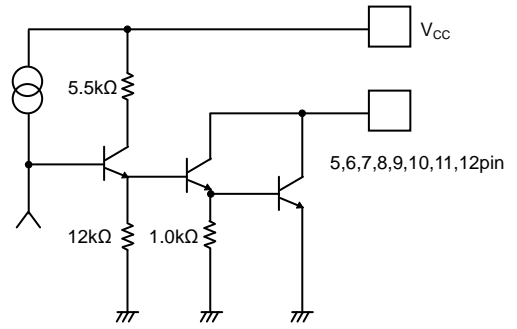
Use for thermal printer (when the timing is 1 phase) example

● Interfaces

(a) Input



(b) Output



(c) Serial data output

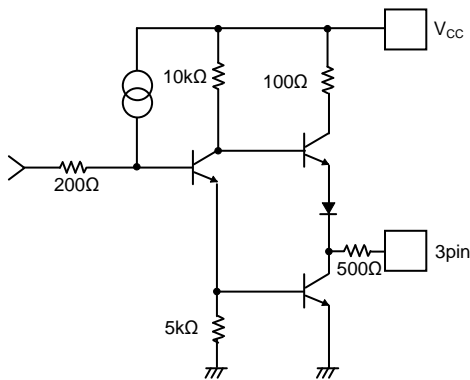
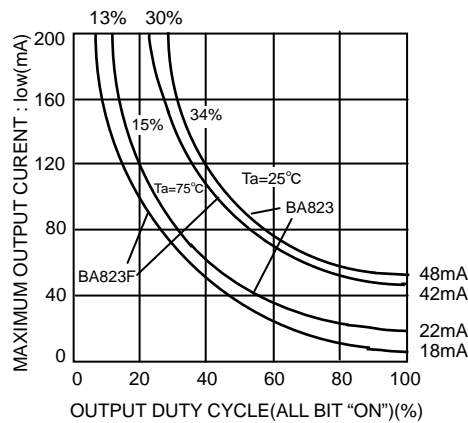


Fig.8

● Thermal derating curve



At repetition frequency 1Hz or higher

Fig.9 Output conditions

### ●Notes for use

#### 1. Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

#### 2. Connecting the power supply connector backward

Connecting of the power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.

#### 3. Power supply lines

Design PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks. Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and the GND terminal. When applying electrolytic capacitors in the circuit, not that capacitance characteristic values are reduced at low temperatures.

#### 4. GND voltage

The potential of GND pin must be minimum potential in all operating conditions.

#### 5. Inter-pin shorts and mounting errors

Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.

#### 6. Actions in strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

#### 7. Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.

#### 8. Regarding input pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:

When  $GND > Pin A$  and  $GND > Pin B$ , the P-N junction operates as a parasitic diode.

When  $GND > Pin B$ , the P-N junction operates as a parasitic transistor.

Parasitic diodes can occur inevitable in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.

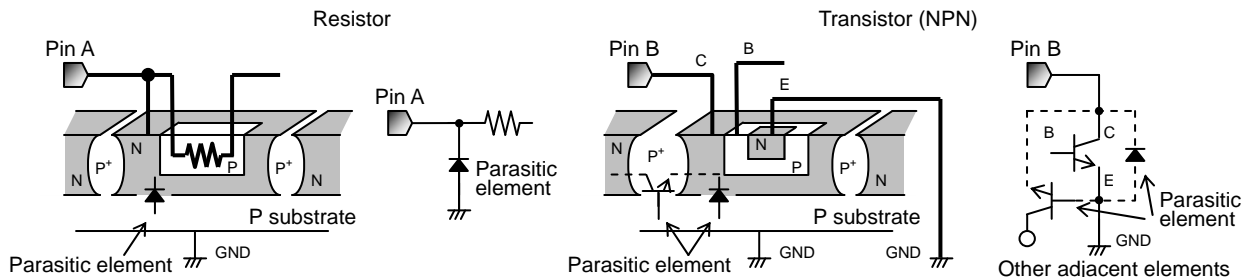
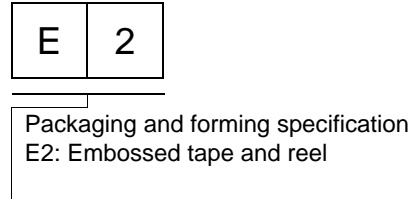
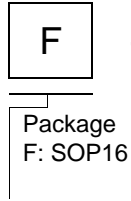
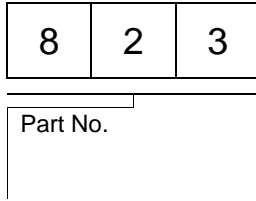
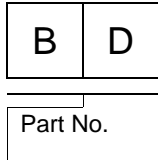


Fig.10 Example of IC structure

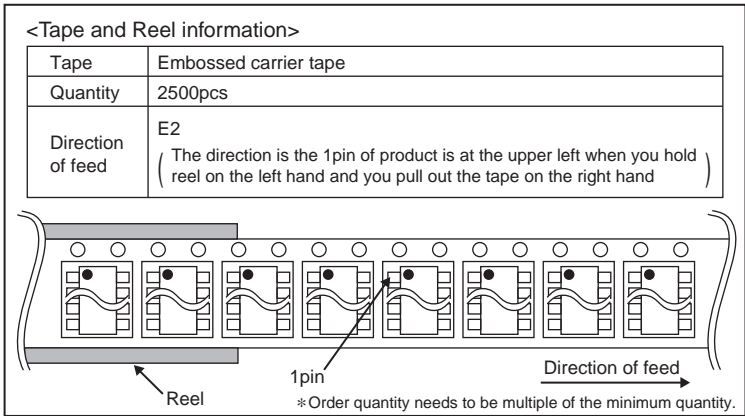
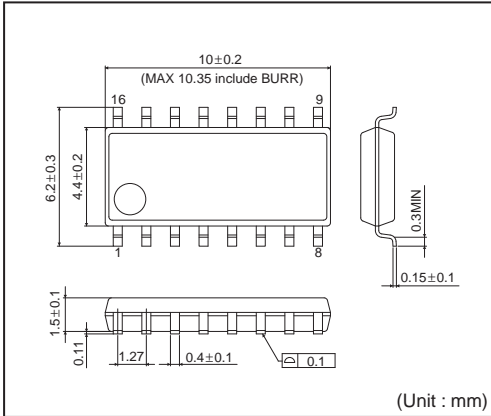
#### 9. Ground Wiring Pattern

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

● Ordering part number



SOP16





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